UNIVERSITY OF TWENTE.

Faculty of Electrical Engineering, Mathematics & Computer Science

Switching ripple reduction in a class-D amplifier using a MOSFET in series with the filter capacitor

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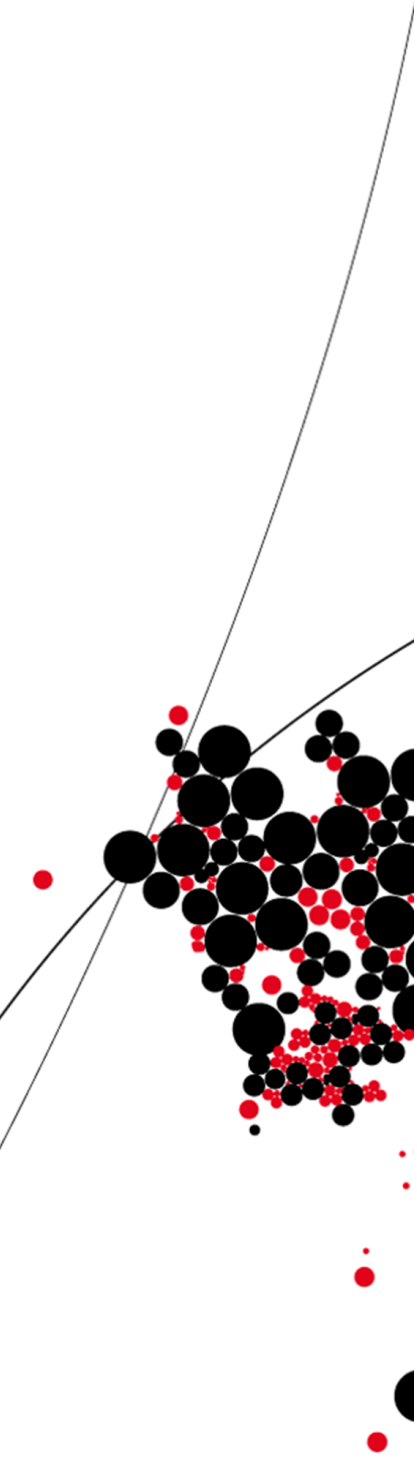

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Abstract

In high frequency PWM switching amplifiers, the output signal contains a ripple at the switching frequency. This can cause EMI effects in nearby applications. This research focuses on power efficient reduction of this ripple in an example class D audio amplifier with a second order output filter and a resistive load. In series with the filter capacitor, a MOSFET is placed. Since the study makes use of Simulink, a level 3 and a surface-potential based MOSFET model are examined. The level 3 model behaves according to theory, but the transition between triode and saturation region is discontinuous and the drain-source current is modelled as constant value in weak inversion. This favors the surface-potential based model to use in the study. It was found that the surface-potential based model lacks a body-diode.

In the class D amplifier, the switching ripple at 0Vdc is examined. The voltage-current relations that exist in the filter capacitor are compared to the voltage-current relations that the MOSFET in triode can create. It was found that the MOSFET can only compensate between 12% and 20% of the values that are apparent in the switching ripple. This is due to the switching ripple having an integrating voltage-current relation, whereas the MOSFET has a linear voltage-current relation. In time, the proposed solution can partially reduce the voltage ripple during 50% of the period. Complete reduction can only be achieved during 9% of the period. Concluding, the proposed solution is not a feasible way to reduce the switching ripple.

Chapter 1

Introduction

Switching amplifiers are commonly used in many fields these days. Applications cover a wide range, for example low power buck or boost converters, high performance audio amplifiers, high efficiency power conversions in for example electromagnetic drivetrains. All these applications follow the same basic principle: they use one or more transistors and storage elements at a high switching frequency to achieve the power conversion. The input signal is converted to a high frequency PWM signal. This PWM signal is used to drive one or more switching devices, which are usually MOSFETs, BJTs or IGBTs. Optionally, the output stage after the switching device can filter or adjust the output signal. After that, the output power signal can be used in the application. Because of the high frequency switching, the output signals of these applications have a small ripple at the PWM frequency.

Now, consider the example of a class D switching audio amplifier. The audible range of frequencies is approximately 20 Hz to 22 kHz. Typical class D amplifiers have a PWM frequency in the range of 350 to 700 kHz. A small ripple in the output signal at these high frequencies will not be audible. However, the small ripple in the power signal will excite electromagnetic radiation, which may induce EMI (electromagnetic interference) effects in other applications nearby.

Many have sought solutions to reduce the switching ripple. For example, by adjusting the switching frequency depending on the load [4] or by creating an adjustable inductance parallel to the load [5]. Another well-known solution is the use of multiphase converters. By using two switching amplifiers on the same load with a 180 degree phase shift in PWM signal, both switching ripples cancel each other [6]. It can be made more efficient by coupling the inductors of both amplifiers [6]. Finally, it is also shown that a current source parallel to the load is able to compensate for the ripple [7].

All of these examples either use a lot of components and space, or require significant power. Therefore, this research focuses on switching ripple reduction with minimal power consumption and a minimal number of components in mind. A simple class D audio amplifier with a second order output filter is taken as an example application.

Chapter 2

Switching amplifier and the small ripple

The schematic of the aforementioned class D audio amplifier is shown in figure 2.1. The input signal is a signal with a maximum frequency of 22 kHz between 0 and 1, which is processed to a high frequency PWM (pulse width modulation) output with a frequency of 350 kHz up to 700 kHz. The PWM signal drives both MOSFETs in such a way that only one switch at a time will be closed.

Both switches are connected in series with a 12V and a -12V voltage source. Since one switch is closed at any time, always one of either voltage sources is electrically connected to the output stage. The output stage consists of a second order LC filter ($L = 22$ μH, $C = 1$ μF) and an output load resistor of 4 Ω. The transfer can be seen in the Bode phase and magnitude plot of figure 2.2. As can be seen, the filter is critically damped just above the maximal audible frequency of 22 kHz.

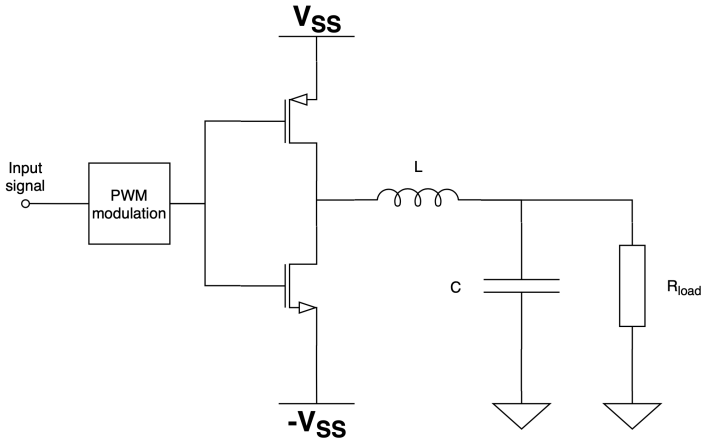

Figure 2.1: *Schematic of an ideal class D amplifier with a second order filter and resistive load*

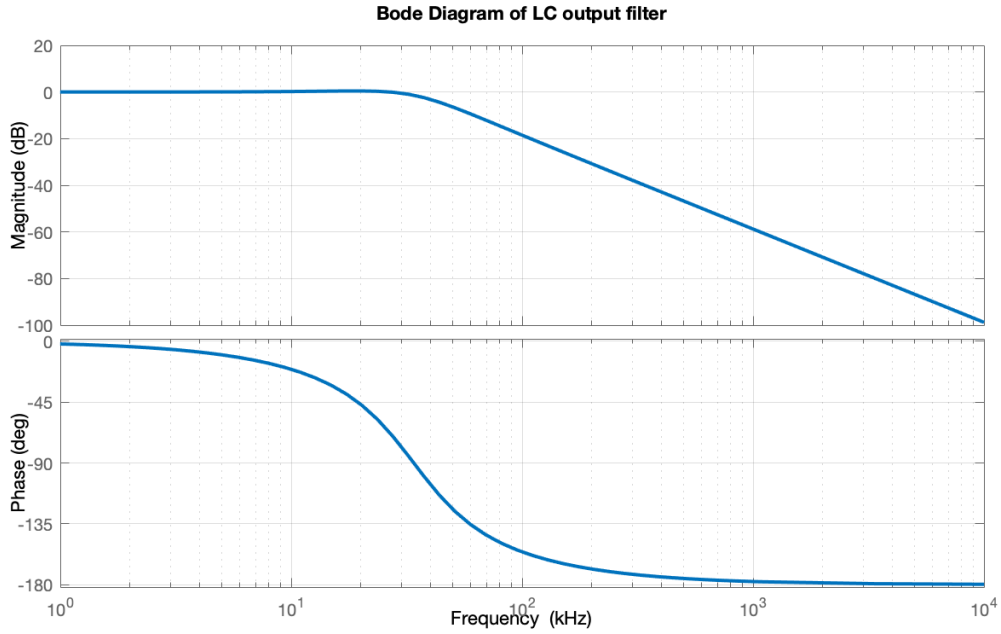

Figure 2.2: *Phase and magnitude plots versus frequency for the LC output filter with $L = 22\mu H$ and $C = 1\mu F$*

Small ripple The inductor in the output stage will charge and discharge on every switching cycle of the amplifier. This results in an inductor current that will rise and fall on every charge and discharge. This is known as the ripple current of the inductor, as explained by Erickson [1]. In short, the ripple current can be approximated by the following reasoning.

The elementary equation of any ideal inductor current and voltage relation is given by:

$$V_L(t) = L\frac{di_L(t)}{dt} \tag{2.1}$$

Rewriting to inductor current and making use of the small ripple approximation (the voltage ripple can be assumed very small in a DC application [1]) gives:

$$\frac{di_L(t)}{dt} = \frac{V}{L} \tag{2.2}$$

Now, using figure 2.3 and equation 2.2, it is possible to express the inductor ripple as the following expression, as stated by Erickson [1]:

$$\Delta i_L = \frac{V_g - V}{2L} DT_g \tag{2.3}$$

with Δi_L the current ripple of the inductor, V_g the source voltage, V the DC output voltage with the ripple neglected, L the inductor value, D the duty cycle of the PWM signal and T_g the switching time of one period of the PWM signal.

In practice, the output voltage V cannot be assumed constant, since the capacitor in the second order filter induces a voltage, depending on the inductor current that flows into it. Ideally, the DC current will flow completely through the load resistor and the ripple current will flow into the capacitor. In practice however, the ripple current charges the capacitor, which does increase the voltage over the capacitor. With the load resistor in parallel, the voltage also increases the current and thus the power dissipated in the load every cycle.

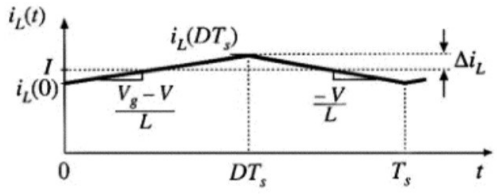

Figure 2.3: *Steady-state inductor current waveform [1]*

The division of current between the two depends on the capacitor value and whether the load is a true resistor. The voltage ripple can be estimated with the steps below (equation 2.4, 2.5 and 2.6) [1]. Note that in practice, the resistive behaviour of the capacitor (equivalent series resistance, ESR) must also be included. For fairly large C, the voltage ripple is simply the inductor current ripple multiplied by the ESR of the output cap [6].

Capacitor voltage-charge relation:

$$q = C(2\Delta v) \tag{2.4}$$

The current waveform is known (see figure 2.3 and equation 2.3). The charge is the integral of the current (Ampere is Coulomb per second). The integral is the area under the charge curve. Since the waveform is a triangle, the area can be calculated with the height (Δi_L), base ($\frac{T_g}{2}$) and divide by two. Hence:

$$q = \frac{1}{2}\Delta i_L \frac{T_g}{2} \tag{2.5}$$

Substituting equation 2.4 and 2.5 gives a solution for the voltage ripple magnitude:

$$\Delta v = \frac{\Delta i_L T_g}{8C} \tag{2.6}$$

Chapter 3

Goal and research question

3.1 Proposed solution

Now that the background behind the switching ripple is known, the approach to reduce the ripple efficiently can be set out. The goal is to use a single MOSFET as a variable resistor in series with the filter capacitor, hereby creating the possibility to regulate the voltage over the capacitor. The schematics of the approach are shown figure 3.1. This is the same class D amplifier as shown in figure 2.1, but with a MOSFET placed in series with the capacitor.

As explained in the previous chapter, the switching causes the inductor to induce a small rising and falling current with every PWM period. This ripple current charges and discharges the capacitor slightly, which results in a rising and falling capacitor voltage. Since the load is parallel to the capacitor, the small voltage ripple causes a slight power ripple in the load.

A MOSFET as a variable resistor in series with the capacitor might be able to compensate for the capacitor voltage ripple, simply by creating an inverse of the voltage ripple over itself. Since the load is now parallel to the capacitor and the MOSFET in series, the load only sees the sum of both voltages. The MOSFET absorbs the voltage ripple, so there will be no ripple in the load.

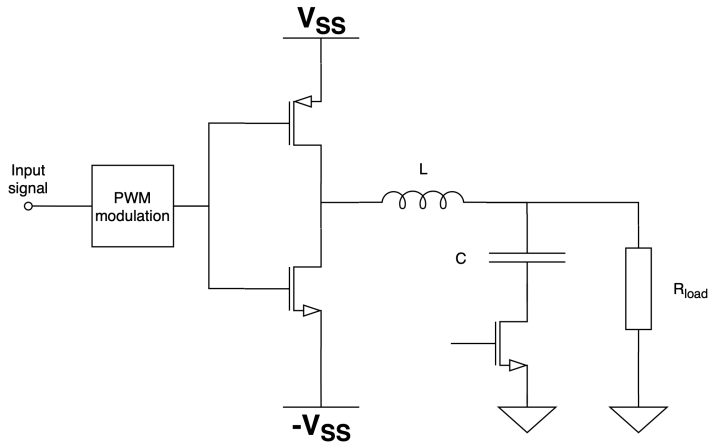

Figure 3.1: *Class D amplifier from figure 2.1 with a FET added in series with the capacitor*

3.2 Research questions

In order to structure this ripple reducing approach during the project, a main research question and sub-questions are composed:

Can the switching ripple in a class D amplifier be reduced by placing a MOSFET in series with the capacitor in a second order LC output filter?

The main research objective is split into 3 sub-questions. These are:

- What type of MOSFET model can be used in Simulink simulation with switching ripple reduction in mind?
- How can the FET be controlled with a maximum ripple reduction in mind?
- What are the effects in terms of current ripple, voltage ripple, efficiency, complexity and feasibility?

The sub-questions facilitate different parts of the research. Firstly, basic background on the characteristics of MOSFETs will be presented. Thereafter, MOSFET models in Simulink will be examined, such that an adequately functioning model can be chosen for the ripple reduction. Secondly, the selected MOSFET model will be used in the ripple reduction approach as shown in figure 3.1. Finally, the results of both the MOSFET model analysis as well as the ripple reduction analysis will be discussed and conclusions will be given.

Chapter 4

MOSFET use in Simulink

4.1 Method

4.1.1 Constraints

The placement of the MOSFET in the circuit of figure 3.1 is a major factor in this research. Due to the filter capacitor, there is no DC current in this branch. This automatically makes this ripple cancellation the approach very efficient: the drain-source voltage over the MOSFET consists solely of (a part of) the ripple voltage and some noise.

The placement also results in a set of constraints and known values for the MOSFET:

1. The maximum V_{ds} of the MOSFET equals the maximum amplitude of the ripple voltage
2. The MOSFET may not go in saturation, since that may lead to very high V_{ds} values
3. The reverse diode is of importance in the analysis, since negative V_{ds} exist in the ripple voltage

4.1.2 Model types

Two different types of MOSFET models are examined in this research. Firstly, a level 3 model is used. In the classical range of level 1, 2 and 3 models, the last one is the most sophisticated one [8]. Secondly a surface-potential based model is used. This was done after concerns about the usability of the level 3 model arose. Surface-potential based models are generally based on underlying physics, rather than straightforward parameters such as threshold voltage.

For both models, multiple plots are created and parameters estimated or calculated, in order to examine the MOSFET model characteristics. The characteristics that are examined for both models are the following:

1. Weak inversion region: drain-source current and dependence on V_{gs}
2. Triode region: the MOSFET as a resistor
3. Saturation region and the transition from triode region
4. Negative V_{ds}

The level 3 model is a SPICE model of the FQP33N10 of Fairchild Semiconductor, which will be used in MATLAB Simulink [9]. This is done since a default level 3 model in Simulink is not ready for simulation. Some parameters need to be set to a number in order to be able to run the simulation. Therefore, a known model is used. The surface-potential based model is a standard model available in the Simscape package of MATLAB Simulink.

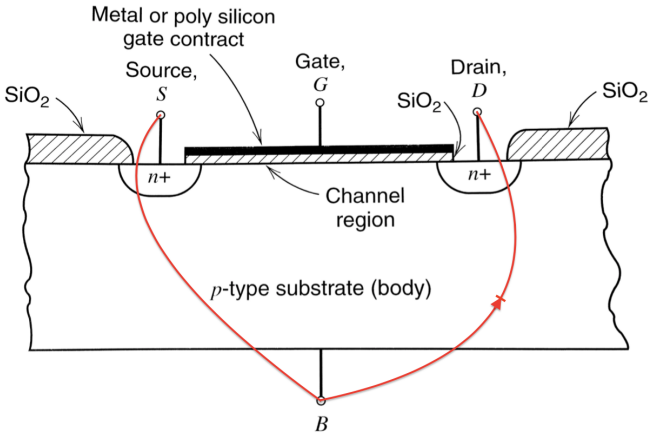

Figure 4.1: *NMOS simplified internals [2] with the body diode connections in red annotation*

4.1.3 MOSFET theory and testing plan

MOSFET basics A MOSFET is a semiconductor device that can be used for many different applications. It can act as a switch, for example in (class D) switching amplifiers, but it can also act as a linear amplifier. Depending on the voltages applied on the terminals of the MOSFET, the device operates in different regions. A good understanding of these regions is necessary before the ripple cancellation in this thesis can be pursued.

A typical MOSFET has three connections: the gate, drain and the source. A fourth connection can be the body (i.e. the substrate). A simplified cross-section is shown in figure 4.1. MOSFETs come in two types: NMOS and PMOS. The difference is the type of material for the substrate and source and drain. It basically determines whether negative or positive voltages allow the substrate to conduct more current. In this research, all MOSFETs mentioned are NMOS types. NMOS transistors have a heavily doped n-type source and drain and a p-type substrate [2].

Threshold voltage The threshold voltage (V_{th}) of a level 3 MOSFET model is specified in the model parameters. However, there is no direct threshold voltage parameter in a surface-potential based model. Therefore, the threshold voltage for the latter model will be determined with the constant current method [3].

This constant current method is widely used, mainly because of its simplicity. For a constant low V_{ds} (generally below 100mV), a sweep over V_{gs} is made. The current can be plotted either logarithmic or linear on the y-axis. In the linear case, one looks at the start of the linear phase of the plot. In the logarithmic case, one looks at the end of the linear line. Both readouts are shown in figure 4.2. A similar explanation and figures can also be found in Gray et al. [2].

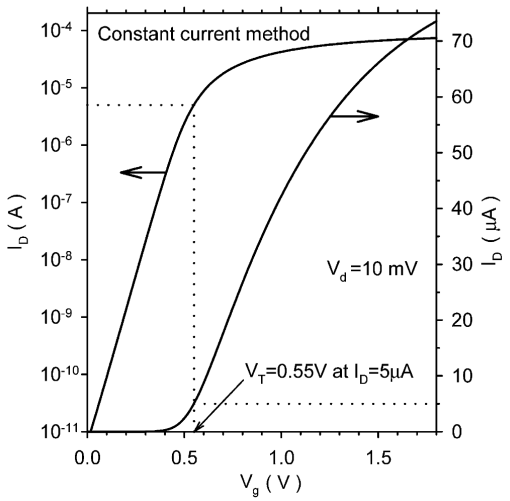

Figure 4.2: *Constant current method as described by Ortiz-Conde et al. [3]. The dotted line shows the location on both the logarithmic and linear curve for the threshold voltage.*

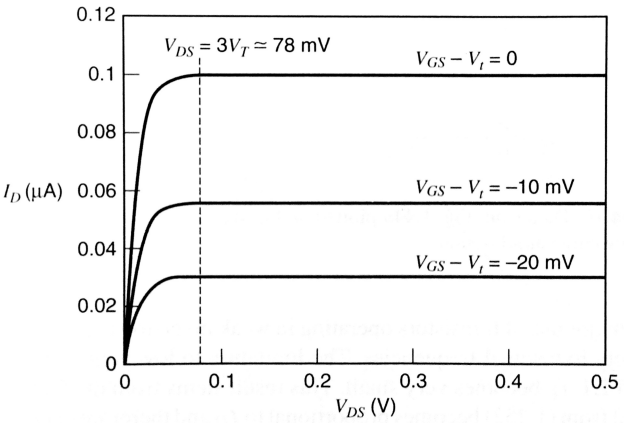

Figure 4.3: *I_{ds} versus V_{ds} for different V_{gs} below threshold [2], according to equation 4.1*

Weak inversion When V_{gs} is below V_{th}, there would ideally be no current I_{ds} at all. However, this is not the case. There is a small current between the drain and the source. This operating region of the MOSFET is called weak inversion. The value can be determined by the following equation (4.1)[2]:

$$I_{ds} \sim e^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)}[1 - e^{\left(-\frac{V_{ds}}{V_{th}}\right)}] \tag{4.1}$$

with I_{ds} the drain-source current and V_T the thermal voltage. Factor n is given by the equation 4.2 below. This equation only holds for MOSFETs where the source is tied to the bulk.

$$n = 1 + \frac{C_{dep}}{C_{ox}} \tag{4.2}$$

Note that in equation 4.1, the equation becomes almost constant when $V_{ds} > 3V_{th}$, because the last term approaches unity [2]. The plot will look like figure 4.3. In this figure, I_{ds} is plotted against V_{ds} for different V_{gs} below V_{th}.

In the results section, the drain-source current will be plotted for different V_{gs} (below V_{th}) and V_{ds}. Since these currents are generally very small, they will be plotted on a logarithmic scale.

Triode region If V_{gs} becomes bigger than V_{th}, two things can happen, dependent on the voltage V_{ds}. If V_{ds} is big enough to satisfy the saturation condition (equation 4.3), the MOSFET acts at a variable current source. If V_{ds} is smaller than that (and thus follows equation 4.4), the MOSFET operates in its triode region. In this region, the relation between V_{ds} and I_{ds} is ideally linear, which indicates Ohmic behaviour. In other words, the MOSFET acts as a variable resistor.

For these values of V_{ds} the MOSFET is in saturation:

$$V_{ds} > V_{gs} + V_{th} \tag{4.3}$$

For these values of V_{ds} the MOSFET is in triode:

$$V_{ds} < V_{gs} + V_{th} \tag{4.4}$$

The linear relation between I_{ds} and V_{ds} can be viewed in a linear graph with both on a linear axis. Such a plot also clearly shows the transition to the saturation region. This graph will be made and both the resistive behaviour in the triode region as well as the transition to the saturation region will be examined for different values of V_{gs} for both MOSFET models. The resistance (R_{ds}) and V_{gs} are related with the following equation (equation 4.5). Note that this is directly the relation between V_{gs}, V_{ds} and I_{ds}, since $R_{ds} = V_{ds}/I_{ds}$.

$$R_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \tag{4.5}$$

Body diode Now that all regions for positive values of V_{ds} are examined, negative values of V_{ds} are considered. In the small voltage ripple that is to be cancelled, negative voltages over the drain-source occur.

There exists a body diode in MOSFETs. This is the case since the p-n junction between bulk and drain or between bulk and source acts as a diode. In order to create a MOSFET with just 3 pins, the bulk and source are usually connected, which only leaves a body diode between bulk and drain. With the bulk connected directly to the source, the body diode can be seen as a diode between source and drain. A picture of this situation is shown in figure 4.1.

Due to the body diode, the MOSFET characteristics are different for negative V_{ds} compared to positive V_{ds}. Between 0 and -0.6V, the MOSFET still operates in triode region. For more negative voltages, the diode starts conducting, since the diode then sees a forward voltage bigger than 0.6V. In terms of V_{ds}, this translates to voltages below -0.6V. For more negative voltages, the body diode in the MOSFET conducts more current exponentially. Since the diode is not ideal, we expect some sort of resistive behaviour, but as a very small equivalent series resistance in the diode.

The same linear graph that is created for the triode region can also be used to examine the behaviour for negative V_{ds}. In this region, it is especially interesting to look at the behaviour around V_{ds} equal to -0.6V, since that is the expected value at which the body diode starts significant current conduction.

4.2 Results

Below, the different regions of both the level 3 and the surface-potential based model will be plotted.

4.2.1 Level 3 MOSFET model

Threshold voltage The threshold voltage of the level 3 model is already one of the parameters, and it is set to 3.88V.

Weak inversion The drain-source current for 7 different gate voltages below the threshold voltage in steps of 0.5V are simulated and plotted in figure 4.4. After close examination, it was found that for all values of V_{gs} below the threshold voltage of 3.88V, the drain-source current is exactly the same. In the plot, this is seen as the dark-brown line. The color is the result of all overlaying graphs of V_{gs} equal to 0.5V up to 3.5V. This behaviour does not correspond with expected behaviour of equation 4.1, in which the current is proportional to V_{gs}. The level 3 model appears to have a fixed leakage current for all values of V_{gs} smaller then V_{th}.

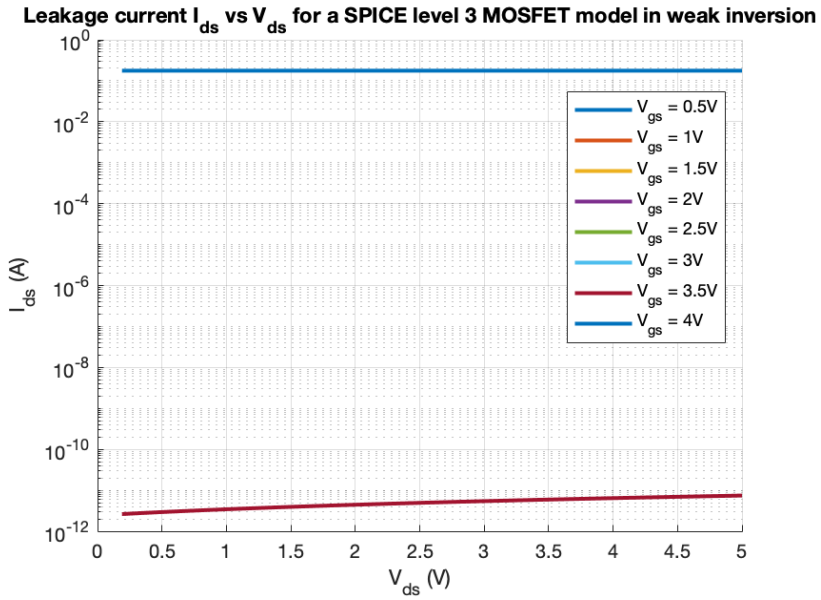

Figure 4.4: *I_{ds} versus V_{ds} for different V_{gs} of a level 3 MOSFET model in weak inversion (i.e. for V_{gs} below V_{th}). Note: $V_{gs} = 0.5V$ up until $V_{gs} = 3.5V$ are all the same line. Only $V_{gs} = 4V$ is separated, since this is above $V_{th} = 3.88V$*

Triode region In figure 4.5, I_{ds} versus V_{ds} for different V_{gs} are plotted for the level 3 MOSFET model. As can be seen, there is a roughly linear phase for small V_{ds}, a small non-linear transition period and then saturation towards higher V_{ds}. However, the transition to saturation seems to be discontinuous. A sharp edge can be seen on every curve right at the moment the saturation condition is met, which indicates that the derivative of the curve is discontinuous. This means there is unknown behaviour of model around that point.

Body diode A quick look at the same I_{ds} vs V_{ds} curve (figure 4.5) for negative values of V_{ds} already show behaviour that is expected to be from a connected reverse body diode. A re-scaled plot of that specific area is shown in figure 4.6. There, it can be seen that there is non-linear behaviour as a result of the diode starting to conduct at negative voltages below 0.6V. Since the

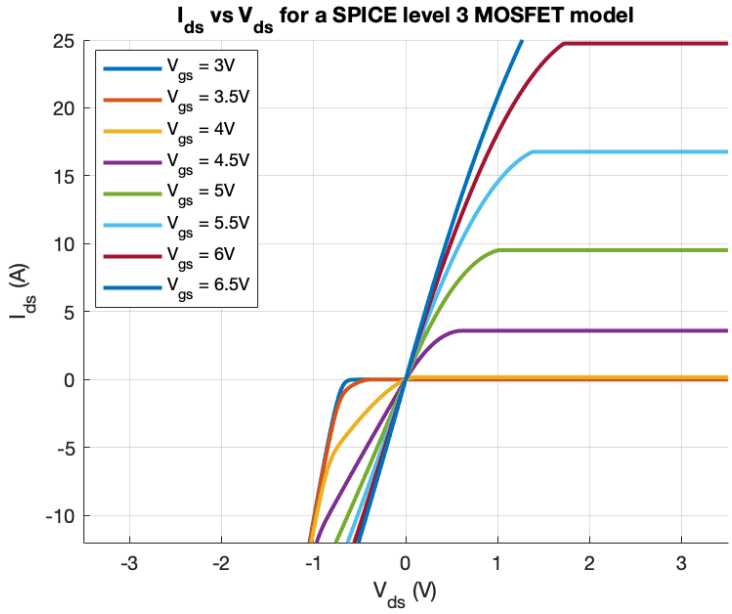

Figure 4.5: *I_{ds} versus V_{ds} for different V_{gs} of a level 3 MOSFET model*

exact drain-source voltage where this happens is dependent of V_{gs}, the conduction is not purely a diode. There is a series resistance connected to the diode as well, and this series resistance is dependent on V_{gs}.

Since the level 3 model in Simulink is not performing as expected in all regions, a surface-potential based model will be examined as well.

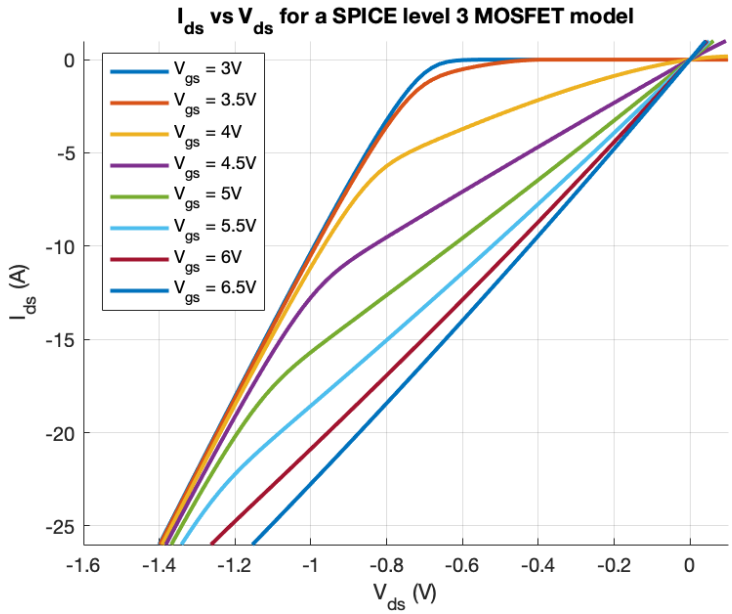

Figure 4.6: *I_{ds} versus negative V_{ds} for different V_{gs} of a level 3 MOSFET model*

4.2.2 Surface-potential based MOSFET model

Threshold voltage The threshold voltage of the surface-potential based model is calculated using the constant current method as described in the method section. The result is shown in figure 4.7. The threshold is estimated to be 3.34V.

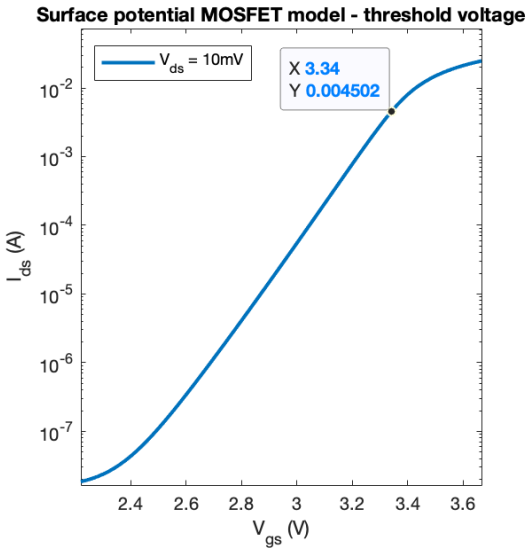

Figure 4.7: *Logarithmic plot of I_{ds} versus V_{gs} for $V_{ds} = 10mV$ of a standard surface-potential based MOSFET model to determine V_{th}*

Weak inversion In figure 4.8, I_{ds} for different V_{gs} below V_{th} is shown. As indicated by equation 4.1, the current is exponentially dependent on V_{gs}.

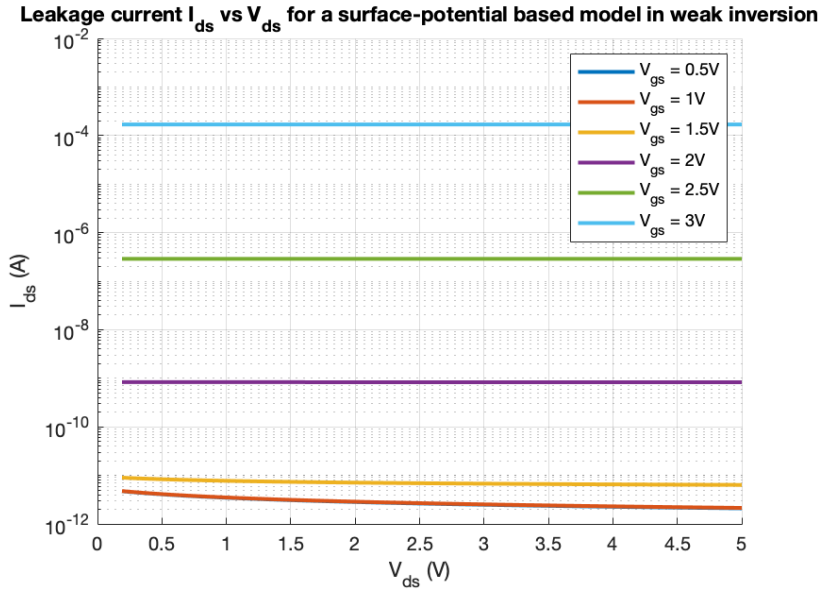

Figure 4.8: *I_{ds} versus V_{ds} for different V_{gs} of a surface-potential based MOSFET model in weak inversion (i.e. for V_{gs} below V_{th}). Note: $V_{gs} = 0.5V$ and $V_{gs} = 1V$ are very close to each other*

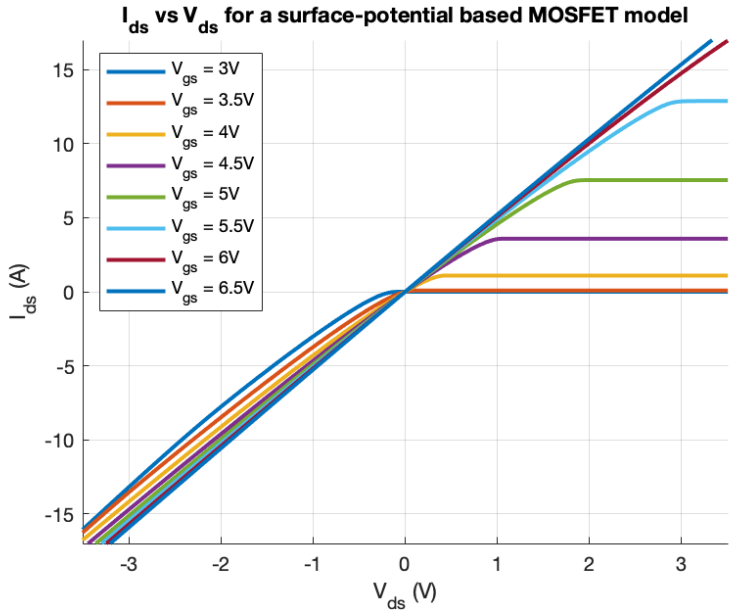

Figure 4.9: *I_{ds} versus V_{ds} for different V_{gs} of a standard surface-potential based MOSFET model*

Triode region In figure 4.9 the drain-source voltage and current are plotted for different values of the gate-source voltage V_{gs}. For positive values of V_{ds}, the resulting current I_{ds} clearly follows a linear line until shortly before the saturation condition is met (equation 4.3). The linear relation between current and voltage indicates resistive behaviour.

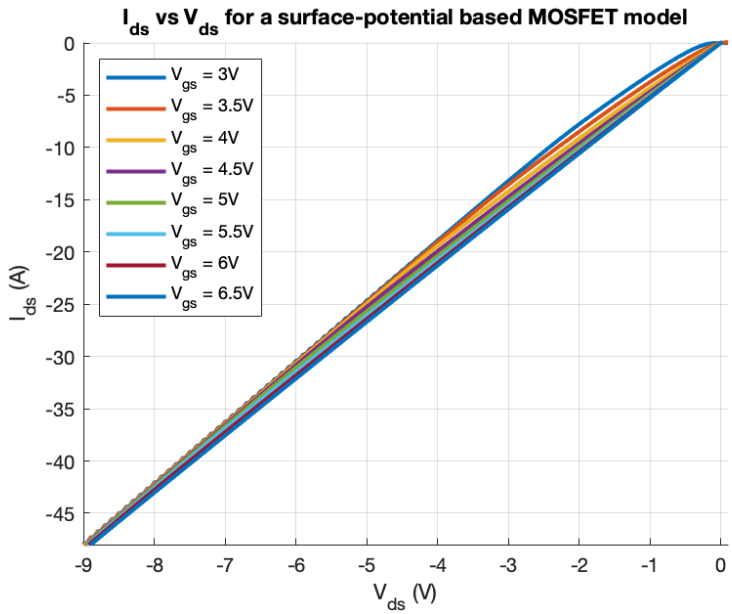

Figure 4.10: *I_{ds} versus negative V_{ds} for different V_{gs} of a standard surface-potential based MOSFET model*

Body diode For negative values of V_{ds}, the same resistive behaviour can be seen as for positive values of V_{ds}. To examine the model further, the results of a simulation for more negative voltages is plotted in figure 4.10. Here, it can be seen that the linear behaviour continues for a wide range of negative drain-source voltages. This invalidates the hypothesis that there is a diode modelled in at any negative value for V_{ds}.

However, the standard settings of the surface-potential based MOSFET imply that there is a body diode in the model. The body diode settings are set to default settings by Simulink and have the following values:

- Reverse saturation current: $5.2 \cdot 10^{-13}$ A
- Built-in voltage: 0.6 V
- Ideality factor: 1
- Zero-bias junction capacitance: 480 pF
- Transit time: $5 \cdot 10^{-8}$ s

Based on these parameters, negative voltages smaller than -0.6V should result in stronger negative currents. Either the diode is either not properly activated in the surface-potential based model, or the resistive behaviour is stronger than the diode. In other words, the diode is not conducting enough, or the 'resistor' is in series with the diode.

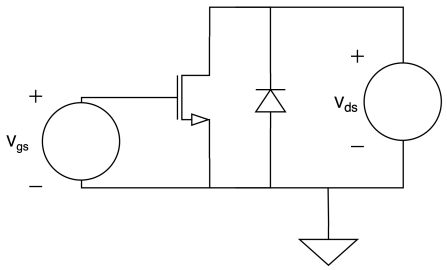

Figure 4.11: *NMOS with an external reverse diode*

In figure 4.11, a diode is placed in parallel with the MOSFET in the same way a reverse body diode would be internally connected. This is the same connection as shown in figure 4.1. A simulation is done with the external diode connected to the surface-potential based model. The result is shown in figure 4.12. Now, the diode behaviour can indeed clearly be seen: at $V_{ds} = -0.6V$ the diode starts conducting independent of V_{gs}, resulting in a sudden transition to more current conduction.

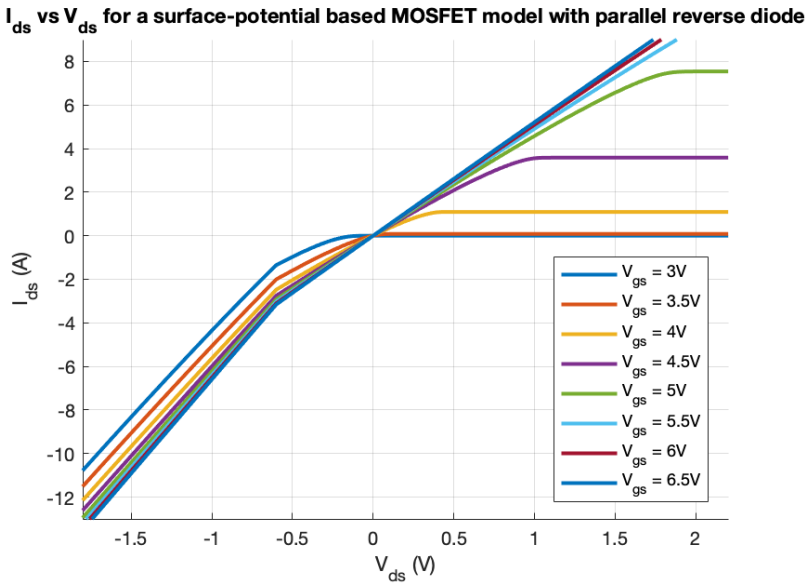

Figure 4.12: *I_{ds} versus V_{ds} for different V_{gs} of a surface-potential based MOSFET model with a diode in parallel as shown in figure 4.11*

Chapter 5

Ripple reduction analysis

5.1 Method

5.1.1 MOSFET use

In the previous chapter on MOSFET use in Simulink, the Simulink behaviour of two different types of MOSFET models was examined. In this part about ripple reduction, only one of the two models will be used. Both the fixed current in weak inversion and the discontinuity between the triode and saturation region of the level 3 model favor the surface-potential based model. Therefore, the surface-potential based model without body diode will be used in the ripple reduction analysis.

5.1.2 Class D parameters

The parameters that will be used in the results section are the as specified in chapter 2 ('Switching amplifier and the small ripple'). For completeness, the complete set of parameters for the class D amplifier is given below:

- $V_{ss} = 12$ V
- $L = 22$ µH
- $C = 1$ µF
- $R_{load} = 4\ \Omega$
- PWM frequency = 400 kHz
- Input signal:

  Amplitude = 0.5 (AC) or 0 (DC)

  Offset = 0.5

  Frequency = 5 kHz (AC) or 0 Hz (DC)

In order to only asses the ripple current and voltage, a DC input value of 0.5 will be used. The input signal of the modulator in figure 2.1 is bounded between 0 and 1. A DC input of 0.5 will result in an output voltage of ideally 0Vdc. This means that all current and voltage differences caused by the inductor ripple can be compared to 0. Therefore, the 0.5 DC input signal forms the basis of the ripple analysis. Whenever an AC input signal used, the parameters are as specified in the list above.

5.1.3 Method

Firstly, the inductor ripple and corresponding voltage ripple for the specified class D amplifier need to be determined. This will be done for both an AC and a DC input signal. For both input signals, the voltage over and the current into the capacitor will be measured and plotted, since the additional MOSFET will be placed in series with the capacitor (as explained under section 3.1 'Proposed solution'). With these plots, it can be verified that the ripple indeed exists in our simulation.

Secondly, the voltages and currents of the ripple will be compared with the voltage-current relations that the MOSFET can create. From this, it can be estimated how much ripple compensation can be accomplished. If a significant amount of compensation values can be reached, a design phase can be started on the actual MOSFET control and implementation in the class D amplifier model.

5.2 Results

The class D amplifier of figure 2.1 is used with the parameters as specified in section 5.1.2 ('Class D parameters'). The output voltage over the load is shown in figure 5.1. Upon close examination, the voltage ripple over the load can be seen in the voltage signal of the figure. The current ripple through the load is the same as the voltage ripple, since the current is linearly proportional to the voltage in a resistive load.

As mentioned before, the voltage over the capacitor equals the voltage over the load. The current through capacitor C of figure 2.1 under the same conditions is shown in figure 5.2. There is a 90 degree phase shift between the voltage of figure 5.1 and the current of figure 5.2 visible. Both figures capture the same time frame.

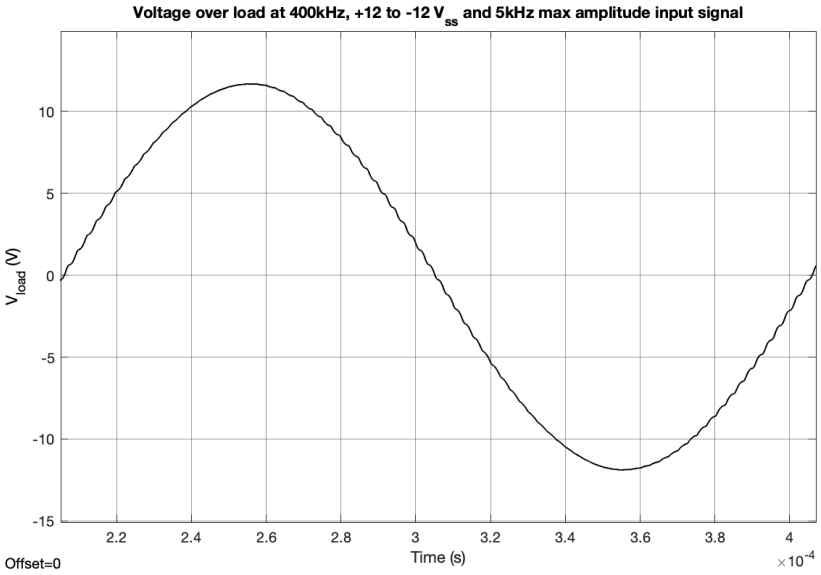

Figure 5.1: *Voltage over the load of the class D amplifier of figure 2.1 with AC input signal*

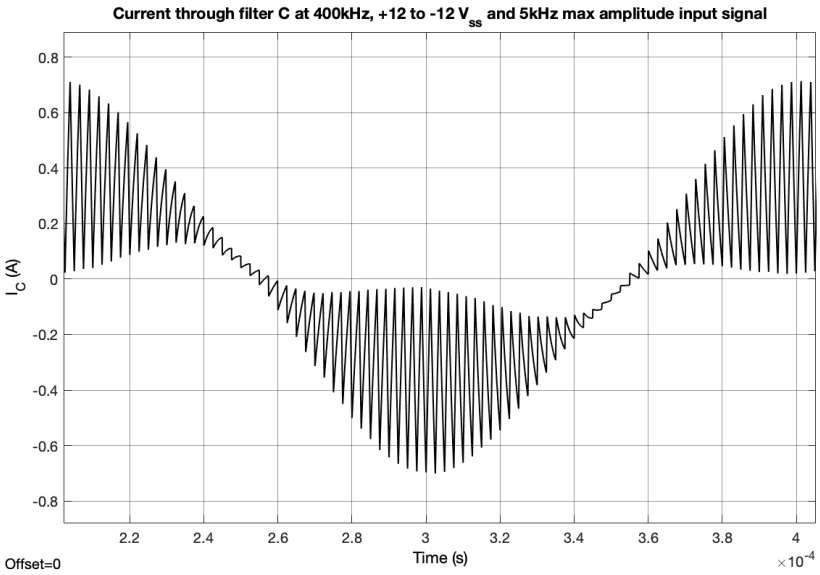

Figure 5.2: *Current through the capacitor of the class D amplifier of figure 2.1 with AC input signal*

The ripple current through the capacitor for a DC input at 0.5 input signal can be seen in figure 5.3. Current is plotted against the voltage. As mentioned in the method, this ripple under 0Vdc load is the basis situation for the ripple reduction analysis.

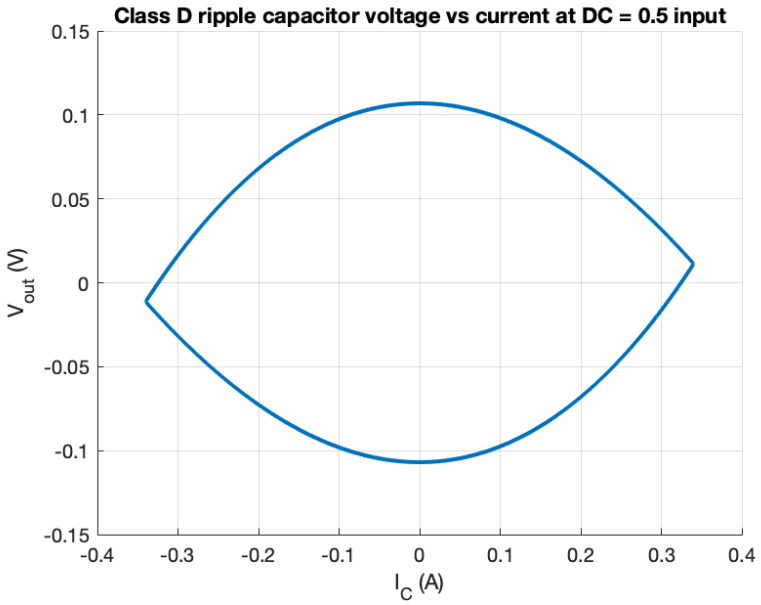

Figure 5.3: *Current versus voltage through the capacitor of the class D amplifier of figure 2.1 with DC input signal*

Now, the result of figure 5.3 needs to be compensated by the MOSFET in series with the capacitor. In figure 5.4, the same circle plot as figure 5.3 is shown, but with the inverse of the voltage at the same current. In other words: that is the range of voltage-current combinations that the MOSFET must be able to make to accomplish full voltage ripple reduction. In the same figure, the range of drain-source voltages that the MOSFET can make for every drain current is plotted. The overlapping zone is marked green. This is the range of voltage-current

combinations that the MOSFET would be able to compensate for.

The highlighted green area is approximately 12,3% of the total ripple. That means, the MOSFET is able to create 12,3% of the existing voltage-current relations of the ripple. The opacitive marked green area is not included in this number, since these values are in the transition between the triode and saturation region of the MOSFET. With these values included, the MOSFET can maximally create roughly 20% of the values of the ripple.

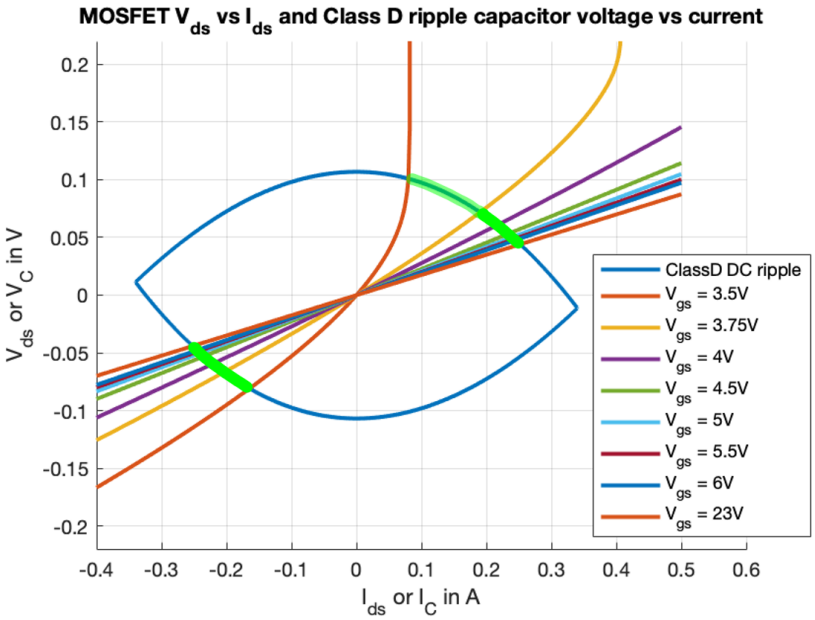

Figure 5.4: *The voltage-current combinations of a surface-potential based MOSFET model and the voltage-current combinations of the ripple in the capacitor of a class D amplifier*

It is also possible to look at the same overlap area of figure 5.4 in time. This is shown in figure 5.5. This figure shows the voltage ripple over the load, the current ripple in the capacitor, and the resistance that is needed to create that voltage given the current. This is the resistance that the MOSFET needs to have in order to be able to compensate the voltage ripple at that point in time. The green zone is the range of resistance values that can be made with V_{gs} between 3.75V and 23V (see table 5.1 for the values). In time, each green area covers 4.5% of the full period. This means that full voltage ripple compensation can only be achieved during 9% of the period. On top of that, the voltage can be partially reduced in a maximum of 50% of the period, but since the wanted resistance shoots to infinity, the reduction will be very minimal.

V_{gs}	R_{ds}
3.75 V	361 mΩ
4 V	285 mΩ
4.5 V	240 mΩ
5 V	218 mΩ
5.5 V	204 mΩ
6 V	199 mΩ
6.5 V	193 mΩ
23 V	175 mΩ

Table 5.1: R_{ds} *values for different* V_{gs} *of a surface-potential based MOSFET model*

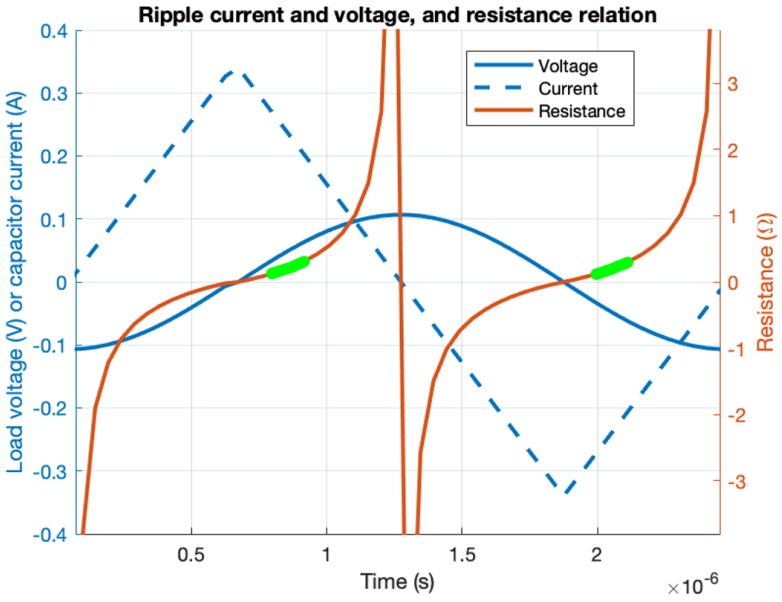

Figure 5.5: *The voltage over the load (blue), the current absorbed by the capacitor (blue dotted) and the division of both expressed in Ohms (orange). In green the resistor values are marked that the MOSFET can create.*

Chapter 6

Discussion

6.1 MOSFET discussion

Differences between level 3 and surface-potential based MOSFET models The level 3 model and the surface-potential based model show different results in every region that is examined. Firstly, in weak-inversion, only the surface-potential based model follows the theoretical ideal behaviour of a V_{gs}-dependent I_{ds}. The level 3 model seems to have a predefined fixed leakage current for all sub-threshold V_{gs}. Secondly, the transition to the saturation phase seems to have a discontinuous derivative in the level 3 model. Finally, the surface-potential based model seems to lack a internal model of the body diode.

Effect on ripple reduction The differences between the two MOSFET models can favour one or the other to use in the proposed ripple reduction application. However, when considering the working area in the application, the triode region, the differences are not very significant. In theory, the weak inversion region will not be used, as is the same for the saturation region. However, this may depend on the actual implementation. For example, if a straightforward PI or PID controller is used, it is hard to limit the minimum and maximum values of the controller output to limits that are real-time dependent on other parameters. This would be needed, since the regions are dependent on both V_{gs} and V_{ds}. Otherwise, the system may make use of other regions than the triode region.

The effect of the body diode by negative V_{ds} is very important. Currently, in the results the surface-potential based model was used, so the resulting values are calculated for a model without body diode. In future implementations, the effect of the body diode can cause sudden discontinuous changes around -0.6V. The control system must then be fast enough to react accordingly.

Simulink as an electrical modelling system The differences between the two MOSFET models are profound, but both models can be used in any application, as long as the limitations are known. This research highlights just a few of the many differences between different types of MOSFET models. The limitations are especially of importance when a well-simulated and tested application is realised with actual components. The choice of model should be chosen based on the best performance in the region of interest.

6.2 Ripple reduction discussion

Integrating vs linear The first thing that becomes immediately clear in the results is the small common voltage-current relations that the switching ripple and the MOSFET share (see figure 5.4). This can be explained by the fact that the switching ripple has an integrating behaviour from the capacitor, while the MOSFET acts as a resistor. The integrating behaviour of the current causes a 90 degree phase shift between the current and the voltage, whereas the resistive MOSFET only has linear voltage-currernt relations between. This results in the following set of voltage-current relations:

- positive current with positive voltage (Capacitor and resistor)
- positive current with negative voltage (Capacitor)
- negative current with positive voltage (Capacitor)
- negative current with negative voltage (Capacitor and resistor)

This would ideally leave only 50% of voltage ripple over the capacitor in time to be compensated with the MOSFET. However, that is still not the case, since in the positive and negative quadrant, the MOSFET is not able to make *all* of those values (as can be seen from figure 4.9). A different type of MOSFET is therefore only going to improve marginally. For every MOSFET, only the same two quadrants can be made.

Control Apart from the small number of voltage-current relations shared between the MOSFET and the switching ripple, the control of the MOSFET is an interesting aspect. As can already be seen from figure 5.5, the needed resistance value goes to plus and minus infinity. This is due to the fact that the current can become 0A. Secondly, if the voltage becomes 0V, the needed resistance value is 0Ω, which can only be approximated with a real world MOSFET.

A feed forward control may need both the current and voltage in its implementation to calculate V_{gs}, for example using equation 4.5. In such an implementation, the 0-values of the current and voltage will introduce problems, with output values of the controller approaching infinity. On the other hand, a feedback design with a PID controller is difficult with respect to the bounded output values, as already mentioned in the 'Effect on ripple reduction' paragraph in the MOSFET discussion.

DC Another major limitation is that this evaluation on the possible ripple cancellation only covers a ripple around 0Vdc output load. In the music application where this amplifier is designed for, the AC input on the system will cause both the output AC signal as well as the ripple to change, as can be seen from figure 5.1 and 5.2. The possibilities to reduce the ripple under different AC loads are not researched.

Chapter 7

Conclusions

The conclusions will be drawn by answering the main research question and the sub-questions. The sub-question were:

1. What type of MOSFET model can be used in Simulink simulation with switching ripple reduction in mind?
2. How can the FET be controlled with a maximum ripple reduction in mind?
3. What are the effects in terms of current ripple, voltage ripple, efficiency, complexity and feasibility?

Question 1 The level 3 MOSFET model has some drawbacks compared to the surface-potential based model. In weak inversion, the level 3 model only models a constant drain-source current, while based on theory an exponential relation with the gate-source voltage was expected. Secondly, the change between the triode region and the saturation region is discontinuous. Based on these two reasons, the surface-potential based model is more favorable for this application. However, in the latter there is no body diode modelled in, but that is of no concern for this application. Concluding, both models might be suitable, since the triode region is theoretically the only operating region in this approach.

Question 2 The ripple can only be fully compensated 9% of the time and only partially at maximum 50% of the time. Also, the maximal range of values that the MOSFET can create is 12% up to a maximum of 20% of the values that are needed for full compensation. If a feed forward design was to be implemented, it would have to deal with being turned on (during reduction opportunities) and off (during negative resistance time) a lot. On top of that, the zero-crossings of the voltage and current will complicate the design. Also, an AC input signal would make the controller even more complicated. A feedback design would have to deal with similar limitations, as well as with output limitations that vary depending on the load.

Question 3 As mentioned, full reduction cannot be accomplished, and partial reduction is still very limited. First of all, a MOSFET in triode cannot not reduce the full switching, due to the fact that the MOSFET acts as a resistor and the ripple is the result of a capacitor. This means the average ripple in the load can be reduced, but this might result in steep edges in the ripple waveform. A MOSFET with different parameters might improve these results only marginally.

Even though very little ripple reduction can be achieved, the solution is very power efficient, since there is no DC power consumed.

In the output stage of the amplifier, the solution very easy. However, the complexity is in the control of the MOSFET. A feed-forward design can be chosen, but with AC input signals

this will become very comprehensive. A feed-back design might be a solution, in similar fashion as feedback class D amplifiers.

Concluding, the solution is not feasible. A real world realisation is still far fetched. A controller would become very complicated and the ripple reduction would be very small.

Can the switching ripple in a class D amplifier be reduced by placing a MOSFET in series with the capacitor in a second order LC output filter?

The answer to the main research question is: Yes, a MOSFET can be used to reduce the switching ripple, but not by much. At best, a theoretical 20% reduction can be achieved. In time, only 9% of the signal can be fully reduced. The solution is very power efficient, but adds a lot of control complexity. Also, a real-world implementation would come with many realisation challenges.

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