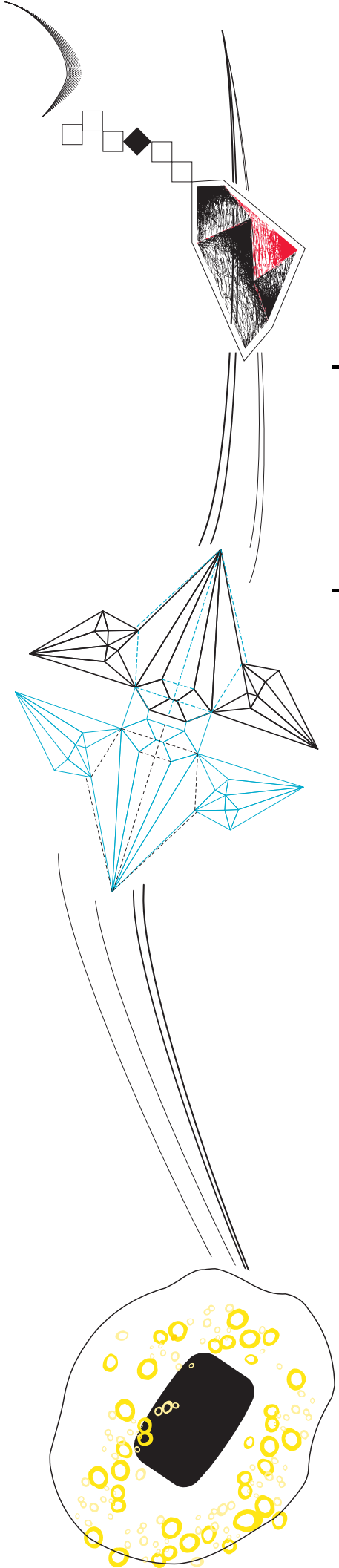

Master thesis

Faculty of Electrical Engineering,
Mathematics and Computer Science

Interface trap density extraction from the subthreshold slope of FDSOI devices

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Preface

During my Bachelor studies in Advanced Technology at the University of Twente I became interested in solid-state physics and semiconductor devices. Especially the switching and amplifying behaviour that could be obtained using these devices amazed me. Therefore, I continued with a master in Electrical Engineering. I followed mainly courses on circuit design and the underlying physics, and I followed courses regarding the fabrication processes used for state-of-the-art devices. After an internship on the modeling of the mobility in GaN transistors, I decided that I wanted to continue working on subjects requiring both measurements and simulations. For my master thesis I went to the Integrated Devices and Systems group, then still the Semiconductor Components group, and was offered the opportunity to work on the extraction of traps in state-of-the-art FDSOI material from Global Foundries. I could not let this opportunity pass and am proud to present the findings and conclusions of this 40 ECTS master thesis project.

Acknowledgements

First, I would like to extend my sincere gratitude to Jurriaan Schmitz and Ray Hueting. Jurriaan Schmitz is the main supervisor of my master thesis project and he is chair of the Integrated Devices and Systems research group at the University of Twente. He offered me the opportunity to work on this assignment, helped me getting started with initial reading material and helped me with the measurement set-up. Additionally, I appreciate the many fruitful discussions regarding the obtained measurement results and draft versions of this report. Then, I would like to thank Ray Hueting, associate professor at the Integrated Devices and Systems group at the University of Twente, and my second supervisor, for handing me additional reading material and for helping me with the TCAD simulation set-up. Additionally, the long discussions regarding the theory and TCAD simulations results have helped me tremendously. I would like to thank Anne-Johan Annema, associate professor at the Integrated Circuit Design group at the University of Twente and external member of my graduation committee, for insightful discussions on theoretical topics and for disccussions about the assumptions made in the described models. This helped me a lot with maintaining the motivation to better understand the underlying theory. Additionally, Anne-Johan is the developer of ProMOST. He helped me getting started with the ProMOST simulation tool and with the BSIM input files. I would like to thank all three of my graduation committee members for tirelessly listening to my many questions, and for patiently answering them.

I would like to thank Gerard Wienk, supporting staff at the Integrated Circuit Design group, for all his work regarding encountered computer or server problems. I would also like to thank Susan Janse-Godschalk, secretary of the Integrated Devices and Systems group, for all group communications forwarding and the planning of several discussion and presentation sessions. Finally, I would like to thank my girlfriend, family and housemates, and all other personnel at the Integrated Devices and Systems and Integrated Circuit Design groups, students and staff alike. During discussions with many of them, or explaining problems to many of them, I found that trying to formulate a question usually results in formulating the answer as well. This was a very useful concept for me and has helped a lot with obtaining the results shown in this work.

Contents

Chapter 1

Introduction

In 1926 the field-effect transistor (FET) was filed for a patent by Lilienfeld. The theoretical description of the FET presented in this patent steered the industry towards fabricating such a device. In 1947, some years later, Bardeen and Brattain invented and fabricated the point-contact transistor. Shockley described the improvements that diffusion contacts would have on this design in 1952. These were the first steps towards the fabrication of solid-state electronic amplification.

This was the beginning of a new electronics industry when Gordon Moore described the advantages of cramming more components, mainly transistors, onto integrated circuits, in 1965 [1]. He described several observations about integrated circuits: the high reliability of integrated circuits in comparison to conventional electronics at that time, the high yields of integrated circuits and the fact that there is no fundamental obstacle to achieving yields of 100%. Most importantly, he described that the cost per component is inversely proportional to the number of components, and that adding more components on a wafer would result in a decreasing yield such that the cost per component increases. From this he observed a minimum in costs at any given time in the evolution of the technology and this minimum in costs decreased over time as more components were being crammed on a certain chip area. [1] This trend is better known as Moore's law: the number of components per integrated function that yields the minimum component costs increases at a rate of roughly a factor of two per year. The number of transistors, or metal-oxide-semiconductor FETs (MOSFETs), per chip area would thus drastically increase.

MOSFET scaling

Dennard et al. then described the MOSFET scaling rules for obtaining simultaneous improvements in the number of components per chip and the transistor switching speed and power dissipation in 1974 [2]. This gave Moore's law a scientific foundation and was quickly adopted by the semiconductor industry as the roadmap for providing systematic and predictable transistor improvements [3].

The constant field (CF) scaling scheme they proposed was the beginning of the happy scaling era. The scheme uses a constant scaling factor κ and scales the device parameters with this such that transistors can be miniaturized while maintaining the same electric field in the device, e.g. device dimensions such as the oxide thickness, gate length and gate width are scaled with $1/\kappa$, the doping is scaled with κ and the supply voltage and resulting current are scaled with κ [2]. The scheme assumes that the effects of source and drain parasitic resistances and velocity saturation are avoided by attempting to keep the drain electric field and power density constant [4].

A schematic of the MOSFET is shown in figure 1.1. In the schematic the length, oxide thickness and channel doping are shown. The width is in y-direction, out-of-plane, and is therefore not shown.

Then, in 1980, two additional schemes were proposed such that the overall scaling trend resembled the scaling observed in industry more closely. The proposed schemes were the constant voltage (CV) and

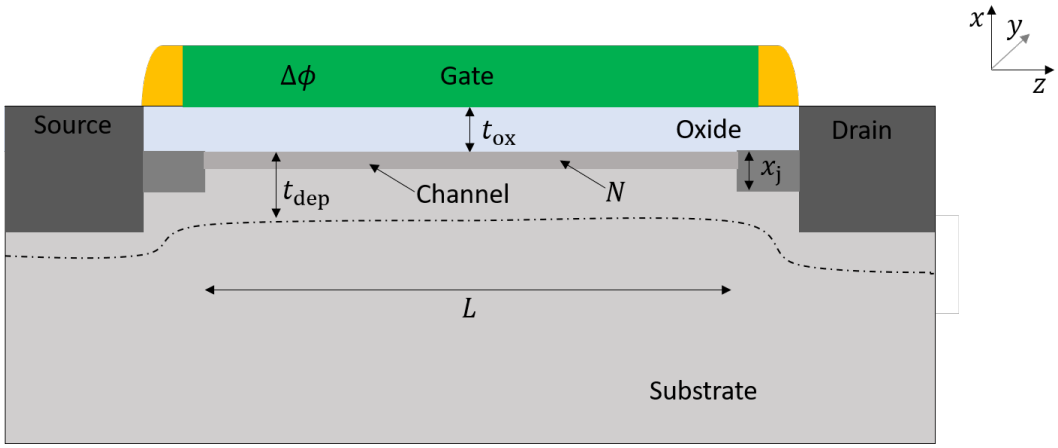


Figure 1.1: Schematic of MOSFET showing the source, drain, substrate and gate with gate workfunction $\Delta\phi$. The oxide layer has a thickness t_{ox}, the channel doping is denoted by N, the source and drain junction depth is denoted by x_j and the gate field penetration depth is denoted by t_{dep}. The distance between the two extension regions is called the electrical or effective gate length or channel length L. The (dielectric) spacers are shown in yellow. The width W of the device is out-of-plane (in y-direction) and is not shown.

quasi-constant voltage (QCV) schemes [4]. The CV scaling scheme maintains a constant supply voltage and scales the gate oxide more gradually, with $1/\sqrt{\kappa}$, to slow the growth of fields in the oxide. This leads to high drain fields and hot carrier related reliability problems [5, 6, 7]. Also, transistors scaled down with this scheme are operated close to severe junction depletion width extensions and oxide breakdown fields [4].

Therefore, scaling with the CF scheme was generally more desired. However, the industry was reluctant to scale down the operating voltages because of the increased difficulty in designing circuit boards for chips that operate at different supply voltages and because scaling down the power supply tends to increase the delay [8]. The industry thus avoided scaling down power supplies for as long as possible.

The QCV scaling scheme scales the supply voltage more slowly than the CF scheme and scales the oxide more rapidly than the CV scheme. One could say that the QCV scheme adopts the good predictions of oxide thickness scaling and doping scaling presented by the CF scheme, with the reluctance to scale the power supply included. Therefore, this scheme is the better indicator of the observed trends in industry until 1995 [8].
The device scaling laws for the three different schemes are summarized in table 1.1.

Description	Parameter	Constant Field (CF)	Quasi-constant Voltage (QCV)	Constant Voltage (CV)
Device Dimensions	L, W	$1/\kappa$	$1/\kappa$	$1/\kappa$
Oxide Thickness	t_{ox}	$1/\kappa$	$1/\kappa$	$1/\sqrt{\kappa}$
Power Supply	V_{DD}	$1/\kappa$	$1/\sqrt{\kappa}$	1
Channel Doping	N	κ	κ	κ

Table 1.1: Device scaling laws for constant field (CF), quasi-constant voltage (QCV) and constant voltage (CV) schemes with scaling factor κ.

MOSFET scaling limits

Scaling of the MOSFET with the discussed scaling schemes could not continue indefinitely. The encountered problems with scaling the MOSFET and the solutions to these problems had to be re-considered and are described next.

The scaling rules assumed that the threshold voltage V_{T} would scale along with the operating voltage, but this ignored the impact of the transistor subthreshold leakage current on the overall chip power consumption. The subthreshold leakage current between source and drain was relatively low when the CF scheme was developed and had only a small contribution to the power consumption. After 30 years of scaling, the leakage current has drastically increased and due to the leakage constraints, difficulties in further scaling the threshold voltage and thus in scaling the power supply result. [3]

Furthermore, scaling down the oxide thickness eventually resulted in oxides of effectively only 1 - 2 nm thick and thus of only a few atoms thick. It would therefore become physically impossible to further scale down the oxide thickness. Also, the direct tunneling current for these thin oxides results in a noticeable gate leakage current. [3] Different insulator materials with a higher dielectric constant, called high-k dielectrics, were incorporated such that the effective oxide thickness (EOT) still decreased. Here, EOT= $t_{\mathrm{ox}}\varepsilon_{\mathrm{k}}/\varepsilon_{\mathrm{ox}}$ with ε_{k} the dielectric constant of the high-k material and $\varepsilon_{\mathrm{ox}}$ the dielectric constant of silicon dioxide. With these materials implemented the limit for scaling down the oxide thickness was reached.

Also, reducing the MOFET channel length results in the threshold voltage becoming dependent on the effective gate length and the applied drain to source voltage. These non-ideal deviations are called short-channel effects (SCE) and the effect of only the drain to source voltage (V_{DS}) on the threshold voltage is a typical SCE called drain-induced barrier lowering (DIBL) [9, 10]. The SCE and especially the DIBL pose a limit for the scaling down of the transistor length, as the ratio between the on-current and off-current, and the amplification given by the product of the transconductance g_{m} and the drain to source resistance R_{DS}, significantly reduce [11]. The effects of the SCE and the DIBL can be translated into electrical parameters with the Voltage-Doping Transformation model proposed by Skotnicki et al. [12].

The threshold voltage for the MOSFET device can be obtained from:

$$V_{\mathrm{T}} = V_{\mathrm{T}\infty} - \Delta V_{\mathrm{T,SCE}} - \Delta V_{\mathrm{T,DIBL}}, \tag{1.1}$$

with $V_{\mathrm{T}\infty}$ the threshold voltage for a long-channel device and with the two ΔV_{T}-terms the influence of SCE and DIBL, as stated by the subscript. The following equations for the influence of SCE and DIBL on the threshold voltage can be used [9, 13]:

$$\Delta V_{\mathrm{T,SCE}} = 0.64\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\left(1+\frac{x_{\mathrm{j}}^2}{L^2}\right)\frac{t_{\mathrm{ox}}t_{\mathrm{dep}}}{L}\cdot\phi_{\mathrm{b}} \equiv 0.64\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\cdot\mathrm{EI}\cdot\phi_{\mathrm{b}} \tag{1.2}$$

and

$$\Delta V_{\mathrm{T,DIBL}} = 0.80\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\left(1+\frac{x_{\mathrm{j}}^2}{L^2}\right)\frac{t_{\mathrm{ox}}t_{\mathrm{dep}}}{L}\cdot V_{\mathrm{DS}} \equiv 0.80\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}}\cdot\mathrm{EI}\cdot V_{\mathrm{DS}}, \tag{1.3}$$

with $\varepsilon_{\mathrm{si}}$ and $\varepsilon_{\mathrm{ox}}$ the dielectric constants of silicon and the oxide, respectively, L the effective or electrical gate length, or channel length, ϕ_{b} the channel-extension potential barrier (or drain or source built-in voltage), x_{j} the source and drain junction depth and t_{dep} the penetration depth of the gate field in the channel region or the depletion region width. The EI parameter is the electrostatic integrity factor and depends on the device geometry. The parameter describes the influence of the electric field lines from the drain on the channel region and should be minimized. The EI will be discussed in more detail further on in this introduction. The observed decrease in threshold voltage due to a decrease in gate length is called threshold voltage roll-off [9]. Even when keeping the supply voltage constant the threshold voltage thus decreases for decreasing transistor lengths.

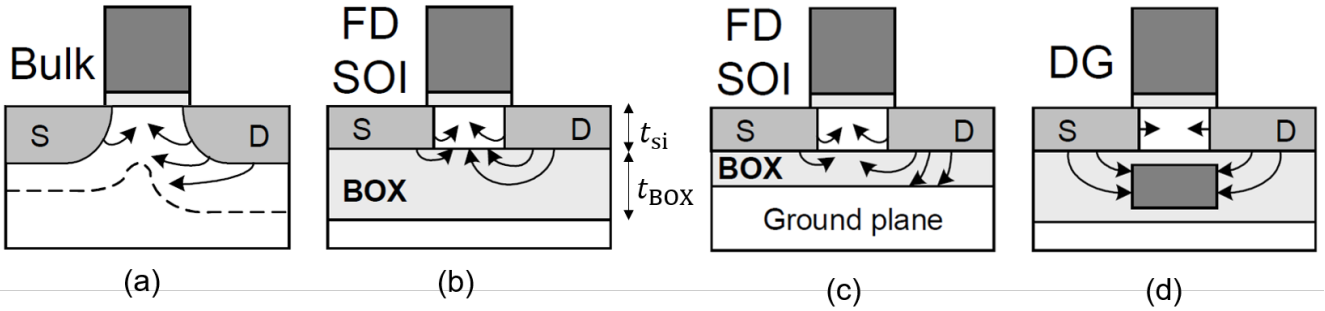


Figure 1.2: Evolution of electrostatic integrity factor. From left to right: bulk MOSFET, single gate (SG) FDSOI FET with thick BOX layer, SG FDSOI FET with thin BOX layer and highly doped substrate and double gate (DG) FET [9]. The silicon channel or film thickness t_{si} and the BOX thickness t_{BOX} are indicated. The black arrows depict the electric field lines from source and drain, as represented by the EI.

Because scaling down of the oxide thickness reached the limit, the depletion depth and junction thickness control the EI. The technological solutions for improving the EI were an increase of local channel doping and the implementation of ultra-shallow junction processes [13]. However, the variability of transistors increased due to the higher channel doping and the resulting threshold voltage mismatch between transistors became unacceptable for e.g. memory circuits [13].

The scaling laws [2, 4] assumed that the channel doping could continuously increase to enable shorter channel lengths. Next to the addressed threshold voltage mismatch, there are two other reasons why this is not the case. For a too high channel doping the impurity scattering increases such that the mobility degrades. Also, the high fields across the oxide result in a high silicon surface electric field. In the highly doped overlap region between gate and drain band bending greater than the silicon band gap energy is produced over a short vertical distance. Band-to-band tunneling can result within this depleted region and a leakage current from drain to bulk could be formed. This drain junction leakage effect is known as gate-induced drain leakage (GIDL). [8]

Using thin silicon films for the channel resulted in a better EI because the depletion depth is then limited to the film thickness (in equations 1.2 and 1.3) such that the channel did not have to be highly doped anymore, solving the channel doping issues [14]. Since less variability could be achieved by using undoped (or lightly doped) channels, switching from bulk MOSFETs to thin-film devices was highlighted as the best solution for improving the EI [13]. The evolution of the electrostatic integrity factor EI for various device structures is shown in figure 1.2 and will be discussed now.

Thin channels could be realized by placing the silicon channel on a buried oxide (BOX) layer such that the so-called silicon-on-insulator (SOI) FET is obtained. For thin enough channels, the depletion region extends all the way through the channel such that the silicon is fully depleted (FD), as explained in appendix A. The changing depletion width observed for bulk devices is thus circumvented for FDSOI. However, the integration of the transistor with the thick BOX layer resulted in electrostatic coupling within the BOX layer due to the penetration of the electric field. This effect was accounted for in the EI by the λ fitting parameter such that the EI is given by [13, 9]:

$$\mathrm{EI} = \left(1 + \frac{t_{si}^2}{L^2}\right) \frac{t_{ox}(t_{si} + \lambda t_{BOX})}{L}. \tag{1.4}$$

The bulk MOSFET and the SOI FET with an EI as given above are shown in figure 1.2(a) and (b), respectively.

Thinning down the BOX layer (reducing t_{BOX}) and increasing the substrate doping directly under the BOX layer was the solution to this problem since this reduces the electrostatic coupling factor λ in

the given equation. Then, the substrate under the BOX layer would function as a ground plane and the EI became mainly controlled by the silicon channel thickness [13, 9]:

$$\mathrm{EI} = \left(1 + \frac{t_{\mathrm{si}}^2}{L^2}\right) \frac{t_{\mathrm{ox}} t_{\mathrm{si}}}{L}. \tag{1.5}$$

This situation is depicted in figure 1.2(c). Instead of using the substrate as ground plane, a second gate could could be placed at the other side of the silicon channel such that the charge in the channel is controlled from two sides. The EI for a symmetrical DG device results and is given by [9]:

$$\mathrm{EI} = \frac{1}{2}\left(1 + \frac{1}{4}\frac{t_{\mathrm{si}}^2}{L^2}\right) \frac{1}{2}\frac{t_{\mathrm{ox}} t_{\mathrm{si}}}{L}. \tag{1.6}$$

This situation is depicted in figure 1.2(d). For improving the EI, both the silicon channel thickness and the BOX thickness thus had to be reduced for single gate (SG) FDSOI devices and the silicon channel had to be reduced for DG devices.

An emerging problem for thin-film devices was the high on-resistance. This problem could be circumvented with the adaptation of a raised source and drain (RSD) region. Another advantage of this is the reduced source and drain region resistance as result of the larger geometrical area. Additionally, the RSD allows for strain engineering such that the mobility in the channel could be improved [15, 16]. This will be discussed in more detail in theory section 2.12.

From an electrostatic integrity point of view, the DG device has the natural advantage of looking twice as thin as the equivalent SG (FDSOI) transistor in figure 1.2, as indicated by the factor of 1/2 in equation 1.6 when compared to equation 1.5. An example of a symmetrical DG device is obtained when the channel is vertically placed on either the substrate or the SOI layer to form a fin and create a so-called bulk or SOI FinFET, respectively. The FinFET is a symmetrical DG device and will be elaborated on in theory section 2.1. This way, a clear comparison with (SG and asymmetrical DG) FDSOI devices can be made.

Despite the better electrostatic integrity achievable for symmetrical DG devices, the FDSOI platform has a lot of advantages. The main advantage of FDSOI devices is the separate second gate which can be biased in order to achieve a variety of threshold voltages. Biasing the second gate, or back-gate, with a positive voltage results in a lower threshold voltage such that the device can be switched faster. This is called Forward body biasing (FBB). Applying a negative potential to the back-gate allows for the threshold voltage to increase such that lower static consumption is obtained [13]. The FDSOI platform is thus well-equipped for internet-of-things (IoT) and sensing applications [16]. Also, FDSOI devices can be co-integrated with bulk devices, since the fabrication processes can be adapted without an area penalty [13]. The technology can thus also be used for systems where the performance of the FDSOI structure is a disadvantage, such as for electrostatic discharge (ESD) diodes.

In this study we examine the FDSOI devices of the Global Foundries 22FDX platform [15, 16, 17].

Interface traps

The Global Foundries 22FDX platform has technologically feasible, extremely thin BOX and Si channel layers such that both front- and back-gate of the FDSOI devices have electrostatic control over the charge in the channel [15, 16, 17]. Mainly interface traps between silicon and front oxide/buried oxide limit the electrostatic control of the gates as will be discussed in the theory, chapter 2. Quantification of these traps is thus needed for further improving the technology or for better use of the devices, and comprises three parameters: the trap density, the energy signature of the traps and the trap time constant.

Conduction in semiconductors involves both drift and diffusion. The free carriers needed for this are obtained from generation. The trapping of these carriers in crystal defects results in recombination. The

trapped charges are freed after some time due to lattice vibrations, called de-trapping. These trapping/de-trapping events result in charge fluctuations and a single trapping/de-trapping event is called a Random Telegraph Signal (RTS). Such a signal is defined by a waveform with an on-state and an off-state and the transitions between these two states are characterized by trapping and de-trapping time constants [18].

The trap density describes the number of traps per unit volume or area and can depend on the spatial coordinates x, y and z. Here, the y- and z-directions describe the trap fluctuations over the oxide interface and the x-direction describes how deep into the oxide or silicon channel the trap levels are. The energy signature is expressed as the energy value within the band gap the traps occupy. This gives information about the type of material or compound responsible for the trap. The trapping and de-trapping time constants give information about the mean time spent in either state (trapped/not trapped) and about the interaction speed of traps. In summary, the interface trap density has to be determined as a function of space and energy and the trapping and de-trapping time constant have to be considered in order to fully understand the behaviour of traps.

Trap density extraction methods

Several methods for extracting this interface trap density have been reported for bulk devices, usually assuming a uniformly distributed trap density such that the spatial dependence in y- and z-direction can be neglected, as summarized by Schroder [19]. The flatband voltage can be related to the trapped charges. This can be used in combination with capacitance-voltage measurement methods. The theoretical and experimental capacitance curves for the flatband capacitance, i.e. the capacitance at the flatband voltage, are then compared in order to extract the trapped charges. Several low frequency (or quasi-static) and high frequency capacitance measurement methods rely on this approach. Another method, the conductance method, relies on extracting the conductance divided by frequency as function of frequency for an MOS capacitor or FET and from that determine the interface trap density and capture time constant. This is the most complete method and one of the most sensitive methods to determine the interface trap density. For SOI FETs these approaches are difficult to use, because at low frequencies the gate leakage is too high and at high frequencies there is a too large series resistance. [19]

The Charge Pumping Method can be used to describe the interface trap density by performing measurements on a MOS capacitor or FET configuration. This is one of the only reliable methods that can actually be applied to SOI material, but only an average trap density over the entire subthreshold regime can be extracted using this method. The interface trap density would thus not be known as function of energy. Also, a body contact is needed to supply the majority carriers and this contact is normally unavailable for SOI material. For the Charge Pumping Method the source and drain are tied together and a pulse is applied to the gate. The resulting charge-pumping current is used to determine the interface trap density. [19]

The interface trap density can also be extracted from the subthreshold slope. The average subthreshold slope over the subthreshold regime has been used to extract an average interface trap density for bulk devices. However, this method was recently adjusted for the application to SOI FinFETs because body contacts are unavailable for SOI FinFETs [20]. The method was adjusted using the symmetry of the FinFET device and uses the subthreshold slope to determine the interface trap density at each specific gate voltage value. Translating the gate voltage to energy then enables the extraction of the interface trap density as function of energy. This extended subthreshold method, called g_m/I_D-method, has the advantage that it contains a simple and elegant model, can be used on FET devices instead of MOS capacitor configurations and that it works for a wide variety of FinFET geometries. For the extraction of the interface trap density in asymmetric FDSOI material a method using the subthreshold slope was proposed as well [21]. This method assumes no interface traps at one of the interfaces. An extension of this method which incorporates both interfaces was proposed [22], but this method uses the comparison of measurement data with an elaborate numerical model and thus significantly reduces the simplicity.

Additionally, both methods proposed for FDSOI material ([21] and [22]) are tested for devices with thick front and buried oxide layers as well as the silicon channel and it is therefore inconclusive if these methods would work for state-of-the-art material.

Report outline

The objective of this research is to find or develop a methodology to extract the trap density at the interfaces for FDSOI FETs against the energy. The main challenge is that FDSOI FETs are asymmetric devices; there are different interfaces and the electrostatic control of the two gates is different. Additionally, it is then desired to determine the trap contribution at each interface specifically. A comparison between symmetric and asymmetric devices is made from an electrostatic viewpoint to exemplify this challenge. Then, several approaches have been investigated, such as employing the $g_{\mathrm{m}}/I_{\mathrm{D}}$ method [20, 23] and employing a combined effort of experiments and analytical modeling [21, 24, 25, 26, 27], compact modeling [22] or TCAD simulations.

Chapter 2

Theory

2.1 FDSOI and FinFET structures

A schematic cross-section of a bulk FinFET is shown in figure 2.1. The left inset figure shows a bird's eye view of the FinFET with the gate layer over the fin in x-direction. The electrons go from source to drain in z-direction for an n-type FET (and holes go in z-direction from source to drain for a p-type FET), following the black arrows depicted. A cross-section of the device along the x-axis over the gate is taken and zoomed-in. The figure shows the fin width W, the fin height H and the oxide thickness t_{ox} of the gate insulator material between the gate and fin. The silicon substrate on which the fin is placed is also shown. The source and drain are out-of-plane and are thus not shown. The current thus flows in the direction of fin length L, which is also out-of-plane. Note that the gate controls the charge in the fin from left and right side and that the gate can only be controlled by a single voltage, i.e. both sides are connected to each other. Basically, since the aspect ratio H/W of the fin is relatively high, the structure can be considered to be a symmetric double gate (DG) FET.

The schematic of an SOI transistor is shown in figure 2.2. The axis system is defined such that the electrons travel in z-direction and the gate controls the channel in x-direction here as well. The length of the channel or body L, the front oxide (FOX) thickness t_{ox1} and burried oxide (BOX) thickness t_{ox2}

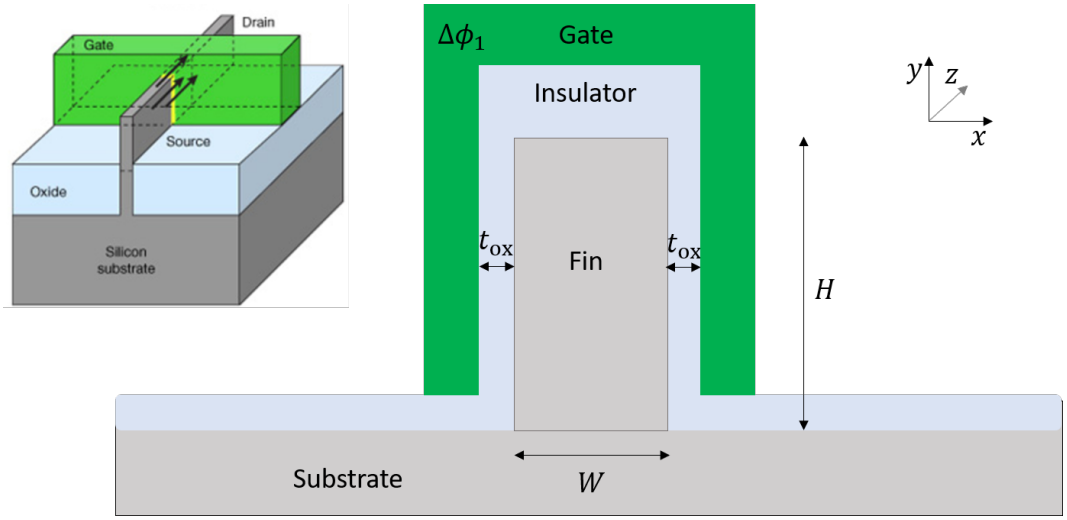


Figure 2.1: A bird's eye view of a FinFET is shown on the top left with substrate, drain, source, gate and oxide denoted [28]. A cross-section along the gate is shown enlarged. The fin height H and width W are shown, just as the gate workfunction $\Delta\phi_1$ and the oxide thickness t_{ox}. The length of the channel is in the z-direction such that source and drain are not shown.

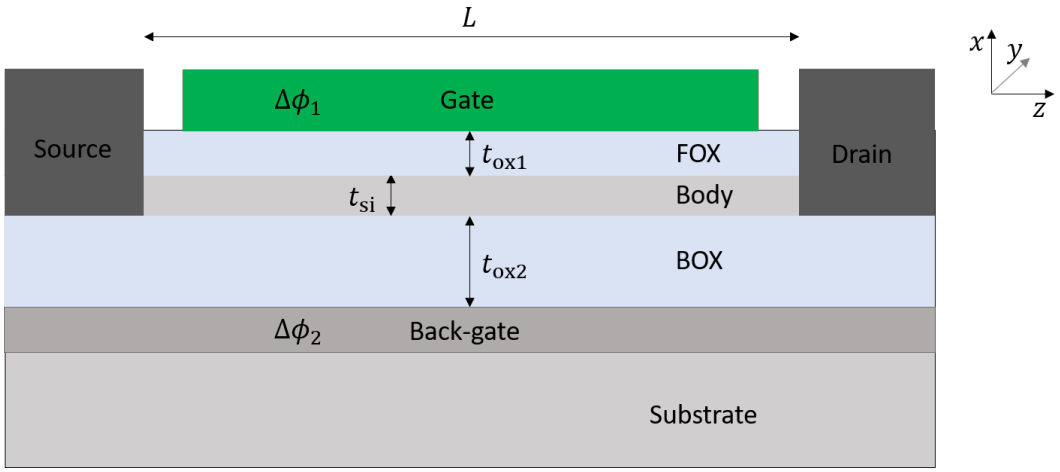


Figure 2.2: Schematic of FDSOI device showing source, drain, gate, back-gate and substrate. The gate workfunction is $\Delta\phi_1$ and the back-gate workfunction is $\Delta\phi_2$. The silicon channel or body thickness is denoted t_{si} and the front-oxide (FOX) and buried oxide (BOX) thickness are denoted t_{ox1} and t_{ox2}, respectively.

and the channel or body thickness t_{si} are indicated. The lightly doped silicon area between the BOX and silicon substrate is called a well. This well can be positively or negatively doped, resulting in a p-well or n-well, respectively, and can be controlled as a second gate or back-gate. The well is denoted as back-gate in the figure. If the SOI device is rotated by 90 degrees an electrostatic comparison with the FinFET device can be made. The left and right part of the FinFET gate are then the equivalent of the gate and back-gate of the SOI device and the left and right oxide correspond to FOX and BOX. The Fin width thus translates to the body thickness and the fin height translates to the body width. The major difference between the two is that the FinFET is in principle symmetric (along the y-axis) and the SOI transistor is not (along the z-axis); the gate and oxide material and the oxide thicknesses of top and bottom parts are different for the SOI device whereas they are the same for the FinFET (for the left and right part). The difference in gate material is denoted by the workfunction $\Delta\phi_x$ with $x = 1, 2$ in the figures. Also, for the SOI device the gates can be separately controlled while this is not possible for FinFET devices.

2.2 Interface trap density estimation in FinFETs

A method to extract the inferface trap density in SOI FinFETs in the subthreshold regime was proposed in [20]. For the method, long-channel devices are used such that short-channel effects can be neglected. We use as criterion that devices with a much higher effective gate length than the characteristic length exhibit long-channel behaviour, as explained in appendix A. The method is explained for NMOS devices but can in principle also be applied to PMOS devices. Also, like in most other extraction techniques, the interface trap density is assumed to be uniform over space and, consequently, only varies as a function of energy. In more detail, we use $D_{it}(x, y, z, E) = D_{it}(x, E)$ where an infinitely thin layer of traps at the interface is assumed such that the x-dependence of D_{it} can be described with a δ-function. The main advantage of this method is that no contact to the silicon film, or body, is required. Also, the method can be used to extract the interface trap density from actual transistor devices, instead of having to use MOS capacitor configurations hence capacitance-voltage (C-V) measurements. The question is, however, whether this interface trap density estimation method could be used for FDSOI devices.

The method is based on the fact that in subthreshold every change in the gate voltage, and thus change in the amount of charge on the gate, changes the amount of charge in the channel accordingly. However, some of these counter-charges in the channel are trapped at the silicon channel to gate insulator

interface, thus reducing the number of free (counter) charges in the channel. This deviation in channel charge with respect to the expected ideal situation can thus be used to estimate the interface trap density. The channel charge relates to the drain current, and consequently, the drain current as function of gate to source voltage can be used to determine the interface trap density.

It should be mentioned that the relation between subthreshold drain current and gate to source voltage is exponential, and not linear. This is because electrons are minority carriers governed by diffusion. Either way, the product of number of holes and electrons stays the same in the channel such that an exponential relation is obtained for the charge carrier density against the gate to source voltage V_{GS}. The basic methodology behind the extraction of the interface trap density is described below. For a more detailed analysis, the reader is referred to [20] and [23].

The drain current for a fully depleted SOI FinFET device in subthreshold is given by:

$$I_{\mathrm{D}} = I_0 \cdot \exp\left(\frac{\psi_{\mathrm{s}}}{u_{\mathrm{T}}}\right)\left(1 - \exp\left(-\frac{V_{\mathrm{DS}}}{u_{\mathrm{T}}}\right)\right), \tag{2.1}$$

with thermal voltage $u_{\mathrm{T}} = k_{\mathrm{B}}T/q$ where k_{B} is Boltzmann's constant, T is the temperature and q is the elementary charge, V_{DS} is the applied drain-to-source voltage, ψ_{s} is the surface potential at the silicon channel and gate oxide interface and

$$I_0 = q\mu_n n_{\mathrm{i}} u_{\mathrm{T}} \frac{WH}{L}, \tag{2.2}$$

where μ_n is the electron mobility, n_{i} is the intrinsic carrier density and W, H an L are the fin width, height and length, respectively, and where this relation holds for a rectangular channel. The cross-sectional area WH can be changed to πR^2 with wire radius R for the method to be applied to nanowire devices.

The drain current as function of gate voltage in the subthreshold regime is often shown on a log-lin scale. The slope is called the subthreshold slope and the inverse of this slope is called the subthreshold swing (SS). The subthreshold swing is given by

$$SS \equiv \frac{dV_{\mathrm{GS}}}{d\log_{10}(I_{\mathrm{D}})} = \frac{dV_{\mathrm{GS}}}{d\psi_{\mathrm{s}}}\frac{d\psi_{\mathrm{s}}}{d\ln(I_{\mathrm{D}})}\ln(10) = m \cdot u_{\mathrm{T}} \cdot \ln(10), \tag{2.3}$$

where the surface potential and gate voltage are related to each other through the ideality factor or body factor [20]:

$$m \equiv \frac{dV_{\mathrm{GS}}}{d\psi_{\mathrm{s}}} = \frac{1}{u_{\mathrm{T}}}\frac{I_{\mathrm{D}}}{g_{\mathrm{m}}} = 1 + \frac{C_{\mathrm{it}}}{C_{\mathrm{ox}}}. \tag{2.4}$$

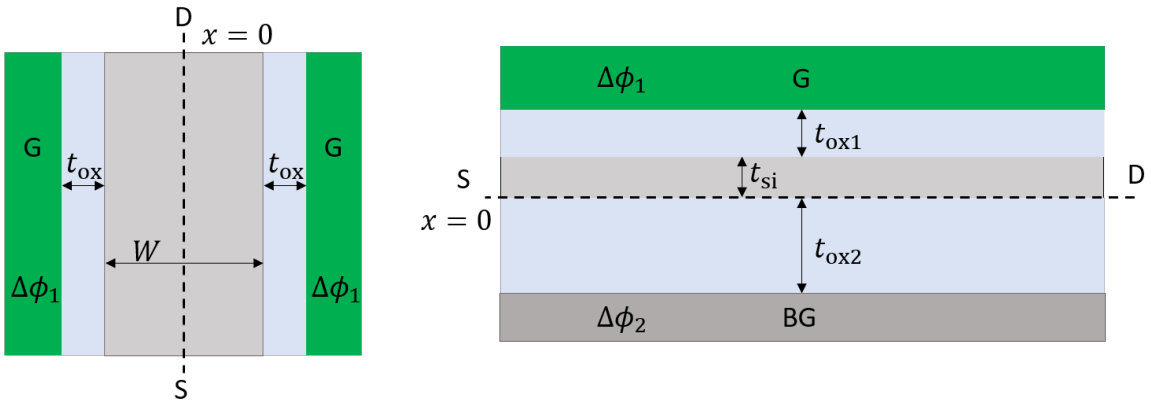
Here, a uniform electric field is assumed and the depletion capacitance is neglected for the fully depleted device. For the second step the transconductance $g_{\mathrm{m}} \equiv dI_{\mathrm{D}}/dV_{\mathrm{GS}}$ is used and the result is rearranged to obtain m on the left-hand side. For the third and last step a simplified one-dimensional capacitor configuration scheme is used where C_{ox} is the oxide or insulator capacitance and C_{it} is the interface trap capacitance. An elaborated analysis of this last step will be given in the next sections.

Following from the above relation the interface trap density can be expressed as function of the insulator capacitance and the ratio between drain current and transconductance as [20]:

$$D_{\mathrm{it}}(\psi_{\mathrm{s}}) \equiv \frac{C_{\mathrm{it}}(\psi_{\mathrm{s}})}{q^2} = \frac{1}{q^2}\left(\frac{1}{u_{\mathrm{T}}}\frac{I_{\mathrm{D}}(\psi_{\mathrm{s}})}{g_{\mathrm{m}}(\psi_{\mathrm{s}})} - 1\right)C_{\mathrm{ox}}. \tag{2.5}$$

For a known temperature and insulator capacitance, the interface trap density can thus simply be obtained from the ratio between drain current and transconductance in the subthreshold regime. The method is called $g_{\mathrm{m}}/I_{\mathrm{D}}$-method for this reason. Also, the interface trap density can thus be probed with the gate voltage, corresponding to the value of the surface potential, for FinFET devices. The energy increases in exactly the same way as the surface potential does with increasing gate voltage such that:

$$E - E_{\mathrm{v}} = \frac{E_{\mathrm{g}}}{2} + q \cdot \psi_{\mathrm{s}}. \tag{2.6}$$



(a) (b)

Figure 2.3: Simplified structures without interface traps are schematically shown for a) the FinFET and b) an SOI FET. A top view (xz-plane in figure 2.1) of the FinFET is shown with the axis of symmetry indicated by the dashed line. Note that $W = 2t_{si}$ when comparing the EI (as discussed in the introduction) of the symmetric DG devices and asymmetric devices with the second gate as ground plane.

The surface potential can be extracted from the drain current using equation 2.1. A measured drain current as function of gate to source voltage in the subthreshold regime can therefore be used to obtain the interface trap density as function of energy, using equations 2.5 and 2.6. The accuracy of the method is limited by the drain current and transconductance measurement error and by the temperature measurement error, as can be deduced from equation 2.5. The error propagation derivation is given in [23].

2.3 Basic electrostatics

The relation between the surface potential and gate voltage in FinFETs is different from that in FDSOI devices due to the asymmetry in FDSOI devices. In order to comprehend this difference the basic electrostatics of both devices is first discussed using a single model for both weak and strong inversion. For a symmetric double gate (DG) device such as a FinFET, the oxide thickness, material and gate workfunction are the same for gate 1 and 2. For an asymmetric DG device such as a SOI transistor, this is not the case. Both situations are shown in figure 2.3. The asymmetric device used in the following example is only asymmetric in workfunction, i.e. gate 1 has an n+ workfunction and gate 2 a p+ workfunction.

The band diagram of a symmetric DG device with a metal workfunction slightly less than at midgap and the band diagram of an asymmetric device are shown in figure 2.4. The band diagram for the symmetric DG device is shown in 2.4(a) at thermal equilibrium. For the asymmetric DG device the band diagram is shown in 2.4(c) at thermal equilibrium. Applying a gate bias of $V_{GS} = V_T$, with threshold voltage V_T the voltage needed for the onset of strong inversion, results in figures 2.4(b) and (d) for the symmetric and asymmetric cases, respectively. Taur determined the potential profile between the oxide plates as a function of the distance without an applied drain to source voltage ($V_{DS} = 0$ V) for a symmetric DG device [24] and for an asymmetric DG device [25] and he determined the potential profile with an applied drain to source voltage for symmetric DG devices [26]. The cases without applied drain-to-source voltage are discussed here.

Starting with the Poisson equation for an n-type device:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \exp\left(\frac{q\psi}{k_B T}\right), \tag{2.7}$$

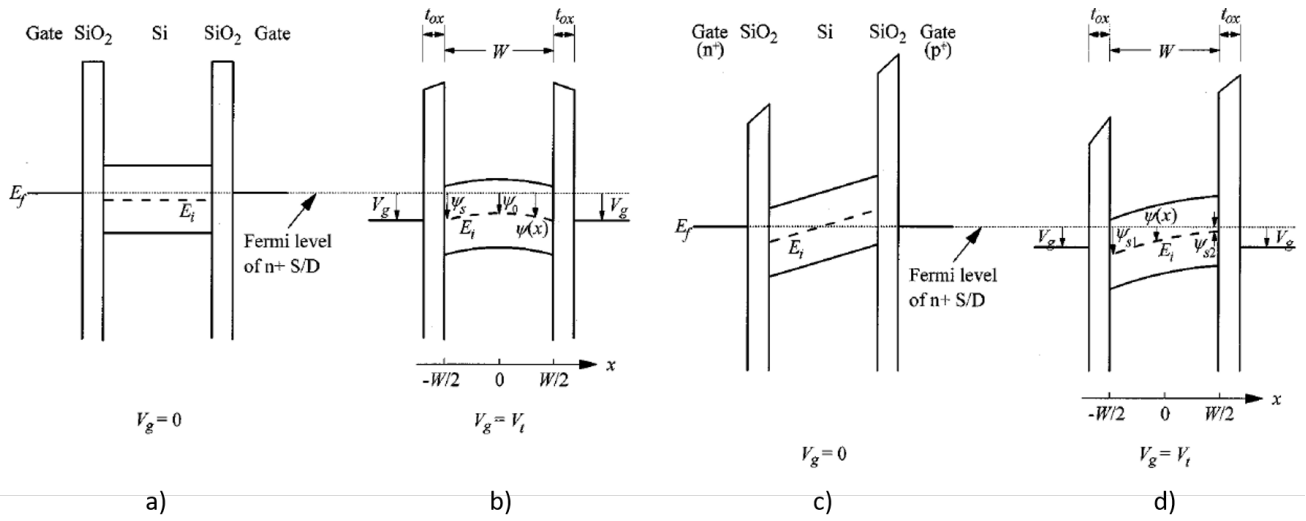


Figure 2.4: Band diagrams of symmetric and asymmetric double gate (DG) devices. Taken from Taur et al. [25]. Figures (a) and (c) show the band diagrams in thermal equilibrium for symmetric and asymmetric devices, respectively. Figures (b) and (d) show the band diagrams when $V_{\mathrm{G}} = V_{\mathrm{T}}$ is applied.

and integrating twice with respect to x using the symmetry boundary condition ($\frac{d\psi}{dx}|_{x=0} = 0$) for a symmetric DG device yields [24]:

$$\frac{q\left(\psi - \psi_0\right)}{2k_BT} = -\ln\left(\cos\left[\sqrt{\frac{q^2 n_{\mathrm{i}}}{2k_BT}}\exp\left(\frac{q\psi_0}{2k_BT}\right)x\right]\right), \tag{2.8}$$

with ψ_0 the lowest potential and thus the potential in the center between the plates, i.e. $\psi_0 = \psi(x = 0)$.

The surface potential is obtained from this by noting that $\psi_s = \psi(x = \pm W/2)$ with W the distance between the plates in figure 2.4. The above equation can simply be extended to the asymmetric case for situations with gate voltages high enough to ensure that both the left and right surface potentials are positive. In that case, the profile is still symmetric, but the minimum potential ψ_0 is not at $x = 0$. In equation 2.8 the x on the RHS can then simply be replaced by $x - x_0$, with x_0 the new minimum potential coordinate which does not have to be between the plates [25].

The minimum potential ψ_0 and, in the asymmetric case, x_0, can be solved from the boundary conditions that relate the surface potentials to the gate to source voltage on left and right hand sides. For example, in figure 2.4(d) the minimum potential is approximately at the right interface such that $x_0 \approx W/2$. For the symmetric case the surface potential at both sides is equal and a minimum potential ψ_0 is observed at the middle between the two oxide plates, where the Fermi level is maximum. For the asymmetric case the resulting surface potentials at the left and right oxide interface, ψ_{s1} and ψ_{s2} respectively, are different for an equal potential applied to both gates. The potential profile is thus asymmetric over the distance between the plates.

An FDSOI device is an asymmetric DG device. As was explained, the device has a thinner top (or front) oxide than bottom oxide, these oxides are mostly made out of a different material, and the top gate material is different from the bottom gate material such that the gates have a different workfunction. Due to different processing steps needed for fabricating the FDSOI device, the silicon body/FOX interface is different from the body/BOX interface, and thus the top and bottom interface trap densities can also be different. Especially if interface traps are added, it would be difficult to define a single analytical model that captures the complete transistor behaviour in both weak and strong inversion for FDSOI devices. Because of this, and since extracting the interface trap density from the subthreshold regime proved fruitful ([20, 21, 22]), we continue with a description of both symmetric and asymmetric devices in the subthreshold regime.

How to operate the FDSOI device, or rather any asymmetric device, in subthreshold then still has to be discussed. Applying an equal voltage to both gates results in an equal surface potential at both interfaces for a symmetric device, while different surface potentials are obtained for an asymmetric device. To obtain a method as elegant as the g_m/I_D-method for the extraction of interface traps in asymmetric FDSOI devices, it would make sense to apply a gate voltage, which could be different for the two gates, such that an equal surface potential at both interfaces results. In that case, we still have a symmetric potential profile in the channel. However, FDSOI devices are normally operated differently. The front gate is used the same as the gate in both FinFETs and bulk MOSFETs, but to the back gate a fixed voltage is applied. This fixed back gate voltage results in an increase or decrease of the threshold voltage such that more dynamic transistor behaviour is obtained. We would thus like to also examine the possible application of this varying front gate/fixed back gate voltage configuration, as it is more similar to the general use of FDSOI devices.

In conclusion: In the following sections we will start with a description of both symmetric and asymmetric devices in the subthreshold regime. Then, we will investigate the possibility of applying either 1) a varying front gate voltage with a fixed back gate voltage or 2) a varying voltage to both front and back gate such that an equal surface potential results.

2.4 Drain current in subthreshold regime

We consider long channel devices only, such that short-channel effects can be neglected. Hence, 1-dimensional electrostatics are discussed. Considering that the free carrier charge in the channel can be neglected in the subthreshold region, it follows that a linearly varying potential (LVP) is present across the body [29, 30, 27]. This is a simplified form of equation 2.8, which is valid only for low gate voltages hence subthreshold.

The drain current for an n-type ultra-thin body (UTB) DG device in the subthreshold regime is then given by [31]:

$$I_D = \mu_n Q \frac{\partial E_{Fn}}{\partial n} \approx \mu_n u_T \frac{dQ}{dx} = \mu_n u_T \left(\frac{Q_S - Q_D}{L} \right) = \mu_n u_T \frac{Q_i}{L} \left(1 - \exp\left(\frac{-V_{DS}}{u_T} \right) \right), \tag{2.9}$$

with Q_i the free carrier inversion charge obtained from integration of the carrier density $n(x)$ over the silicon channel [32]:

$$Q_i = q \int_0^{t_{si}} n(x) \cdot dx = -q n_i t_{si} u_T \left(\frac{\exp\left(\frac{\psi_{s2}}{u_T}\right) - \exp\left(\frac{\psi_{s1}}{u_T}\right)}{\psi_{s2} - \psi_{s1}} \right). \tag{2.10}$$

With the relations between the surface potential(s) and gate voltage(s) for symmetric and asymmetric DG devices the drain current in the subthreshold regime can thus be computed.

In case a symmetric DG device is considered, $\psi_{s1} = \psi_{s2} = \psi_s$. A first order Taylor expansion of equation 2.10 around $\psi_{s2} - \psi_{s1}$ then results in [31]:

$$Q_i = -q n_i t_{si} \exp\left(\frac{\psi_s}{u_T} \right), \tag{2.11}$$

which results in the same drain current as described for the g_m/I_D-method.

The drain current is now obtained as a function of the surface potentials. Assuming we have negligible recombination in the hole-devoid channel, the relation between the drain current and the surface potentials is independent of interface traps. The relation between the surface potentials and the gate voltage, the electrostatics, does depend on the interface trap density. For the g_m/I_D-method, the ideality factor is extracted from the drain current (as function of V_{GS}) using equation 2.3. Then, the interface trap capacitance is extracted from this using equation 2.4. For asymmetric UTB DG devices, such as FDSOI

devices, we will therefore evaluate the relations for the surface potentials and ideality factors, with as goal to obtain an equation similar to equation 2.4. We discuss both symmetric and asymmetric cases for comparison.

2.5 Electrostatics in subthreshold regime

From the boundary conditions at the silicon-insulator interfaces in combination with the LVP profile resulting from the Poisson integration the following two relations between front and back gate voltage and front and back surface potential are obtained by Wouters et al. [29]:

$$V_{\mathrm{GS1}} = V_{\mathrm{FB1}} + \psi_{\mathrm{s1}} \left(\frac{C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}}{C_{\mathrm{ox1}}} \right) + \psi_{\mathrm{s2}} \left(-\frac{C_{\mathrm{si}}}{C_{\mathrm{ox1}}} \right) + \frac{|Q_{\mathrm{D}}|}{2C_{\mathrm{ox1}}}, \tag{2.12a}$$

$$V_{\mathrm{GS2}} = V_{\mathrm{FB2}} + \psi_{\mathrm{s2}} \left(\frac{C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}}{C_{\mathrm{ox2}}} \right) + \psi_{\mathrm{s1}} \left(-\frac{C_{\mathrm{si}}}{C_{\mathrm{ox2}}} \right) + \frac{|Q_{\mathrm{D}}|}{2C_{\mathrm{ox2}}}, \tag{2.12b}$$

where V_{FB1} and V_{FB2} are front and back flat band voltages, C_{ox1} and C_{ox2} are front and back oxide capacitances per unit area, C_{it1} and C_{it2} are the front and back interface trap capacitances per unit area, respectively, $C_{\mathrm{si}} \equiv \varepsilon_{\mathrm{si}}/t_{\mathrm{si}}$ is the depleted silicon film capacitance per unit area for a silicon body or channel of thickness t_{si}, and Q_{D} is the depletion charge per unit area. The flat band voltages are defined by $V_{\mathrm{FB}x} = \Delta\phi_x - Q_{\mathrm{ox}x}/C_{\mathrm{ox}x}$ with $x = 1, 2$ where $\Delta\phi_x$ is the workfunction difference between the gate material and silicon and $Q_{\mathrm{ox}x}$ is the oxide trapped charge.

A simple relation without interface traps given by Van der Steen et al. is first discussed to obtain better insights [31]. To obtain the same simplified relation, we assume $Q_{\mathrm{D}} = 0$ for the fully depleted film and take $C_{\mathrm{it1}} = C_{\mathrm{it2}} = 0$ for the case without interface traps. Also, a negligible drain to source voltage is assumed, i.e. $V_{\mathrm{DS}} \approx 0$. The equations are rewritten to the same form as obtained from the charge conservation relations by using Gauss' law:

$$\frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox1}}} \left(V_{\mathrm{G1}} - \Delta\phi_1 - \psi_{\mathrm{s1}} \right) = \varepsilon_{\mathrm{si}} F_1, \tag{2.13a}$$

$$\frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox2}}} \left(V_{\mathrm{G2}} - \Delta\phi_2 - \psi_{\mathrm{s2}} \right) = \varepsilon_{\mathrm{si}} F_2. \tag{2.13b}$$

We take $V_{\mathrm{G1}} = V_{\mathrm{G2}} = V_{\mathrm{G}}$ for the gate potential and note that in the subthreshold regime $\psi_{\mathrm{s2}} - \psi_{\mathrm{s1}} = -F_0\, t_{\mathrm{si}}$ with $F_0 = F_1 = -F_2$ a simple relation for the electric field in the channel is obtained [31]:

$$F_0 = \frac{\Delta\phi_2 - \Delta\phi_1}{\frac{t_{\mathrm{ox1}} + t_{\mathrm{ox2}}}{\varepsilon_{\mathrm{ox}}} + \frac{t_{\mathrm{si}}}{\varepsilon_{\mathrm{si}}}}. \tag{2.14}$$

Substitution of the above relation into equations 2.13 and rewriting to obtain the surface potentials results in [31]:

$$\psi_{\mathrm{s1}} = V_{\mathrm{G}} - \left[\frac{\Delta\phi_1 \left(\frac{t_{\mathrm{si}}}{\varepsilon_{\mathrm{si}}} + \frac{t_{\mathrm{ox2}}}{\varepsilon_{\mathrm{ox}}} \right) + \Delta\phi_2 \left(\frac{t_{\mathrm{ox1}}}{\varepsilon_{\mathrm{ox}}} \right)}{\left(\frac{t_{\mathrm{si}}}{\varepsilon_{\mathrm{si}}} \right) + \left(\frac{t_{\mathrm{ox1}} + t_{\mathrm{ox2}}}{\varepsilon_{\mathrm{ox}}} \right)} \right], \tag{2.15a}$$

$$\psi_{\mathrm{s2}} = V_{\mathrm{G}} - \left[\frac{\Delta\phi_2 \left(\frac{t_{\mathrm{si}}}{\varepsilon_{\mathrm{si}}} + \frac{t_{\mathrm{ox1}}}{\varepsilon_{\mathrm{ox}}} \right) + \Delta\phi_1 \left(\frac{t_{\mathrm{ox2}}}{\varepsilon_{\mathrm{ox}}} \right)}{\left(\frac{t_{\mathrm{si}}}{\varepsilon_{\mathrm{si}}} \right) + \left(\frac{t_{\mathrm{ox1}} + t_{\mathrm{ox2}}}{\varepsilon_{\mathrm{ox}}} \right)} \right]. \tag{2.15b}$$

From this final relation for the front and back surface potential of a DG device some important conclusions can be drawn. The surface potentials increase linearly with the gate voltage at both the front and back interface. Only the offset is different. Assuming $\Delta\phi_1 = \Delta\phi_2$ results in

$$\psi_{\mathrm{s1}} = \psi_{\mathrm{s2}} = V_{\mathrm{G}} - \Delta\phi_1, \tag{2.16}$$

such that taking a partially symmetric device or taking a fully symmetric device (where we also have $t_{ox1} = t_{ox2}$, i.e. a FinFET) results in the same relation for the surface potentials. The relation between the surface potential and gate voltage is equal for both cases and is independent of the oxide thickness. The same result is obtained for assuming $t_{ox1} \ll t_{ox2}$, which is the case for a strongly asymmetric device (such as an SOI device with a thick BOX layer) [31]. In other words, for both a fully symmetric device, a partially symmetric device (with only different workfunctions) and for a strongly asymmetric device (with negligible BOX capacitance) we obtain an ideality factor of unity, $\partial V_{GS}/\partial\psi_{s1} = \partial V_{GS}/\partial\psi_{s2} = 1$.

The ideality factor is unity for both symmetric and asymmetric devices, and thus for both FinFETs and FDSOI devices without interface traps. However, care should be taken for calculating the current, since the channel thickness has a different influence on the EI for both cases, as depicted by the dashed lines in figure 2.3. These dashed lines represent axes of symmetry from an electrostatic point of view, and can be regarded as a virtual ground. Then, it becomes evident that indeed a FinFET device has only half the effective channel thickness, $W \approx 2t_{si}$. This is in agreement with comparing the EI for SG FDSOI and DG devices (see introduction, equations 1.5 and 1.6).

Now incorporating the effect of the interface traps in equations 2.13 the charge conservation relations obtained are:

$$\frac{\varepsilon_{ox}}{t_{ox1}}\left[V_{G1} - \Delta\phi_1 - \psi_{s1}\left(1 + \frac{t_{ox1}}{\varepsilon_{ox}}C_{it1}\right)\right] = \varepsilon_{si}F_1, \tag{2.17a}$$

$$\frac{\varepsilon_{ox}}{t_{ox2}}\left[V_{G2} - \Delta\phi_2 - \psi_{s2}\left(1 + \frac{t_{ox2}}{\varepsilon_{ox}}C_{it2}\right)\right] = \varepsilon_{si}F_2. \tag{2.17b}$$

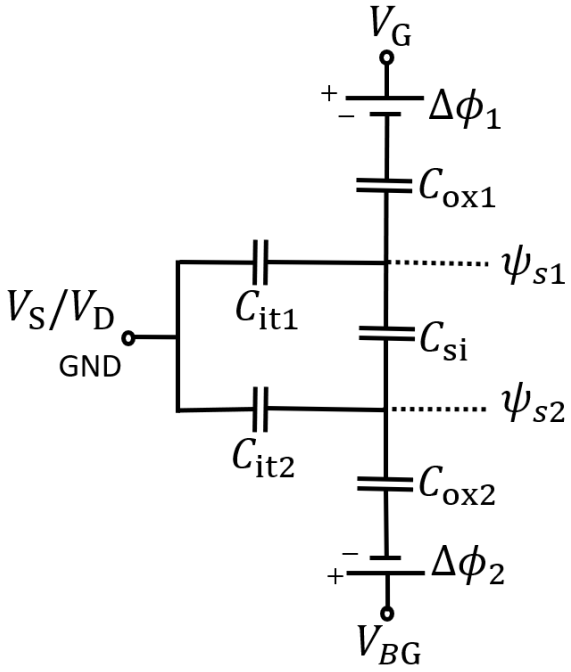


Figure 2.5: Capacitance division scheme for fully depleted DG devices ($Q_D = 0$). The scheme figuratively describes the electrostatic relation between the gate voltages and the surface potentials. Gate and back gate leakage currents and thus resistances are neglected. The lateral electric field is negligible for small V_{DS} such that the Fermi potential is defined by the source in the entire channel. We thus assume $V_{DS} \approx 0$ such that the ground of the electrostatic system is defined by the source Fermi potential. Subthreshold conditions are assumed: minority charge can in principle be ignored for the electrostatics.

Again using $\psi_{s2} - \psi_{s1} = -F_0 t_{si}$ with $F_0 = F_1 = -F_2$ we now find:

$$F_0 = \frac{\left(1 + \frac{t_{ox2}}{\varepsilon_{ox}} C_{it2}\right)(V_{G1} - \Delta\phi_1) - \left(1 + \frac{t_{ox1}}{\varepsilon_{ox}} C_{it1}\right)(V_{G2} - \Delta\phi_2)}{\left(1 + \frac{t_{ox1}}{\varepsilon_{ox}} C_{it1}\right)\frac{t_{ox2}}{\varepsilon_{ox}}\varepsilon_{si} + \left(1 + \frac{t_{ox2}}{\varepsilon_{ox}} C_{it2}\right)\frac{t_{ox1}}{\varepsilon_{ox}}\varepsilon_{si} + \left(1 + \frac{t_{ox1}}{\varepsilon_{ox}} C_{it1}\right)\left(1 + \frac{t_{ox2}}{\varepsilon_{ox}} C_{it2}\right) t_{si}}. \tag{2.18}$$

Substitution of the above relation into equations 2.17 and rewriting to obtain the surface potentials then results in:

$$\psi_{s1} = \frac{(V_{G1} - \Delta\phi_1) C_{ox1} (C_{si} + C_{ox2} + C_{it2}) + (V_{G2} - \Delta\phi_2) C_{si} C_{ox2}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}, \tag{2.19a}$$

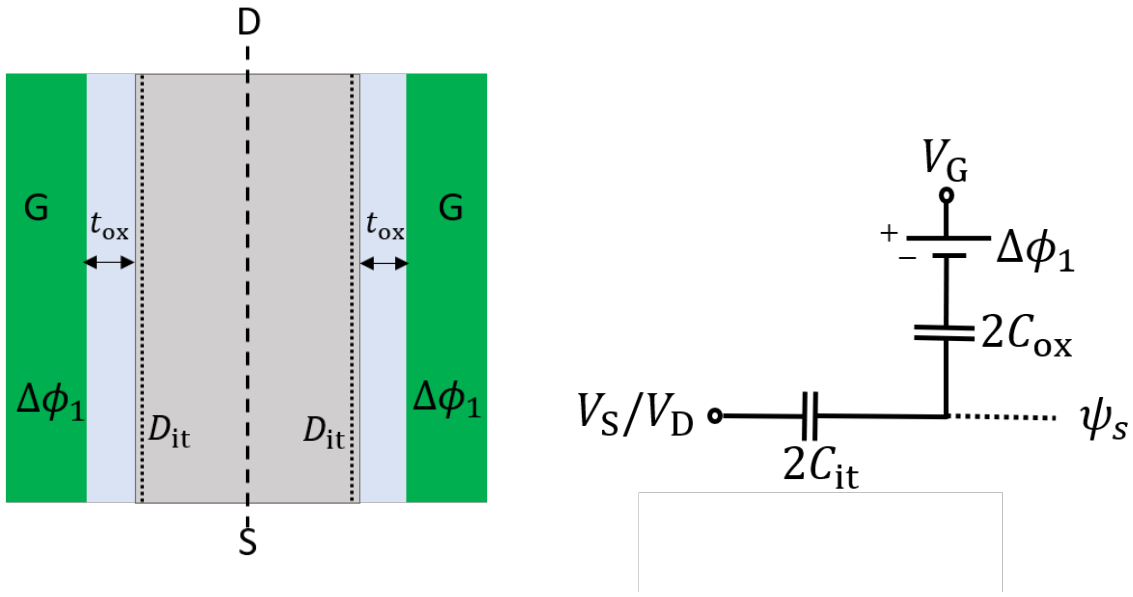
$$\psi_{s2} = \frac{(V_{G2} - \Delta\phi_2) C_{ox2} (C_{si} + C_{ox1} + C_{it1}) + (V_{G1} - \Delta\phi_1) C_{si} C_{ox1}}{(C_{si} + C_{ox2} + C_{it2})(C_{si} + C_{ox1} + C_{it1}) - C_{si}^2}, \tag{2.19b}$$

where $C_{oxx} = \varepsilon_{ox}/t_{oxx}$ with $x = 1, 2$ and where $C_{si} = \varepsilon_{si}/t_{si}$. We consider material with negligible oxide trapped charge, i.e. $Q_{oxx} = 0$ with $x = 1, 2$, and thus use $V_{FBx} = \Delta\phi_x$ in equations 2.12. Because $Q_D = 0$ for the fully depleted device, equations 2.12 and 2.19 are then equal. The result obtained here is thus the same as that obtained by Wouters et al. [29].

The capacitor division scheme corresponding to equations 2.19 is shown in figure 2.5. This scheme is valid when considering DC electrostatics and for neglecting leakage currents from the gate and back gate. The scheme can be used to obtain the surface potentials and from that the charge density, not necessarily the current. The current can be obtained from the product of the charge density and the electric field (with the field given by the slope in Fermi energy, Fermi potential, or electrochemical potential).

The relationships for the surface potentials reduce to the previously obtained equations 2.15 for $V_{G1} = V_{G2} = V_G$, $\Delta\phi_2 = \Delta\phi_1$ and $C_{it1} = C_{it2} = 0$. With the same assumptions this also follows from the capacitor division scheme in figure 2.5: the surface potentials become equal to each other and to the applied voltage.

When taking the front and back gate voltages equal it can be shown that the rate of change between surface potential and gate voltage, the ideality factor, is not unity anymore for a fully symmetric DG



(a) (b)

Figure 2.6: (a) Simplified FinFET structure with uniformly distributed interface traps and (b) corresponding capacitance scheme.

device. This is because the capacitor division scheme now also incorporates the interface trap capacitance. We substitute $C_{\mathrm{it1}} = C_{\mathrm{it2}} = C_{\mathrm{it}}$, $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = t_{\mathrm{ox}}$, $V_{\mathrm{G1}} = V_{\mathrm{G2}} = V_{\mathrm{G}}$ and $\Delta\phi_1 = \Delta\phi_2$ and obtain:

$$\psi_{\mathrm{s1}} = \psi_{\mathrm{s2}} = \psi_{\mathrm{s}} = \frac{V_{\mathrm{G}} - \Delta\phi_1}{1 + \frac{C_{\mathrm{it}}}{C_{\mathrm{ox}}}}. \tag{2.20}$$

The FinFET structure and capacitor division scheme corresponding to the given relation are shown in figure 2.6.

The ideality factor can be determined from the given relation to be

$$m = 1 + \frac{C_{\mathrm{it}}}{C_{\mathrm{ox}}}. \tag{2.21}$$

This corresponds to the scheme used for the $g_{\mathrm{m}}/I_{\mathrm{D}}$-method, i.e. the third term in equation 2.3. Methods to extract the interface trap density from FDSOI devices using the obtained surface potential and ideality factor relations will now be discussed. First we discuss the case of varying the front gate at a fixed back gate voltage, followed by the case with equal front and back surface potentials.

2.6 Single gate sweep for an asymmetric device

A relation for the subthreshold slope of an FDSOI device with varying front gate bias for a fixed back gate bias was derived in [29], where results are given depending on the applied back gate bias. The most important results for this work are discussed here and some additional information is added.

Figure 2.7 shows the potential distribution of an FDSOI device for varying front gate voltages at a fixed back gate voltage. The back surface potential then changes as the front gate voltage varies despite the fixed back gate voltage. This cross-coupling between front and back surface potentials at least has to be accounted for, for front and back surface potentials differing by more than u_{T} [29]. The device behaves differently for this front gate sweep at a fixed back gate bias depending on the major current contribution. In figure 2.7(a) the front channel drain current I_{D1}, i.e. the current near the front interface, dominates the total current for all drawn front surface potentials. Figure 2.7(d) denotes a situation where the back channel drain current I_{D2} dominates the total current despite the varying front surface potentials. Figures 2.7(b) and 2.7(c) show intermediate situations.

From the shown potential distributions it becomes intuitively apparent that the back gate voltage has an influence on the threshold voltage. Since the back gate voltage partially controls the back surface potential, the potential needed for inverting the channel can be increased or decreased with the back gate voltage. Therefore, the threshold voltage is influenced by the back gate voltage. A simple relation for this without accounting for interface traps is given by [13]:

$$\gamma = \frac{\Delta V_{\mathrm{T}}}{\Delta V_{\mathrm{BG}}} \approx \frac{C_{\mathrm{ox2}} C_{\mathrm{si}}}{C_{\mathrm{ox1}}(C_{\mathrm{ox2}} + C_{\mathrm{si}})} \tag{2.22}$$

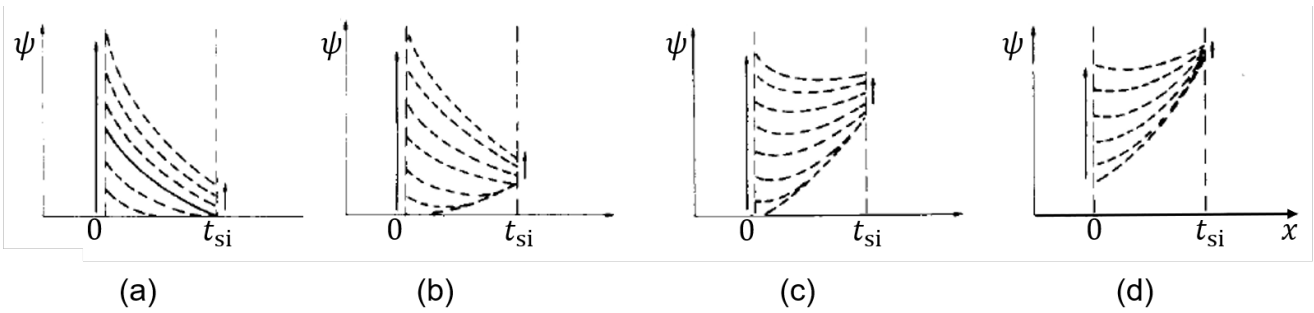


Figure 2.7: Schematic of the potential distribution for a front gate sweep at a different fixed back gate bias, increasing from (a) to (d) [29].

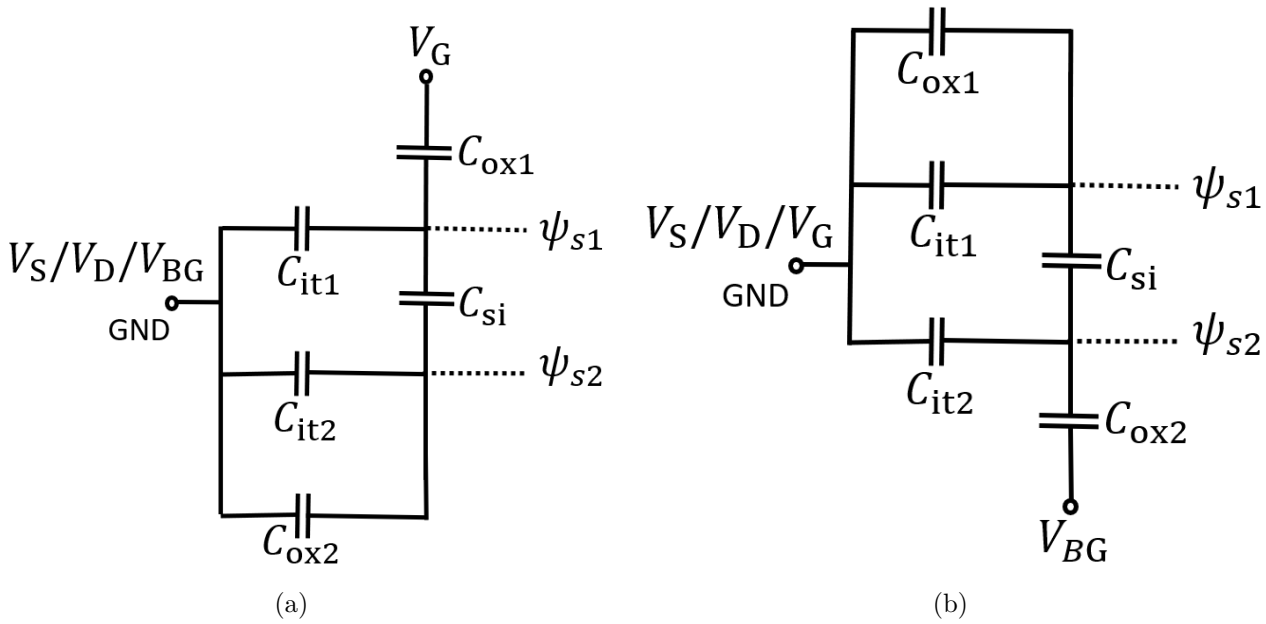


Figure 2.8: Schematically shown simplified capacitance scheme of an asymmetric device for a) $V_{\mathrm{BG}} = 0$ and b) $V_{\mathrm{G}} = 0$. For simplifying the comparison between the ideality factors we use $V_{\mathrm{G}} = V_{\mathrm{G1}} - \Delta\phi_1$ and $V_{\mathrm{BG}} = V_{\mathrm{G2}} - \Delta\phi_2$ in the figures.

This threshold voltage control is used in FDSOI circuit design to obtain a more dynamically applicable transistor. That is, the threshold voltage can be decreased to enhance performance or increased to reduce leakage. As the device is intended to be used like this, we examine the possibility of applying the varying front gate/fixed back gate voltage first.

The following discussion starts with obtaining an expression for the ideality factor for single gate control and continues with incorporating the cross-coupling between front and back surface potentials. With cross-coupling we mean the variation of the surface potential at the fixed gate interface as result of the variation of the other surface potential. In figure 2.7 the cross-coupling is schematically shown by the variation in the surface potential at the right interface, as indicated by the arrow.

We start with equation 2.19(a) and set $V_{\mathrm{G2}} - \Delta\phi_2 = 0$. Taking the derivative with respect to the front gate voltage, the following is found for the ideality factor:

$$m_{1,1} = \frac{dV_{\mathrm{G1}}}{d\psi_{\mathrm{s1}}} = 1 + \frac{C_{\mathrm{it1}}}{C_{\mathrm{ox1}}} + \frac{C_{\mathrm{si}}(C_{\mathrm{ox2}} + C_{\mathrm{it2}})}{C_{\mathrm{ox1}}\,(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})}, \tag{2.23}$$

where the subscript of the ideality factor $m_{a,b}$ corresponds to the two terms in the derivative, $V_{\mathrm{G}a}$ and $\psi_{\mathrm{s}b}$.

Starting with the capacitor division scheme given in figure 2.5(b) and taking $V_{\mathrm{BG}} \equiv V_{\mathrm{G2}} - \Delta\phi_2 = 0$ we arrive at the capacitor division scheme shown in figure 2.8(a). The scheme corresponds with the given relation for the ideality factor and is common in literature for describing the subthreshold behaviour of SOI devices [27, 29, 30]. In the scheme we also use $V_{\mathrm{G}} \equiv V_{\mathrm{G1}} - \Delta\phi_1$ because the given scheme can then more directly be compared to the given ideality factor. It can be noted that the first two terms of the right-hand side correspond to the ideality factor for a symmetric device, given by equation 2.4. The third term is the cross-coupling term and is equal to γ (equation 2.22) if the interface traps are neglected. Assuming the capacitance of the depleted silicon film (C_{si}) can be neglected, the given expression reduces to equation 2.4. This is expected since there is no cross-coupling through the silicon film. However, for devices with thin silicon films, as used here, this capacitance can no longer be neglected.

We would like to examine the influence of the interface traps on γ and thus check whether the cross-coupling term needs to incorporate the interface trap dependence. For this, we assume $C_{\mathrm{ox1}} = 2.66\ \mu\mathrm{F/cm^2}$ (i.e. $t_{\mathrm{ox1}} = 1.3$ nm), $C_{\mathrm{ox2}} = 0.17\ \mu\mathrm{F/cm^2}$ (i.e. $t_{\mathrm{ox2}} = 20$ nm) and $C_{\mathrm{si}} = 1.72\ \mu\mathrm{F/cm^2}$ (i.e. $t_{\mathrm{si}} = 6$ nm). For $C_{\mathrm{it2}} = 0.1\ \mathrm{nF/cm^2}$ the resulting cross-coupling is approximately equal with or without interface traps, $\gamma = 59.1$ mV/V. For $C_{\mathrm{it2}} = 0.1\ \mu\mathrm{F/cm^2}$ we obtain a cross-coupling of 88 mV/V and the influence of traps is thus significant. Actually, for $C_{\mathrm{it2}} > 1\ \mathrm{nF/cm^2}$ the interface traps are significant, as their influence is ~ 1 mV/V or more then.

To completely describe the behaviour of the device, the influence of the front gate voltage on the back surface potential is given as well:

$$m_{1,2} = \frac{dV_{\mathrm{G1}}}{d\psi_{\mathrm{s2}}} = \frac{(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})\,(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}) - C_{\mathrm{si}}^2}{C_{\mathrm{si}} C_{\mathrm{ox1}}}, \tag{2.24}$$

which can be derived both from equation 2.19b and from the capacitor scheme, similar to $m_{1,1}$.

The influence of the surface potential difference for non-linearly varying fields within the film is described next. Starting from a basic diffusion current equation, a box shaped carrier profile is used to approximate the inversion channel thickness as the distance over which the potential drops by u_{T} [29]. This is done in order to obtain a simple relation for the drain current which depends on the surface electric field. The $\frac{d\psi_s}{d\ln(I_D)}$-relation, which contributes to the subthreshold swing in equation 2.3, is now different from the previously obtained $\frac{d\psi_s}{d\ln(I_D)} = u_{\mathrm{T}}$. The increase in drain current with increasing surface potential (given by the $I_{\mathrm{D}}(\psi_{\mathrm{s}})$ relation) is now smaller as result of the increasing surface electric field. This increasing field results from the increasing front surface potential at a mildly increasing back surface potential (due to the fixed back-gate bias). The resulting inverse subthreshold slope incorporates a correction factor for this in the relation between drain current and front surface potential and the correction factor also incorporates the effect of channel depletion. The given equation for the subthreshold slope can therefore be applied to both FD and partially depleted (PD) SOI devices [29]:

$$\frac{d\ln(I_{\mathrm{D1}})}{d\psi_{\mathrm{s1}}} = \frac{1}{u_{\mathrm{T}}} - \frac{\frac{\partial}{\partial\psi_{\mathrm{s1}}}\left(\frac{\partial\psi(x)}{\partial x}\Big|_{x=t_{\mathrm{si}}}\right)}{-\frac{\partial\psi_{\mathrm{s1}}}{\partial x}} = \frac{1}{u_{\mathrm{T}}} - \frac{\frac{1}{t_{\mathrm{si}}}\left(1 - \frac{\partial\psi_{\mathrm{s2}}}{\partial\psi_{\mathrm{s1}}}\right)}{-\frac{\partial\psi_{\mathrm{s1}}}{\partial x}} = \frac{1}{u_{\mathrm{T}}} - \frac{\frac{1}{t_{\mathrm{si}}}\left[1 - \frac{C_{\mathrm{si}}}{C_{\mathrm{si}}+C_{\mathrm{it2}}+C_{\mathrm{ox2}}}\right]}{\frac{\psi_{\mathrm{s1}}-\psi_{\mathrm{s2}}}{t_{\mathrm{si}}} + \frac{qN_{\mathrm{A}}t_{\mathrm{si}}}{2\varepsilon_{\mathrm{si}}}}} \equiv \frac{1}{u_{\mathrm{T}}} - C, \tag{2.25}$$

where x is the direction along the channel height, as shown in section 2.1, and C is the correction factor. The numerator of this correction factor relation corresponds to the electric field at the front surface due to the back surface potential ψ_{s2} and the denominator corresponds to the front surface electric field due to front surface potential ψ_{s1}. The ratio thus shows the relative influence of (the inequality of) the two surface potentials on the front surface potential. So, for $\partial\psi_{\mathrm{s2}}/\partial\psi_{\mathrm{s1}} \to 1$, the correction term $C \to 0$ such that the same result is obtained as for the FinFET devices (for the relation between drain current and front surface potential). The qN_{A}-term in the denominator describes the film depletion in the silicon channel and this term can be neglected for fully depleted films (e.g. FD SOI). Then, the correction term simplifies to

$$C = \frac{1}{\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}}} \cdot \frac{C_{\mathrm{it2}} + C_{\mathrm{ox2}}}{C_{\mathrm{si}} + C_{\mathrm{it2}} + C_{\mathrm{ox2}}}, \tag{2.26}$$

such that

$$\frac{d\ln(I_{\mathrm{D1}})}{d\psi_{\mathrm{s1}}} = \left(u_{\mathrm{T}} \frac{(\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}})(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})}{(\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}})(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}) - (C_{\mathrm{ox2}} + C_{\mathrm{it2}})}\right)^{-1}. \tag{2.27}$$

The relation for the correction factor implies that $C \to \infty$ for $\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}} = 0$. However, in this case we have $\partial\psi_{\mathrm{s2}}/\partial\psi_{\mathrm{s1}} \to 1$ which results in $\frac{d\ln(I_{\mathrm{D1}})}{d\psi_{\mathrm{s1}}} = \frac{1}{u_{\mathrm{T}}}$ (see equation 2.25) and equation 2.26 is not valid then.

Combining the ideality factor $m_{1,1}$ and the corrected relation between surface potential and drain voltage results in the subthreshold swing of an FD SOI device, for sweeping the front gate voltage at a

fixed back gate voltage:

$$\frac{\partial V_{\mathrm{GS1}}}{\partial \log_{10}(I_{\mathrm{D1}})} = u_{\mathrm{T}} \frac{(\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}})(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})}{(\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}})(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}) - (C_{\mathrm{ox2}} + C_{\mathrm{it2}})} \left(1 + \frac{C_{\mathrm{it1}}}{C_{\mathrm{ox1}}} + \frac{C_{\mathrm{si}}(C_{\mathrm{ox2}} + C_{\mathrm{it2}})}{C_{\mathrm{ox1}}\,(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})}\right) \ln(10). \tag{2.28}$$

This equation is valid within the applied front gate voltage range where the front surface potential is higher than the back surface potential for the entire subthreshold region under consideration, i.e. $\psi_{\mathrm{s1}} > \psi_{\mathrm{s2}}$. In other words, the front channel current has to be higher than the back channel current for the entire subthreshold region under consideration. This is one of the three possible cases for front gate sweeping at a fixed back bias discussed in [29]. The two other cases are the following; 1) the back surface potential is higher than the front surface potential, such that the back channel current is dominant, and 2) the back surface potential is so low that the back channel is in accumulation. A severe degradation of the subthreshold slope results in both cases [29]. As a result, the interface trap density would be more difficult to extract in the two other cases.

Assuming the front and burried oxide thicknesses and the silicon film thickness to be known and constant, the interface trap capacitance is described as function of subthreshold swing and front and back surface potentials. The stated assumptions are the same as for the FinFET interface trap density extraction [20, 23]. Solely using equation 2.28 would still not enable the extraction of the interface trap density, as too many parameters remain unknown. A different model for the subthreshold swing was proposed in [27] and is shown in appendix B. However, this method uses a simplification on the relation between front and back surface potentials and is therefore too inaccurate for our goal. If a relation similar to equation 2.28 can be obtained for the back gate voltage at a fixed front gate voltage, it might be possible to extract the interface trap density using a single gate sweep method.

A method to determine the interface trap capacitance and thus the interface trap densities could be proposed at which the front channel subthreshold slope and the back channel subthreshold slope are determined for the same device. The formulation of the back channel subthreshold slope is similar to that of the front channel subthreshold slope (see equation 2.28) and the derivation is shown in appendix B. Performing measurements such that both surface potentials change at the same rate during both measurements (such that $\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}}$ is the same for both measurements) then allows for solving the system of two equations and two unknowns. However, also the surface potential difference has to be known for this method and this makes the procedure significantly more difficult to use.

2.7 Dual gate sweep for an asymmetric device

A method to determine the back interface trap density from the subthreshold current as a function of a simultaneous front and back gate sweep is described in [21]. The method relies on a constant back gate voltage V_{GS2} to front gate voltage V_{GS1} ratio such that $V_{\mathrm{GS2}} = kV_{\mathrm{GS1}}$. From the relations between front gate and back gate voltage as a function of front and back surface potentials (equations 2.12a and 2.12b) the derivatives of the surface potentials with respect to the front gate voltage, $\frac{d\psi_{\mathrm{s1}}}{dV_{\mathrm{GS1}}}$ and $\frac{d\psi_{\mathrm{s2}}}{dV_{\mathrm{GS1}}}$, can be obtained for substitution of the gate bias ratio k. For the surface potentials we obtain:

$$\psi_{\mathrm{s1}} = \frac{C_{\mathrm{ox1}}\,(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}) + kC_{\mathrm{si}}C_{\mathrm{ox2}}}{(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}})\,(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}) - C_{\mathrm{si}}^2} \cdot V_{\mathrm{GS1}} - \frac{\Delta\phi_1 C_{\mathrm{ox1}}\,(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}) + \Delta\phi_2 C_{\mathrm{si}}C_{\mathrm{ox2}}}{(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}})\,(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}) - C_{\mathrm{si}}^2} \tag{2.29a}$$

and

$$\psi_{\mathrm{s2}} = \frac{kC_{\mathrm{ox2}}\,(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}) + C_{\mathrm{si}}C_{\mathrm{ox1}}}{(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})\,(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}) - C_{\mathrm{si}}^2} \cdot V_{\mathrm{GS1}} - \frac{\Delta\phi_2 C_{\mathrm{ox2}}\,(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}) + \Delta\phi_1 C_{\mathrm{si}}C_{\mathrm{ox1}}}{(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})\,(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}) - C_{\mathrm{si}}^2}, \tag{2.29b}$$

where we separated the gate voltage dependent term (first RHS term) and the gate voltage independent term (second RHS term), such that the first term can directly be interpreted as the mentioned derivative

(for the complete derivation, see appendix C). This derivative can also be obtained from the capacitor scheme shown in figure 2.5. For this, the superposition principle can be used. An example is given for the front surface potential: we extract the two transfer functions $\frac{d\psi_{s1}}{dV_{G1}}$ and $\frac{d\psi_{s1}}{dV_{G2}} = \frac{d\psi_{s1}}{d\psi_{s2}}\frac{d\psi_{s2}}{dV_{G2}}$, add the two contributions and substitute $V_{G2} = kV_{G1}$ to arrive at the same result.

The coupling between the front and the back surface potentials can be optimized by making both surface potentials equal. Otherwise, the surface potentials always effectively counteract each other such that the control over the channel charge is less ideal. In this study we define the same optimum coupling for a different reason: when both surface potentials are equal the formalism for defining the subthreshold swing is more straight-forward.

Optimum coupling can be obtained when the two surface potentials change at the same rate [21]:

$$\frac{d\psi_{s1}}{dV_{GS1}} = \frac{d\psi_{s2}}{dV_{GS1}}. \tag{2.30}$$

The corresponding optimal gate bias ratio is obtained for substituting equations 2.29 into the above equation. We obtain:

$$k_0 = \frac{C_{ox1}\left(C_{ox2} + C_{it2}\right)}{C_{ox2}\left(C_{ox1} + C_{it1}\right)}. \tag{2.31}$$

The front channel subthreshold swing is defined as:

$$SS_1 = \frac{dV_{GS1}}{d\log_{10}\left(I_D\right)} = \ln(10)\cdot\left(\frac{d\ln(I_D)}{d\psi_{s1}}\frac{d\psi_{s1}}{dV_{GS1}} + \frac{d\ln(I_D)}{d\psi_{s2}}\frac{d\psi_{s2}}{dV_{GS1}}\right)^{-1}, \tag{2.32}$$

where the subscript of SS_a indicates with respect to which gate voltage the subthreshold swing is defined, i.e. with respect to V_{GSa}. Effectively this thus means that e.g. SS_1 contains both $m_{1,1}$ and $m_{1,2}$ and that their combined effect is written as m_1 here.

It can be assumed that the exact drain current as given by equation 2.9 can be approximated for gate bias ratios close to the optimal gate bias ratio. In this approximation, the total current is split over two separate charge channels with each if these channels being related to one of the two surface potentials. We thus have $I_{Di} \propto \exp\left(\psi_{si}\right)$ with $i = 1, 2$ for the front and back interface, such that we can define two current ratios; $I_{D1}/I_D = \alpha$ and $I_{D2}/I_D = 1 - \alpha$. In this case, equation 2.32 can be simplified to [21]':

$$SS_1 = \ln(10)\cdot I_D\cdot\left(\frac{dI_{D1}}{d\psi_{s1}}\frac{d\psi_{s1}}{dV_{GS1}} + \frac{dI_{D2}}{d\psi_{s2}}\frac{d\psi_{s2}}{dV_{GS1}}\right)^{-1} = u_T\ln(10)\cdot\left(\alpha\frac{d\psi_{s1}}{dV_{GS1}} + (1-\alpha)\frac{d\psi_{s2}}{dV_{GS1}}\right)^{-1}, \tag{2.33}$$

The subthreshold swing is then expressed in terms of the capacitor components by substituting equations 2.29 into equation 2.33:

$$SS_1 = \ln(10)u_T\frac{\left(C_{si} + C_{ox1} + C_{it1}\right)\left(C_{si} + C_{ox2} + C_{it2}\right) - C_{si}^2}{\alpha\left(C_{ox1}\left(C_{si} + C_{ox1} + C_{it1}\right) + kC_{ox2}C_{si}\right) + (1-\alpha)\left(kC_{ox2}\left(C_{si} + C_{ox1} + C_{it1}\right) + C_{ox1}C_{si}\right)}. \tag{2.34}$$

Substitution of the optimal gate bias ratio, $k = k_0$, then results in the optimal subthreshold swing [21]:

$$SS_1 = \ln(10)u_T\left(1 + \frac{C_{it1}}{C_{ox1}}\right). \tag{2.35}$$

This subthreshold swing is equal to the subthreshold swing for a FinFET device given by equation 2.3, because the channel is a virtual ground in case of the optimal gate bias condition, such that the situation reduces to the described electrostatics for symmetric devices.

First, the situation where there are no interface traps is discussed. In this case we use equation 2.31 to find $k_0 = 1$. This is in agreement with the earlier discussed results (equation 2.16) for the symmetric and asymmetric devices without interface traps.

In practice, however, we do have interface traps and the methodology for extracting the interface trap density at the front and back interface is as follows. The subthreshold swing can be obtained for a variety of k-values, i.e. choosing a single front gate voltage sweeping range and adjusting the back gate voltage sweeping range. This results in two situations next to the optimal situation. A non-ideal, too high, subthreshold swing is observed for too low k-values. This is because the back surface potential cannot follow the front surface potential increase such that an intermediate case is observed between the optimal subthreshold swing, as given by equation 2.35, and a higher subthreshold swing for fixed back gate bias, as given by equation 2.28. On the other hand, a subthreshold swing seemingly better than optimal is observed for too high k-values. Then, the back channel conducts current because of a high enough back gate voltage already before the front channel starts conducting current. This could result in subthreshold swings lower than the ideal value of $\ln(10)u_{\mathrm{T}}$. Equation 2.33 should then not be literally interpreted as an actual SS since this equation relies on the fact that both channels start conducting at the same time, such that the back channel current can be written as function of the front channel voltage. This is no longer the case for only back-gate control, such that the subthreshold swing seems to be better than ideal.

For the described method to extract the interface trap densities, both front and back oxide capacitances are assumed to be known. Then, we have two equations, 2.31 and 2.35, with which three unknowns have to be found; k_0, C_{it1} and C_{it2}. Therefore, this system cannot be directly solved. Assuming a certain front interface trap capacitance C_{it1} allows one to calculate the optimal subthreshold swing and from that obtain the back interface trap density. In [21] the authors use material in which the front interface trap density can be neglected with respect to the front oxide capacitance. Then, the system reduces to a single equation with one unknown and can be solved:

$$k_0 \approx \left(C_{\mathrm{ox2}} + C_{\mathrm{it2}}\right)/C_{\mathrm{ox2}}, \tag{2.36}$$

and

$$SS_1 \approx \ln(10)u_{\mathrm{T}}, \tag{2.37}$$

which is equal to the ideal subthreshold swing. For the material used in this study this assumption is invalid and the front interface trap density has to be taken into account. Still, this set of equations provides an estimate for the (maximum) back interface trap density.

Because the same methodology could be applied for the back channel current, the subthreshold swing referred to the back-gate can be obtained as well. This would result in another set of two equations with the same unknowns such that the system can be solved. Now using $V_{\mathrm{GS1}} = pV_{\mathrm{GS2}}$ the optimal gate bias ratio is defined as:

$$p_0 = \frac{C_{\mathrm{ox2}}\left(C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right)}{C_{\mathrm{ox1}}\left(C_{\mathrm{ox2}} + C_{\mathrm{it2}}\right)} = \left(k_0\right)^{-1}. \tag{2.38}$$

Applying the same procedure with substitution of the optimal gate bias ratio, $p = p_0$, then results in the optimal subthreshold swing:

$$SS_2 = \ln(10)u_{\mathrm{T}}\left(1 + \frac{C_{\mathrm{it2}}}{C_{\mathrm{ox2}}}\right). \tag{2.39}$$

As stated, $k_0 = \left(p_0\right)^{-1}$, which makes sense since the optimal subthreshold swing should be obtained at the same optimal gate bias ratio, independent of the reference frame. In other words, referring the subthreshold swing to the front or back gate should have no effect on the optimal gate bias ratio.

Assuming no back interface traps ($C_{\mathrm{it2}} = 0$) an estimate for the (maximum) front interface trap density can be obtained. Then:

$$p_0 \approx \left(C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right)/C_{\mathrm{ox1}}, \tag{2.40}$$

and

$$SS_2 \approx \ln(10)u_{\mathrm{T}}. \tag{2.41}$$

In summary, an estimate for either the (maximum) front or back interface trap density can be obtained from a simplified model. For this, equations 2.36 and 2.37 are used to extract D_{it2} and equations 2.40 and 2.41 are used to extract D_{it1}. In both cases the other interface trap density is assumed to be 0.

In order to obtain the front and back interface trap densities simultaneously, and thus obtain the correct values, the following procedure has to be used. Assuming C_{ox1} and C_{ox2} to be known, the front and back interface trap densities can now be determined from the total system of equations 2.31, 2.35, 2.38 and 2.39. This can be explained as follows: assuming a certain C_{it1}, SS_1 can be calculated from equation 2.35. k_0 can be obtained for this SS_1 from the measurement and C_{it2} can then be calculated from equation 2.31 for the same assumed C_{it1}. As k_0 is known, p_0 is also known since its simply the inverse. For the given p_0, SS_2 can be obtained from the measurement. Equation 2.39 can then be used to compare the obtained SS_2 with the calculated RHS. For a correctly chosen C_{it1}, the two values should ideally be the same. Therefore, this procedure can be applied iteratively until the combination of C_{it1} and C_{it2} satisfying the convergence criterium is obtained.

A similar method has been applied by [22]. However the devices used had a relatively thick silicon body ($t_{\mathrm{si}} \approx 85$ nm) and BOX layer ($t_{\mathrm{ox2}} = 200$ nm) in comparison to the devices used in this study. Also, the devices are either enhancement-mode transistors or transistors with a lower threshold voltage than that for the devices used in this study (judging from the shown $I_{\mathrm{D}} - V_{\mathrm{G}}$ curves with $V_{\mathrm{T}} \approx 0$ V). The error propagation has not been described such that the accuracy of the shown results is unknown and, finally, the methodology behind the computation of the two drain current contributions was not accurately described, i.e. it is not stated whether this computation was done by hand or whether a simulation tool was used. The methodology presented does result in the interface trap densities as function of energy, as is required here.

For the combination of the front gate referred and back gate referred subthreshold swing under dual gate operation we have an additional remark with respect to the practical aspect. For the described method with the subthreshold swing referred to the front gate, the front gate voltage sweeping range $\mathbb{R}(V_{\mathrm{GS1}})$ is maintained constant and the back gate voltage range $\mathbb{R}(V_{\mathrm{GS2}})$ is varied to obtain different k. At a fixed sample number (or fixed number of measurement points) for a fixed $\mathbb{R}(V_{\mathrm{GS1}})$, a varying k is obtained as function of V_{GS1} where all sample points can be used. In case a varying front gate voltage range would be used at a fixed back gate voltage range, the resulting data has to be interpolated to be able to express k for all the same front-gate voltage values. The interpolation between data points introduces an additional error. Therefore, it is convenient to keep the range of the gate voltage to which the subthreshold swing is referred constant. For the method described for the back gate referred subthreshold swing, this implies that the range $\mathbb{R}(V_{\mathrm{GS2}})$ is maintained constant and the front gate voltage range $\mathbb{R}(V_{\mathrm{GS1}})$ is varied. Therefore, a trade-off in errors emerges when we choose either of two options. 1) A single measurement series is used. Since the resulting optimal gate bias ratio is inherently the same, the error between repetitive measurements is eliminated. We do have an interpolation error in this case. 2) Two measurement series have to be used in order to refrain from using interpolation.

2.8 Limits of the subthreshold regime

A description of the limits of the subthreshold regime for symmetric and asymmetric DG devices and thus for both FinFET and FDSOI devices is needed to utilize the described models to their full extent.

In the subthreshold regime the channel is in weak inversion or depletion. The upper and lower boundaries of the subthreshold regime are therefore defined by the gate voltage or surface potential at which the channel either becomes accumulated or strongly inverted. In terms of surface potentials, the lower limit is defined by the flatband voltage, for which $\psi_{\mathrm{s}} = 0$. For a symmetric DG device we can exclude interface traps and use equation 2.16 or include interface traps and use equation 2.20 to obtain the same result for the lower limit: $V_{\mathrm{G}} = \Delta\phi_1$. Comparing with equations 2.12 it can be stated that the

gate voltage is equal to the flatband voltage at the lower limit. Because the angle of the cosine function in equation 2.8 cannot exceed $\pi/2$, ψ_0 is pinned to an upper bound [24]. The upper limit of the subthreshold regime is defined by this maximum value of ψ_0 and is given by [20]:

$$\psi_{0,\max} = 2u_{\mathrm{T}} \ln\left(\frac{2}{t_{\mathrm{si}}}\sqrt{\frac{2\varepsilon_{\mathrm{si}} u_{\mathrm{T}}}{q n_{\mathrm{i}}}}\right), \tag{2.42}$$

from which the threshold voltage can be approximately expressed as $V_{\mathrm{T}} = \Delta\phi_1 + \psi_{0,\max}$ [24]. Here, the contribution of the interface trap density is neglected. In practice, this contribution cannot be neglected and the dependence of the interface trap density on the surface potential makes the determination of the threshold voltage complicated. Therefore, the gate voltage value corresponding to the drain current $I_{\mathrm{D}}(\psi_{0,\max})$ is defined as the threshold voltage for a symmetric DG device [20].

For an asymmetric DG device the surface potentials at the two interfaces do not have to be equal which makes the definition of the lower and upper limits of the subthreshold regime difficult. First of all, the limits are different depending on how the FET is operated. Only varying the voltage of the front gate at a fixed back gate bias results in different limits than sweeping both gates. Here we discuss the case where front and back gate voltages are both varied with a fixed ratio $k = V_{\mathrm{G2}}/V_{\mathrm{G1}}$, since that appears to be the correct method for the interface trap density extraction. See also section 2.7.

Both for the lower limit and for the upper limit we obtain two values, since one of the two interfaces starts accumulating or inverting before the other. The lower limit can be defined as the front gate voltage at which the first of the two surface potentials becomes 0. Further decreasing the front gate voltage would result in this surface potential becoming negative and the second surface potential would eventually become 0. However, the entire channel should be in depletion for the device to operate in the subthreshold regime, such that we define the first transition to be the lower limit of the subthreshold regime for asymmetric DG devices.

We use equations 2.29 with $\psi_{\mathrm{s1}} = 0$ and $\psi_{\mathrm{s2}} = 0$ and obtain:

$$V_{\mathrm{G1,s1}} = \frac{\Delta\phi_1 C_{\mathrm{ox1}} \left(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}\right) + \Delta\phi_2 C_{\mathrm{si}} C_{\mathrm{ox2}}}{C_{\mathrm{ox1}} \left(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}\right) + k C_{\mathrm{si}} C_{\mathrm{ox2}}} \tag{2.43a}$$

and

$$V_{\mathrm{G1,s2}} = \frac{\Delta\phi_2 C_{\mathrm{ox2}} \left(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right) + \Delta\phi_1 C_{\mathrm{si}} C_{\mathrm{ox1}}}{k C_{\mathrm{ox2}} \left(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right) + C_{\mathrm{si}} C_{\mathrm{ox1}}}. \tag{2.43b}$$

The first expression is the result for $\psi_{\mathrm{s1}} = 0$, as denoted by the subscript s1, and the second expression is the result for $\psi_{\mathrm{s2}} = 0$, as denoted by the subscript s2. The highest of the two computed values then determines the lower limit of the subthreshold regime. A rough estimate for the upper limit can be made with threshold criteria $\psi_{\mathrm{s1}} = E_{\mathrm{G}}/2q$ and $\psi_{\mathrm{s2}} = E_{\mathrm{G}}/2q$ [25]:

$$V_{\mathrm{T1}} = \frac{E_{\mathrm{G}}}{2q} + V_{\mathrm{G1,s1}} \tag{2.44a}$$

and

$$V_{\mathrm{T2}} = \frac{E_{\mathrm{G}}}{2q} + V_{\mathrm{G1,s2}}. \tag{2.44b}$$

In this case, the lowest of the two computed values determines the upper limit of the subthreshold regime. Actually, after the first threshold, that interface is inverted and the channel (or body) is screened from the corresponding gate. For example, in case the front interface inverts first, the $\psi_{\mathrm{s1}} = E_{\mathrm{G}}/2q$ criterium is first met and the bottom channel is screened from V_{G1} by the inverted charge. Thus, the bottom interface has a different threshold criterium than the one stated above since the electric field can be neglected [25]. Also, the lower and upper subthreshold limits depend on k, where the values decrease with increasing k. However, for too high k the criteria stated above are no longer valid, because equations 2.29 are not valid anymore, as was described in section 2.7.

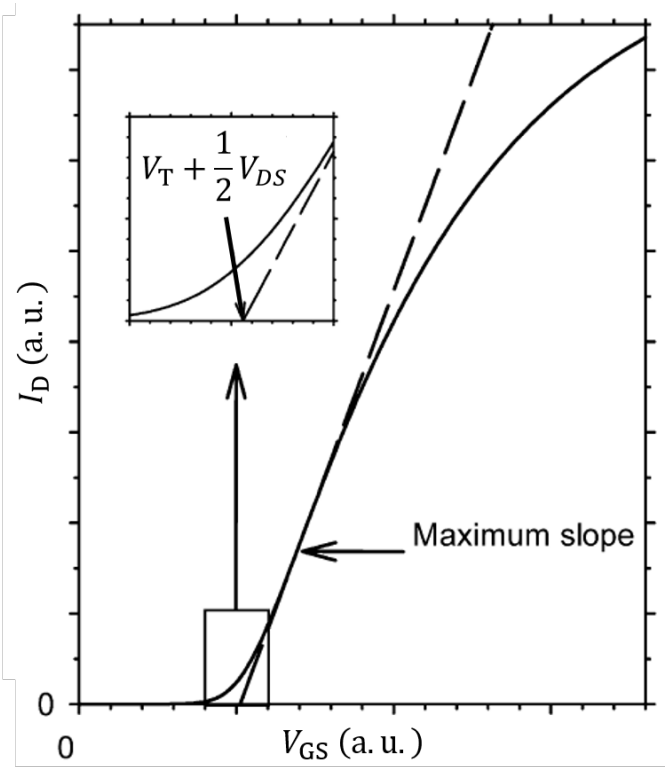


Figure 2.9: Determination of the threshold voltage using the method of extrapolation in the linear regime (ELR). Taken from Ortiz-Conde et al. [34].

For our FDSOI devices a high-k metal-gate (HKMG) stack of which the workfunction is around midgap is placed on top of the silicon channel [33]. The threshold voltage can be tailored with the back-gate doping type and concentration [16]. Here, we assume the silicon channel to be undoped. Then, the workfunction difference between the front gate and the silicon channel, i.e. the front gate workfunction difference, is $\Delta\phi_1 \approx 0$. The workfunction difference between the back-gate and the silicon channel, the back-gate workfunction difference, depends on the n-well doping concentration and is given by:

$$\Delta\phi_2 = -u_T \ln\left(\frac{N_{well}}{n_i}\right), \tag{2.45}$$

with N_{well} the doping concentration of the n-well used as back-gate and with $n_i = 1.2 \cdot 10^{10}$ cm^{-3} the intrinsic carrier concentration of silicon. For example, $N_{well} = 5 \cdot 10^{17}$ cm^{-3} results in $\Delta\phi_2 = -0.45$ eV. Now assuming $t_{ox1} = 1.33$ nm, $t_{ox2} = 20$ nm, $C_{si} = 6$ nm and $k = 1$ results in $V_{G1,s1} = -27.5$ mV and $V_{G1,s2} = -27.9$ mV for the lower limits and in $V_{T1} = 510.3$ mV and $V_{T2} = 509.9$ mV for the upper limits of the subthreshold regime. We thus have -27.5 mV $<$ Subthreshold regime $<$ 509.9 mV.

However, since the above description for the upper limit of the subtreshold regime for asymmetric DG devices is only a rough estimate, its practical relevance is limited. In practice, we use the method of extrapolation in the linear regime (ELR) to determine the threshold voltage [34], where the gate voltage axis intercept ($I_D = 0$) of the linear extrapolation of the I_D-V_G curve yields V_T. To be more specific, the extrapolation is performed from the drain current corresponding to the gate voltage at the maximum drain current slope, or transconductance (g_m). Half the drain-source voltage then has to be subtracted from the obtained gate voltage axis intercept to obtain the threshold voltage. This is shown in figure 2.9. In summary, the threshold voltage is obtained from:

$$V_T = \frac{g_{m,max} V_{GS,max} - I_{D,max}}{g_{m,max}} - \frac{1}{2}V_{DS}, \tag{2.46}$$

where the max subscript indicates that the value is taken at the corresponding maximum value of the transconductance. The actual upper limit of the subthreshold regime is defined by this threshold voltage, instead of equations 2.44. It might, however, still be insightful to compare both.

2.9 Conclusion electrostatics

Sections 2.2 to 2.8 are summarized here. The $g_\mathrm{m}/I_\mathrm{D}$ method cannot be applied to asymmetric DG devices, such as the FDSOI devices used in this study. This is because the method relies on symmetry to establish a simple relationship between the interface trap density and the subthreshold slope ideality. In other words, the method uses only a single surface potential ($\psi_{\mathrm{s}1} = \psi_{\mathrm{s}2} = \psi_\mathrm{s}$) and this is generally incorrect for asymmetric devices.

Applying a voltage to only one of the two gates while keeping the second gate at a fixed voltage is also impractical for the extraction of interface traps, because the cross-coupling between the front and back surface potentials complicates the analysis. This also implies that a model, being either numerical or analytical, is required for the extraction.

The most promising method for the extraction of the interface trap density for FDSOI devices seems to be double gate control, where the front and back gate voltages are related to each other with a fixed ratio of $k = V_\mathrm{BG}/V_\mathrm{G}$. Equations 2.31, 2.35, 2.38 and 2.39 are then used as an analytical model. The range of validity of this analytical model is described by a lower limit defined by equations 2.43 and an upper limit defined by equation 2.46.

Using the described electrostatics relations we want to extract $D_{\mathrm{it}i}(E)$ with $i = 1, 2$ for the front or back interface. The interface trap density has a significant influence on the electrostatics and this can be used to extract the interface trap density, as has now been extensively discussed. We continue by describing some additional effects that change the subthreshold swing, such as the lateral field contribution, i.e. the influence of the relation between current and asymmetric surface potentials.

Additionally, the method for relating the interface trap density to energy has not yet been discussed. The energy landscape in FDSOI material could be different from that in FinFETs such that equation 2.6 is no longer valid. Also, quantum-mechanical confinement and strain engineering might influence the band gap energy and therefore the energy landscape. Extracting the energy levels the traps occupy could be significantly influenced by these band gap energy changes. For this reason, quantum-mechanical confinement and strain engineering are discussed next.

2.10 Additional subtreshold swing theory

The relation for the subthreshold swing referred to the front gate voltage V_GS is redefined as:

$$\begin{aligned} SS = \frac{dV_\mathrm{GS}}{d\log_{10}(I_\mathrm{D})} &= \frac{dV_\mathrm{GS}}{d\psi_{\mathrm{s}1}}\frac{d\psi_{\mathrm{s}1}}{d\ln(I_\mathrm{D})}\ln(10) \; + \frac{dV_\mathrm{GS}}{d\psi_{\mathrm{s}2}}\frac{d\psi_{\mathrm{s}2}}{d\ln(I_\mathrm{D})}\ln(10) \\ &\equiv m_{11}\cdot\delta\psi_{\mathrm{s}1}\cdot\ln(10) \; + m_{12}\cdot\delta\psi_{\mathrm{s}2}\cdot\ln(10)\;, \end{aligned} \tag{2.47}$$

where all the terms relate to the partial derivatives in their respective order. We thus need to obtain relations for m_{yx} and $\delta\psi_x$, with $x = 1, 2$ the front or back surface (potential) and with $y = 1, 2$ the front or back gate (voltage). Here, the m_{yx}-terms describe the electrostatics contribution to the subthreshold swing, and the $\delta\psi_x$-terms describe the transverse field contribution.

The electrostatics and thus how to obtain the m_{yx}-terms has already been described (see equations 2.29 and appendix C). Here we study the transverse field contribution, $\frac{d\ln(I_\mathrm{D})}{d\psi_x}$, for the two described analytical models for the subtreshold drain current. Then, we study the impact of a field-dependent mobility, that of a workfunction difference and that of a depletion capacitance.

Lateral field contribution for general drain current

The general analytic relation for the drain current of a UTB FDSOI device (from equation 2.9) is:

$$I_{\mathrm{D}} = A \cdot u_T \cdot \frac{\exp\left(\frac{\psi_{\mathrm{s2}}}{u_T}\right) - \exp\left(\frac{\psi_{\mathrm{s1}}}{u_T}\right)}{\psi_{\mathrm{s2}} - \psi_{\mathrm{s1}}}. \tag{2.48}$$

For extracting the SS parameters relating current and surface potential from e.g. TCAD simulations, we use the central finite difference theorem. We can then define

$$\delta\psi_{\mathrm{s1}} = \frac{\psi_{\mathrm{s1}}(i+1) - \psi_{\mathrm{s1}}(i-1)}{\ln(I_{\mathrm{D}}(i+1)) - \ln(I_{\mathrm{D}}(i-1))} = \frac{d\psi_{\mathrm{s1}}}{d\ln(I_{\mathrm{D}})}, \tag{2.49}$$

with index i indicating that the i-th numerical value should be used in case of (numerical) simulation or measurement data. $\delta\psi_{\mathrm{s1}}$ actually denotes a ratio; the ratio between the front surface potential and the natural logarithm of the drain current. Actually, we then refer the drain current to the front surface potential and attribute all of its change to the front surface potential. However, we also have the back surface potential.

In order to include the influence of the front and back surface potentials on the current as referred to one of the two surface potentials, we include the coupling effects in both surface potentials. We obtain:

$$\delta\psi_{\mathrm{s1}} = \left(\frac{d\ln(I_{\mathrm{D}})}{d\psi_{\mathrm{s1}}} + \frac{d\ln(I_{\mathrm{D}})}{d\psi_{\mathrm{s2}}}\frac{d\psi_{\mathrm{s2}}}{d\psi_{\mathrm{s1}}}\right)^{-1}, \tag{2.50a}$$

$$\delta\psi_{\mathrm{s2}} = \left(\frac{d\ln(I_{\mathrm{D}})}{d\psi_{\mathrm{s2}}} + \frac{d\ln(I_{\mathrm{D}})}{d\psi_{\mathrm{s1}}}\frac{d\psi_{\mathrm{s1}}}{d\psi_{\mathrm{s2}}}\right)^{-1}. \tag{2.50b}$$

Using the definitions for $\delta\psi_{\mathrm{s}x}$ in equations 2.50 in combination with the analytical model gives the same results as using equation 2.49 (for $\delta\psi_{\mathrm{s1}}$) in combination with TCAD. We substitute equation 2.48 into the current-surface potential derivatives of equations 2.50 to obtain:

$$\delta I_{\mathrm{D1}} \equiv \frac{d\ln(I_{\mathrm{D}})}{d\psi_{\mathrm{s1}}} = \frac{\exp\left(\frac{\psi_{\mathrm{s1}}}{u_T}\right)(\psi_1 - \psi_{\mathrm{s2}} - u_T) + u_T\exp\left(\frac{\psi_{\mathrm{s2}}}{u_T}\right)}{u_T\left(\exp\left(\frac{\psi_{\mathrm{s1}}}{u_T}\right) - \exp\left(\frac{\psi_{\mathrm{s2}}}{u_T}\right)\right)(\psi_{\mathrm{s1}} - \psi_{\mathrm{s2}})} \tag{2.51a}$$

and

$$\delta I_{\mathrm{D2}} \equiv \frac{d\ln(I_{\mathrm{D}})}{d\psi_{\mathrm{s2}}} = \frac{\exp\left(\frac{\psi_{\mathrm{s2}}}{u_T}\right)(\psi_2 - \psi_{\mathrm{s1}} - u_T) + u_T\exp\left(\frac{\psi_{\mathrm{s1}}}{u_T}\right)}{u_T\left(\exp\left(\frac{\psi_{\mathrm{s2}}}{u_T}\right) - \exp\left(\frac{\psi_{\mathrm{s1}}}{u_T}\right)\right)(\psi_{\mathrm{s2}} - \psi_{\mathrm{s1}})}. \tag{2.51b}$$

The derivative of both surface potentials with respect to each other in equations 2.50 can be obtained from the equations given in the electrostatics part (equations C.11). Rewriting equation 2.29 (b) such that we obtain a function $V_{\mathrm{GS}} = f(\psi_{\mathrm{s2}}, k)$ we find:

$$\psi_{\mathrm{s1}} = \frac{f_{11} + k \cdot f_{21}}{f_{12} + k \cdot f_{22}}\psi_{\mathrm{s2}} = \frac{f_1}{f_2}\psi_{\mathrm{s2}} = \frac{m_{12}}{m_{11}} \equiv f_k \cdot \psi_{\mathrm{s2}}, \tag{2.52}$$

such that $\frac{d\psi_{\mathrm{s1}}}{d\psi_{\mathrm{s2}}} = f_k$, with

$$f_k = \frac{C_{ox1}(C_{si} + C_{ox2} + C_{it2}) + k \cdot C_{si}C_{ox2}}{k \cdot C_{ox2}(C_{si} + C_{ox1} + C_{it1}) + C_{si}C_{ox1}}. \tag{2.53}$$

So, for the symmetric DGFET (with an equal front and buried oxide thickness):

$$f_k = \frac{(1+k)C_{\mathrm{ox}}C_{\mathrm{si}} + C_{\mathrm{ox}}(C_{\mathrm{ox}} + C_{\mathrm{it2}})}{(1+k)C_{\mathrm{ox}}C_{\mathrm{si}} + k \cdot C_{\mathrm{ox}}(C_{\mathrm{ox}} + C_{\mathrm{it1}})}, \tag{2.54}$$

such that we obtain $f_k = 1$, independent of any capacitance, for a symmetric trap distribution with $k = 1$. For this symmetric case with $k = 1$, we have $\psi_{s1} = \psi_{s2}$. Taking equations 2.51 to the limit of $\psi_{s2} \to \psi_{s1}$, we obtain $\delta I_{D1} = \delta I_{D2} = \frac{1}{2u_T}$. Thus, for the symmetric DGFET we simply obtain $\delta\psi_{s1} = \delta\psi_{s2} = u_T$ such that the subthreshold swing as described for the g_m/I_D-method is obtained. This confirms that the methodology used above is correct.

In the general case, which is also applicable for asymmetric DG devices, substitution of equations 2.51, 2.53 into equations 2.50 results in the transverse field contribution of the subthreshold swing.

Lateral field contribution for approximate drain current

The approximate analytic relation for the drain current of a UTB FDSOI device is [21, 22]:

$$I_D = A \cdot 0.5 \cdot \left(\exp\left(\frac{\psi_{s1}}{u_T}\right) + \exp\left(\frac{\psi_{s2}}{u_T}\right) \right) \tag{2.55}$$

We then obtain:

$$\delta I_{D1} \equiv \frac{d\ln(I_D)}{d\psi_{s1}} = \frac{\exp\left(\frac{\psi_{s1}}{u_T}\right)}{u_T\left(\exp\left(\frac{\psi_{s1}}{u_T}\right) + \exp\left(\frac{\psi_{s2}}{u_T}\right)\right)} = \frac{A \cdot 0.5 \cdot \exp\left(\frac{\psi_{s1}}{u_T}\right)}{u_T \cdot I_D} \tag{2.56a}$$

and

$$\delta I_{D2} \equiv \frac{d\ln(I_D)}{d\psi_{s2}} = \frac{\exp\left(\frac{\psi_{s2}}{u_T}\right)}{u_T\left(\exp\left(\frac{\psi_{s1}}{u_T}\right) + \exp\left(\frac{\psi_{s2}}{u_T}\right)\right)} = \frac{A \cdot 0.5 \cdot \exp\left(\frac{\psi_{s2}}{u_T}\right)}{u_T \cdot I_D} \tag{2.56b}$$

The relation for f_k remains the same, so substitution of equations 2.56 instead of equations 2.51 then results in the approximate $\delta\psi_x$. The subthreshold swing we then obtain is equal to equation 2.33 or 2.34, which validates this method for obtaining transverse field contribution.

Lateral field contribution with field-dependent mobility

Until now we assumed the mobility to be constant. In practice, the mobility depends on many factors, such as doping, temperature and electric field strength. Here we discuss the dependence of the mobility on the electric field. The influence of the mobility on the subthreshold swing only propagates through the transverse field contribution, i.e. only $\delta\psi_{sx}$ changes with a changing mobility. This is because the mobility influences the current and not the charge density, such that the electrostatics is not changed.

From equation 2.50 we know that we need $\frac{d\ln(I_D)}{d\psi_{s1}}$ and $\frac{d\ln(I_D)}{d\psi_{s2}}$. We assumed a relation between current and surface potentials in the form of $I_D = A \cdot h(\psi_{s1}, \psi_{s2})$ (see equation 2.48 and 2.55). We examine what changes in case the mobility is field dependent and thus surface potential dependent. In that case, the relation is of the form $I_D = B \cdot \mu(\psi_{s1}, \psi_{s2}) \cdot h(\psi_{s1}, \psi_{s2})$, where $B = A/\mu$.

We then find

$$\frac{d\ln(I_D)}{d\psi_{s1}} = \frac{d\mu}{d\psi_{s1}}\frac{1}{\mu} + \frac{dh}{d\psi_{s1}}\frac{1}{h} = \frac{d\mu}{d\psi_{s1}}\frac{1}{\mu} + \delta I_{D1}, \tag{2.57}$$

Where $\mu = \mu(\psi_{s1}, \psi_{s2})$ and with δI_{D1} the derivative as obtained with a constant mobility (equations 2.51 or 2.56). A similar expression can be obtained with respect to the back surface potential:

$$\frac{d\ln(I_D)}{d\psi_{s2}} = \frac{d\mu}{d\psi_{s2}}\frac{1}{\mu} + \delta I_{D2}. \tag{2.58}$$

We thus simply obtain an additional term in $\frac{d\ln(I_D)}{d\psi_{sx}}$, depending on the mobility. The mobility reduces due to the transverse field, i.e. $\frac{d\mu}{d\psi_{sx}}$ is negative. Therefore, with an increase in the difference between surface potentials, $\frac{d\ln(I_D)}{d\psi_{sx}}$ reduces and as a result, $\delta\psi_{sx}$ increases. For the electrostatics being the same, the subthreshold swing thus increases once the field-dependence of the mobility has been included.

Electrostatics with workfunction difference

For the k-sweep method it was explained that the optimal subthreshold swing could be obtained by aiming for an equal change in surface potential, i.e. $\frac{\partial \psi_{s1}}{\partial V_{GS}} = \frac{\partial \psi_{s2}}{\partial V_{GS}}$. Implicitly, it was assumed that this is sufficient for obtaining equal surface potentials and thus a symmetric situation.

We consider the case where we have a device with an asymmetric workfunction, i.e. the difference in workfunction between that of the front gate and the back gate. In that case, only taking the change in surface potentials to be equal is not sufficient for obtaining a symmetric situation.

We start by looking back at the electrostatics equations (see equations 2.29 and C.1) and give the relations for the workfunction-dependent parts of the electrostatics equations, $g_1(\Delta\phi)$ and $g_2(\Delta\phi)$:

$$g_1(\Delta\phi) = \frac{\Delta\phi_1 C_{ox1}(C_{si} + C_{ox2} + C_{it2}) + \Delta\phi_2 C_{ox2} C_{si}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}, \tag{2.59a}$$

$$g_2(\Delta\phi) = \frac{\Delta\phi_2 C_{ox2}(C_{si} + C_{ox1} + C_{it1}) + \Delta\phi_1 C_{ox1} C_{si}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}. \tag{2.59b}$$

So far the workfunctions of both front and back gate have been considered midgap, $g_1 = g_2 = 0$. In general, this is not the case, and we need $g_1 = g_2$ in addition to an equal change in surface potentials in order to obtain equal surface potentials.

In case of the symmetric DG device with a non-midgap workfunction, $\Delta\phi_1 = \Delta\phi_2 = \Delta\phi$, $C_{ox1} = C_{ox2} = C_{ox}$ and $C_{it1} = C_{it2} = C_{it}$ hence $g_1 = g_2$. In case the workfunctions of both gates are the same, the electrostatics remain the same. The subthreshold swing is thus the same, but the current is higher (for $\Delta\phi > 0$).

For an asymmetric DG device we need an additional degree of freedom to obtain $g_1 = g_2$. We use $V_{BGS} = k \cdot V_{GS} + V_{off}$ with V_{off} a correction term for the workfunction difference.

Inserting this in equations 2.19 results in the same m-parameters, but the workfunction-dependent parameters change to:

$$g_1(\Delta\phi) = \frac{\Delta\phi_1 C_{ox1}(C_{si} + C_{ox2} + C_{it2}) + (\Delta\phi_2 - V_{off}) C_{ox2} C_{si}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}, \tag{2.60a}$$

$$g_2(\Delta\phi) = \frac{(\Delta\phi_2 - V_{off}) C_{ox2}(C_{si} + C_{ox1} + C_{it1}) + \Delta\phi_1 C_{ox1} C_{si}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}. \tag{2.60b}$$

For the case without traps we then find that $V_{off} = (\Delta\phi_2 - \Delta\phi_1)/q$. The elementary charge is added here for conversion from energy (eV) to voltage (V). For example, we take an FDSOI device without traps with a midgap front gate, $\Delta\phi_1 = 0$ eV, and with a donor-doped well as back-gate with $N_{well} = 5 \cdot 10^{17}$ cm^{-3}. Then, the (back-gate) workfunction difference is $\Delta\phi_2 = -0.45$ eV and we should use $V_{off} = -0.45$ V.

For the case with interface traps we obtain:

$$V_{off} = \Delta\phi_2 - \Delta\phi_1 \frac{C_{si} C_{ox1} - C_{ox1}(C_{si} + C_{ox2} + C_{it2})}{C_{si} C_{ox2} - C_{ox2}(C_{si} + C_{ox1} + C_{it1})} \tag{2.61}$$

The asymmetric FDSOI devices with midgap front gate workfunction can therefore still be controlled with $V_{off} \approx \Delta\phi_2/q$. This introduces an error depending on how large the workfunction difference between the front gate and the silicon channel, $\Delta\phi_1$, actually is.

Electrostatics with depletion capacitance of the n-well

Until now we have assumed the device to be a G/tox1/Si/tox2/BG stack with a back-gate workfunction difference, but the actual device consists of a G/tox1/Si/tox2/Nwell/BG stack. The effect of the (asymmetric) oxide thickness, the workfunction and the field-dependence of the mobility was described.

Next to the BG workfunction difference resulting from the N_{well} doping, we also obtain a depletion region in the Nwell due to the voltage drop across the stack. The depletion capacitance can be described as [35]:

$$C_{\text{dep}} = \frac{dQ}{dV} = \frac{d\left(qN_{\text{well}}W_{\text{dep}}\right)}{d\left(\frac{qN_{\text{well}}}{2\varepsilon_{si}}W_{\text{dep}}^2\right)} = \frac{\varepsilon_{si}}{W_{\text{dep}}} = \sqrt{\frac{q\varepsilon_{si}N_{\text{well}}}{2}}\frac{1}{\sqrt{\psi_{\text{s3}} - 2u_{\text{T}}}}, \tag{2.62}$$

With ψ_{s3} the surface potential at the BOX/n-well-interface which is defined as the difference in potential at this interface and the potential "in the bulk" of the Nwell. In other words, ψ_{s3} refers to the voltage across the depletion capacitor. For $k = k_0$, we have $\psi_{\text{s1}} = \psi_{\text{s2}}$ and thus $\psi_3 = 0$ and for increasing $|\psi_{\text{s2}} - \psi_{\text{s1}}|$ we have an increasing ψ_3.

The depletion capacitance effect is difficult to take into account, as ψ_3 is not readily known. We can see a clear trend with ψ_3 and N_{well}, however, and will therefore qualitatively analyze the situation including depletion. For increasing k we see an increasing ψ_{s3} and thus a decreasing C_{dep} with square-root proportionality. On the other hand, increasing N_{well} increases C_{dep} with the square-root proportionality.

The effect of C_{dep} can be incorporated in a new C_{bot} which is the series capacitance of C_{dep} and C_{ox2}. We thus have $Z_{\text{bot}} = Z_{\text{dep}} + Z_{\text{ox2}}$ such that

$$C_{\text{bot}} = \frac{C_{\text{ox2}}C_{\text{dep}}}{C_{\text{ox2}} + C_{\text{dep}}}. \tag{2.63}$$

For $C_{\text{dep}} \gg C_{\text{ox2}}$ we then obtain $C_{\text{bot}} = C_{\text{ox2}}$. Thus, for increasing k we see an increasing effect of C_{dep} and for increasing N_{well} we see a decreasing effect.

2.11 Quantum-mechanical confinement

The electrostatics of symmetric and asymmetric devices were described with a semi-classical model in the previous sections; the peak charge density in the silicon channel is at the oxide/silicon interface. We have to account for quantum-mechanical confinement of the carriers, when the thickness of the silicon channel is reduced to values in the order of the De Broglie wavelength [11]:

$$t_{\text{si}} \leq \frac{2\pi\hbar}{\sqrt{2m_{d,v}^* q u_{\text{T}}}}, \tag{2.64}$$

where $\hbar$ is the reduced Planck constant ($\hbar = h/2\pi$) and $m_{d,v}^*$ the effective mass (to be discussed in more detail later on in this section). For an electron with a thermal voltage of $u_{\text{T}} = 26$ mV and a mass of $m_{d,v}^* = 0.19m_0$ [11], with $m_0 = 9.1 \cdot 10^{-31}$ kg being the electron rest mass, the De Broglie wavelength is about ~ 17 nm. For silicon channels of only 6 nm thick, as used for this study, quantum-mechanical confinement effects should thus be considered. For this research, it is important that the effect of quantum confinement would be an effective increase of the band gap. This could be important for the extraction of the trap energy levels.

Basics of Quantum-Mechanics

The following description of the influence of quantum-mechanical confinement is adopted from Van der Steen [11]. In quantum-mechanics, an electron is represented by the three-dimensional wave equation $\Psi(x, y, z)$ of which the square modulus represents the probability density that an electron resides at

position (x, y, z). The time-independent three-dimensional Schrödinger equation to which this wave equation is a solution is given by:

$$-\frac{\hbar^2}{2m}\left(\frac{d^2\Psi}{dx^2}+\frac{d^2\Psi}{dy^2}+\frac{d^2\Psi}{dz^2}\right)+V(x,y,z)\Psi(x,y,z)=E\Psi(x,y,z), \tag{2.65}$$

with m the electron mass, V the potential energy and E the total energy. Near the conduction band edge the carriers move approximately according to the following parabolic dispersion relation:

$$E=\frac{\hbar^2k_x^2}{2m_x^*}+\frac{\hbar^2k_y^2}{2m_y^*}+\frac{\hbar^2k_z^2}{2m_z^*}, \tag{2.66}$$

with the effective mass associated with each direction being proportional to the energy dispersion of the valley minimum, given by

$$m_i^*=\left(\frac{1}{\hbar^2}\frac{d^2E}{dk_i^2}\right)^{-1}, \tag{2.67}$$

with $i = x, y, z$ depending on the direction. The energy dispersion is thus assumed to be parabolic such that a constant effective mass can be used, which is called the effective mass approximation (EMA). This parabolic energy dispersion holds in close vicinity of conduction and valence band minima, respectively maxima. Thus, moving away from the conduction band edge the non-parabolicity has to be taken into account, but this will be omitted here. Also, the valence band energy is anisotropic and non-parabolic in theory and it is therefore less trivial to compute.

The obtained energy dispersion relation does not include confinement yet and is thus correct near the conduction band of a bulk MOSFET. Confinement can be generally subdivided in two types: electrical and structural confinement. Electrical confinement can be achieved in strongly inverted channels and structural confinement is due to spatial confinement in one or more physical dimensions. We consider the case of FDSOI devices where solely the thin silicon channel confines the potential. This is only a limiting case valid within the subthreshold regime, as a combination of both structural and electrical confinement has to be considered in strong inversion. An elaborate analysis of the different confinement types is given in [36]. In case of structural confinement, a box-shaped potential well (or square well) can be used to approximate the conduction and valence band discontinuity which occurs in a thin silicon channel between two oxide layers. This is important in subthreshold hence in this work.

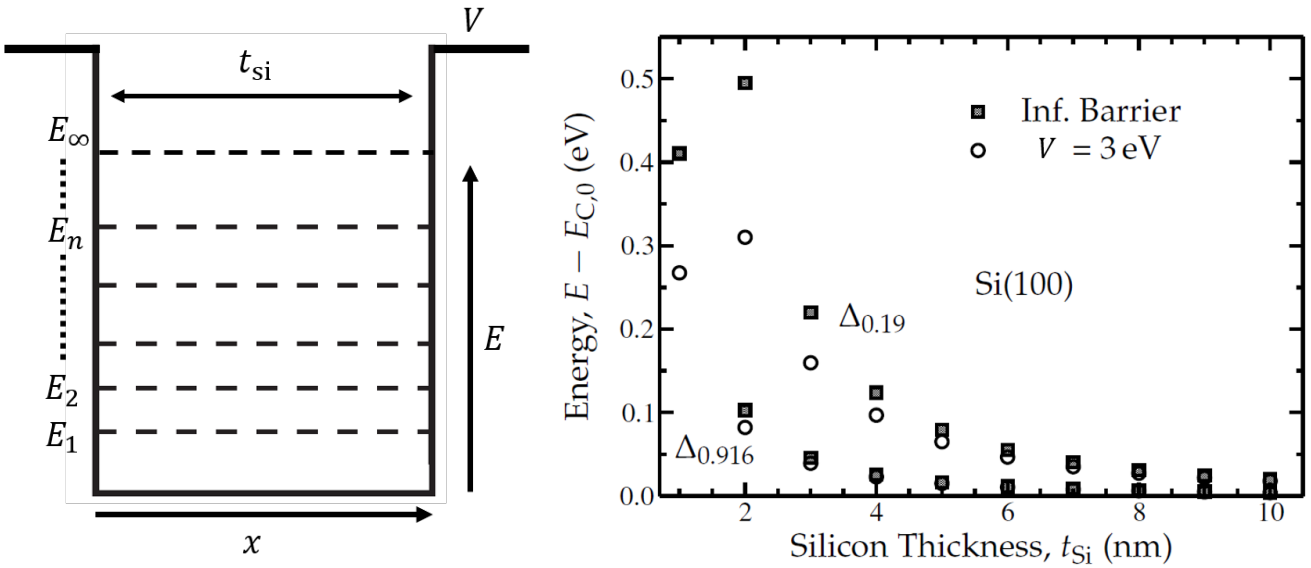
Potential barrier

Here, the potential profile is assumed to be known and is taken to be an idealized square well with an infinitely high potential barrier. The solution is simply stated below and the implications are explained. The derivation of this solution, as well as the solution for a finite confining potential and the solutions obtained using more elaborate numerical models, can be found in [11].

For the infinitely high potential barrier, the confining potential is infinite ($V(x) = \infty$) outside of the well and therefore the wave function should be 0 at the boundaries (hence zero gate current). Also, the confining potential is zero ($V(x) = 0$) inside the well ($-t_{si}/2 \leq x \leq t_{si}/2$). This situation is shown for the conduction band in figure 2.10(a) and can be mirrored horizontally to obtain the situation for the valence band. Then, the wave function does not extend into the barrier, i.e. the chance of finding an electron outside of the square well is 0 and the wave function reads:

$$\Psi(x)=\sqrt{\frac{2}{t_{si}}}\sin\left[\frac{n\pi}{t_{si}}\left(x+\frac{t_{si}}{2}\right)\right], \tag{2.68}$$

with n the subband index, which can take values from 1 to infinity.



(a) (b)

Figure 2.10: (a) Schematically shown square well with $V(x) = 0$ between $-t_{si}/2$ and $t_{si}/2$, in the well and with $V(x) = V$ outside of the well. The allowed energy levels are quantized to E_n, with the first two subbands explicitly indicated. For the infinite potential barrier case $V = \infty$. (b) Energy of the first subband minimum relative to the conduction band edge as a function of the silicon thickness for silicon in the (100) direction. The values are shown for the $\Delta_{0.916}$ and $\Delta_{0.19}$ valleys and for an infinite confining potential (Inf. barrier) and for a potential barrier of $V(x) = 3$ eV. Taken from Van der Steen [11].

To be more precise, for one electron $n = 1$, for a second electron we then have $n = 2$ due to the Pauli exclusion principle, and so on. The carriers motion is thus restricted in the x-direction, the direction of confinement, while the carrier is still free to move in y- and z-direction. The resulting total energy is given by

$$E(k_y, k_z) = \frac{\hbar^2}{2m_x^*}\left(\frac{n\pi}{t_{si}}\right)^2 + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{\hbar^2 k_z^2}{2m_z^*}, \tag{2.69}$$

with n taking integer values from 1 to infinity. Comparing this result with the previously shown result without confinement (equation 2.66) it can be noted that the continuous $E(k_x)$ is now replaced by a quantized E_n:

$$E_n = \frac{\hbar^2}{2m_x^*}\left(\frac{n\pi}{t_{si}}\right)^2, \tag{2.70}$$

with each value representing the energy minimum of the subband with index n. In more detail, equation 2.66 describes how constant energy surfaces, or iso-energy surfaces, result in all three k-space directions. Taking a single effective mass the silicon crystal thus has six of these constant energy surfaces, or valleys. This is usually denoted by the valley degeneracy factor g_v. For the bulk silicon case we thus had $g_v = 6$, while this is no longer the case for the quantized solution given by equation 2.69. There, $g_v = 2$ for the x-direction and $g_v = 4$ for the two other directions assuming the effective mass in these directions is the same.

Taking a finite confining potential results in two algebraic transcendental expressions for the even- and odd-symmetric energy minima, which have to be solved by equating the wave function inside and outside of the barrier at the boundaries. However, this is outside the scope of this work. The only aspect to be noted for the finite potential barrier with respect to the infinite potential barrier, is that the chance of finding an electron outside the well is no longer 0 for a finite potential barrier.

For silicon confined in the (100) direction the $\Delta_{0.916}$ valley is two-fold degenerate ($g_v = 2$) and the $\Delta_{0.19}$ valley is four-fold degenerate ($g_v = 4$), where the valley subscript denotes the relative value of the effective mass compared to the electron rest mass [37]. From the results shown in figure 2.10(b) it can be concluded that the infinite potential barrier results are a worst-case scenario compared to the finite potential barrier results. For the square well with infinite potential barrier, the first subband minima can be taken from figure 2.10(b) or calculated from equation 2.70. The first subband minimum of the $\Delta_{0.19}$ valley is highest with a value of $\Delta E_{\mathrm{C}} \equiv E - E_{\mathrm{C},0} \approx 55$ meV for $t_{\mathrm{si}} = 6$ nm and that the energy offset of the first subband minimum of the $\Delta_{0.916}$ valley is $\Delta E_{\mathrm{C}} \approx 11$ meV. We assume that the quantum confinement effects are similar for the valence band, where $\Delta E_{\mathrm{V}} \equiv E - E_{\mathrm{V},0}$ has to be obtained. The valence band contains the light-hole (LH) and heavy-hole (HH) valleys that contribute to the band gap, where the effect of the LH valley ($\Delta_{0.20}$) is $\Delta E_{\mathrm{V}} \approx -52$ meV and the effect of the HH valley ($\Delta_{0.29}$) is $\Delta E_{\mathrm{V}} \approx -36$ meV [38]. The effective increase in conduction band energy is determined by the lowest value, as this determines the lowest allowed energy state. An increase in the band gap energy of $\Delta E_{\mathrm{G}} \equiv \Delta E_{\mathrm{C}} - \Delta E_{\mathrm{V}} \approx 47$ meV then results. As the silicon band gap is $E_{\mathrm{G}} = 1.12$ eV, this thus means that the effective or apparent band gap energy has increased due to quantization to $E_{\mathrm{G,qm}} = 1.167$ eV for a silicon channel with a thickness of $t_{\mathrm{si}} = 6$ nm.

Space charge density distribution

In order to obtain the charge density distribution within the silicon film, also the density of states (DOS) and state occupancy have to be incorporated. The DOS is the number of states associated with a given energy. The state occupancy then tells us how many of these states are occupied at a certain energy and is linked to the Fermi energy and thus temperature and gate voltage. By incorporating the square modulus of the wave equation at each subband n of valley v, with this square modulus defining the probability of finding an electron at position x, the electron concentration distribution can be obtained [11]:

$$\rho_e(x) = \sum_{v,n} |\Psi_{v,n}(x)|^2 \cdot D_v \cdot \ln\left[1 + \exp\left(\frac{E_{\mathrm{F}} - E_{v,n} - E_{\mathrm{C},0}}{k_{\mathrm{B}}T}\right)\right], \tag{2.71}$$

with the DOS of each valley v given by

$$D_v = \frac{g_v m^*_{d,v} k_{\mathrm{B}} T}{\pi \hbar^2}. \tag{2.72}$$

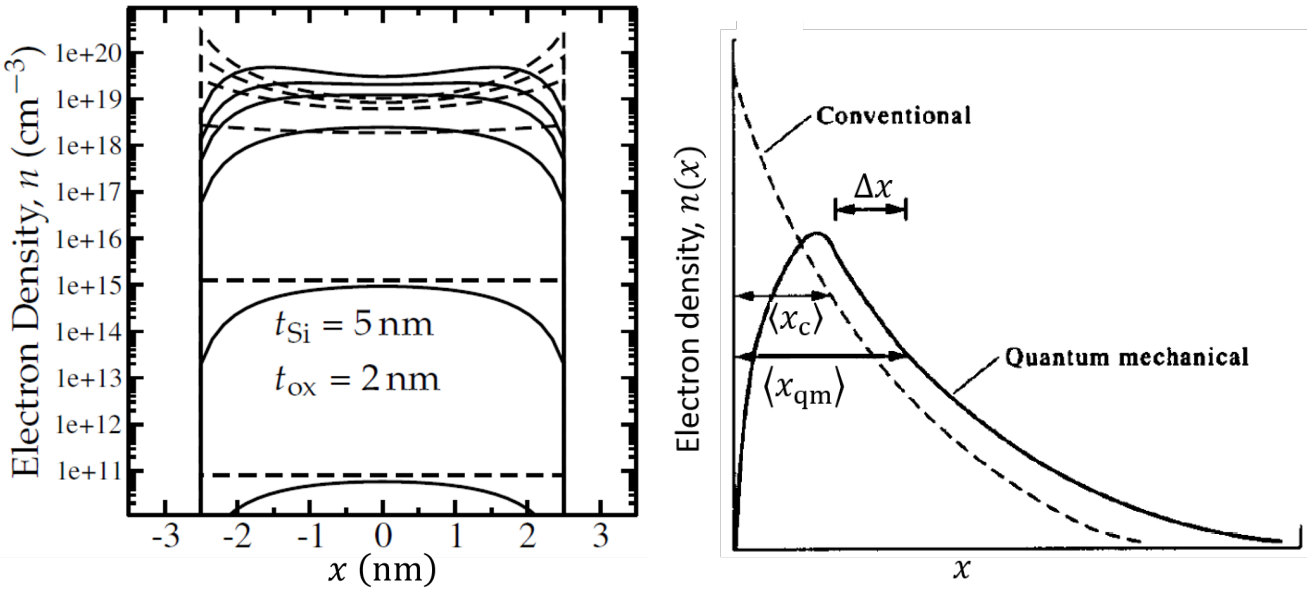
For each valley v, $E_{v,n}$ is the energy minimum of subband n relative to the bulk conduction band edge $E_{\mathrm{C},0}$ and $m^*_{d,v}$ is the DOS effective mass of valley v in subband n. The quantum-mechanical electron concentration can then be obtained from integrating the electron concentration distribution over the channel. For an infinite confining potential this results in:

$$n_{\mathrm{qm}} = \sum_{v,n} \frac{g_v m^*_{d,v} k_{\mathrm{B}} T}{\pi \hbar^2} \cdot \exp\left(\frac{E_{\mathrm{F}} - E_{v,n} - E_{\mathrm{C},0}}{k_{\mathrm{B}}T}\right). \tag{2.73}$$

It is insightful to compare the quantum-mechanical electron density with the semi-classical electron density. The semi-classical electron density is implicitly used in equation 2.7 and is given by:

$$n_{\mathrm{c}} = n_{\mathrm{i}} \cdot \exp\left(\frac{q\psi}{k_B T}\right) \tag{2.74}$$

Figure 2.11(a) is taken from [11] and shows the semi-classical and quantum-mechanical electron density for varying V_{GS}. For weak inversion conditions, the semi-classical electron density is nearly constant and the quantum-mechanical electron density is 0 at the surface and has a maximum in the middle of the channel. The value of the classical electron density is approximately equal to the quantum-mechanical



(a) (b)

Figure 2.11: (a) Electron density as function of silicon channel thickness on a log-lin scale for $V_{GS} = -1, -0.5, -0.25, 0.25, 0.5, 1$ V ($\Delta\phi = -0.52$ eV) for a symmetric DG device. The dashed lines represent the conventional distribution and the solid lines represent the quantum-mechanical distribution. Taken from Van der Steen [11]. (b) Schematically shown semi-classical (conventional) and quantum-mechanical electron density distribution for triangular potential well, with the distance from the edge of the silicon channel to a certain electron population indicated. For the semi-classical or conventional model the distance is $\langle x_c \rangle$ and for the quantum-mechanical model the distance is $\langle x_{qm} \rangle$. The difference between the two distances (Δx) accounts for the extra band bending needed. Taken from Van Dort [39].

electron density maximum. For strong inversion, the classical electron density is highest at the interfaces, while the quantum-mechanical electron density has two maxima some distance away from the interface.

Usually, the quantum-mechanical confinement effects are accounted for by using the method proposed by Van Dort et al. [39]. The displacement of the electron distribution effectively increases the oxide thickness by

$$t_{ox,eff} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \Delta x, \tag{2.75}$$

where Δx accounts for the extra band bending needed to obtain a certain electron population in the conduction band, assuming a simple relation for $\Delta x(E)$ [39]. The comparison between classical and quantum-mechanical electron densities is shown in figure 2.11(b), where Δx is indicated. To give a numerical example, taking the quantum-mechanical electron density halfway the channel to be equal to the classical electron density at 1 nm away from the interface, such that $\Delta x = 2$ nm, would result in an increase in the oxide thickness of 0.66 nm. This effect and the effect of the additional band gap energy ΔE_G are summarized by the quantum-mechanical surface potential:

$$\psi_{s,qm} = \psi_{s,c} + \frac{\Delta E_G}{q} + F \Delta x, \tag{2.76}$$

with $\psi_{s,c}$ the classical surface potential and F the electric field perpendicular to the interface. The effect of Δx is (approximately) related to that of ΔE_G and is incorporated in a new band gap energy, which is used to obtain the quantum-mechanical electron density in [39]. However, the exact methodology presented is verified for a triangular shaped potential well, i.e. for electrical confinement hence strong inversion.

In this work the subthreshold regime is considered. For a FDSOI FET in subthreshold mode operation we obtain [9]:

$$\nabla^2\psi = \frac{\partial\psi}{\partial x} = -\frac{\rho(x)}{\varepsilon_{\text{si}}} \approx 0, \tag{2.77}$$

where $\rho(x)$ is the volume charge density as function of the position along the confinement direction (assuming uniformity along the y- and z-direction). Looking back at the general relation for the surface potential of an n-type DG device, equation 2.8, and taking the above approximation, we find:

$$\frac{q\left(\psi - \psi_0\right)}{2k_BT} = 0, \tag{2.78}$$

with a surface potential minimum ψ_0. The surface potential profile in subthreshold is thus constant, hence independent of the charge density, such that the Δx-term in equation 2.76 can be omitted.

In conclusion, in subthreshold the quantum-mechanical confinement effect only propagates through an increase in band gap energy of $\Delta E_{\text{G}} \approx 47$ meV.

2.12 Strain-induced mobility enhancement

In order to increase the on-current of FET devices, once approach is to increase the mobility of electrons and holes in the channel, for which three options can be used. One option is the fabrication of the channel from materials other than silicon, with a higher mobility. Drawbacks of this are that applicable materials usually have a lower DOS and are more vulnerable to band-to-band tunneling [14].

A second option is to rotate the wafers (by 45%) to align the transistors with another crystal direction (from $\langle 110\rangle$ to $\langle 100\rangle$), such that the electron distribution among valleys is not changed but the hole distribution is. This new transport direction corresponds to the most effective hole transport.

The third option is the use of strain engineering to increase the mobility in the silicon channel. For example, the hole mobility can increase by 40% with a resulting increase in current of 15% for a strained channel [16]. This third approach is applied to the FDSOI material used in this study.

Effect of strain on the mobility

In order to describe why an increase in strain results in an increase in mobility, we use [14]

$$\mu = \frac{q\tau}{m_c^*}, \tag{2.79}$$

with τ the average scattering time and m_c^* the effective conductivity mass. The mobility is thus inversely proportional to the effective conductivity mass. Also, the effective mass of an electron is different for the longitudinal (in direction of axis) and transverse (in direction perpendicular to axis) direction.

Starting from the bulk energy dispersion relation (equation 2.66), where $g_v = 6$, a summary of the influence of strain on the electron and hole mobility is given in table 2.12 [14]. In order to comprehend the information given in the table, the full analysis for the biaxial tensile train case (which is the first case in the figure) will be carried out, as adopted from Skotnicki et al. [14].

In the example, compressive stress is applied in the x-direction such that the silicon crystal is squeezed together in this direction. Indicating the two-fold degenerate valley by Δ_2 and the four-fold degenerate valley by Δ_4, the energy of the Δ_2 valley is lowered as result of the induced strain. Therefore, the Δ_4 valleys lose energy to the Δ_2 valleys. The Δ_2 valleys are transverse with respect to the direction of current and the electrons in these valleys thus have a transverse effective mass, which is lower than the longitudinal effective mass. This is because the effective mass is inversely proportional to the curvature of the energy of the valley (see equation 2.67). On the other hand, the Δ_4 valleys contain two transverse valleys and two longitudinal valleys. This means that the shift in energy from the Δ_4 valleys to the Δ_2

valleys results in more electrons with a transverse effective mass (T-electrons) on average. The average conductivity mass thus decreases, and from equation 2.79 the mobility increases. The splitting of the subbands due to quantum confinement reduces the probability of intervalley scattering such that the average scattering time increases. The electron mobility increase is thus further enhanced by quantum confinement.

Regarding the holes for the mentioned example, the energy of the light-hole subband decreases under influence of strain such that the amount of light holes relative to the amount of heavy holes increases. The average conductivity mass will thus decrease and the hole mobility increases. Interband passages of holes are prevented due to the subband splitting for adding quantum confinement. The scattering time thus increases and the hole mobility further increases.

The overall effect of strain and quantum confinement on the mobility can be seen in the last column of table 2.12, where the effective mobility is shown as function of effective field. The resulting mobility is compared to the regular mobility curve for both weak and strong inversion. Strain indeed increases the mobility of holes and electrons depending on the type of stress applied and this effect should thus be considered for e.g. calculations of the current. The same methodology as applied above can be used to describe the change in mobility in strong inversion, for which the reader is referred to [14], and to describe the mobility for the other types of strain.

Effect of strain on the apparent band gap

For this research the impact of strain on the apparent band gap should be highlighted, since this could influence the extraction of the trap energy level. We therefore focus on the "Impact of quantization" column and quantize the shown trend in order to develop some insight in the influence of strain relative to the influence of quantum confinement. The channel stress σ is related to the induced strain ϵ according to Hooke's law [40]:

$$\sigma_i = E\epsilon_i, \tag{2.80}$$

where E is the modulus of elasticity, or Young's modulus, and where $i = x, y, z$ denotes the direction in which the stress is applied. If the applied stress is uniaxial, i.e. only in the z-direction, and the material is isotropic, the constrictions posed on the other two directions can be related to the z-direction with Poisson's ratio. Poisson's ratio is thus defined as the ratio of the lateral and axial strains [40]:

$$\nu = -\frac{\epsilon_x}{\epsilon_z} = -\frac{\epsilon_y}{\epsilon_z}. \tag{2.81}$$

From the applied stress we can thus determine the strain in all three directions. The effect of the strain on the conduction and valence band can be summarized as [41]:

$$\Delta E_{\mathrm{C},k} = \Xi_d \left(\epsilon_x + \epsilon_y + \epsilon_z\right) + \Xi_u \epsilon_k \tag{2.82a}$$

and

$$\Delta E_{\mathrm{V},k} = -a \left(\epsilon_x + \epsilon_y + \epsilon_z\right) \pm \sqrt{\frac{b^2}{2}\left[\left(\epsilon_x + \epsilon_y\right)^2 + \left(\epsilon_y + \epsilon_z\right)^2 + \left(\epsilon_x + \epsilon_z\right)^2\right]}, \tag{2.82b}$$

where Ξ_d, Ξ_u, a and b are the dilatational deformation potential, uniaxial deformation potential, valence band deformation potential and valence band shear deformation potential, respectively, where the $\pm$ separates the LH and HH valleys and where ϵ_k is the directional strain that results in the minimal $\Delta E_{\mathrm{C},k}$.

Novel FDSOI material contains a strained silicon channel for the NFET and a strained silicon germanium ($Si_{1-x}Ge_x$) channel, with $x = 0.25$ the mole fraction of germanium, for the PFET [42]. The stress is applied by integrated in-situ boron doped (ISBD) $Si_{1-x}Ge_x$ raised source and drain (RSD) for the PFET and in-situ phosphorous doped (ISPD) Si:C (Silicon with 1 - 2% carbon) RSD for the NFET. The NFET RSD provides channel stresses as high as 500 MPa [15].

We first consider the NFET, where the Si:C RSD lattice is smaller than the Si lattice of the channel. This results in uniaxial tensile stress in the y-direction (channel) and therefore in biaxial compressive stress in the x- and z-direction. The given situation thus corresponds to the fourth case of table 2.12. Assuming silicon in the (100) crystallographic direction, $E = 130.2$ GPa and $\nu = 0.278$ [40]. From equations 2.80 and 2.81 we then obtain $\epsilon_z = 0.38\%$, $\epsilon_x = -0.1\%$ and $\epsilon_y = -0.1\%$ for a stress of $\sigma = 500$ MPa. The deformation potentials for silicon are $\Xi_d = 1.1$ eV, $\Xi_u = 10.5$ eV, $a = 2.1$ eV and $b = -2.33$ eV [41]. From equations 2.82 we then obtain $\Delta E_{\mathrm{C},k} \approx -11$ meV and $\Delta E_{\mathrm{V},k} \approx 7$ meV such that the total band gap energy becomes smaller, i.e. $\Delta E_{\mathrm{G}} \approx -19$ meV.

Next, we consider the PFET, with a $Si_{0.75}Ge_{0.25}$ channel. The lattice constant of germanium is larger than that of silicon, such that biaxial tensile stress results in the channel, perpendicular to the direction of current. This corresponds to the third case of table 2.12. The band gap energy offset is determined by the valence band offset for $Si_{1-x}Ge_x$. That is, $\Delta E_{\mathrm{V}} >> \Delta E_{\mathrm{C}}$ such that $\Delta E_{\mathrm{G}} \approx -\Delta E_{\mathrm{V}}$ [43]. The strain-dependent valence band offset and thus band gap offset is given by [43]:

$$\Delta E_{\mathrm{G}} \approx -\Delta E_{\mathrm{V}} = 0.74 \cdot x. \tag{2.83}$$

From this equation we obtain $\Delta E_{\mathrm{G}} = -0.185$ eV for the effect of strain on the PFET.

In conclusion, the band gap narrowing due to strain is approximately half the band gap widening due to quantum confinement for the NFET. Both effects are negligible, such that the band gap is approximately equal to the bulk value and is $E_{\mathrm{G}} = 1.15$ eV. For the PFET, however, the band gap is significantly narrower due to the combination of strain and a different channel material than silicon, while the effect of quantum confinement can be neglected. We obtain $E_{\mathrm{G}} = 0.98$ eV.

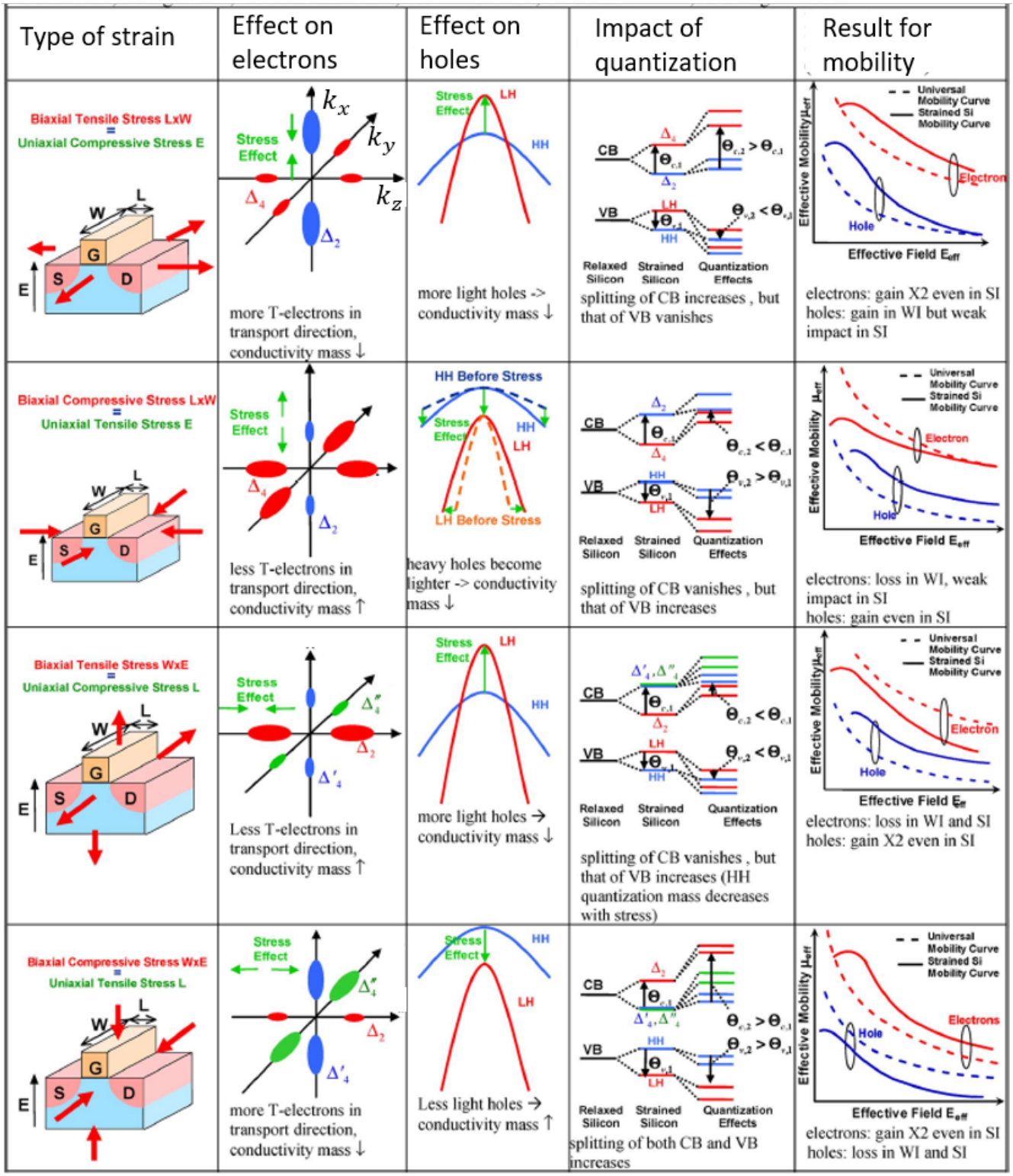


Figure 2.12: Effect of strain on electron and hole mobilities. Indicated are the lenght L, width W and height H of the transistor, as well as the gate G, source S and drain D. Also, several short notations are used: T means transverse effective mass, LH means light holes, HH means heavy holes, CB means conduction band, VB means valence band, WI means weak inversion and SI means strong inversion. Note that Δ_2 valley electrons are transverse to the direction of current flow and are therefore lighter than the Δ_4 valley electrons. Taken from Skotnicki et al. [14].

Chapter 3

Measurements

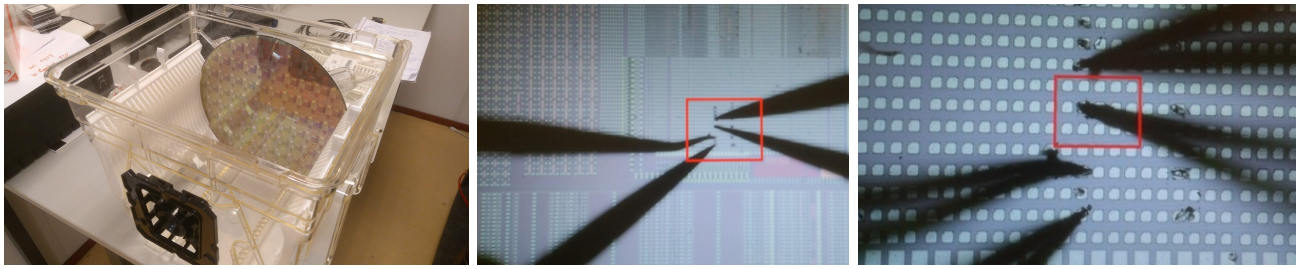
3.1 Measurement method

3.1.1 Wafer Lay-out

This study comprises measurements on FDSOI devices from the 22FDX Global Foundries (GF) technology. A single 300 mm diameter wafer was provided by GF. This wafer contains many equivalent dies (or reticles) with on each die many blocks. These blocks consist of different types of devices, depending on the block. For this study, measurements were mainly performed on a single block. The measurements were performed on different dies for the sake of repeating measurements to ensure reproducibility. The measured block contains many arrays of 25 bond pads, called 25-bond pad arrays, with each of these arrays containing the connections to the electrical terminals for S, D, G, BG and substrate of many transistors. The bond pads are 25x25 μm^2. Each transistor can thus be controlled using 5 bond pad connections. However, the number of transistors is more than the nominal $25/5 = 5$, because several bond pads are connected to multiple transistors, i.e. the connections to either of the mentioned terminals is in parallel for many transistors. The wafer and two zoomed-in pictures of the wafer are shown in figure 3.1.

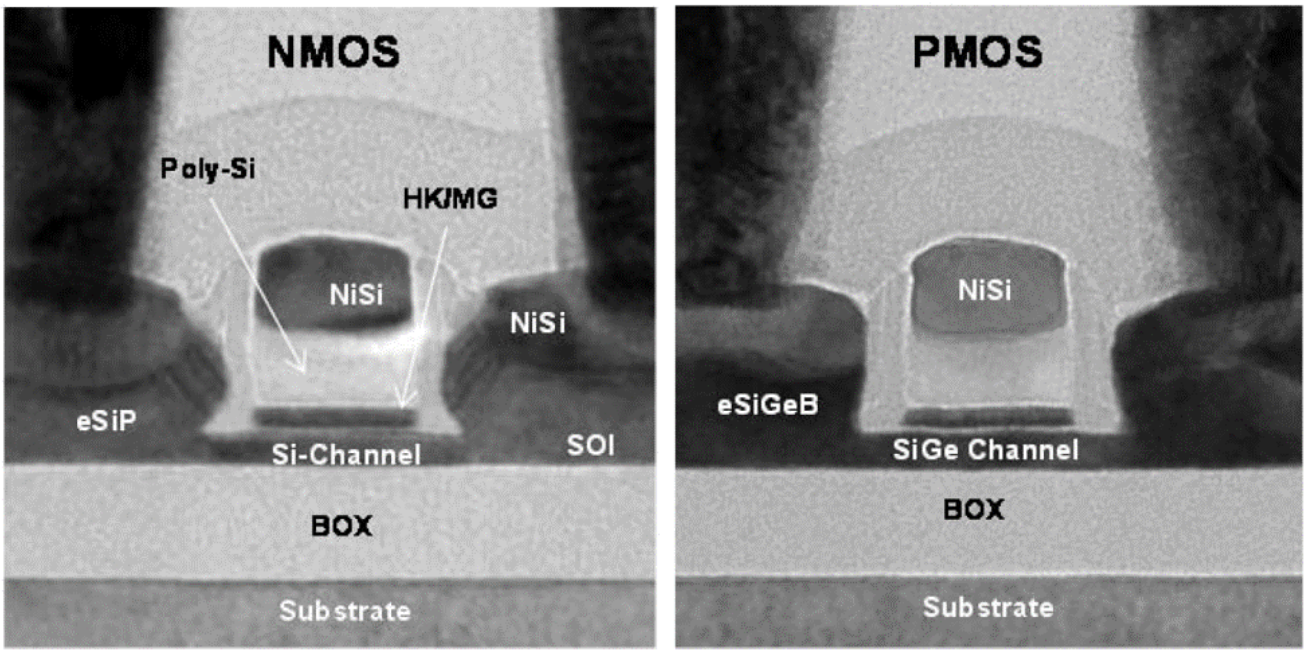
3.1.2 Device specifications

In this study measurements were performed on both NMOS and PMOS FDSOI FETs. A typical cross-section of the used NMOS and PMOS transistor is shown in figure 3.2. Both devices contain a high-k (dielectric) insulating material and a metal gate. The oxide/front gate stack is thus a high-k metal gate (HKMG) stack, as patterned by the standard gate-first approach [16]. The front gate workfunction is



(a) (b) (c)

Figure 3.1: Picture of (a) the 300 mm wafer, showing several repeated structures and thus dies, (b) a zoom-in (2x) of part of a die, showing several blocks, and (c) a zoom-in (10x) of part of a 25-bond pad array. The 25-bond pad array is in vertical direction and several of these arrays (containing different types of devices) are shown in horizontal direction.



(a) (b)

Figure 3.2: Typical cross-section of NMOS and PMOS transistors. Taken from Carter et al. [16].

approximately at midgap, i.e. $\Delta\phi_1 \approx 0$. The NMOS contains an in-situ phosphorous doped (ISPD) Si:C raised source/drain (RSD), also called eSiP, and a strained Si channel. The PMOS contains an in-situ boron-doped (ISBD) SiGe RSD, also called eSiGeB, and a strained SiGe channel [15]. Device constructions use the flip-well architecture for the NMOS and the regular architecture for the PMOS. Both types of FETs are thus placed in n-type wells. The flip-well configuration is well suited for performance enhancement and enables forward body biasing (FBB) such that the devices have a super low threshold voltage (SLVT) and the regular well configuration allows for a leakage current reduction by increasing the threshold voltage via reverse body biasing (RBB) [16]. The configurations are schematically shown in figure 3.3.

Conventionally, transistor devices are distinguished by their effective (front) oxide thickness (EOT): to a thin oxide (up to 2 nm) is referred as SG, to a regular oxide (2 - 5 nm) as EG and to a thick oxide (more than 5 nm) as ZG.

The measured devices contain a body or channel of thickness $t_{\mathrm{si}} \approx 6$ nm, a buried oxide (BOX) of thickness $t_{\mathrm{ox2}} \approx 20$ nm and a front oxide (FOX) of thickness $t_{\mathrm{ox1}} \approx 1.3$ nm. The described devices are thus SG devices and are used for all measurements, unless stated otherwise. We used SG devices with three different channel lengths: $L = 20, 70, 1000$ nm with $W = 1000$ nm.

Additionally, devices with a thick front oxide of $t_{\mathrm{ox1}} \approx 3.5$ nm are used as this results in a more balanced front and back capacitance ratio. These devices are thus EG devices and only NMOS EG devices have been obtained and measured for this study. For the EG devices we used $L = 150, 500, 2000$ nm with $W = 2000$ nm.

3.1.3 Measurement set-up and protocol

The measurement system consists of a Keithley 4200-SCS semiconductor characterization system connected to a Süss Microtech PM300 probe station with a ProbeShield Faraday cage for external field cancellation. The signal through two channels of the characterization system was amplified with the Keithley 4200-PA remote pre-amplifier. The temperature of the workbench chuck can be controlled with the ATT systems temperature control unit. An EA-3008-24 power supply (28V, 3.6A) was used.

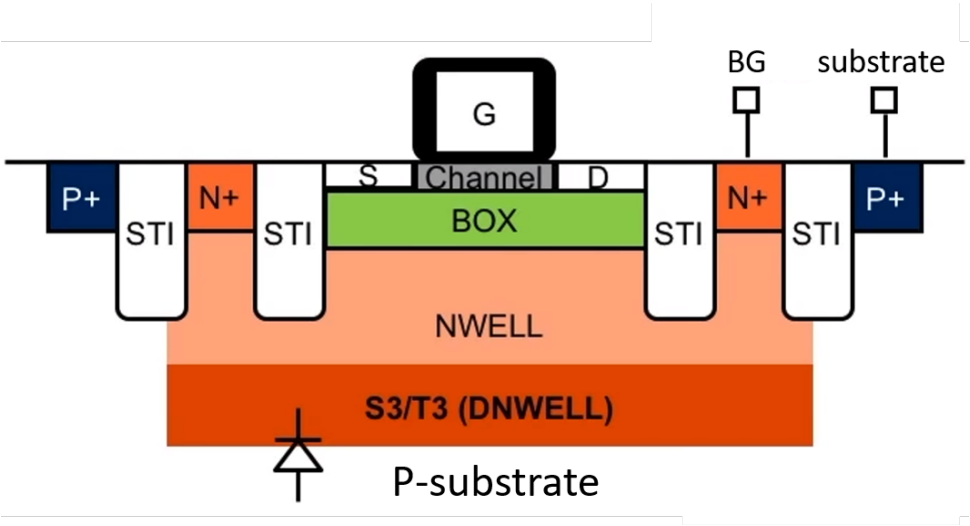


Figure 3.3: Schematically shown FDSOI transistor with n-type well [44]. The figure corresponds to a flip-well NMOST with gate (G), source (S), drain (D), back gate (BG), subtrate, channel, burried oxide (BOX), n-type well (Nwell), n-type deep well (DNwell) and shallow trench isolation (STI) indicated. Additionally, the diode between DNwell and substrate is indicated. The architecture is similar for a regular PMOST. In that case, only the DNwell is replaced by a deep p-type well (DPwell). As a result, a diode between Nwell and DPwell exists as well.

For this study, the drain current was measured as a function of the (front or back) gate to source voltage, such that the transistor transfer characteristics and thus the characteristics of the subthreshold regime are obtained. Output characteristics were not measured. At most four SMUs (source measurement units) were used for the measurements, with Tungsten probe needles of at most 15 μm thick. We connected the SMUs to the S, D, G and BG bond pads and ground the chuck of the measurement set-up, i.e. the substrate was grounded. The source voltage was set to 0 V as default and is taken as ground, i.e. all voltages are referred to the source voltage. As only two pre-amplifiers were available for most measurements, the drain and front gate terminals were connected via the pre-amplifiers, such that the data obtained from these terminals is more accurate. For all measurements, the operation speed was set to "quiet" and the measurement range of at least the drain current was set to "automatic". This enabled the most accurate measurement performance throughout a large voltage range. The temperature of the chuck was set to 298.15 ± 0.5 K (25 ± 0.5 °C) for all measurements.

First we discuss the general measurement procedure for the NMOST. Then, we give some additional remarks.

NMOST measurement procedure

For the single sweep measurements, as discussed in theory section 2.6, the drain current was measured as function of the front gate to source voltage. The back gate is set at a fixed voltage. The default value for this is $V_{\mathrm{BGS}} = 0$ V, but measurements with $V_{\mathrm{BGS}} = -1$ and $V_{\mathrm{BGS}} = 1$ V were performed. Here, V_{GS} is V_{G1} from the theory, when referred to the source, and V_{BGS} is V_{G2}. We set $V_{\mathrm{DS}} = 25$ mV as default, such that the lateral electric field is negligible. Additionally, some initial characterization was performed for $V_{\mathrm{DS}} = 0.8$ V. For the front gate voltage we took $-0.5 \leq V_{\mathrm{GS}} \leq 0.8$ V with a stepsize of $\Delta V_{\mathrm{GS}} = 5$ mV for the general transfer characteristics and we took a smaller range for the front gate voltage, with limits depending on the fixed back gate bias, with $\Delta V_{\mathrm{GS}} = 0.2$ mV for the subthreshold measurements. The subthreshold measurement stepsize is near the limit of the measurement device capabilities and could therefore not be taken much smaller.

For the dual sweep measurements, as discussed in theory section 2.7, the drain current was measured as function of gate to source voltage. Both the front gate and back gate were varied, with the two voltages being related to each other with a constant ratio $V_{\mathrm{GS}} = kV_{\mathrm{BGS}}$. The drain to source voltage was taken the same as for the single sweep measurements and we took $0 \leq V_{\mathrm{GS}} \leq 0.3$ V with $\Delta V_{\mathrm{GS}} = 0.2$ mV for the subthreshold measurements. Measurements were performed for several k-values, ranging between 0 and 25.

All measurement series were started with a measurement for a gate voltage range of $-0.5 \leq V_{\mathrm{GS}} \leq 0.8$ V and a stepsize of $\Delta V_{\mathrm{GS}} = 20$ mV where all currents were observed to check for broken devices or contact issues. For the accurate measurements only the drain current was saved as function of front gate voltage (and back gate voltage, for dual sweep measurements), as this saved a lot of time.

Measurement procedure remarks

The well-type has a limit for the back gate voltage range that can be used. In order to explain this, the reader is referred to figure 3.3. For the flip-well NMOST, applying a potential more negative than the substrate potential results in a forward-biased DNwell/substrate diode. Thus, $V_{\mathrm{BGsub}} > 0$ V, with V_{BGsub} the back gate voltage referred to the substrate. For our dual sweep measurement this does not pose any problem, but for the single sweep measurements we could not apply $V_{\mathrm{BGS}} = -1$ V. In order to solve this issue, we increased all probe voltages (S, D, G and BG voltages) by 1 V. Then, $V_{\mathrm{BGsub}} = 0$ V while we still applied $V_{\mathrm{BGS}} = -1$ V. The same voltage level shift is applied for $V_{\mathrm{BGS}} = 1$ V for obtaining equal measurement procedures. Note that this voltage level shift should not cause any additional problems, since the only increasing fields are from the S/D/G to the substrate, and these fields are across the shallow trench isolation (STI) between the devices.

3.1.4 Data analysis

Drain-source voltage

Ideally, no drain-source voltage should be applied such that the influence of the lateral field on the drain current is non-existent. However, in this situation no current would flow. In order to be able to measure an appreciable drain current, a small voltage thus has to be applied to the drain. The influence of this applied voltage on the surface potentials should be negligible in order to ensure that the influence on the drain current is negligible. We used the change in the surface potentials due to thermal fluctuations as the criterium. The applied drain to source voltage should be smaller than these thermal fluctuations to not influence the observed subthreshold characteristics. The surface potentials corresponding to the thermal fluctuations are $\psi_{\mathrm{s1}} = \psi_{\mathrm{s2}} = u_{\mathrm{T}} = 25.8$ mV at room temperature. We used $V_{\mathrm{DS}} = 25$ mV such that the requirement $V_{\mathrm{DS}} < u_{\mathrm{T}}$ is met.

Regression analysis

Additionally, the drain current measurement exhibits measurement noise. The slope of the drain current, the transconductance, can be quite noisy because the measurement fluctuations are enhanced for obtaining the slope such that we additionally obtain numerical fluctuations. Therefore, for subthreshold regime measurements, we averaged the drain current within a certain interval before taking the derivative. For the averaging we used a regression analysis of which the window is defined by the thermal voltage. This is because also the regression window has to be smaller than the change in surface potential due to thermal fluctuations in order to ensure that the averaging does not influence any physical results. Thus, the datapoints we used for our regression should in principle be within the same physical limits.

The regression window is given by the gate voltage step size ΔV_{GS} times the number of data points over which we regress, n. Within this window we use the characteristic of the subthreshold regime that the drain current (approximately) exponentially depends on the surface potentials, hence gate voltage.

A linear regression analysis was used on the logarithm of the drain current as function of gate-source voltage within the window $n\Delta V_{\mathrm{GS}} \leq u_{\mathrm{T}}$. For our subthreshold measurements with $\Delta V_{\mathrm{GS}} = 0.2$ mV we can take $n < 129$. We took $n = 41$ ($\rightarrow n\Delta V_{\mathrm{GS}} = 8.2$ mV), such that enough data points are used for proper data smoothing but that we were still significantly below the thermal voltage. For $n = 41$, the first subthreshold swing value or ideality factor value corresponds to the 21st actual measurement data point. The last value corresponds to the $N + 1 - 21$st measurement data point, with N the total number of data points. We thus lost a number of measurement data points equal to the regression window size, half of which at the beginning and half at the end of the measurement window.

Mathematically, the relation for linear regression is given by

$$y = b_0 + b_1 \cdot x, \tag{3.1}$$

with x the independent variable, y the dependent variable, b_0 the offset and b_1 the slope. The least-squares method is then used to determine the slope and offset parameters:

$$b_1 = \frac{\sum_i^n (x_i \cdot y_i) - \sum_i^n (x_i) \sum_i^n (y_i)}{n \cdot \sum_i^n (x_i^2) - \sum_i^n (x_i) \sum_i^n (x_i)}, \tag{3.2a}$$

$$b_0 = \frac{\sum_i^n (x_i^2) \sum_i^n (y_i) - \sum_i^n (x_i) \sum_i^n (x_i \cdot y_i)}{n \cdot \sum_i^n (x_i^2) - \sum_i^n (x_i) \sum_i^n (x_i)}, \tag{3.2b}$$

with $n = 41$ the regression window.

From the definition of the subthreshold swing (equation 2.3) we find that the $\log_{10}$ of the drain current is linearly related to the gate-source voltage within the small regression window of size n. Therefore, we take $y = \log_{10}(I_{\mathrm{D}})$ and $x = V_{\mathrm{GS}}$ to find b_0 and b_1. The regression drain current value is then given by:

$$I_{\mathrm{D,reg}} = I_{\mathrm{reg,0}} \cdot \exp(b_0 + b_1 \cdot V_{\mathrm{GS}}), \tag{3.3}$$

where $I_{\mathrm{D,reg}}/I_{\mathrm{reg,0}}$ is unitless, just as the RHS of the equation, with $I_{\mathrm{reg,0}} = 1$ A/μm. From this the transconductance is given to be $g_{\mathrm{m}} \equiv dI_{\mathrm{D,reg}}/dV_{\mathrm{GS}} = b_1 \cdot I_{\mathrm{D,reg}}$. The subthreshold swing, or actually the ideality factor, can then be determined from the ratio of drain current and transconductance according to equation 2.4 ($m = \frac{1}{u_{\mathrm{T}}} \frac{I_{\mathrm{D}}}{g_{\mathrm{m}}}$).

As discussed, the drain current exponentially depends on the surface potential(s) for a symmetric DG device (see equation 2.1) and this is still approximately true for asymmetric DG devices with k around k_0. For the regression window used here (8.2 mV) the difference between the regressed transconductance and the transconductance obtained using the central finite difference theorem seems to be negligible, as will be shortly discussed in section 4.2 (in paragraph "Extracting the transconductance"). For cases with significant differences between the two surface potentials, care should be taken with the regression analysis described above. In those cases, the given relation for the regressed drain current is not actually true, as the linear surface potential terms (see equation 2.10) start to dominate. The result is that the obtained transconductance has an additional analysis-induced error. This error has then also been incorporated in the extracted ideality factor.

For cases with a significant difference between the two surface potentials and for measurements outside of the subthreshold regime, the transconductance should be obtained using the central finite difference theorem.

In summary, for measuring in the subthreshold regime we used the regression analysis. From the slope and intercept of the regression line within a window of n data points the regressed drain current was determined and from this the corresponding regressed transconductance. The drain current and (regressed) transconductance were then used to determine the ideality factor, from which the interface trap density can in turn be determined. If we simply want to obtain the transconductance, such as for strong inversion, we used the central finite difference theorem.

Interface trap extraction

For the interface trap extraction we use the method as described in the theory, section 2.7 [21]. The measured ideality factor as a function of the gate-source voltage for several k-values is used to extract k_0 from, as a function of the gate-source voltage. Here, k_0 is extracted by interpolating between the datapoints to obtain k at $m = 1$. We then assume that one of the two interfaces contains no traps and thus attribute all the traps to the other interface. We use the simplified equations, 2.36, 2.37, 2.40 and 2.41, to obtain the trap capacitance and density at the trap-containing interface.

3.2 Measurement Results & Discussion

We discuss results for both single sweep and dual sweep measurements, in that order. General transistor characteristics are described for the single sweep measurements, as this is the general use of FDSOI devices. For the dual sweep measurements we mainly focus on the k-sweep method (see theory section 2.7). Measurement are performed on SG NMOSTs, unless stated otherwise, and the width of the devices is $W = 1$ μm.

3.2.1 Measurement results for single gate sweep

General transfer characteristics

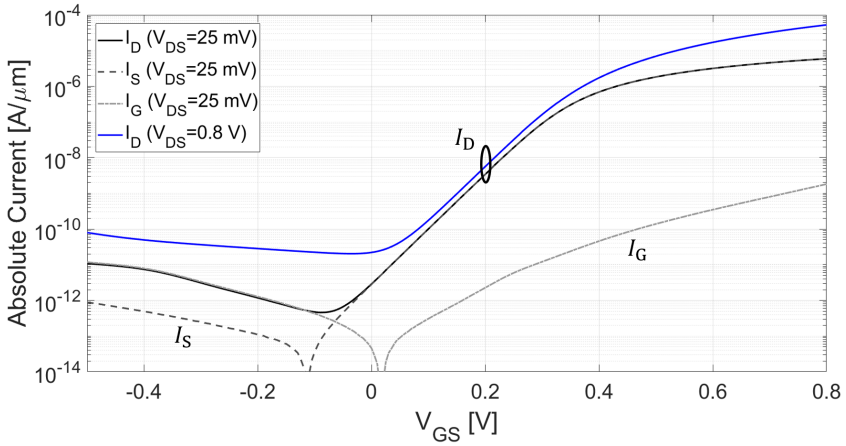
The general NMOST transfer characteristics on a logarithmic (log-lin) and linear (lin-lin) scale are shown in figure 3.4 for a (long channel) device with $L = 1$ μm and $V_{\mathrm{BGS}} = 0$ V.

Figure 3.4 (a) shows the absolute drain current, source current and front gate current for $V_{\mathrm{DS}} = 25$ mV, with the drain current also shown for $V_{\mathrm{DS}} = 0.8$ V, on a logarithmic scale. The back-gate current is negligible ($< 10^{-14}$ A/μm) and is not shown. The absolute values are given per unit gate width. Actually, the source and gate current are negative and the drain current is positive.
Three regions of operation can be distinguished: 1) for high front gate voltages (approximately $V_{\mathrm{GS}} > 0.4$ V) the drain current starts to saturate. 2) for smaller positive front gate voltages ($0 < V_{\mathrm{GS}} < 0.4$ V) the device operates in the subthreshold regime and the drain current seems to exponentially depend on the front gate voltage. 3) for negative front gate voltages ($V_{\mathrm{GS}} < 0$ V) the drain current slightly increases.

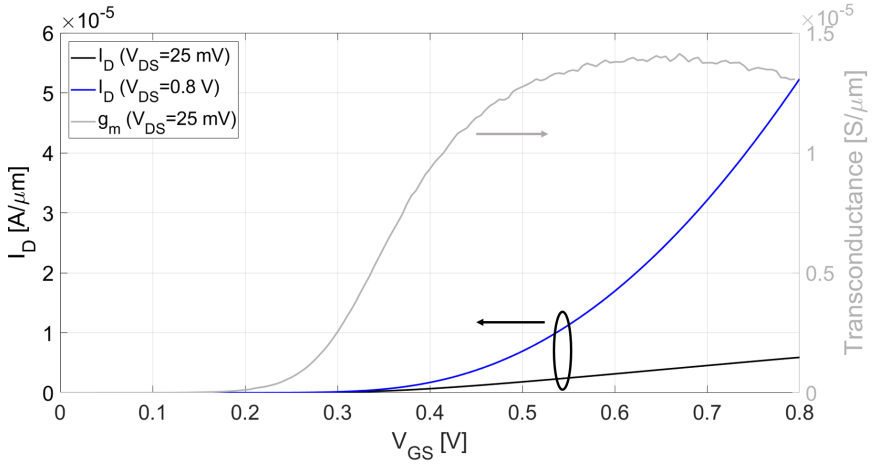
In the first two regions of operation the drain current is dominated by the source current contribution. Thus, the device behaves as intended and we do not have significant gate leakage. In the first region of operation the gate current does seem to increase more rapidly than drain and source current and care should thus be taken for further increasing the front gate voltage. Still, the gate current is approximately more than 3 orders lower than the drain and source current. In the third region of operation the drain current is dominated by the gate current due to gate leakage.

Additionally, the drain current is shown for $V_{\mathrm{DS}} = 0.8$ V. The same three regions can be distinguished and the contributions of source and gate current are similar (not shown). Due to the higher drain-source voltage, the electric field resulting in GIDL is reached at lower front gate voltages, as can be observed. In the subthreshold regime the curve seems to have shifted to the left for the higher drain-source voltage. This effect is called drain-induced barrier-lowering (DIBL) and was also mentioned in the introduction. The higher drain potential effectively pulls down the energy bands in the channel resulting in a lower threshold voltage. Here the effect is approximately 19 mV/V (shift in front gate voltage in subthreshold regime per added unit of drain-source voltage).

Figure 3.4 (b) shows the drain current for $V_{\mathrm{DS}} = 25$ mV and for $V_{\mathrm{DS}} = 0.8$ V on a linear scale. Also, the transconductance for $V_{\mathrm{DS}} = 25$ mV is shown. The maximum transconductance is at approximately $V_{\mathrm{GS}} = 0.65$ V. The transconductance for $V_{\mathrm{DS}} = 0.8$ V (not shown) does not have a maximum in the measurement range. The method of extrapolation in the linear regime (ELR), as given by equation 2.46 and shown in figure 2.9 in the theory, is used to determine the threshold voltage for $V_{\mathrm{DS}} = 25$ mV. We obtain $V_{\mathrm{T}} = 365$ mV.



(a)



(b)

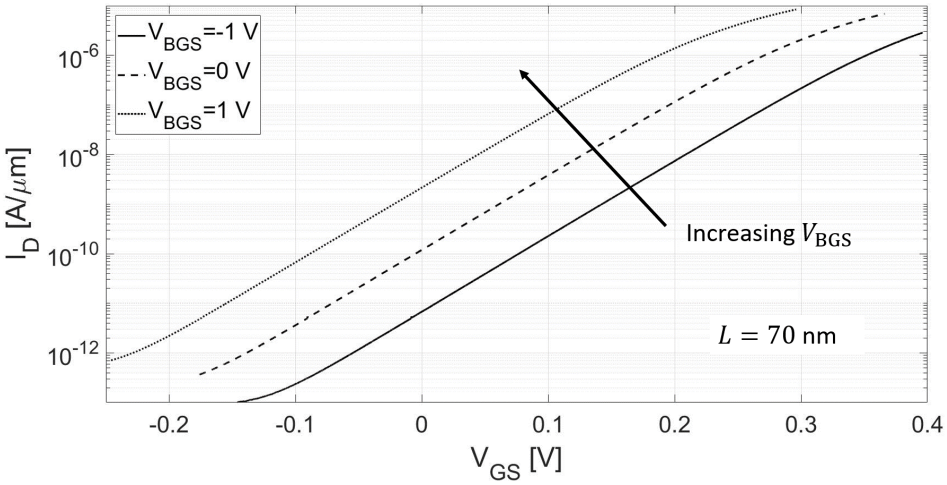
Figure 3.4: Drain current per unit width as a function of gate-source voltage at $V_{\mathrm{BGS}} = 0$ V for a $W/L = 1/1$ μm device on a (a) log-lin scale and (b) lin-lin scale. (a) shows the drain current I_{D}, absolute source current I_{S} and absolute gate current I_{G} for $V_{\mathrm{DS}} = 25$ mV and the drain current for $V_{\mathrm{DS}} = 0.8$ V. (b) shows the drain current I_{D} for $V_{\mathrm{DS}} = 25$ mV and $V_{\mathrm{DS}} = 0.8$ V (left y-axis) and the transconductance g_{m} for $V_{\mathrm{DS}} = 25$ mV (right y-axis).

Back gate bias effect

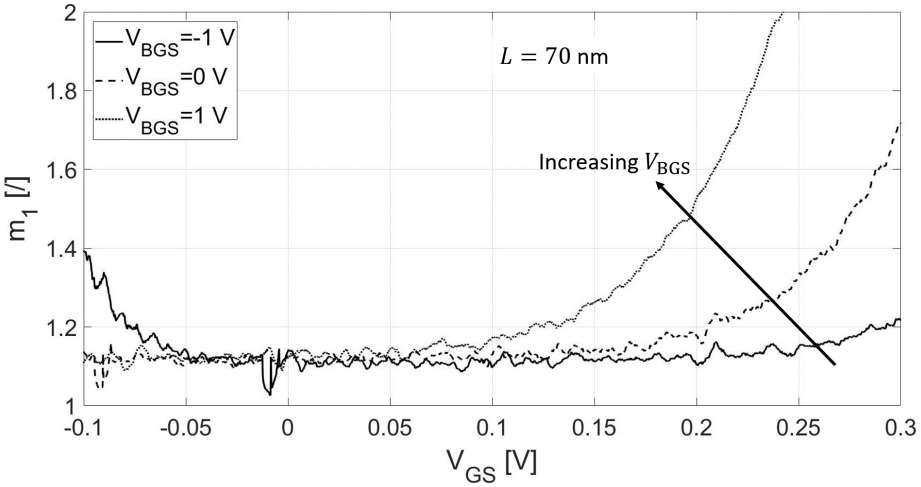
The effect of applying a fixed back gate bias voltage is demonstrated in figure 3.5 for a device with $L = 70$ nm. The fixed back gate voltage is taken to be -1 V, 0 V or 1 V.

Figure 3.5 (a) shows the drain current per unit gate width as a function of the front gate voltage, where the curves shift leftwards/upwards for an increasing back gate voltage. Referring to the shift as upwards thus shows how the current increases for an increasing back gate voltage. Referring to the shift as leftwards describes how the increase in back gate voltage translates to a threshold voltage change. Note that this is just a single physical effect explained in two ways.

This threshold voltage shift can be expressed in device parameters (see equation 2.22) and is expressed in units of threshold voltage change per unit of back gate bias. From the given figure this threshold voltage shift can thus be estimated from the shift in the subthreshold curve to the left. For a device with $L = 70$ nm, we obtain $\Delta V_{\mathrm{T}}/\Delta V_{\mathrm{BGS}} \approx 80$ mV/V and for a device with $L = 1$ μm (not shown) we obtain 83 mV/V.



(a)

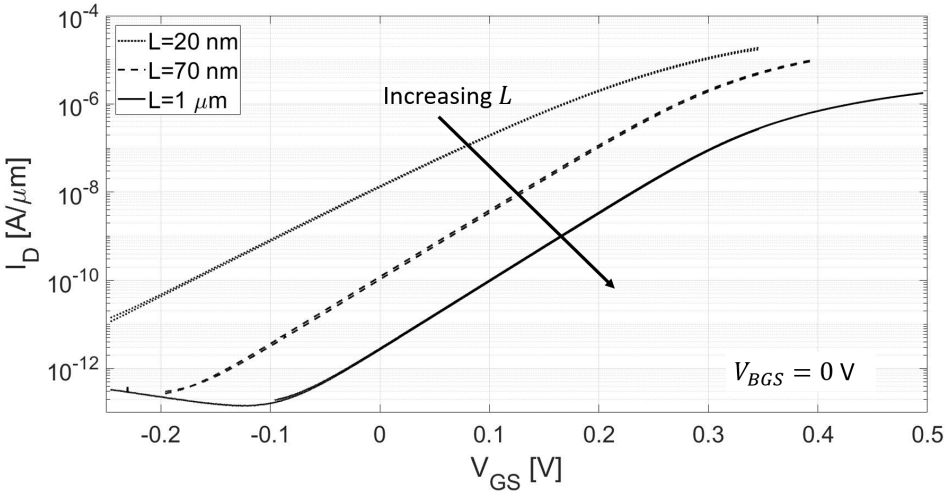


(b)

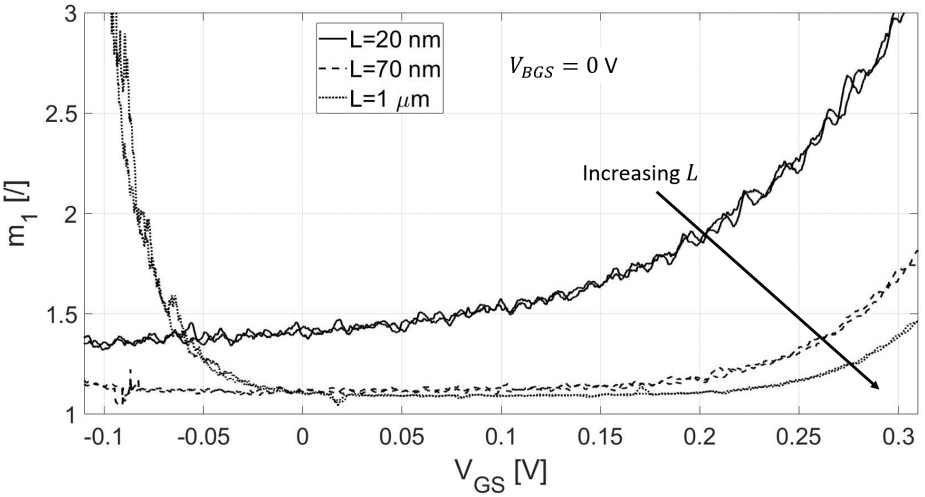
Figure 3.5: (a) Drain current per unit width (left y-axis) as a function of gate-source voltage for a back gate voltage of $V_{\mathrm{BGS}} = -1, 0, 1$ V for a $W/L = 70/1000$ nm device and (b) corresponding ideality factor m_1 as a function of gate-source voltage.

Figure 3.5 (b) shows the ideality factor (referred to the front gate voltage) as a function of the front gate voltage. The shown ideality factor is obtained using the regression analysis. The deviation of the subthreshold swing from the ideal case (SS= $m \cdot \ln(10) u_{\mathrm{T}}$) is thus examined at each front gate voltage value. Note that, in contrary to what the name suggests, a higher value for the ideality factor actually means a less ideal subthreshold swing.

The minimal value for the ideality factor is approximately equal for all three back gate voltages and is $m_1 \approx 1.12$. The ideality factor curve shifts to the left for increasing back-gate voltages, just as the curves for the drain current. Note that the ideality factor has already significantly increased before the threshold voltage. For example, for $V_{\mathrm{BGS}} = 0$ V at $V_{\mathrm{GS}} = 0.25$ V the value of the ideality factor has doubled with respect to the minimal value. Since the threshold voltage was found to be $V_{\mathrm{T}} = 365$ mV previously, this non-ideal behaviour sets in for much lower front gate voltages (approximately 100 mV lower) than expected. This unexpected increased ideality factor is called the apparent conduction band edge [20].



(a)



(b)

Figure 3.6: (a) Drain current per unit width (left y-axis) and transconductance per unit width (right y-axis) as a function of gate-source voltage for a channel length of $L = 20, 70, 1000$ nm for a 1 μm width device and (b) corresponding ideality factor m_1 as a function of gate-source voltage. Results for each channel length are given for measurements at two different dies, to show die-to-die variability.

Channel length effect

The effect of the channel length is demonstrated in figure 3.5 for a device with $V_{\mathrm{BGS}} = 0$ V. The examined channel lengths are 20 nm, 70 nm and 1 μm. The measurement results are shown for measurements on two different dies and show only a small deviation.

Figure 3.6 (a) shows the drain current per unit gate width as function of the front gate voltage. The curve shows the same trend as was shown for the different back gate voltages (figure 3.5). The current increases for shorter devices, as can be expected since the channel resistance decreases. Also, the leftward shift of the curve means that the decrease in channel length effectively decreases the threshold voltage. The most important aspect of the shown curves for this work, however, is the subthreshold swing. In the shown drain current figure it is already clearly visible that the subthreshold swing increases for a 20 nm device with respect to the other two because of SCE. The difference between the 70 nm and 1 μm devices is not so apparent.

Figure 3.6 (b) shows the ideality factor (referred to the front gate voltage) as a function of the front gate voltage. The ideality factor has a minimum value of $m_1 \approx 1.10$ for $L = 1$ μm and $m_1 \approx 1.12$ for $L = 70$ nm, which is the same as for figure 3.5 (b). Devices with these two channel lengths thus show a minimal subthreshold swing degradation as result of a change in channel length. The main effect is the threshold voltage change and thus shift of the curve to the left for a decreasing channel length. The minimum ideality factor value is $m_1 \approx 1.35$ - 1.5 for a device with a channel length of $L = 20$ nm. The ideality factor does not show a minimum plateau such that the bathtub shape obtained for all other cases is not present. This bathtub shape is well-known and is caused by channel accumulation (left edge) or depletion (right edge). This right edge should be around the threshold voltage, but it is found that usually an apparent conduction band edge is observed for lower gate-source voltages [20]. Significant degradation of the subthreshold swing is observed for decreasing the channel from 70 to 20 nm. So, where using the interface trap extraction method on a device with a 70 nm channel length might still be valid, this is definitely not the case for a device with a 20 nm channel length. The observed trend is the result from short-channel effects (SCE).

Measurement deviations

The influence of measurement deviations is shown in figures 3.7 and 3.8 for a device with $V_{\mathrm{BGS}} = 0$ V and $L = 70$ nm. Assessing the measurement deviation is needed as this presents the absolute lower limit of our accuracy.

In figure 3.7 we examine this accuracy by means of the deviation in the ideality factor. The average (avg) and standard deviation (std) of the ideality factor for $n = 3$ measurements are shown.

The std for $n = 3$ measurements can be determined for each front gate voltage:

$$\mathrm{std} = \sum_{i}^{n} \left(\frac{(x_i - x_{\mathrm{avg}})^2}{n-1} \right), \tag{3.4}$$

with $x = m_1$ for the calculation of the std of the ideality factor.

The obtained std is subtracted from and added to the avg ideality factor, and the resulting band is shown in the figure around the average ideality factor. If we sum the std and avg ideality factor over all measured V_{GS} and divide the two the total relative std is obtained (=std/avg).

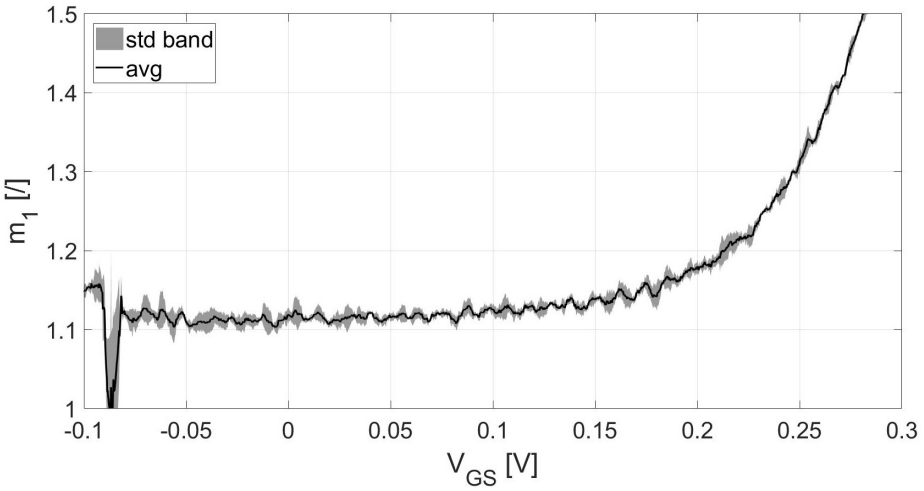


Figure 3.7: Average (avg) ideality factor m_1 as function of gate-source voltage with standard deviation (std) band indicating the std around the average value for $n = 3$ measurements at $V_{\mathrm{BGS}} = 0$ V for a $W/L = 1000/70$ nm device.

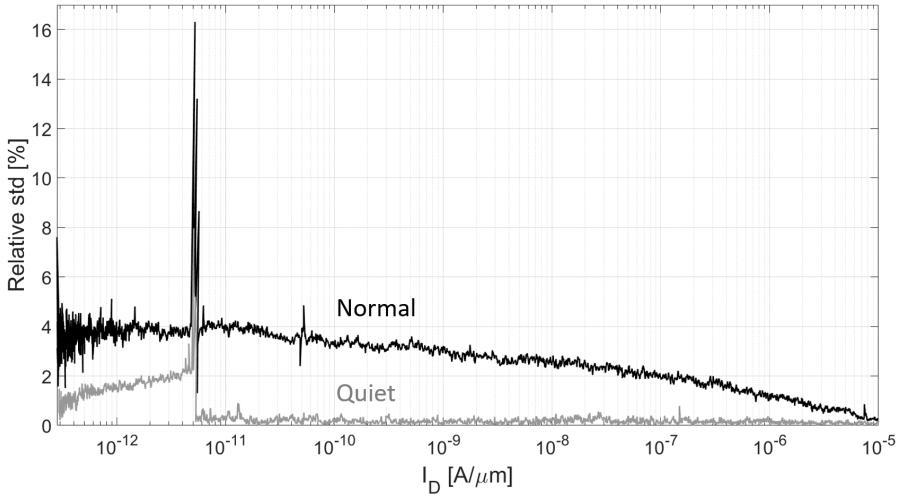


Figure 3.8: Ratio of standard deviation of the drain current to the average drain current as a function of drain current for measurements performed at "normal" and "quiet" measurement speeds for $n = 3$ measurements at $V_{\mathrm{BGS}} = 0$ V for a $W/L = 1000/70$ nm device.

For the given figure we obtain a total relative std of 1 %. This, however, exaggerates the std for positive front gate voltages, since a higher deviation is observed for negative front gate voltages (because of the lower and more noisy drain current).

In figure 3.8 the relative std is examined for drain current value. In order to do so, we use equation 3.4 with $x = I_{\mathrm{D}}$ and then define the relative std as the ratio std/avg at each front gate voltage value. We then plot the relative std at each drain current value corresponding to this front gate voltage value to obtain the shown figure. The procedure is performed for "normal" and for "quiet" measurement speeds.

First of all, the "normal" measurement speed has a higher relative std than the "quiet" measurement speed. A peak in relative std is shown at $I_{\mathrm{D}} \approx 5 \cdot 10^{-12}$. This peak corresponds to a front gate voltage of $V_{\mathrm{GS}} \approx -85$ mV for the shown measurement. For measurements with a normal speed the relative std is around 4% for $V_{\mathrm{GS}} = -0.2$ V (lowest drain current value) and slowly decays to 1% at $V_{\mathrm{GS}} = 0.3$ V (highest drain current value). For quiet measurements the relative std is around 0.5% for $V_{\mathrm{GS}} > -85$ V or $I_{\mathrm{D}} > 5 \cdot 10^{-12}$. The results obtained with quiet measurements for the described range are therefore accurate to 0.5%.

The peak in the relative std is attributed to a change in the measurement range (due to the "automatic" setting). The results obtained at this specific drain current (or front gate voltage corresponding to this, depending on the measurement method and device parameters) effectively show a measurement artifact. This artifact is clearly visible in figure 3.4 (b), 3.6 (b) and 3.7.

The Keithly manual describes the measurement errors for various ranges of measured current. In the range of 0.1 A $< I <$ 0.1 nA the specified measurement error is around 0.1 - 0.2%. For currents smaller than this, down to the measurement limit, the measurement error increases to approximately 2%. The shown increase in error for the small currents with the quiet measurement setting is thus expected.

We now assessed the FDSOI device characteristics under standard industry use: varying the front gate voltage and using the back gate as threshold voltage modulator. Note that the front gate voltage range for the m_1 figures is different from the range of the corresponding I_{D} figures. This is because the actual range is zoomed in on to obtain the range shown, to better show the minimal ideality factor value and its bathtub shaped curve.

3.2.2 Measurement results for dual gate sweep

General k-sweep results

The subthreshold characteristics for a k-sweep measurement are shown in figure 3.9 for a device with $L = 70$ nm. We use gate bias ratios $k \equiv V_{\mathrm{BGS}}/V_{\mathrm{GS}} = 0, 1, 2, 3, 5, 7, 10, 15, 20, 25$ such that the maximum back gate voltage is $V_{\mathrm{BGS}} = 0, 0.3, 0.6, 0.9, 1.5, 2.1, 3.0, 4.5, 6.0, 7.5$ V. Thus, the number of back gate voltage steps is equal to the number of front gate voltage steps, but the stepsize and range are different depending on k. Note that $k = 0$ corresponds to a fixed back gate voltage of $V_{\mathrm{BGS}} = 0$ V.

Figure 3.9 (a) shows the drain current as a function of the front gate voltage for different k-values. The subthreshold swing clearly improves for higher k and the threshold voltage decreases.

The improvement in subthreshold swing is better visualized with the ideality factor in figure 3.9(b). Solely taking into account the FOX and BOX thickness, the drain current is expected to barely change with the back gate-source voltage in case of a relatively thick BOX layer. That is, for $t_{\mathrm{ox2}}/t_{\mathrm{ox1}} \to \infty$ it could even be argued that the interface of the BOX and silicon channel is a virtual ground for e.g. $k = 1$. This expectation is evidently incorrect for $t_{\mathrm{ox2}}/t_{\mathrm{ox1}} = 20/1.3 \approx 15$, as $k = 1$ already shows a significant increase in the subthreshold swing with respect to $k = 0$ (fixed back gate bias at $V_{\mathrm{BGS}} = 0$ V). For example, increasing k from $k = 0$ to $k = 1$ and to $k = 25$ results in the ideality factor dropping from $m_1 \approx 1.11$ to $m_1 \approx 1.03$ and to $m_1 \approx 0.37$, respectively.

The ideality factor is shown as a function of k in figure 3.9 (c) at $V_{\mathrm{GS}} = 23.8$ mV. The corresponding ideality factor values are indicated by the dotted line in figure 3.9 (b). For the given ideality factor m_1 as function of k in combination with m_2 as function of p the interface trap densities can be extracted.

To start with, we take the cases where one of the two interface trap densities is assumed to be 0 (see equations 2.36 and 2.37 to extract D_{it2} and equations 2.40 and 2.41 to extract D_{it1}). For example, assuming $C_{\mathrm{it1}} = 0$ F/m^2 (no front interface traps) we know that $m_1 = 1$. This procedure is denoted in the figure. The horizontal dotted line denotes $m_1 = 1$ and the solid black dot shows the interpolated value corresponding to $m_1 = 1$ (equation 2.37). This value is needed to obtain the corresponding value of k_0, as indicated with the vertical dotted line.

For this figure we obtain $k_0 \approx 1.37$. From this value of k_0 we can then determine the back interface trap density (equation 2.36).

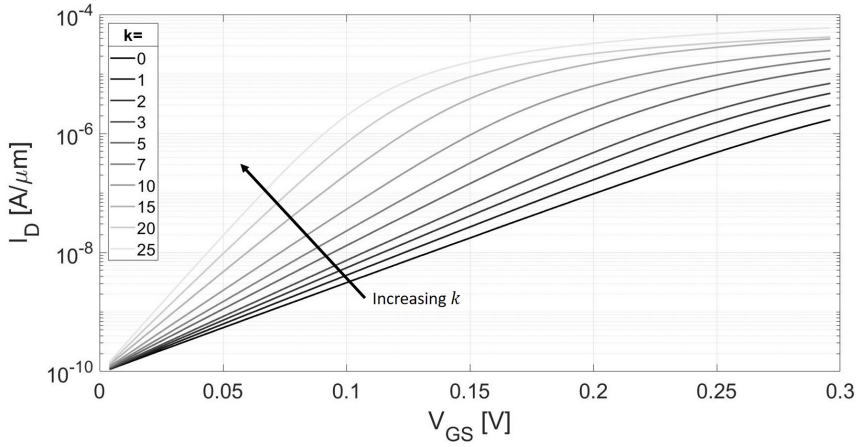
In order to improve the procedure speed and quality, we use less k-values and we take more values within the range of $k = 1$ - 2, respectively. Taking less values reduces the needed measurement time. Taking more values within the mentioned range allows for a smaller interpolation error. Also, we use a long channel device with $L = 1$ μm to ensure no SCE are of influence.

Single interface trap extraction

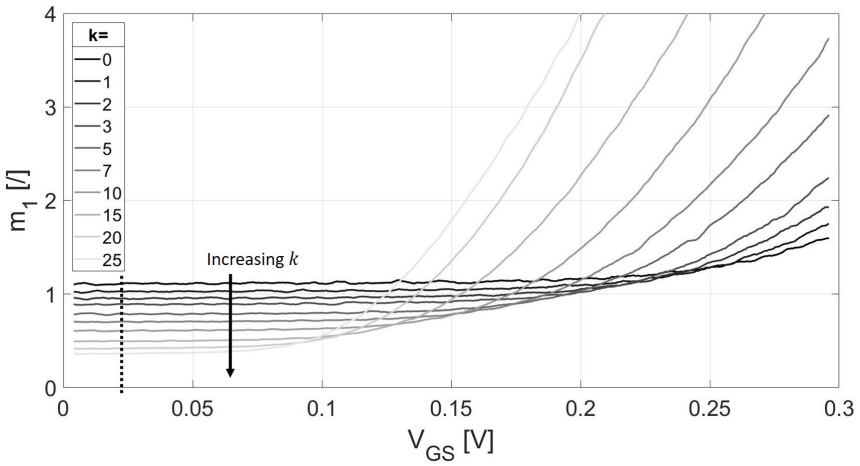
The extraction of the optimal gate bias ratio k_0 is demonstrated in figure 3.10 from measurements with $k = 1, 1.2, 1.5, 2$ for a device with $L = 1$ μm.

Figure 3.10 (a) shows the drain current as a function of the front gate voltage. The increasing subthreshold slope for increasing k is indicated. From the given four curves the optimal gate bias ratio is extracted at each front gate voltage. The resulting optimal gate bias ratio as a function of the front gate voltage is shown in figure 3.10 (b). The fluctuations in the ideality factor caused that the optimal gate bias ratio could not be extracted for all front gate voltages, from the given four k-values. This is because in some cases $m_1 < 1$ for all k, as can be observed from the gaps at e.g. $V_{\mathrm{GS}} = 0.05$ V. Also, for too high front gate voltages the ideality factor deviates so much from the ideal value that $m_1 > 1$ for all k. Therefore, values for the optimal gate bias ratio could only be obtained for approximately $V_{\mathrm{GS}} < 0.22$ V.

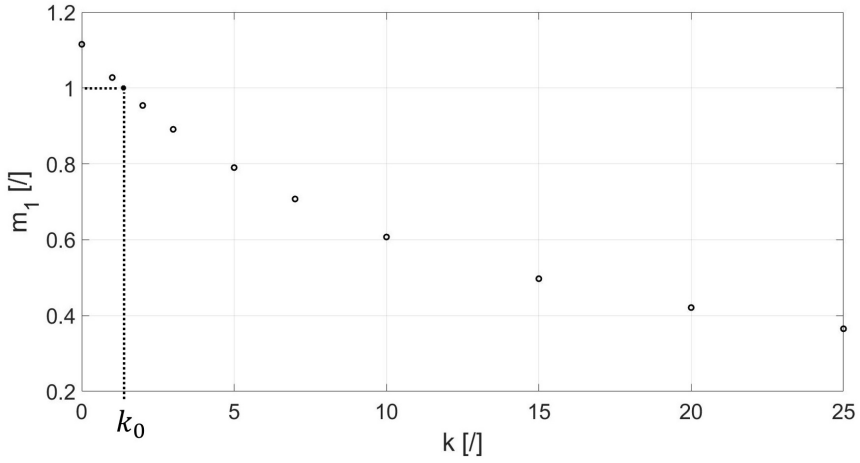
From the extracted k_0 in combination with the front gate referred subthreshold swing SS_1 we can extract the back interface trap capacitance using equations 2.36 ($k_0 \propto C_{\mathrm{it1}}$) and 2.37 (ideal SS_1, thus $m_1 = 1$). We can thus simply compute C_{it2} assuming $C_{\mathrm{it1}} = 0$ F/cm^2 from the extracted k_0.



(a)

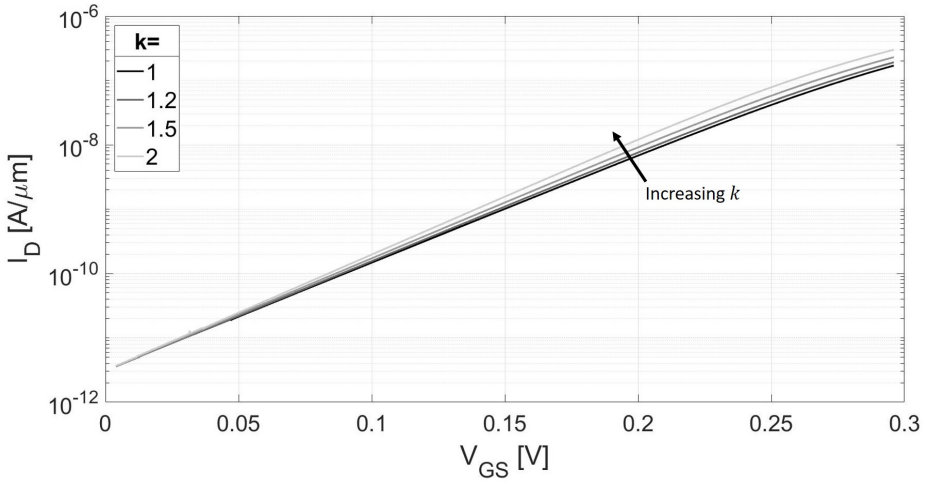


(b)

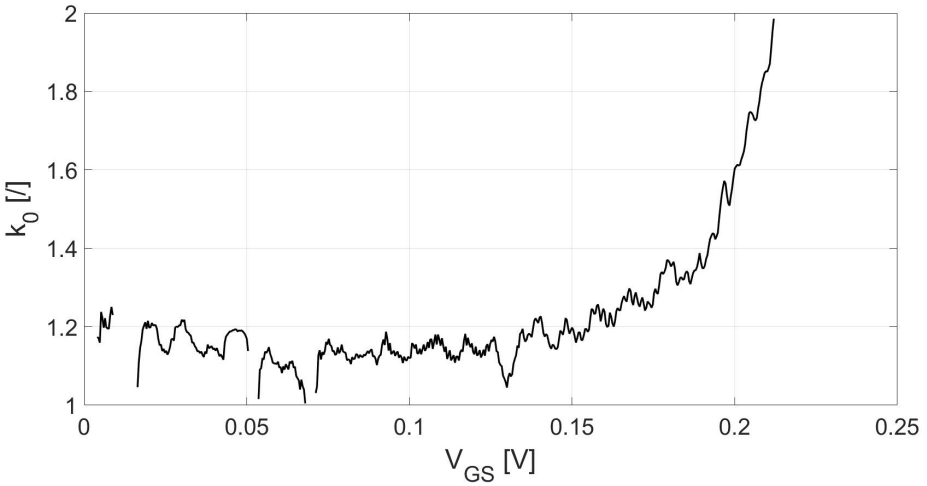


(c)

Figure 3.9: (a) Drain current per unit width as a function of gate-source voltage for a back to front gate voltage ratio of $V_{\mathrm{BGS}}/V_{\mathrm{GS}} \equiv k = 0, 1, 2, 3, 5, 7, 10, 15, 20, 25$ for a $W/L = 1000/70$ nm device, (b) corresponding ideality factor m_1 as a function of gate-source voltage and (c) corresponding ideality factor m_1 as a function of k at a gate-source voltage of $V_{\mathrm{GS}} = 23.8$ mV. This is depicted by the dotted line in (b). The solid black dot shows an interpolated value for $m_1 = 1$ with which the value of k_0 can be calculated assuming $C_{\mathrm{it1}} = 0$ F/cm^2, as indicated by the dotted lines.



(a)



(b)

Figure 3.10: (a) Drain current per unit width as a function of gate-source voltage for a back to front gate voltage ratio of $V_{\mathrm{BGS}}/V_{\mathrm{GS}} \equiv k = 1, 1.2, 1.5, 2$ for a $W/L = 1/1$ μm device and (b) corresponding value of k_0 as a function of gate-source voltage extracted by assuming $C_{\mathrm{it1}} = 0$ F/cm^2.

The procedure is repeated for m_2 and p to obtain C_{it1} for the same device, assuming $C_{\mathrm{it2}} = 0$ F/cm^2. We thus use equations 2.40 ($k_0 \propto C_{\mathrm{it2}}$) and 2.41 (ideal SS_2, thus $m_2 = 1$). For this, the same data is used, but from the data the values of m_2 are determined for the V_{GS}-range by interpolating higher k value data within the given range.

To understand why this is needed we give an example. For a measurement series with $k = 1$ and $k = 2$, we have $0 < V_{\mathrm{GS}} < 0.3$ V for both measurements and $0 < V_{\mathrm{BGS}} < k \cdot 0.3$ V for the two measurement series. Thus, the range for the back-gate voltage is not the same for all measurements and m_2 cannot be easily expressed for a specific range numerically.

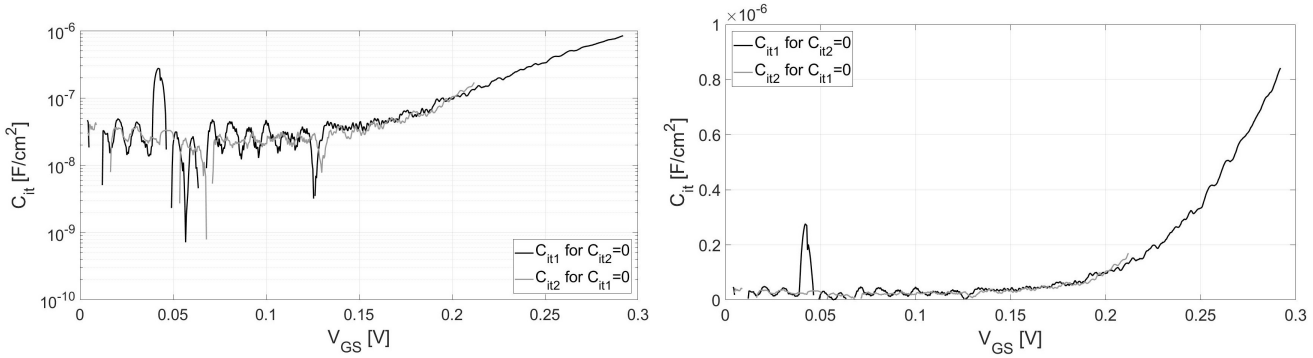
In order to do so, we take the range for $k = 1$ and take the lower half of the range for $k = 2$, where we thus obtain $0 < V_{\mathrm{BGS}} < 0.3$ V. However, the measurement series for $k = 2$ contains the same number of datapoints, and thus only half the number of datapoints in the given range. To obtain a value for m_2 at every datapoint as specified by the $k = 1$-range, we interpolate the measurement series for $k = 2$ within the specified voltage range. From this m_2 as a function of $p = 1/k$ we then extract p_0.

The results for C_{it1} are thus less accurate, but they can be compared to the C_{it2} results. With the mentioned procedure the same values should be obtained for both the front and back interface trap

capacitance. This is the case, because the method implies that the surface potentials at the front and the back side of the channel are the same for the extraction of k_0 (p_0). Therefore, it does not matter which interface trap density is assumed to be 0 and which is extracted, since the deviation of the ideality factor is in both cases fully attributed to the interface traps.

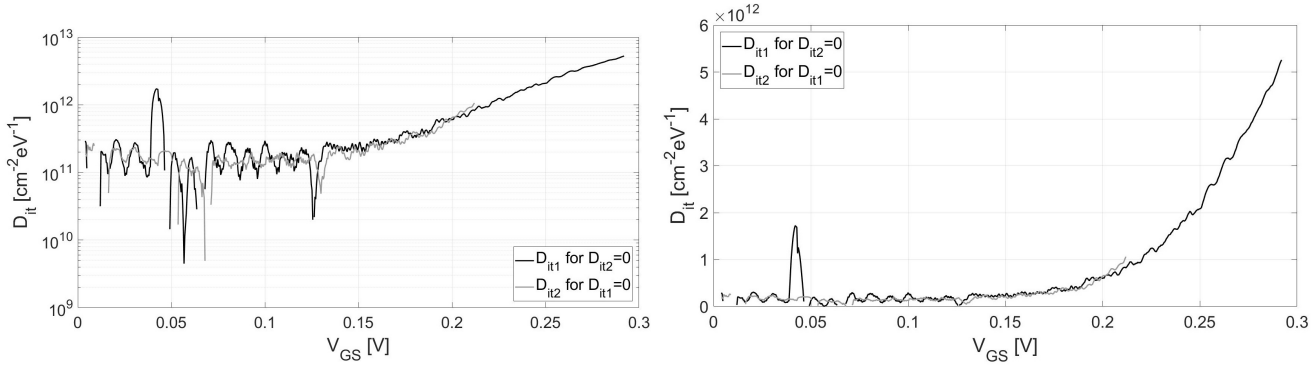
The extracted interface trap capacitance as a function of the gate-source voltage for both cases is shown in figure 3.11, on a logarithmic and linear scale. The interface trap density $D_{\mathrm{it}x}$ is determined from this, using a simple division by q (as is evident from equation 2.5). The extracted interface trap density as a function of the gate-source voltage for both cases is shown in figure 3.12, on a logarithmic and linear scale. The figures show consistent front and back interface trap capacitances and densities for the two cases (of either assuming $C_{\mathrm{it1}} = 0$ F/cm^2 or $C_{\mathrm{it2}} = 0$ F/cm^2).

The high peak in the C_{it}- and D_{it}-curves for $C_{\mathrm{it2}} = 0$ F/cm^2 around 0.04 V is attributed to the effect of the measurement range-change artifact on the measurement for $k = 1$ (as discussed in the "Measurement deviations" paragraph in this section). See the small discrepancy in the drain current at this gate voltage in figure 3.10(a), for $k = 1$.



(a) (b)

Figure 3.11: Interface trap capacitance per unit area as a function of gate-source voltage for a $W/L = 1/1$ μm device on a (a) log-lin scale and (b) lin-lin scale. The results for the interface trap capacitance at one interface are obtained for assuming no interface traps at the other interface. For example, C_{it1} is obtained by assuming $C_{\mathrm{it2}} = 0$.



(a) (b)

Figure 3.12: Interface trap density per unit area per energy as a function of gate-source voltage for a $W/L = 1/1$ μm device on a (a) log-lin scale and (b) lin-lin scale. The results for the interface trap density at one interface are obtained for assuming no interface traps at the other interface. For example, D_{it1} is obtained by assuming $D_{\mathrm{it2}} = 0$.

For the GF FDSOI material used in this study it is known that the BOX/channel interface is of a high quality, since this interface consists of a natural SiO_2/Si interface and the quality of such an interface is known to be generally good. However, the front interface consists of HK/Si, where the exact composition of the HK oxide is unknown to the authors, and the quality of this interface could be poorer [45]. The assumption that the back interface trap density is 0 and that the front interface trap density can be determined could therefore be valid.

In that case, we obtain $D_{\text{it1}} \approx 2 \cdot 10^{11}$ cm^{-2}eV^{-1}, away from the band edge. Near the band edge, the value increases to $\approx 5 \cdot 10^{12}$ cm^{-2}eV^{-1}. In case this assumption is found to be invalid, we have determined the limiting cases here.

3.2.3 Conclusion measurement results

The general single gate sweep measurement characteristics are shown and the effect of the fixed back-gate bias voltage is demonstrated to be $\Delta V_{\text{T}}/V_{\text{BGS}} \approx 80$ mV/V. Also significant short channel effects were shown for $L = 20$ nm. We discussed the drain current measurement accuracy of 0.5% and showed that our measurements contain a measurement artifact, which had to be considered for the processed data.

For the dual gate sweep measurements the effect of k on the drain current is discussed. The resulting difference in the suthreshold swing (or ideality factor) is demonstrated and we showed how to extract k_0 from the given curves. Then we demonstrated how to extract k_0 and p_0 (not shown) as a function of the front gate voltage. From this, the interface trap capacitance and interface trap density was determined for a single interface, assuming the other interface to not contain any traps. From this, considering the back interface to be much better than the front interface, we concluded that $D_{\text{it1}} \approx 2 \cdot 10^{11}$ cm^{-2}eV^{-1}, away from the band edge. We thus extracted the total interface trap density at each gate-source voltage value, i.e. we extracted a value from which the trap density at the front or back interface cannot be distinguished.

For this extraction, we assumed that no short channel effects played a role. Furthermore, we assumed the effects of an unequal front and back gate workfunction to be insignificant, just as the effect of back-gate depletion.

Although not discussed or shown in this chapter, we also performed measurements on PMOS devices. The same trends were observed as for NMOS devices, such that our conclusions did not change.

We thus obtained the front interface trap density in a simplified manner, which can be used to benchmark the obtained results for considering both interfaces simultaneously. Before we do so we would first like to validate the obtained results. For this, we can either use a compact model such as that developed by the BSIM group, or we can use a technology computer-aided design (TCAD) tool such as Silvaco Atlas. We continue with validating the extracted total interface trap density at each gate-source voltage using the BSIM compact model.

Chapter 4

Compact Model Simulations

4.1 Compact modeling method

The compact modeling is described in this section. First we discuss the models, tools and parameters used. Then, the simulation results and their implications are discussed. The BSIM group of the University of California, Berkeley, developed the independent multi-gate (IMG) model [46]. With this model the electrical characteristics of double-gate structures like FDSOI devices can be described by controlling the two gates separately. We use version 102.9.1 of the model for this research [46]. We use the ProMOST simulation tool to run the BSIM model.

4.1.1 Default parameters

Several default parameters can be implemented in the BSIM model, where all of these parameters can be used to fit the electrical characteristics to the measured devices. We used the GF 22FDX default input file for SLVT devices, which corresponds to the measured devices. The input file was adjusted for this work, such that several of the normally constant parameters could be varied, e.g. the oxide thickness, the Nwell doping, the interface trap capacitance and the gate length. For controlling the ProMOST simulations a MATLAB file was used, in which the variable parameters and the bias conditions to be used for the simulations were defined. In this way, the bias conditions as needed for the k-sweep method, i.e. $V_{\mathrm{BGS}} = k \cdot V_{\mathrm{GS}}$, could be transferred to the ProMOST. ProMOST then performed the simulation using the BSIM model with these parameters and the default values from the input file. The required results were then requested by MATLAB such that the electrical characteristics can be stored locally. This way, the output data could be analyzed in the same way as the measurement data.

We distinguished between variable parameters and bias conditions in the following way. The variable parameters are device parameters, i.e. constants for a given device, that we set in MATLAB. These had to be maintained constant throughout a single simulation. An example would be the gate length. The bias conditions can be varied during the simulations and only comprise voltages in our case. In principle, also the device currents or even the interface trap capacitance could be varied. Varying the current then resembles a current source. Varying the interface trap capacitance resembles the different interface trap densities per energy (and thus per voltage). The interface trap capacitance is actually a device parameter but it can be varied with the bias conditions in order to fit the measurement data. We used the following variable parameters with the respective default values: the device width ($W = 1$ μm), gate length ($L = 1$ μm), the (effective) front oxide thickness ($t_{\mathrm{ox1}} = 1.3$ nm), the (effective) buried oxide thickness ($t_{\mathrm{ox2}} = 20$ nm) and the Nwell doping ($N_{\mathrm{well}} = 5e17$ cm^{-3}). For the bias conditions we use V_{GS} and k. Therefore, we thus also vary V_{BGS}. We also define $V_{DS} = 25$ mV and $T = 298.15$ K ($T = 25$ ^{o}C), but these values are maintained constant throughout the simulations. The interface trap capacitance is actually a device parameter, but as it could be voltage-dependent we desire the value to be determined at each bias condition. The interface trap capacitance had a default value of $C_{\mathrm{it}} = 7 \cdot 10^{-8}$ F/cm2.

4.1.2 ProMOST implementations

Several characteristic parameters of the simulated device are difficult to request from ProMOST directly, as these parameters are used "in the background" of the simulation. That is, they are used in the calculation but no explicit value is given by ProMOST. For example, the workfunctions are difficult to extract, but they are used and they can in principle be computed form the available parameters. It would then be easier to compute the wanted parameter, such as the workfunction, indirectly. This can be done by consulting the BSIM-IMG technical manual and computing the parameter in the same way as performed by ProMOST using the BSIM model. The variables needed for the computation can then either be taken from the input file (which e.g. states the Nwell doping) or they can be requested during the simulation (such as the voltages or currents).

The interface trap capacitance is implemented in BSIM directly. The effect of the interface trap capacitance is modeled for the subthreshold slope degradation and the effect is accounted for the in ideality factor as follows:

$$m_{\mathrm{BSIM}} = 1 + \frac{(C_{\mathrm{dsc}} + C_{\mathrm{it}})\,(C_{\mathrm{si}} + C_{\mathrm{ox2}})}{C_{\mathrm{ox1}}\,(C_{\mathrm{si}} + C_{\mathrm{ox2}}) + C_{\mathrm{si}}C_{\mathrm{ox2}}}, \tag{4.1}$$

with C_{dsc} describing the back-gate bias sensitivity of the coupling capacitance to the channel, depending on length and the applied V_{DS} (and thus the lateral field).

A simplified form of the Poisson equation (with simplified electrostatics) is then solved using Halley's algorithm for $x = \frac{\psi_{\mathrm{s1}}}{m_{\mathrm{BSIM}} u_{\mathrm{T}}}$. From this, the front surface potential is then obtained and from the simplified electrostatics the back surface potential can then be obtained from the front surface potential. Thus, the interface trap capacitance influences the obtained front surface potential. However, the model only incorporates a single interface trap capacitance. We thus have to remark that the BSIM model cannot be used to obtain a separate front and back interface trap density; only an "averaged" C_{it} and thus D_{it} can be obtained. We obtained a value for this, which can be used to validate the measurement results.

4.2 Compact modeling results

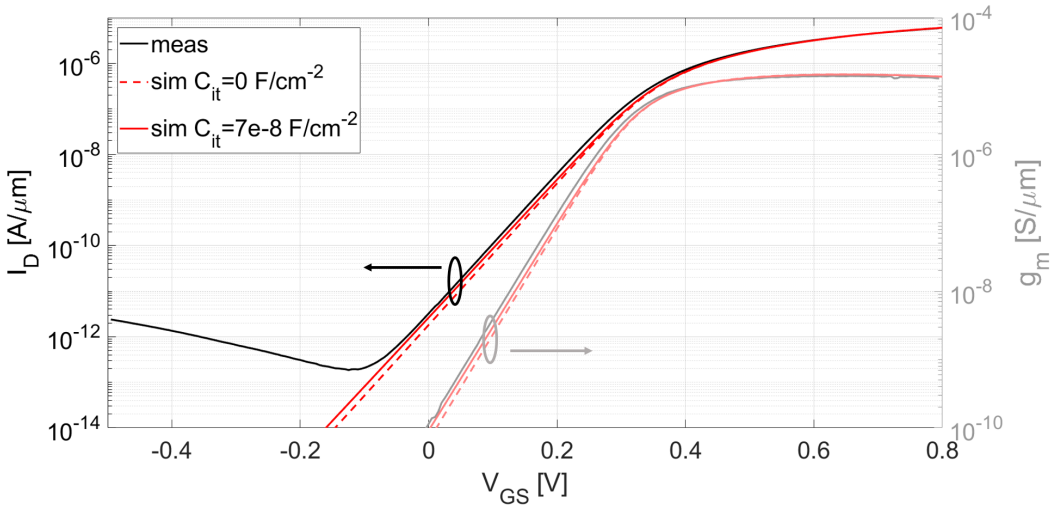
We discuss results for both single sweep and dual sweep ProMOST (or BSIM) simulations, in that order. General transistor characteristics are described for the single sweep measurements, as this is the general use of FDSOI devices. For the dual sweep measurements we mainly focus on the k-sweep method. Measurements are performed with the specified default parameters, unless stated otherwise.

4.2.1 Compact model results for single gate sweep

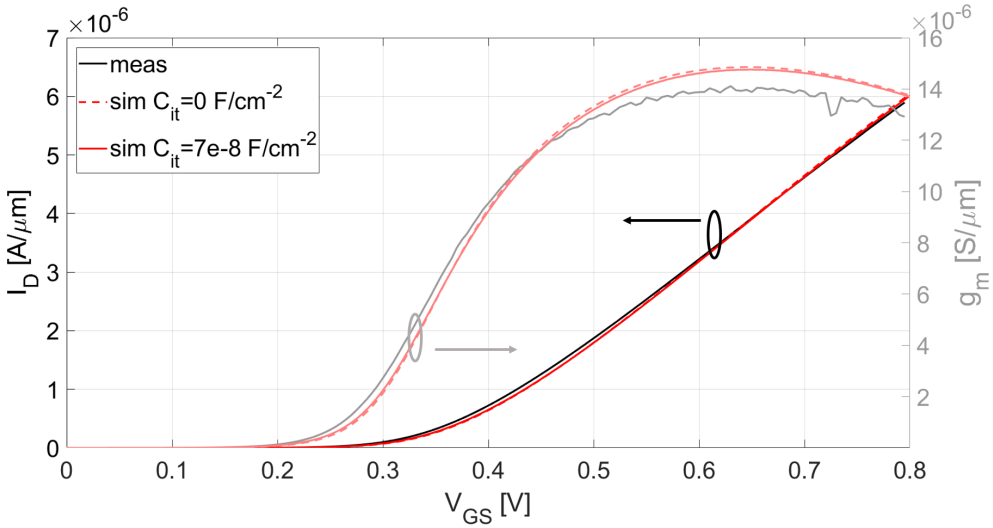
Three different threshold voltage input files were available for the GF 22FDX material; the SLVT, LVT and RVT input files. We compared the drain current as a function of the front gate voltage for all three input files with the measured drain current, and found that the SLVT input file corresponds closest with the measurement data. The material used for the measurements is SLVT material according to the specifications, so this is the expected result.

Interface trap capacitance effect

We continue by showing the single gate sweep characteristics as obtained for different constant (over the gate voltage range) interface trap capacitance values and for different gate lengths. Figure 4.1 shows the drain current per unit width (black/red) and transconductance per unit width (gray/pink) for measurements and for two simulated C_{it} profiles for $L = 1$ μm, on a logarithmic (Figure 4.1(a)) and linear (Figure 4.1(b)) scale. Both on logarithmic and linear scale the simulation curves seem to match reasonably well. Figure 4.1(b) shows clearly that also the measured drain current and transconductance at higher voltages is well-approximated by the model. The effect of interface traps can be extracted from



(a)



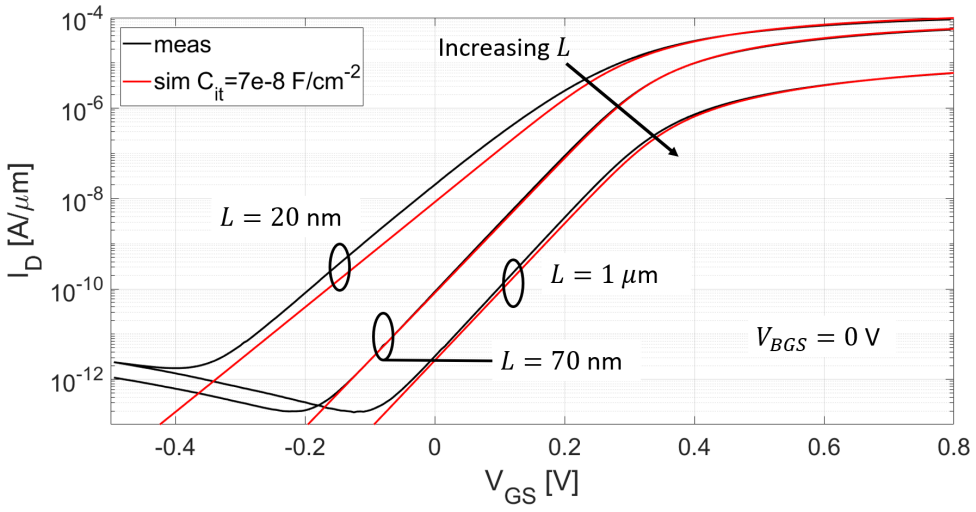
(b)

Figure 4.1: Drain current (measurements in black, simulations in red, left y-axis) and transconductance (measurements in gray, simulations in pink, right y-axis) per unit width as a function of gate-source voltage at $V_{BGS} = 0$ V for a $W/L = 1/1$ μm device on a (a) log-lin scale and (b) lin-lin scale. The figures show the measurement curve and the curves obtained from the compact model with $C_{\text{it}} = 0$ F/cm^2 and $C_{\text{it}} = 7 \cdot 10^{-8}$ F/cm^2.

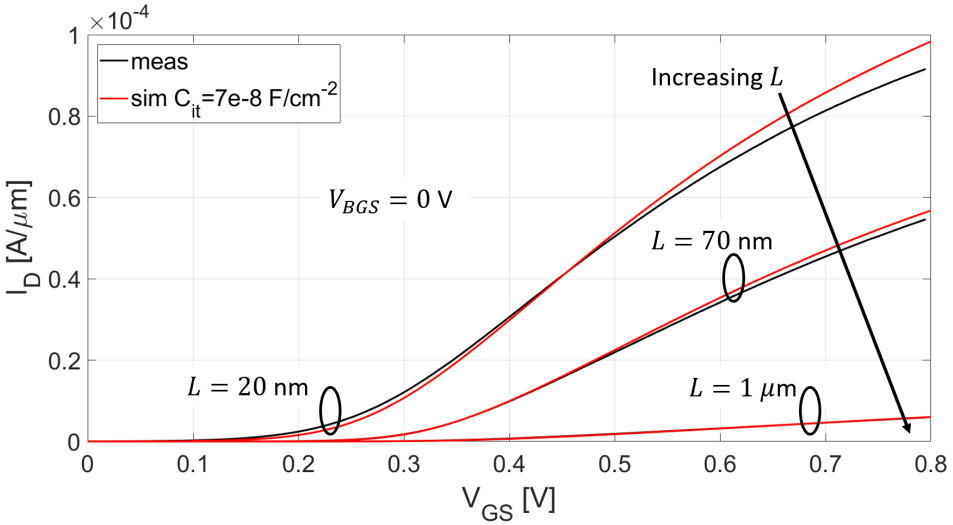
the subthreshold regime, where a clear distinction between the curves is observed. On the linear scale, the difference between the simulation curves is virtually non-existent, especially in comparison to the difference between simulation and measurement curves.

Channel length effect

Figure 4.2 shows the drain current per unit width as a function of the gate-source voltage for measurements and simulations (with default $C_{\text{it}} = 7 \cdot 10^{-8}$ F/cm^2), for devices with three different gate lengths: 20 nm, 70 nm and 1 μm. Figure 4.2(a) shows the drain current on a logarithmic scale. The simulation curves for the larger two gate lengths are in good agreement with the measurement. For the gate length of 20 nm, the difference between simulation and measurement is significant. On the linear scale shown in



(a)



(b)

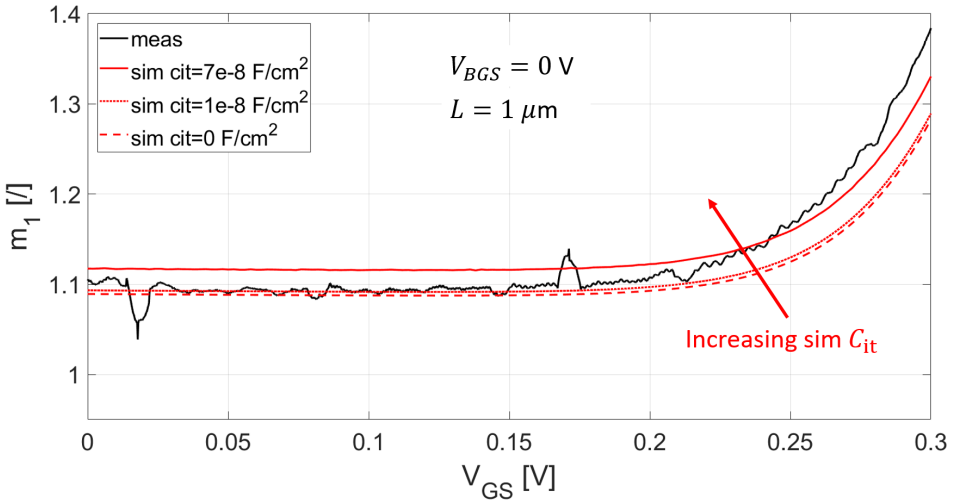
Figure 4.2: Drain current per unit width as a function of gate-source voltage at $V_{BGS} = 0$ V for a device with $L = 1$ μm, 70 nm and 20 nm on a (a) log-lin scale and (b) lin-lin scale. The figures show the measurement curve (black) and the curves obtained from the compact model (red) with $C_{\text{it}} = 7 \cdot 10^{-8}$ F/cm^2.

figure 4.2(b) the same trend is observed. We use the ELR threshold voltage determination method to obtain the threshold voltage for the simulations. For devices with a gate length of 20 nm, 70 nm and 1 μm we obtain $V_{\text{T}} = 0.30$ V, $V_{\text{T}} = 0.35$ V and $V_{\text{T}} = 0.37$ V for the simulations with the default C_{it} as compared to $V_{\text{T}} = 0.24$ V, $V_{\text{T}} = 0.32$ V and $V_{\text{T}} = 0.36$ V for the measurements, respectively. Especially the values for larger gate lengths match well, as is evident from the drain current figures.

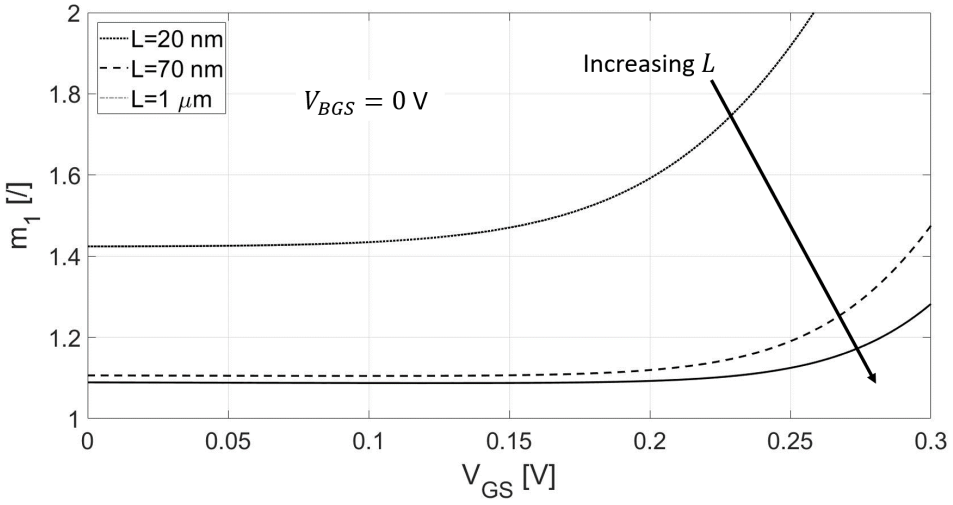
Extracting the transconductance

The drain current and transconductance in the described compact simulation figures were both extracted directly from ProMOST for the simulations. For the measurements, g_{m} was obtained from the regression analysis. The effect of the regression analysis was tested on the ProMOST data, where the exact extracted transconductance could be compared to the transconductance obtained from the regression analysis. It

was found that no significant error is introduced due to regression, even for the linear regime. Although applying the regression analysis with an exponential relation to the linear regime is physically incorrect (and should therefore not be done), the fact that the error introduced by this is only small is an additional argument in favour of the used regression method. Applying regression within a window of u_{T} did not alter the extracted characteristics significantly. Within the subthreshold regime, applying regression with an exponential relation does make physical sense. It should be noted that the actual subthreshold relation between front gate voltage and drain current is not exactly exponential (see equation 2.48), but the error introduced by this within the regression window was found to be insignificant with respect to the measurement limit ($|g_{\mathrm{m,BSIM}} - g_{\mathrm{m,regression}}|/g_{\mathrm{m,BSIM}} < 0.01\%$). Also, from the residuals no unexplained relation is observed for regression within the subthreshold regime.



(a)



(b)

Figure 4.3: The subthreshold swing expressed as ideality factor m_1 is shown as a function of the gate-source voltage at $V_{BGS} = 0$ V. (a) The measurement curve (black) and the curves obtained from the compact model (red) with $C_{\mathrm{it}} = 0$ F/cm^2, $C_{\mathrm{it}} = 1 \cdot 10^{-8}$ F/cm^2 and $C_{\mathrm{it}} = 7 \cdot 10^{-8}$ F/cm^2 For a $W/L = 1/1$ μm device are shown. (b) The compact model curves for a device with $L = 1$ μm, 70 nm and 20 nm are shown.

Subthreshold characteristics

Figure 4.3 shows the obtained subthreshold swing expressed as the ideality factor. For obtaining the ideality factor we use $m_1 = \frac{1}{u_T}\frac{I_D}{g_m}$. In figure 4.3(a) the results are shown for different C_{it} profiles and in figure 4.3(b) the results are shown for different gate lengths. Figure 4.3(a) shows simulation results for the same two interface trap capacitance values as shown in the previous drain current figures ($C_{it} = 0$ F/cm^2 and default). The curve for the higher (default) C_{it} might seem to catch the behaviour of the measured drain current better (see figure 4.1), but when looking at the ideality factor it becomes clear that the behavior is better described with a lower C_{it}. The value of $C_{it} = 1 \cdot 10^{-8}$ F/cm^2 is taken for an additional simulation curve since no clear trend can be observed for only two curves. The curve for this C_{it} describes the subthreshold behaviour well in the range of $0.05 < V_{GS} < 0.15$ V. For larger gate voltages a higher interface trap capacitance value is needed to describe the subthreshold swing. Figure 4.3(b) shows the effect of the gate length on the subthreshold characteristics for $C_{it} = 0$ F/cm^2. The short channel effects are clearly observed, as was also the case for the measurements. Short channel effects in the subthreshold regime are observed as an upward shift of the subthreshold characteristics. Additionally, the effects of the apparent conduction band edge (the curvature around $V_{GS} = 0.3$ V) are observed at a lower gate-source voltage, i.e. at $V_{GS} = 0.3$ V the ideality factor is higher.

4.2.2 Compact model results for dual gate sweep

General k-sweep results

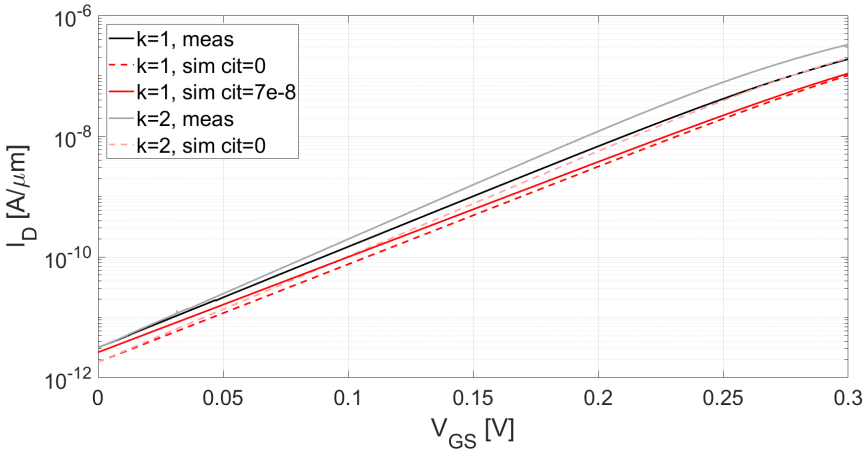
In figure 4.4 the simulations for $k = 1, 1.2, 1.5$ and 2 for $C_{it} = 0$ F/cm^2, $C_{it} = 1 \cdot 10^{-8}$ F/cm^2 and $C_{it} = 7 \cdot 10^{-8}$ F/cm^2 are compared to measurement results.

Figure 4.4(a) shows the drain current per unit width as a function of the gate-source voltage for $k = 1$ (measurement in black, simulations in red) for $C_{it} = 0$ F/cm^2 and $C_{it} = 7 \cdot 10^{-8}$ F/cm^2 and for $k = 2$ (measurement in gray, simulation in pink) for $C_{it} = 0$ F/cm^2. The result for $C_{it} = 1 \cdot 10^{-8}$ F/cm^2 and for the other two k-values are not shown in order to keep the figure neat. The curves for $k = 2$ all have a steeper slope than the curves for $k = 1$, as should be. The curves for $C_{it} = 0$ F/cm^2 start (at $V_{GS} = 0$ V) at a lower drain current value and increase more rapidly, to the same drain current value at $V_{GS} = 0.3$ V as the curves for $C_{it} = 7 \cdot 10^{-8}$ F/cm^2. The measured drain current starts at the same value at $V_{GS} = 0$ V as the curves for $C_{it} = 7 \cdot 10^{-8}$ F/cm^2, but then the increase in current with voltage seems to be similar to that of the curves for $C_{it} = 0$ F/cm^2. This is to be expected, since the same trend was observed for the single gate sweep data.

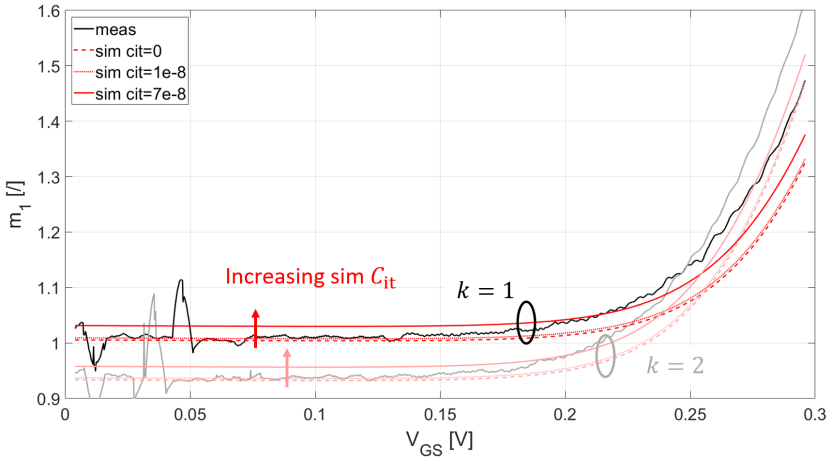
The similarity or difference in slopes can better be interpreted from figure 4.4(b), where the corresponding subthreshold swing (expressed as ideality factor $m_1 = \frac{SS_1}{u_T \ln(10)}$) is shown as a function of the gate-source voltage. Results are shown for $k = 1$ (measurement in black, simulations in red) and for $k = 2$ (measurement in gray, simulations in pink) for $C_{it} = 0$ F/cm^2, $C_{it} = 1 \cdot 10^{-8}$ F/cm^2 and $C_{it} = 7 \cdot 10^{-8}$ F/cm^2. The measurement results are comparable to the simulation curves for low V_{GS}. Near the apparent band edge (at $V_{GS} = 0.3$ V) the measurement curve has a more rapidly increasing value for both k-values. This indicates that we would find an increasingly higher interface trap density near this apparent band edge, in case we would extract the interface trap density from the measurement curve using BSIM simulation data.

This can better be illustrated with figure 4.4(c). The ideality factor m_1 as a function of k is shown at $V_{GS} = 0.1$ V for the measurements (black) and simulations (red) with $C_{it} = 0$ F/cm^2, $C_{it} = 1 \cdot 10^{-8}$ F/cm^2 and $C_{it} = 7 \cdot 10^{-8}$ F/cm^2. The measurement curve (which misses a data point for $k = 0.5$) fits the simulation curve for $C_{it} = 1 \cdot 10^{-8}$ F/cm^2 well. We can thus conclude that the measured device has an interface trap capacitance of $C_{it} \approx 1 \cdot 10^{-8}$ F/cm^2 at $V_{GS} = 0.1$ V, as extracted from the BSIM simulation data.

In this same way, we obtain a similar result in the range of $0.05 < V_{GS} < 0.15$ V. However, when further increasing the gate-source voltage, the extracted interface trap capacitance is found to increase



(a)



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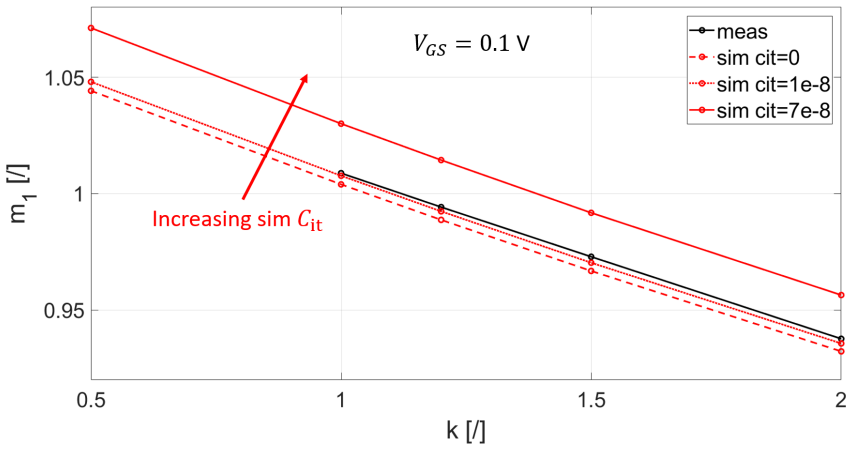


(c)

Figure 4.4: The effect of interface traps for different k is demonstrated. (a) Drain current per unit width as a function of the gate-source voltage for $k = 1$ (measurement in black, simulations in red) for $C_{\text{it}} = 0$ F/cm^2 and $C_{\text{it}} = 7 \cdot 10^{-8}$ F/cm^2 and for $k = 2$ (measurement in gray, simulation in pink) for $C_{\text{it}} = 0$ F/cm^2. (b) The corresponding ideality factor as a function of the gate-source voltage. (c) The corresponding ideality factor as a function of k at $V_{\text{GS}} = 0.1$ V is shown for measurements (black) and simulations (red).

(which we call apparent conduction band edge). For example, at $V_{GS} = 0.2$ V the measurement curve in figure 4.4(b) crosses the simulation curve for $C_{it} = 7 \cdot 10^{-8}$ F/cm^2, such that this value would be extracted. We would thus find that the interface trap density ($D_{it} = C_{it}/q$) changes from approximately $6 \cdot 10^{10}$ to $4 \cdot 10^{11}$ cm^{-2}eV^{-1} (corresponding to the two mentioned interface trap capacitances, respectively) in the range of $0.05 < V_{GS} < 0.2$ V.

As discussed in theory section 2.7, the subthreshold slope should be ideal without interface traps such that $m = 1$ for $k = 1$. This is not the case for the simulations performed here, where we extract $k_0 \approx 1.07$ (or $m \approx 1.004$ at $k = 1$) for $C_{it} = 0$ F/cm^2 from figure 4.4(c). There might be some other source of non-ideal behaviour which is accounted for in the BSIM model, but not in the analytical model described in theory section 2.7. In order to be able to trust and understand the results, we need to investigate this other source of non-ideal behavior.

In order to understand what happens, the reason for the offset in k_0 is investigated. Therefore, we continue by discussing the influence of the drain-source voltage, the oxide thickness and the back gate or n-well doping (which defines the back gate workfunction and depletion).

Drain-source voltage effect

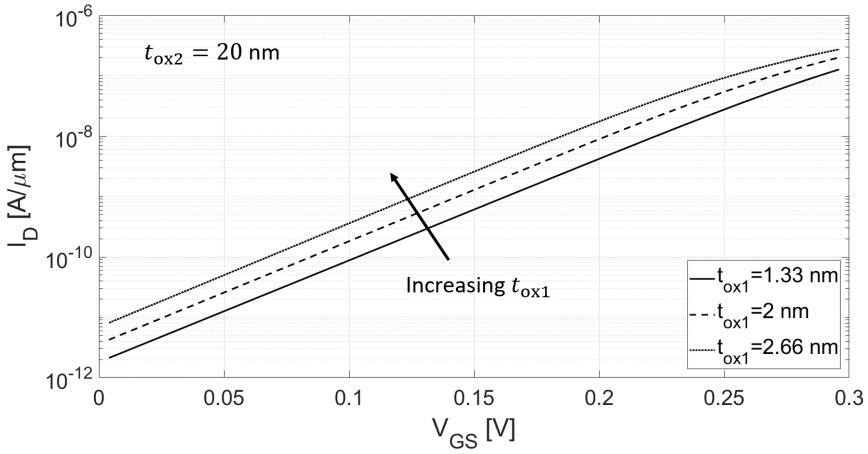
The drain-source voltage has an influence on the drain current, as was described by the drain current analytical models (with $I_D \propto \left(1 - \exp\left(-\frac{V_{DS}}{u_T}\right)\right)$, see equation 2.9). However, to the drain current as a function of the gate-source voltage, this effect only contributes a constant. Thus, no effect of the drain-source voltage on the subthreshold swing is expected from the model. From the BSIM simulation results we conclude that this is indeed true for low gate-source voltages, but for higher gate-source voltages within the subthreshold regime ($0.2 < V_{GS} < 0.3$ V), an increase in subthreshold swing is observed. That is, the value of the subthreshold swing apparent conduction band edge increases for increasing V_{DS}. See appendix D for the results.

Oxide thickness effect

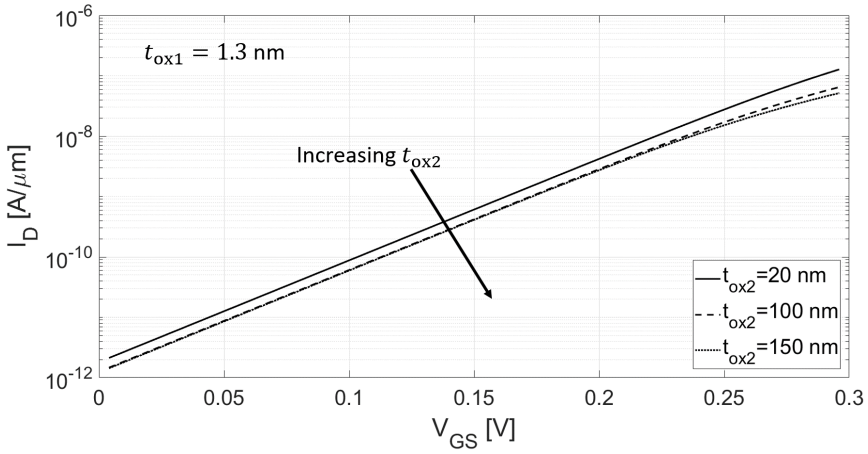
We discuss the BSIM simulation results for the asymmetric case with $t_{ox1}/t_{ox2} = 1.3/20$ nm (corresponding to the measured devices) and compared the BSIM simulation results for asymmetric cases with either thicker front oxides or thicker buried oxides. For the cases with thicker front oxides we use $t_{ox1} = 2$ nm and $t_{ox1} = 2.66$ nm and for the cases with thicker buried oxides we use $t_{ox2} = 100$ nm and $t_{ox2} = 150$ nm. In both cases the other oxide is left at the default thickness ($t_{ox1} = 1.3$ nm and $t_{ox2} = 20$ nm). On the one hand the oxide thickness might have an influence on the subthreshold swing at $k = 1$ such that the observed discrepancy is explained. On the other hand we obtain some qualitative understanding of the effect of an error in the front or buried oxide thickness of the measured device, according to the BSIM model.

The drain current per unit width as a function of the gate-source voltage is shown in figure 4.5. Figure 4.5(a) shows that the current increases for an increasing front oxide thickness, while figure 4.5(b) shows that the current decreases for increasing buried oxide thicknesses. Intuitively, one might expect that increasing the oxide thickness reduces the gate control (i.e. worsens the EI). This is thus not the case for increasing the front oxide thickness.

The reason for this is that the workfunction difference between the front gate and the channel is $\Delta\phi_1 \approx 0$ eV, while the workfunction difference between the back gate and the channel is determined by the n-well doping and is $\Delta\phi_2 \approx -0.45$ eV. This negative workfunction difference results in an increased surface potential at the back interface. Due to the coupling between the two surface potentials, the front surface potential then also increases. A small applied voltage to the front gate then decreases the surface potentials. For thicker front oxides the front gate has reduced control over the channel (hence surface potentials), such that the effect of this back-gate workfunction difference is more significant. Both the



(a)



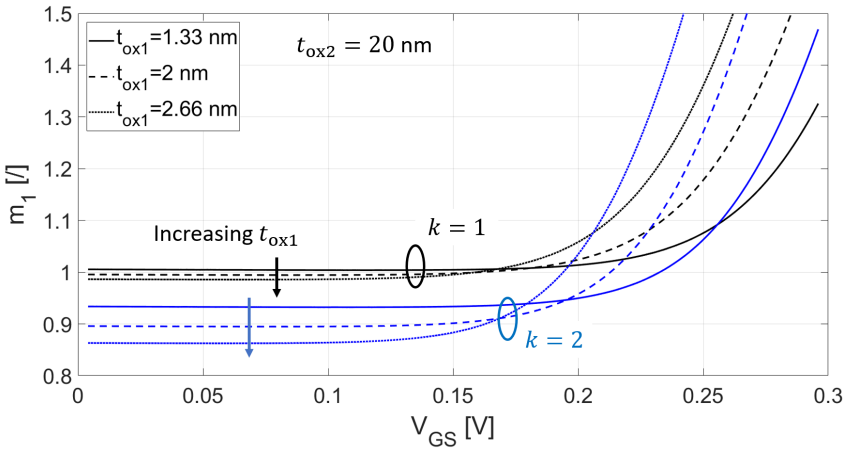
(b)

Figure 4.5: Drain current per unit width as a function of gate-source voltage at $k = 1$ for a $W/L = 1/1$ μm device. We compare the results of BSIM simulations performed on the default device (with $t_{ox1}/t_{ox2} = 1.3/20$ nm) with (a) results for $t_{ox1} = 2$ nm and $t_{ox1} = 2.66$ nm and (b) results for $t_{ox2} = 100$ nm and $t_{ox2} = 150$ nm.

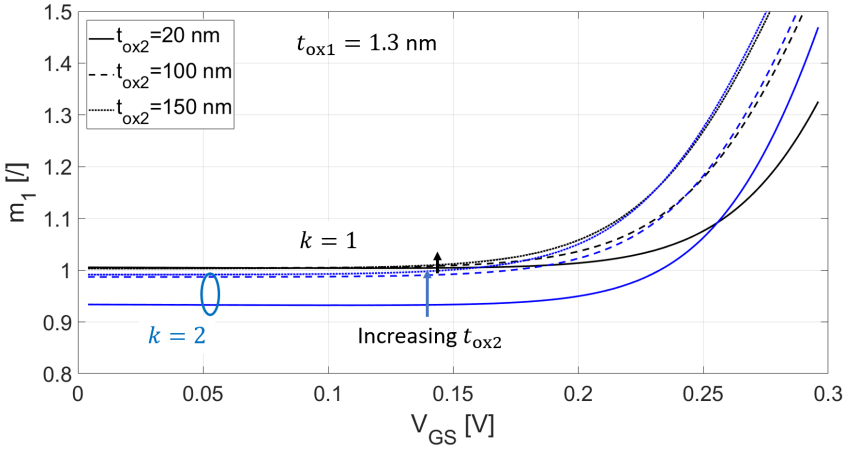
front and back surface potentials thus increase due to the back-gate workfunction difference for thicker front oxides. As the surface potentials are higher, the drain current is higher as well.

For increasing the buried oxide thickness, the opposite holds, the back gate workfunction difference propagates less through the buried oxide and the silicon film and the surface potentials are lower as compared to the case with a thinner BOX layer. However, for the cases described here, the effect of this for the relatively thick buried oxides is insignificant. We show the limit of increasing the buried oxide thickness by the negligible influence of increasing the thickness from 100 to 150 nm.

Figure 4.6 shows that the subthreshold swing decreases for an increasing front oxide thickness and that the subthreshold swing increases for an increasing buried oxide thickness. The reason for this is the relative control of the front gate with respect to the back gate, as was explained for the drain current. For thicker front oxides, the back-gate control increases such that the subthreshold swing as referred to the front gate seems to improve (and thus has a lower value). The results are shown for $k = 1$ (black) and for $k = 2$ (blue), where the difference between the subthreshold swings for a different thickness increases for a higher k. In addition to the relative influence of the back-gate workfunction, the relative influence of the gate voltages also changes for changing the oxide thickness. For thicker front oxides the



(a)



(b)

Figure 4.6: Subthreshold swing expressed as ideality factor m_1 as a function of the gate-source voltage at $k = 1$ (black) and $k = 2$ (blue) for a $W/L = 1/1$ μm device. We compare the results of BSIM simulations performed on the default device (with $t_{ox1}/t_{ox2} = 1.3/20$ nm) with (a) results for $t_{ox1} = 2$ nm and $t_{ox1} = 2.66$ nm and (b) results for $t_{ox2} = 100$ nm and $t_{ox2} = 150$ nm.

relatively higher back-gate voltage for $k = 2$ (then $V_{BGS} = 2V_{GS}$) has an increased influence. Thus, the subthreshold swing for the different front oxide thicknesses deviates more for higher k. For increasing the buried oxide thickness, the subthreshold swing increases, since the relative back-gate control is reduced and the subthreshold swing referred to the front gate thus seems to worsen. Also for the buried oxide thickness the deviation in subthreshold swing increases for higher k. Notice that the oxide thickness also influences the apparent conduction band edge significantly.

An overview of the relation between the subthreshold swing and k is shown for all discussed asymmetric situations in appendix D. Additionally, some simulation results for symmetric cases ($t_{ox} = 1.33$ nm and $t_{ox} = 2.66$ nm) are shown in appendix D.

Effect of doping concentration of n-well

We performed simulations with an n-well with doping concentrations of $N_{well} = 5 \cdot 10^{16}$, $5 \cdot 10^{17}$ (default) and $5 \cdot 10^{18}$ cm^{-3}. The doping concentration influences the back-gate workfunction and the back-gate depletion and might therefore have an effect on both the drain current and subthreshold swing.

For the three different doping concentrations, we expect a theoretical workfunction difference between the back-gate and silicon channel according to $\Delta\phi_2 \propto \ln\left(\frac{N_{\text{well}}}{n_i}\right)$ (assuming an undoped channel, see equation 2.45) of $\Delta\phi_2 = -0.39$ eV, $\Delta\phi_2 = -0.45$ eV and $\Delta\phi_2 = -0.51$ eV, respectively. The back-gate depletion effect is more difficult to quantify as it depends on the voltage across the depletion region, which is not known. We expect the depletion capacitance to depend on the doping concentration according to $C_{\text{dep}} \propto \sqrt{N_{\text{well}}}$ (see equation 2.62).

In the BSIM model the depletion capacitance can be turned on and off. We investigated the difference between both and found only an insignificant influence of the back-gate depletion effect. The model is calibrated against the GF material with the depletion capacitance being turned off, because the model is known to not accurately describe the back-gate depletion and inversion behavior (from e-mail correspondence with GF [47]). We can therefore draw no conclusion about the back-gate depletion effect from the BSIM simulation results.

We investigated the influence of the workfunction difference resulting from the different doping concentrations. The drain current (as a function of the gate-source voltage) increases for higher doping concentrations. This corresponds to the increase in the back (and front) surface potential associated with the increase in (negative) workfunction difference. The only significant influence of the back gate doping on the subthreshold swing is in the apparent conduction band edge shift to lower voltages for higher back gate doping densities. That is, the apparent conduction band edge sets in at lower voltages for a higher n-well doping concentration.

The results for the different n-well doping concentrations are shown in appendix D.

4.2.3 Conclusion BSIM simulations

The BSIM simulation results as obtained using ProMOST have been compared to measurement results. For single gate sweep simulations, we show that the simulations fit the measured drain current and transconductance for 70 nm and 1 μm devices well. The effect of interface traps in the BSIM model are demonstrated and the measured subthreshold swing is compared to that of simulations with several different interface trap capacitance inputs.

For the dual gate sweep, the BSIM simulation results are compared to measurement results for several k-values. We show that the obtained simulation results for $C_{\text{it}} = 1 \cdot 10^{-8}$ F/cm^2 fit the measurement subthreshold swing curve best in the range of $0.05 < V_{\text{GS}} < 0.15$ V. This is the same result as obtained from the single gate sweep subthreshold swing simulation as compared to the measurement. For higher gate voltages a higher interface trap capacitance value is obtained, corresponding to the apparent conduction band edge. The obtained interface trap capacitance corresponds well to that obtained using the simplified k-sweep method (see section 3.2, "Single interface trap extraction"). As explained in section 4.1, only an averaged C_{it} or D_{it} is used in the BSIM model. Therefore, extracting C_{it1} and C_{it2} separately is not possible with the BSIM model in ProMOST and for that we need another tool.

We investigated the influence of the drain-source voltage, the oxide thickness and the n-well doping concentration. The drain-source voltage only has a small influence on the absolute current and the apparent conduction band edge of the subthreshold swing curve. The front and buried oxide thickness have an influence on the drain current and subthreshold swing as explained by the back-gate workfunction difference. Increasing the front oxide increases the current and decreases the subthreshold swing, while the opposite is observed for increasing the buried oxide thickness. Back-gate depletion is not included in the BSIM model for the GF material. The workfunction difference resulting from the n-well doping concentration influences absolute current and the apparent conduction band edge, i.e. increasing the doping increases the current and apparent conduction band edge. We could not draw a clear conclusion about the cause of the non-ideal value of the ideality factor at $k = 1$.

We continue our study with a TCAD tool such as Silvaco Atlas with as goal to extract C_{it1} and C_{it2} separately. We first validate the extended analytical model and then use it to extract the interface trap density from both interfaces simultaneously.

Chapter 5

TCAD Simulations

5.1 TCAD Simulation method

For the TCAD simulations described in this section the input decks and the parameters used in these decks are first discussed. Then, a comparison between TCAD results and the analytical model is made and the results are described. Finally, the TCAD simulation results are used as "measurements" and we extract the interface trap density from the TCAD simulations using the validated analytical model. For our TCAD simulations we use Silvaco Atlas [48] and we run the simulations within the Deckbuild environment [49].

5.1.1 Input decks

We start by discussing the two used input decks, the "DGFET" deck and the "SOIFET" deck, for which the schematic cross-section of the devices are shown in figure 5.1. The only real difference between both decks is the n-well, which is incorporated in the SOIFET deck and not in the DGFET deck. We use the DGFET deck for initial simulations without having to consider the effects of a non-midgap back-gate and without having to consider back-gate depletion effects. To start even simpler, we use a symmetric DG device in our DGFET deck, i.e. $t_{ox1} = t_{ox2} = t_{ox}$, as default. This default DGFET deck is called "symmetric DGFET".

We then perform simulations iteratively with adding detail to the DGFET deck such that the obtained

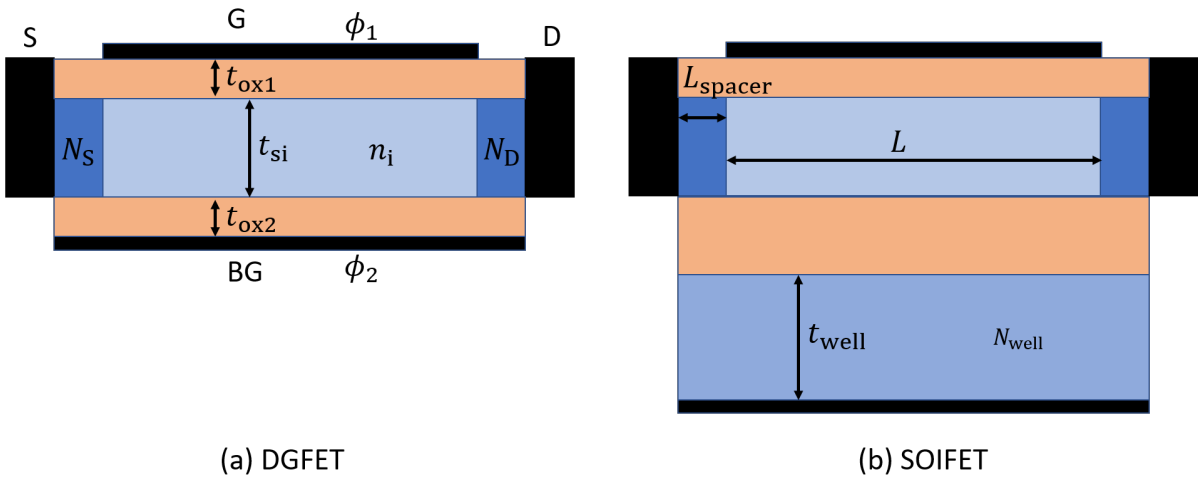


Figure 5.1: Schematic cross-sections used in the TCAD input decks.

Parameter	Description	Default value
General parameters		
L	Gate length or channel length	1 μm
L_{spacer}	Length of spacer and S/D extension region	0.1 μm
t_{si}	Channel thickness	6 nm
ϕ_1	Front gate workfunction	4.73 eV (midgap, i.e. $\Delta\phi_1 \approx 0$ eV)
$N_{\text{S/D}}$	S/D extension region doping density	$1 \cdot 10^{19}$ cm^{-3}
n_{i}	Intrinsic silicon carried density [*]	$1 \cdot 10^{10}$ cm^{-3}
DGFET parameters		
t_{ox1}	Front oxide thickness	2 nm
t_{ox2}	Buried oxide thickness	2 nm
ϕ_2	Back gate workfunction	4.73 eV (midgap, i.e. $\Delta\phi_2 \approx 0$ eV)
SOIFET parameters		
t_{ox1}	Front oxide thickness	1.3 nm
t_{ox2}	Buried oxide thickness	20 nm
t_{well}	n-well thickness	0.25 μm
N_{well}	S/D extension region doping density	$5 \cdot 10^{17}$ cm^{-3} ($\Delta\phi_2 \approx -0.45$ eV [+])

Table 5.1: Parameters used for TCAD simulations. We spit the table in three sections. In the general parameters section the parameters equal for all simulations are described, in the DGFET parameters section we describe the specific default values for DGFET simulations and in the SOIFET parameters section we describe the specific default values for FDSOI simulations. [*] the intrinsic silicon carrier density is computed from $n_{\text{i}} = \sqrt{N_{\text{C}} N_{\text{V}}} \exp\left(-\frac{E_{\text{G}}}{2qu_{\text{T}}}\right)$ with $N_{\text{C}} = N_{\text{V}} = 2.9 \cdot 10^{19}$ cm^{-3}. [+] For calculating the workfunction difference between the n-well (hence the back-gate) and the undoped silicon channel we use equation 2.45 (with $\Delta\phi_2 \propto \exp(N_{\text{well}})$).

behaviour becomes more like the SOIFET deck. The first step towards the SOIFET deck is to use oxides with an unequal thickness. This deck is called "asymmetric DGFET". After that, we can implement a workfunction difference and finally the SOIFET deck can be used (which then also contains back-gate depletion effects). All default values used in the decks are given in table 5.1. The general parameters are first given, followed by the parameters with specific values for either the DGFET or SOIFET decks. Note that the default DGFET deck is the symmetric DGFET.

The grid or mesh of the input decks is defined similarly for all three input decks. Mesh lines are defined at all interfaces, including material interfaces, contact interfaces and doping interfaces. The mesh gradually changes over the device, with the horizontal grid spacing (in x-direction, i.e. from source to drain) between 5 and 50 nm and the vertical grid spacing (in y-direction, i.e. from gate to back-gate) between 0.1 and 50 nm. Especially the mesh at the FOX/channel and BOX/channel interface is fine, with a (vertical) spacing of 0.1 nm. In comparison, the (vertical) spacing in the n-well of 50 nm is rather course.

5.1.2 Modeling framework

The general framework for TCAD simulations on the described input decks with Atlas is provided by three equations. The first equation is the Poisson equation, which relates the surface potential and the charge density. The second and third equation are the electron and hole carrier continuity equations and drift-diffusion equations. These equations describe the relation between the electron and hole (charge) densities, electric fields, and the electron and hole current densities, respectively. Furthermore, certain physical models should be specified.

For the latter, several physical models are defined in TCAD, which can be grouped in five classes:

mobility, recombination, carrier statistics, impact ionization, and tunneling. For the thin fully-depleted films we use, with $n \gg p$, the effect of recombination is insignificant (as validated with a recombination model including a concentration-dependent lifetime, the *CONSRH* model).
Impact ionization only plays a role at high reverse biases and can thus be excluded.

We do not use tunneling models for two reasons. From the measurements it was concluded that the back-gate leakage current is insignificantly small in the entire range of $-0.5 < V_{\mathrm{GS}} < 0.8$ V. Thus, for the back-gate we do not need to include a tunneling current. For the measurements, the front-gate leakage current was much smaller than the drain current, with the minimal difference $I_{\mathrm{D}} - I_{\mathrm{G}}$ being approximately 2 decades at $V_{\mathrm{GS}} = 0$ V.

It might be more accurate to incorporate the front gate leakage current with some tunneling effect, as this order of magnitude difference can influence the drain current in such a way that the analytical model is not correct anymore. However, we do not know the composition of front oxide materials and we do not know the actual front oxide thickness, only the effective oxide thickness (EOT) of an equivalent silicon dioxide layer. In conclusion, although this might result in some small error, we did not include tunneling models in our simulations.

We incorporated two carrier statistics models in order to better model the behaviour of the n-well and the heavily doped source and drain extension regions. We included the *Fermi*(-Dirac statistics) model to account for a reduced carrier concentration and we included the *BGN* (bandgap narrowing) model to incorporate a narrower bandgap. Furthermore, to obtain accurate results for FET simulations, the mobility degradation in inversion layers had to be accounted for.

The degradation due to (transverse) surface electric fields as a function of both doping density and temperature is incorporated in stand-alone models which incorporate all the effects required for simulating the carrier mobility. We used the Lombardi *CVT* model, as it is one of the most complete models for silicon FETs. In order to test for the effect of a field-dependent mobility, simulations with a constant mobility of $\mu_n = 600$ cm^{2}V^{-1}s^{-1} were also performed.

In addition, the change in device behaviour for spatially or electrically confined devices due to quantum-mechanics (QM) can be implemented using several independent models. The self-consistent coupled Schrödinger-Poisson model can be used to self-consistently solve Poisson's equation for the potential and Schrödinger's equation for energies and carrier wavefunctions. However, this model should not be used to look at carrier transport problems.

An easier approach at implementing QM effects is using the Hansch QM model or the Van Dort model. In these models the shift of the charge density peak away from the interfaces is considered. The Hansch QM model is a modification of the density of states as a function of depth below the silicon/oxide interface. The Van Dort model incorporates the QM effects by broadening the bandgap near the surface. We tested both the Hansch QM and Van Dort model for $k = 1$, but found no significant change in behaviour (in the subthreshold regime). Therefore, we did not include any QM effects in our simulations.

5.1.3 Bias conditions

We want to extract the drain current as a function of the gate-source voltage for these devices, just as we did for the measurements and BSIM simulations. We thus used a temperature of $T = 298.15$ K (25 °C) and we connected the source to ground. We used $V_{\mathrm{DS}} = 25$ mV unless stated otherwise, and we simulated for $0 < V_{\mathrm{GS}} < 0.3$ V with the back-gate voltage range specified by k.

The TCAD simulation results showed to exhibit only a small amount of (numerical) noise. This is in contrast to the measurements, where we had to use a regression analysis method to extract an acceptable transonductance and subthreshold swing. For the TCAD simulations we therefore used $\Delta V_{\mathrm{GS}} = 2$ mV, instead of the used $\Delta V_{\mathrm{GS}} = 0.2$ mV for the measurements.

For the SOIFET simulations we used $V_{\mathrm{BGS}} = k \cdot V_{\mathrm{GS}} + V_{\mathrm{off}}$, with $V_{\mathrm{off}} = -0.45$ V $\approx \Delta\phi_2$ for the default N_{well}. Thus, V_{off} was used to create a flat-band situation, as described in section 2.10. For the DGFET simulations this simplified to $V_{\mathrm{BGS}} = k \cdot V_{\mathrm{GS}}$, since the back-gate workfunction difference is

$\Delta\phi_2 = \Delta\phi_1 \approx 0$ eV so that $V_{\text{off}} = 0$ V. Here we thus state that the front and back gate workfunction are the same and the subthreshold swing is unaffected by both. Additionally, both workfunction differences are approximately 0 eV such that the current is unaffected too.

5.1.4 Trap implementation

Traps are implemented in Silvaco Atlas by adjusting the space charge density term of the Poisson equation. Normally, this term simply contains all free and doping charge but now a trap charge term should be added, i.e. $q(n + p + N_D + N_A) + Q_{\text{T}}$. This total trapped charge only consists of interface traps in our case and is defined by [48]:

$$Q_{\text{T}} = q\left(N^+_{\text{tD}} + N^-_{\text{tA}}\right), \tag{5.1}$$

where N^+_{tD} and N^-_{tA} are the total densities of ionized donor-like and acceptor-like traps, respectively, with $N^-_{\text{tA}} = 0$ cm^{-2} in our case. The total ionized donor-like density of traps for multiple traps at multiple energy levels is given by [48]:

$$N^+_{\text{tD}} = \sum_{i=1}^{n} N^+_{\text{tD}i}, \tag{5.2}$$

with n the total number of donor-like traps and $N^+_{\text{tD}i} = F_{\text{tD}} \cdot DENSITY$, where the probability of ionization F_{tD} assumes that the capture cross-section σ is a constant for all energies. This probability of ionization is a function of the capture cross-sections and the electron and hole emission rates: $F_{\text{tD}} = f(\sigma, e_{\text{nD}})$. For the electron and hole transmission rates we have [48]

$$e_{\text{nD}} \propto n_{\text{i}} \exp\left(E_{\text{t}} - E_{\text{Fi}}\right) \tag{5.3a}$$

and

$$e_{\text{pD}} \propto n_{\text{i}} \exp\left(E_{\text{Fi}} - E_{\text{t}}\right). \tag{5.3b}$$

with E_{t} the trap energy level and E_{Fi} the intrinsic Fermi level.

We implemented the interface traps using the *INTTRAP* statement. With this statement, interface traps can be implemented at the silicon/oxide interface within a certain defined box. These traps have a specific trap density *DENSITY*, cross-section σ and energy level E_{t}.

In order to obtain a uniformly constant continuous trap profile of e.g. $D_{\text{it}i} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1}, we have to define the interface trap density at each energy in a box around the front interface (for D_{it1}), in a box around the back interface (for D_{it2}) and in a box around both interfaces for obtaining two to-be-added contributions (for D_{it1} and D_{it2}, addition is done by TCAD with equation 5.2). For defining a trap density at each energy level, a Python script (provided by Boni Boksteen, author of [20]) was used. We defined the desirable number of discrete trap energy levels within the range of $E_{\text{G}}/2$ to E_{C} and used a quadrature integration scheme to integrate the desired interface trap density profile between two points:

$$DENSITY(i) = \int_{E_{\text{t}}(i-1)}^{E_{\text{t}}(i)} D_{\text{it}} \cdot dE, \tag{5.4}$$

with $i = 1, 2, ...n$ an integer number defining which of the discrete energy levels we want to obtain the *DENSITY* for, where n is the total number of discrete energy levels. An example of an interface trap density profile as a function of the gate-source voltage that could be used is given in figure 5.2, as well as the integral of the profile. The shown integral was then used as input for TCAD.

A statement for the *INTTRAPS* with the *DENSITY* was printed together with the corresponding trap energy level E_{t} and the other (default Atlas) parameters for each i, such that n statements are obtained. The total set of statements was then implemented in the TCAD input file.

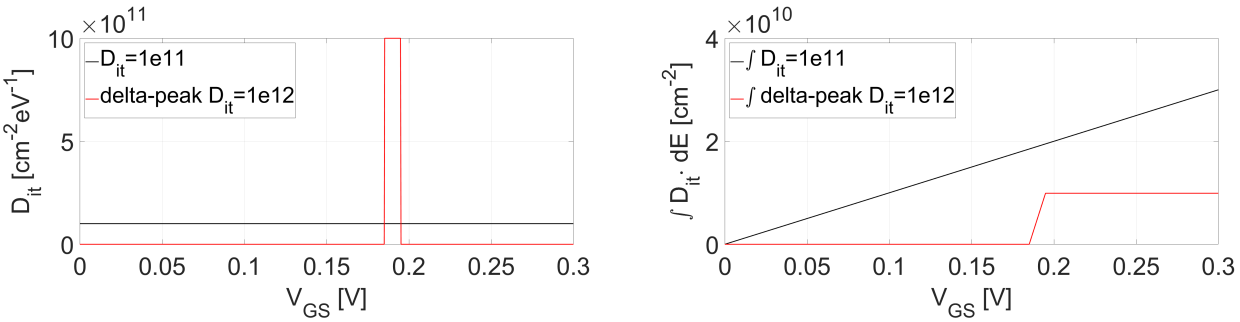


Figure 5.2: Exemplary input D_{it} profiles and their integrals. We show (a) the desired interface trap density and (b) the integral of the respective interface trap densities, to be used as input for TCAD.

5.1.5 Fitting procedure

Here we describe how the TCAD data was fitted with the analytical model. We mainly used this fitting procedure on TCAD data, but the goal would be to fit the measurement data in this way. The data to-be-fitted was used as input data, from which we used the gate-source voltage, the drain current and the k-values. From this input data we extracted the subthreshold swing. For the TCAD data we could do this using the central finite difference theorem. For measurement data we would use the regression analysis (as described in section 3.1 and verified in section 4.2). The SS is then obtained as a function of V_{GS} and k. For every V_{GS}-value the SS as a function of k is fitted using the MATLAB *fit()* algorithm. This algorithm uses the non-linear least-squares method to fit a given input function (the analytical model in our case) for a given number of fitting parameters. We thus let this algorithm fit the TCAD SS as a function of k with the analytical model, where D_{it1} and D_{it2} are the fitting parameters. The procedure was repeated for all V_{GS} such that the total system of SS as a function of V_{GS} and k was fitted. At every V_{GS}-value the optimal-fit parameters (D_{it1} and D_{it2}) were extracted.

5.2 TCAD simulation results

The results obtained from the TCAD simulations are described in this section. We started by testing the symmetric DGFET deck at $k = 1$. In that case, we expect $SS = SS_{\text{ideal}} \approx 59$ mV/dec. As it is easier to interpret the results from the ideality factor m, for $k = 1$, we used $m = \frac{SS}{u_{\text{T}} \ln(10)}$ and simply looked at the offset with respect to $m = 1$.

For the symmetric DGFET deck at $k = 1$ we found $m \approx 1.0006$. This might seem to be close enough to the ideal value of $m = 1$, but this was not the case. Every order of magnitude error in the ideal value of m, i.e. the value of m at $k = 1$, propagates in the extracted interface trap capacitance as compared to the oxide capacitance directly (see equation 2.4). If this error cannot be explained by any physical phenomenon, we might be looking at some numerical limit or noise, and that would be problematic for the further use of TCAD. A similar problem (with an even higher m at $k = 1$) was encountered for the BSIM simulations (section 4.2.2).

We tested the effect of the mesh, the oxide thickness and the drain-source voltage on the offset in the ideality factor. Using a courser or finer mesh and using thicker or thinner oxides has a similar influence on the ideality factor. In both cases, we found that m varies between 1.0004 and 1.0007. This is unexpected, since both factors should have no influence on the ideality factor according to our model. The drain-source voltage has no influence on the ideality factor, except for the apparent conduction band edge, as was described for the BSIM simulations too (see 4.2, paragraph "Drain-source voltage effect").

We found that the mesh/oxide influence is actually a short-channel effect. The width of the depletion

region at the N+/channel interface changes with the oxide thickness or mesh spacing at this interface. The depletion width change relative to the channel length is comparable in one order of magnitude to the m-effect. We thus effectively see a shorter channel for e.g. thicker oxides. We validated this conclusion with a simulation for $L = 5$ μm, where indeed the SS dropped to a value closer to 1.0004. This appears to be about the lower limit, where the remaining "offset" in m is attributed to the neglected inversion charges (in the channel) for deriving analytical relations. This is discussed later in this section.

For the remainder of the results we studied the subthreshold swing directly. It should be noted that expressing the subthreshold swing by the ideality factor for any case other than a symmetric device with symmetric control is actually misleading, as this might give the impression that we expect $m = 1$ to be ideal for those cases, which is not true. More importantly, we extensively discuss the electrostatic behaviour in this section, and the use of m-parameters for both the electrostatics and the total subthreshold swing would be confusing. We therefore refrain from further use of the ideality factor to describe the entire SS for asymmetric devices and for asymmetric control ($k \neq 1$) and then use the m-parameters to describe the electrostatics only.

After analyzing the symmetric DGFET for $k = 1$, we continued with testing and verifying the analytical model for cases without traps.

5.2.1 Comparison of the analytical model and TCAD results

We discuss the validation of the analytical model using TCAD simulations. For this, we needed to examine all contributions to the subthreshold swing separately.

In more detail, the subtreshold swing as a function of the gate-source voltage should be obtained from TCAD directly (using $SS = \frac{dV_{GS}}{d\log_{10}(I_D)}$) and indirectly (using $SS = m_{11} \cdot \delta\psi_{s1} \cdot \ln(10) + m_{12} \cdot \delta\psi_{s2} \cdot \ln(10)$) as described in equation 2.47. We studied the subthreshold swing using both methods for two reasons. First of all, the surface potential as used for the indirectly obtained subthreshold swing has to be obtained from TCAD simulations. For this, we "probe" the potential at the interfaces ($y_1 = t_{ox1}$ and $y_2 = t_{ox1} + t_{si}$) at $x = L/2$. By comparing both subthreshold swing curves we could thus validate this probing method. For the directly and indirectly obtained SS similar results were obtained. Secondly, after validating whether or not the direct and indirect extraction result in the same SS, we could use the separate terms

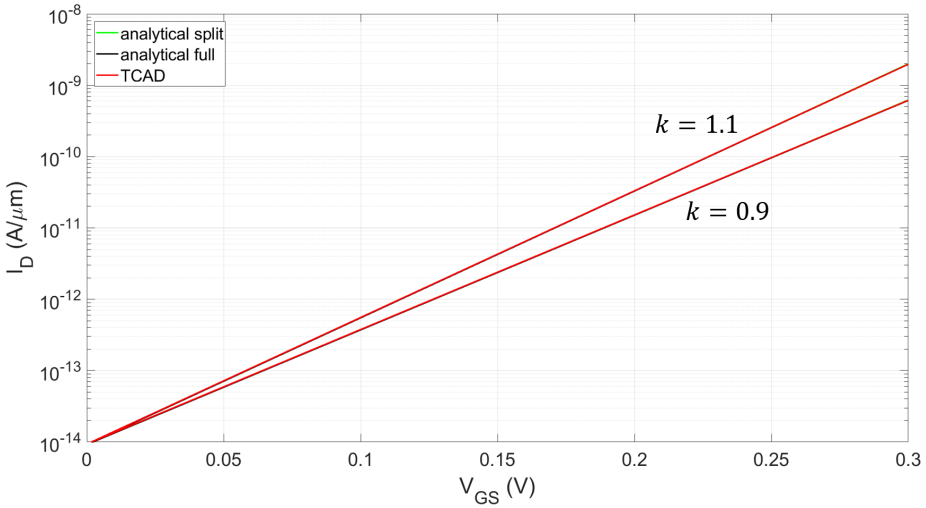


Figure 5.3: Drain current per unit gate width as a function of the gate-source voltage for $k = 0.9$ and $k = 1.1$ on a log-lin scale. The TCAD drain current (symmetric DGFET), the split model drain current and the full model drain current nicely overlap, such that it appears that only two lines (for the two k) are shown.

to determine the contribution of the electrostatics part (the m-parameters) and transverse field part (the $\delta\psi_{sx}$-parameters) separately. Additionally, we compared the "split" current model (equation 2.55) to the "full" current model (equation 2.48). For more details on the mentioned equations in this chapter, see section 2.10.

Symmetric DGFET

We manually fitted the "full" and "split" analytical drain current model with TCAD data. For this, we simply used the same parameters as used for the TCAD deck. For example, we know that $n_{\mathrm{i}} = 1 \cdot 10^{10}$ cm^{-3}, $V_{\mathrm{DS}} = 25$ mV, $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 2$ nm and $\mu_n = 600$ cm^{2}V^{-1}s^{-1}. We calculated the drain current for a set of k-values using TCAD and the analytical model(s). We used nine k-values with a difference between the values of 0.025: $k = 0.9, 0.925, 0.95, 0.975, 1, 1.025, 1.05, 1.075$ and 1.1.

The obtained drain current as a function of the gate source voltage is shown in figure 5.3. We only show the drain current for the highest and lowest k-values for figure-readability. For both k the split and full model fit the TCAD current nicely.

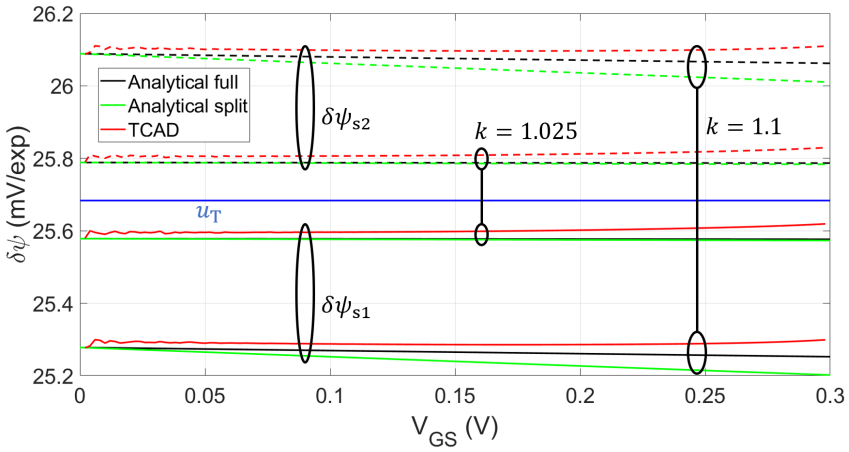
Transverse field contribution We then compare both analytical drain current models. We start by considering the transverse field contribution in order to determine the errors introduced by both models. The transverse field contribution to the SS ($\delta\psi_{sx}$ with $x = 1, 2$) was extracted from TCAD and calculated from the "split" and "full" analytical drain current models.

We show the obtained $\delta\psi_{sx}$ in figure 5.4 together with u_{T}, which is the value $\delta\psi_{sx}$ converges to for $k \to 1$ according to the analytical models. Figure 5.4(a) shows the transverse field contribution as a function of the gate-source voltage for $k = 1.025$ and $k = 1.1$. Both analytical models describe the behaviour of the transverse field well for k close to $k = 1$, i.e. symmetric control of the channel by the gates. However, for k deviating increasingly more from the symmetric control situation, the results obtained by the analytical models tend to deviate from the TCAD results. We can clearly see that the "split" current model describes $\delta\psi_{sx}$ rather poorly at $k = 1.1$, as compared to the "full" current model. We therefore use the "full" current model in the remainder of this work, and we will refer to this model as "the analytical model" or simply "analytical".

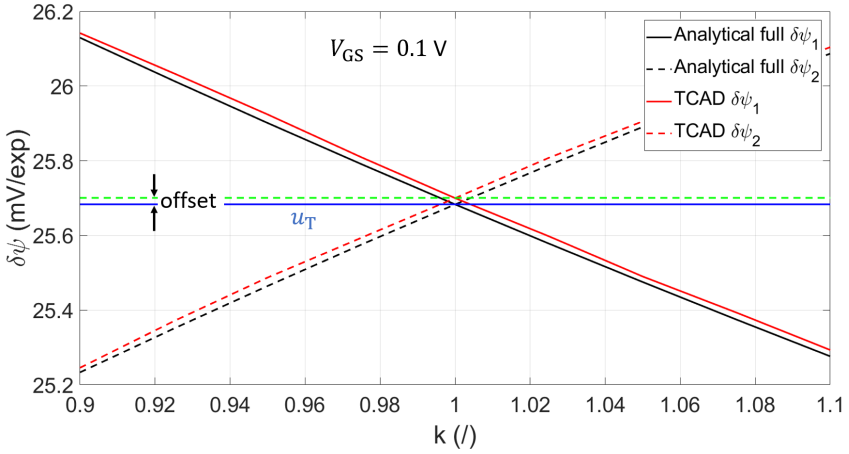
Next to the model deviation for higher k, we note that the curves for $\delta\psi_{s1}$ and $\delta\psi_{s2}$ are symmetric around u_{T} for the analytical model with respect to each other. This is to be expected from the equations, but interestingly the TCAD curves seem to be symmetric around a value slightly higher than u_{T}.

This offset of the symmetry line is more clearly shown in figure 5.4(b). The transverse field contribution is shown as a function of k at $V_{\mathrm{GS}} = 0.1$ V. The point where $\delta\psi_{s1}$ and $\delta\psi_{s2}$ cross is at $k = 1$, and the corresponding value of $\delta\psi_{sx}$ can better be approximated by u_{T} with $T = 25.2$ ^{o}C instead of $T = 25$ ^{o}C (green dashed line). The described offset might be the result of some minor workfunction difference of the gates with respect to the channel or of some short-channel effect. We will discuss this in more detail when describing the behaviour for the asymmetric case.

Electrostatics contribution We discussed the transverse field contribution and found that the analytical model fits the TCAD results reasonably well, especially for k-values close to $k = 1$ i.e. symmetric control. We continue with the electrostatics part, as shown in figure 5.5(a). The front surface potential to front gate voltage ratio m_{11} is shown as a function of the gate-source voltage for five k-values. Additionally, we show $m = 1$ as a reference. The analytical electrostatics model fits the TCAD results well and we can clearly see that m_{11} increases for increasing k. Only for approximately $V_{\mathrm{GS}} > 0.28$ V we can see some deviation between the analytical model and the TCAD data which represents the earlier discussed apparent conduction band edge. We obtained a similarly nice fit of the analytical electrostatics model as compared to the TCAD data for m_{12}. We also found the same band edge discrepancy in the electrostatics model.



(a)



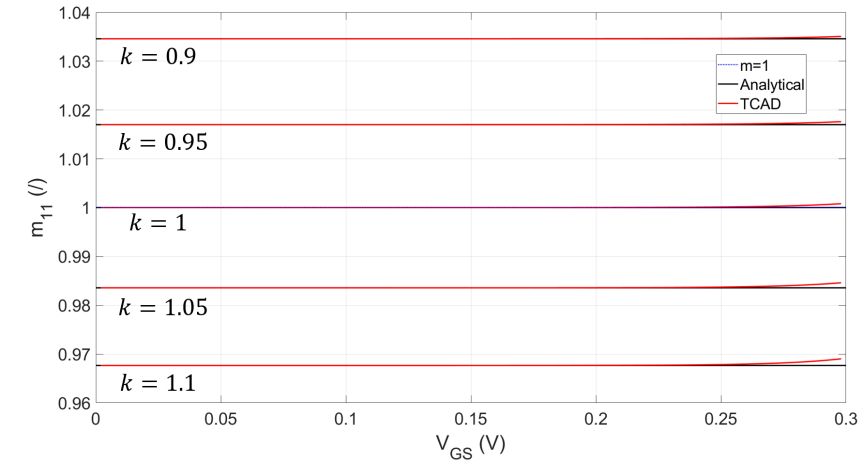
(b)

Figure 5.4: Transverse field contribution in mV per factor of e in drain current (mV/exp) (a) as a function of the gate-source voltage and (b) as a function of k. In (a) the results are shown for $\delta\psi_{s1}$ and $\delta\psi_{s2}$, for $k = 1.025$ and for $k = 1.1$, as indicated by the black circles. The results are shown for the "full" and the "split" analytical models, and for the TCAD simulations (symmetric DGFET). In (b) the results are shown at $V_{GS} = 0.1$ V for the "full" analytical model and for the TCAD simulations. The symmetry point for the analytical model is u_T (solid blue line), and the offset between u_T and the symmetry point of the TCAD simulations (dashed green line) is indicated.

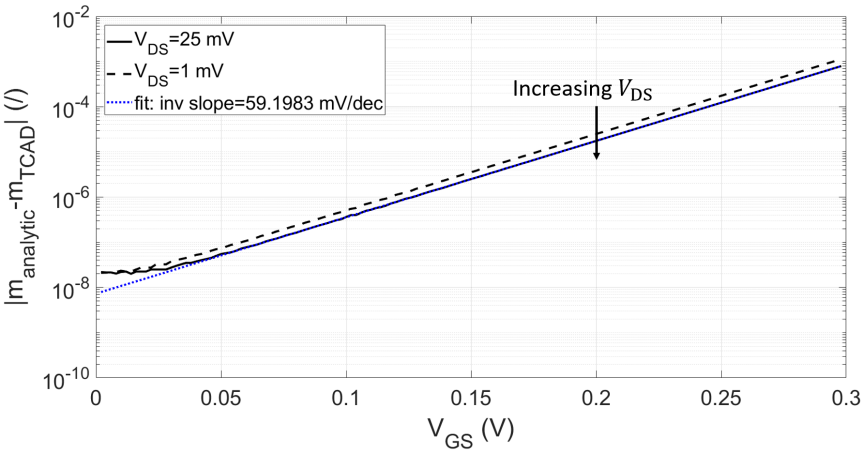
We continue by describing the phenomenon we called "apparent conduction band edge" since the analytical model does not contain this effect. We compared the analytical electrostatics with the TCAD electrostatics for $k = 1$. For doing this, we subtracted the TCAD m_{11} from the analytical one and took the absolute value, as shown in figure 5.5(b). The figure shows the mentioned difference, or analytical model error, as a function of the gate-source voltage for $V_{DS} = 25$ mV and $V_{DS} = 1$ mV. The result for $V_{DS} = 25$ mV is fitted and the inverse of the slope of the fit (dotted blue line) is found to be ≈ 59 mV/dec.

The observed trend is similar for the asymmetric DGFET and SOIFET. We tested the influence of the *Fermi*(-Dirac statistics) model and *BGN* model on this trend. Also, we tested the influence of V_{DS} and L. The trend shifts down for a higher drain-source voltage (indicated by the black arrow), but the slope remains the same. The other cases (not shown) had no effect on the observed trend.

We attribute the observed behaviour to inversion charge carriers in the channel, which was ignored for the derivation of the analytical models.



(a)



(b)

Figure 5.5: (a) Electrostatics parameter m_{11} as a function of the gate-source voltage for $k = 0.9, 0.95, 1, 1.05$ and 1.1 for the analytical model and TCAD simulations (symmetric DGFET). The ideal symmetric situation is indicated in the legend ($m = 1$, blue dotted line) for comparison. (b) The absolute value of the difference between the analytal m_{11} and the extracted m_{11} from TCAD (symmetric DGFET) is shown as a function of the gate-source voltage. Curves are shown for $V_{\mathrm{DS}} = 1$ mV and $V_{\mathrm{DS}} = 25$ mV. The latter is fitted (dotted blue line) and the inverse slope of the fit is ≈ 59 mV/dec.

The behaviour of the inversion charge is expected to increase the electrostatics $\propto u_{\mathrm{T}} \ln(10)$, as is shown by the inverse of the slope of the fitted curve here.

Subthreshold swing The combined effect of the transverse field contribution and the electrostatics is now demonstrated in figure 5.6, which shows the subthreshold swing. Figure 5.6(a) shows SS as a function of the gate-source voltage for five k-values. The analytical model captures the behaviour for all k well. As expected, we see that the apparent band edge propagates into the SS.

We can also show how well the analytical model describes the TCAD SS with figure 5.6(b), where the subthreshold swing is shown as a function of k at $V_{\mathrm{GS}} = 0.1$ V. Only a minor offset, resulting from the transverse field contribution, can be observed.

The errors obtained from the analytical electrostatics and transverse field contributions as compared to the TCAD results are similar in magnitude for $V_{\mathrm{GS}} > 0.25$ V.

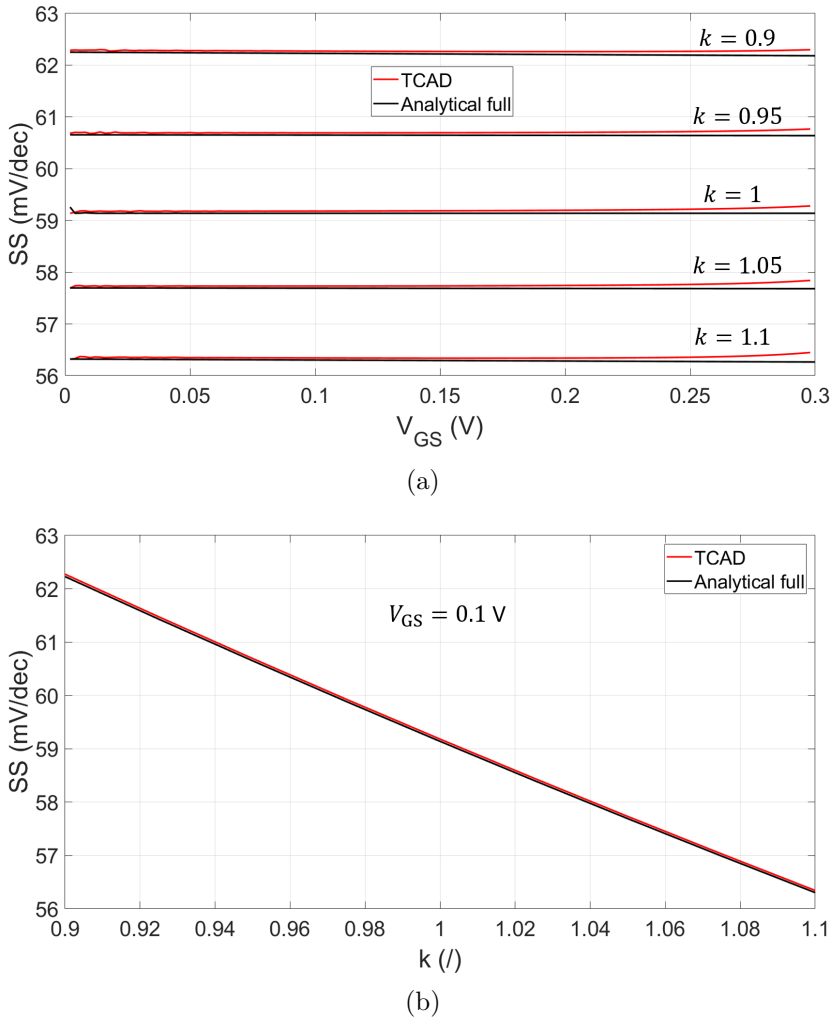


Figure 5.6: The subthreshold swing is shown for TCAD simulations (symmetric DGFET) and the analytical model (a) as a function of the gate-source voltage for $k = 0.9, 0.95, 1, 1.05$ and 1.1 and (b) as a function of k at $V_{\mathrm{GS}} = 0.1$ V.

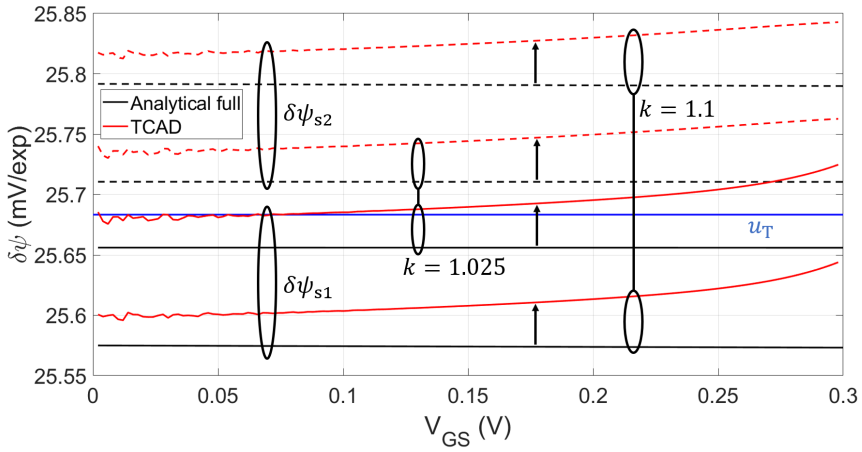
For smaller gate-source voltages the error induced by the transverse field contribution dominates.

Asymmetric DGFET

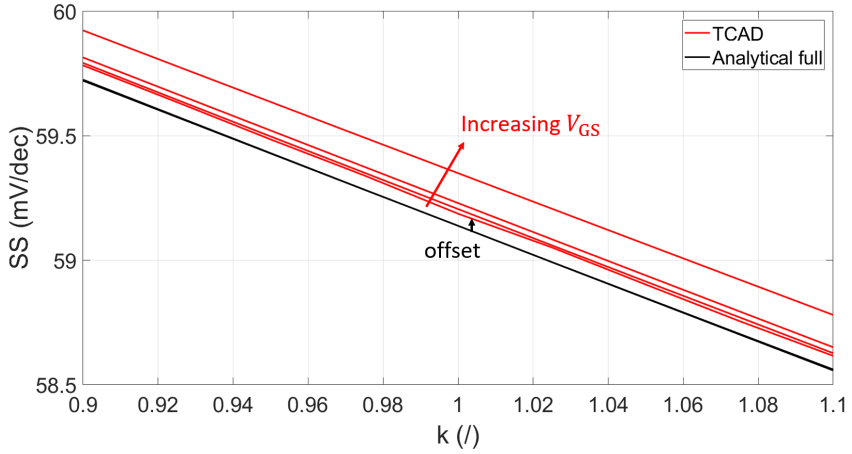
We considered the asymmetric DGFET deck (with $t_{\mathrm{ox1}} = 1.3$ nm and $t_{\mathrm{ox2}} = 20$ nm) and found that the electrostatics model also fits the TCAD data nicely. However, the effect of k on the spacing between the curves of m_{11} as a function of the gate-source voltage has reduced, as can be expected for a thicker BOX layer.

This minor influence of k (due to a weaker back-gate control) also results in a significant deviation between the analytical and TCAD transverse field contribution. Referring back to the transverse field contribution as obtained with the "split" and "full" current model for the symmetric DGFET, we notice that the reduced influence of k as observed for the asymmetric DGFET would result in the errors introduced by the "split" model to be even more significant, as compared to the spacing between the curves for several k-values.

Figure 5.7(a) shows the transverse field contribution as a function of the gate-source voltage for $k = 1.025$ and for $k = 1.1$. The offset between the analytical and TCAD curves is indicated (black arrows)



(a)



(b)

Figure 5.7: (a) Transverse field contribution in mV per factor of e in drain current (mV/exp) as a function of the gate-source voltage for the analytical model and TCAD simulations (asymmetric DGFET, $t_{\mathrm{ox1}} = 1.3$ nm and $t_{\mathrm{ox2}} = 20$ nm). The results are shown for $\delta\psi_{\mathrm{s1}}$ and $\delta\psi_{\mathrm{s2}}$, for $k = 1.025$ and for $k = 1.1$, as indicated by the black circles. The analytical $\delta\psi_{sx}$ is symmetric around u_{T} (solid blue line). (b) Subthreshold swing as a function of k for the analytical model and TCAD simulations (asymmetric DGFET, $t_{\mathrm{ox1}} = 1.3$ nm and $t_{\mathrm{ox2}} = 20$ nm). Results are shown at $V_{\mathrm{GS}} = 0.02, 0.1, 0.2$ and 0.3 V. The analytical model is gate-source voltage independent (black lines overlap) and for the TCAD simulations the trend for increasing V_{GS} is indicated (red arrow). For both (a) and (b) the offset between the analytical model and the TCAD simulations is indicated (black arrows).

and is approximately 0.04 mV/exp. Additionally we found that the TCAD results show a considerable slope as a function of the gate-source voltage, whereas no such slope exists for the analytical model. The offset between TCAD and analytical model was already described for the symmetric case, and comparing the offset for both cases shows that the offset is the same for low V_{GS}. However, the offset increases with the gate-source voltage for the asymmetric case with a thicker BOX layer, as indicated by the considerable slope. This effect might be due to a workfunction difference. We tested what happened to $\delta\psi_{sx}$ by changing the back-gate workfunction to $\phi_2 = 4.7$ eV for the symmetric DGFET deck, and we observed no change. We therefore expect this effect to be the result of short-channel effects. For the relatively thin oxides used for the symmetric DGFET this results in an almost constant offset with respect to the "spacing" in $\delta\psi_{sx}$ as obtained by k. The more closely-spaced curves for the asymmetric DGFET

experience a relatively large offset. Especially the significant slope of the transverse field contribution is due to the oxide being so thick that the length of the channel is of a more significant influence. This expectation has not been supported by any simulation data yet and still has to be validated.

The mentioned offset and slope propagate through in the subthreshold slope. We show the SS as a function of k in figure 5.7(b), at four gate-source voltage values: $V_{\mathrm{GS}} = 22$ mV, $0.1, 0.2$ and 0.3 V. The offset due to the transverse field contribution is shown (black arrow), together with the effect of the gate-source voltage on the curve (red arrow). It must be noted that the effect of V_{GS} for high V_{GS}-values is partially due to the apparent band edge of the electrostatics model.

The offset in SS of the TCAD results for the asymmetric DGFET as compared to the analytical results, for $V_{\mathrm{GS}} < 0.2$ V, is in the range of 0.04 to 0.1 mV/dec. For the symmetric DGFET in this V_{GS}-range, the offset is in the range of 0.04 to 0.06 mV/dec. The lower limit of the offset corresponds to the obtained error in SS for $k = 1$ (discussed in the first paragraph of this section), which further supports our claim for the observed trend to be a short-channel effect.

Similar results for the transverse field contribution as discussed here were obtained for the SOIFET deck. This is expected, as the front and buried oxide thickness of both decks are the same. However, the SOIFET incorporates depletion effects such that we obtain slightly different results in general. The effects of the back-gate depletion capacitance on the results will be discussed now.

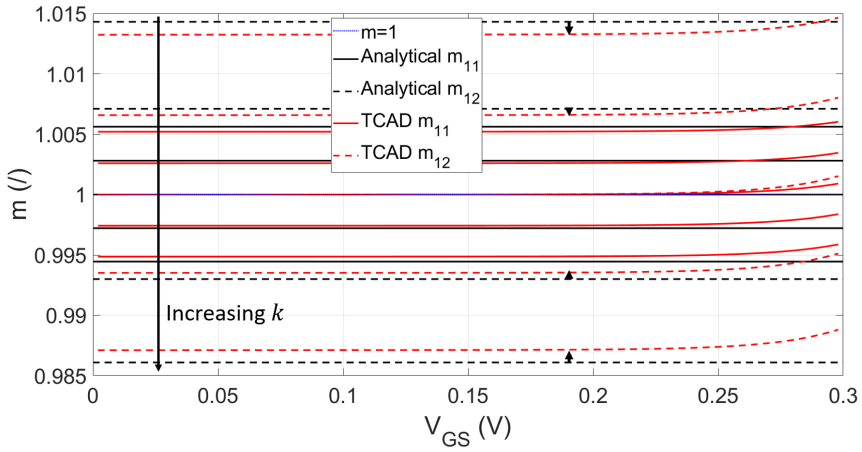
SOIFET and depletion

For determining the influence of back-gate depletion we use the SOIFET deck with (default) $N_{\mathrm{well}} = 5 \cdot 10^{17}$ cm^{-3} (such that $\Delta\phi_2 = -0.45$ eV). As a reminder, some other default parameters of the deck that were used for the TCAD simulations discussed here are $\Delta\phi_1 = 0$ eV, $t_{\mathrm{ox1}} = 1.3$ nm and $t_{\mathrm{ox2}} = 20$ nm. Also, we used $V_{\mathrm{BGS}} = k \cdot V_{\mathrm{GS}} + V_{\mathrm{off}}$. This effectively renders the effect of the workfunction difference due to the n-well to be insignificant, as almost all effects introduced by this workfunction difference are canceled out by V_{off}.

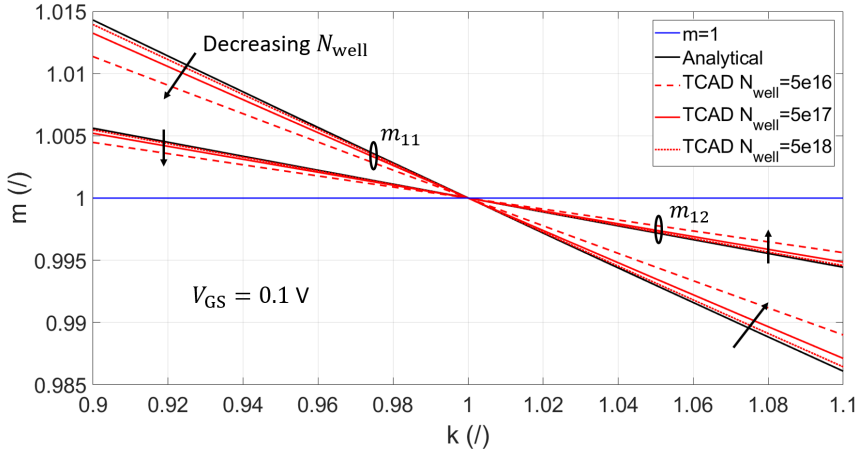
The electrostatics parameters m_{11} and m_{12} are shown in figure 5.8(a) as a function of the gate-source voltage for the analytical model (where the depletion capacitance is neglected) and that for the TCAD simulation. The figure shows that the m-curves are more closely spaced for TCAD results than for the analytical model, i.e. k has a smaller influence (indicated by the black arrows). The reason for this is the depletion capacitance. As explained in the theory (section 2.10), a more lightly-doped n-well results in a smaller C_{dep}. Because the depletion capacitance and BOX capacitance are in series, the total bottom capacitance then reduces. Therefore, the electrostatics are less influenced by k explaining the shown curves. One could also say that the depletion region width results in a thicker "effective" buried oxide layer. Considering that the spacing between the m-curves decreased for increasing the buried oxide thickness (for the asymmetric DGFET as compared to the symmetric DGFET), this would be an intuitive description.

In order to clearly demonstrate this spacing as a function of the N_{well}, figure 5.8(b) shows the same electrostatics parameters as a function of k at $V_{\mathrm{GS}} = 0.1$ V for three different n-well doping concentrations: $N_{\mathrm{well}} = 5 \cdot 10^{16}$ cm^{-3}, $N_{\mathrm{well}} = 5 \cdot 10^{17}$ cm^{-3} (default) and $N_{\mathrm{well}} = 5 \cdot 10^{18}$ cm^{-3}. A clear decrease in slope of the m-curves as a function of k is observed for decreasing N_{well} (black arrows). That is, the TCAD curves start to deviate more from the analytical model for decreasing n-well doping concentrations.

We found that the slope of the transverse field contribution as a function of k also slightly changed, with respect to the results obtained for the asymmetric and symmetric DGFET. This is because the transverse field contribution is slightly influenced by the electrostatics through the coupling between the surface potentials ($d\psi_{\mathrm{s1}}/d\psi_{\mathrm{s2}}$, see equation 2.50). This effect is less significant in comparison to the change in m, however, such that the main change observed in the SS due to back-gate depletion results from the electrostatics m-parameters.



(a)



(b)

Figure 5.8: Electrostatics parameters m_{11} and m_{12} for TCAD simulations (SOIFET) and the analytical model (a) as a function of the gate-source voltage for $k = 0.9, 0.95, 1, 1.05$ and 1.1 and (b) as a function of k at $V_{\mathrm{GS}} = 0.1$ V. The ideal symmetric situation is indicated in the legend ($m = 1$, blue line) for comparison. (a) Results for $N_{\mathrm{well}} = 5 \cdot 10^{17}$ cm^{-3} (TCAD simulations) are more closely spaced than analytical model results, as indicated (black arrows). (b) Results for $N_{\mathrm{well}} = 5 \cdot 10^{16}$ cm^{-3}, $N_{\mathrm{well}} = 5 \cdot 10^{17}$ cm^{-3} and $N_{\mathrm{well}} = 5 \cdot 10^{18}$ cm^{-3} (TCAD simulations, SOIFET) are shown and the trend with decreasing N_{well} is indicated (black arrows).

CVT mobility model influence

The influence of a field-dependent mobility on the results is demonstrated in this paragraph. The CVT model incorporates the transverse electric field and is used to model the field-dependent mobility for this research.

We start by testing the influence of the CVT model as compared to several constant mobilities for $k = 1$. In figure 5.9 the subthreshold swing is shown as a function of the gate-source voltage for a mobility as obtained from the CVT model and for three constant mobilities: $\mu_{\mathrm{n}} = 600$ cm^{2}V^{-1}s^{-1}, $\mu_{\mathrm{n}} = 200$ cm^{2}V^{-1}s^{-1} and $\mu_{\mathrm{n}} = 20$ cm^{2}V^{-1}s^{-1}. Until now we used a constant mobility of $\mu_{\mathrm{n}} = 600$ cm^{2}V^{-1}s^{-1}, and the value taken clearly does not have an influence on the SS. It should be mentioned that the value does have an influence on the drain current. The SS obtained from calculations using the CVT model is already slightly different from that obtained with a constant mobility for $k = 1$.

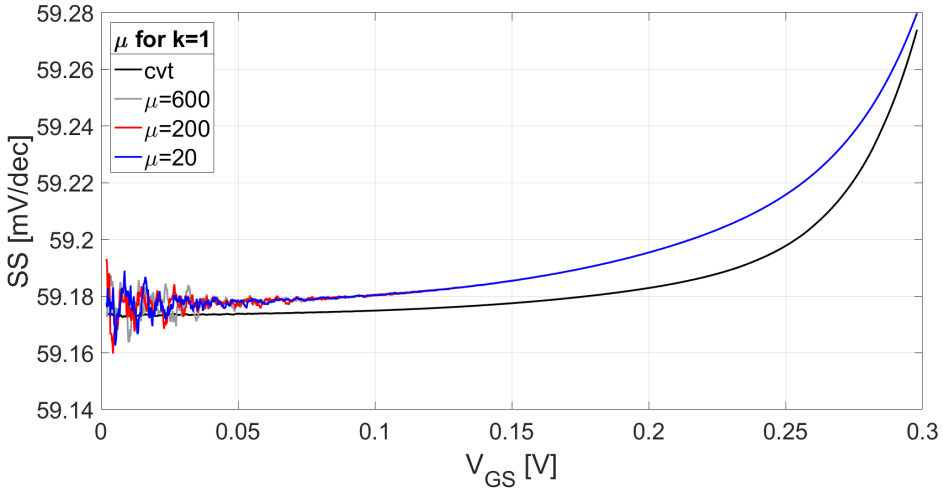
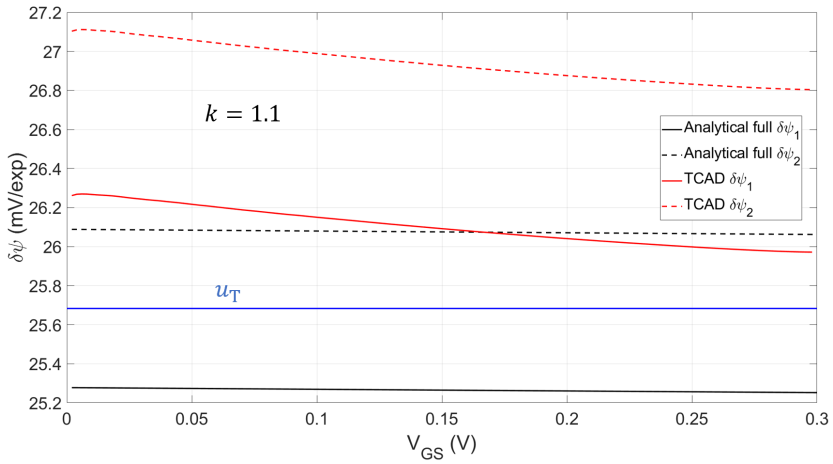


Figure 5.9: Subthreshold swing as a function of the gate-source voltage for $k = 1$ from TCAD simulations (symmetric DGFET) with a constant mobility of 20, 200 and 600 $\mathrm{cm^2V^{-1}s^{-1}}$ and from TCAD simulations with the mobility as defined by the CVT model.

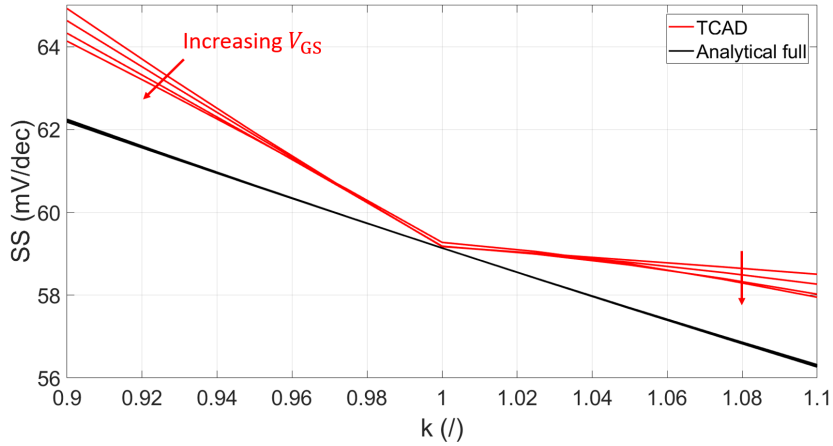
We found that the drain current for TCAD data with the CVT model can be reasonably well approximated using a constant mobility of $\mu_\mathrm{n} = 1050\ \mathrm{cm^2V^{-1}s^{-1}}$ in the analytical model, for all used k. However, the transverse field contribution of the subthreshold swing is severely influenced by the field-dependent mobility, especially for $k \neq 1$. This is shown in figure 5.10(a), where $\delta\psi_{sx}$ is plotted as a function of the gate-source voltage for $k = 1.1$. The TCAD curves clearly deviate from the analytical model curves and even have an opposite slope as compared to that obtained for considering the asymmetric DGFET (see figure 5.7(a)). The electrostatics remain the same despite changing the mobility to a field-dependent one, so the SS is only different because of this transverse field contribution. Figure 5.10(b) shows the SS as a function of k at four different gate-source voltages. Indeed the TCAD SS at $k = 1$ is still well-approximated by the analytical model, and the TCAD SS deviates for increasing or decreasing k with respect to $k = 1$. The deviation as obtained with the CVT model seems to slightly diminish for increasing V_GS (black arrows). This was already evident from the decreasing slope with respect to the gate-source voltage in figure 5.10(a). Additionally, the TCAD curves for the subthreshold swing seem to be symmetric with respect to the analytical model around $k = 1$. That is, the difference between the TCAD curves and analytical curves seems to increase the same for increasing or decreasing k, with respect to $k = 1$. We tested the influence of the oxide thickness on this trend, but found that the same symmetric trend was observed for an asymmetric DGFET with $t_\mathrm{ox2} = 10$ nm and $t_\mathrm{ox2} = 20$ nm (for $t_\mathrm{ox1} = 1.3$ nm).

The symmetry and deviation of the subthreshold swing (as a function of k) can be explained with the mobility for the CVT model. Figure 5.11(a) shows the mobility as extracted from TCAD for an asymmetric DGFET ($t_\mathrm{ox1} = 1.3$ nm and $t_\mathrm{ox2} = 20$ nm) as a function of the gate-source voltage.

From figure 5.10(b) we observed that any change in k other than $k = 1$ did not change the behaviour with respect to the analytical model. This is validated here, where no difference in mobility is obtained for either a higher or lower k-value (with respect to $k = 1$). Therefore, we define $\Delta k = |k - 1|$. A decreasing mobility with respect to the gate-source voltage is observed for an increasing Δk. That is, the mobility decreases with the gate-source voltage since increasing the gate-source voltage means increasing the transverse field. This increase in transverse field is higher for a higher Δk, such that the mobility drops more. The mobility was probed halfway the length of the channel at the top and bottom interface, and in the middle of the channel. This results in 3 curves for each k-value. Additionally, the curves for higher and lower k-values are close to identical, as was explained. We therefore obtain 6 curves for each



(a)

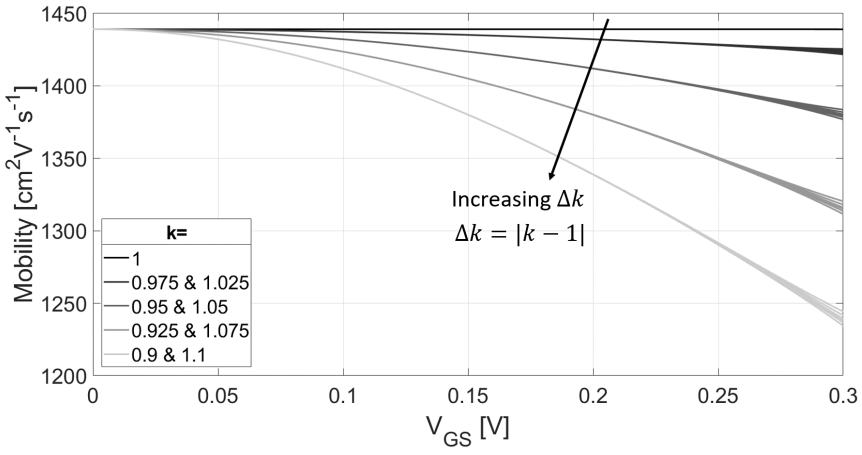


(b)

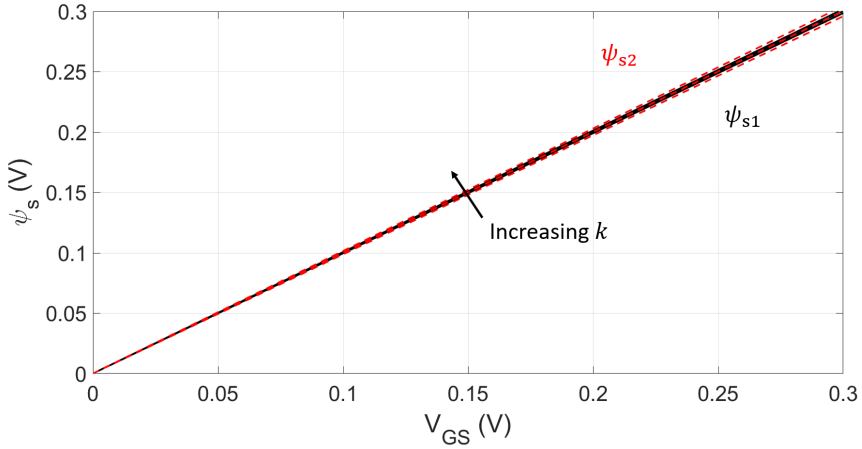
Figure 5.10: (a) Transverse field contribution in mV per factor of e in drain current (mV/exp) as a function of the gate-source voltage for the analytical model and TCAD simulations (symmetric DGFET). The results for $\delta\psi_{s1}$ and $\delta\psi_{s2}$ are shown for $k = 1.1$. The analytical $\delta\psi_{sx}$ is symmetric around u_T (solid blue line). (b) Subthreshold swing as a function of k for the analytical model and TCAD simulations (symmetric DGFET). Results are shown at $V_{GS} = 0.02, 0.1, 0.2$ and 0.3 V. The analytical model is gate-source voltage independent (black lines overlap) and for the TCAD simulations the trend for increasing V_{GS} is indicated (red arrow).

Δk. These 6 curves can be distinguished around $V_{GS} = 0.3$ V. The mobility drops by approximately 14% for $\Delta k = 0.1$ ($k = 0.9$ and $k = 1.1$) at $V_{GS} = 0.3$ V. In order to comprehend the significance of this change, we show the surface potentials as a function of the gate-source voltage in figure 5.11(b). The effect of k is shown (black arrow) to increase the surface potentials. However, the increase in surface potentials by changing from $k = 0.9$ to $k = 1.1$ is only about 3% for ψ_{s2} and 1% for ψ_{s1}.

We continue with discussing the influence of the CVT model on the results obtained for the SOIFET deck. Also for the SOIFET deck the field-dependence of the mobility has no influence on the electrostatics. We therefore discuss the transverse field component only. Figure 5.12 shows the transverse field contribution as a function of the gate-source voltage for $k = 0.9, 0.95, 1, 1.05$ and 1.1. First of all, the figure shows that also for the SOIFET the analytical model does not describe the transverse field contribution well for a field-dependent mobility. This is indicated by the bad correspondence between black



(a)



(b)

Figure 5.11: (a) The mobility obtained from TCAD simulations using the CVT model (asymmetric DGFET, $t_{ox1} = 1.3$ nm and $t_{ox2} = 20$ nm) is shown as a function of the gate-source voltage for $k = 0.90.925, 0.95, 0.975, 1, 1.025, 1.05, 1.075$ and 1.1. The curves for k are grouped according to the same $\Delta k = |k - 1|$ having the same color. The trend with increasing Δk is indicated (black arrow). (b) The corresponding surface potentials (ψ_{s1} in black, ψ_{s2} in red) are shown as a function of the gate-source voltage for $k = 0.9, 0.95, 1, 1.05$ and 1.1. The trend with increasing k is indicated (black arrow).

and red curves. Additionally, the analytical curves for $\delta\psi_{s1}$ and $\delta\psi_{s2}$ are symmetric with respect to each other around $k = 1$. This results in the curves (black solid and dashed) to overlap. For the TCAD results with the CVT model this is clearly no longer the case. The most important observation is the kink in the TCAD curves for $k = 1.1$ and $k = 1.05$ (indicated by the vertical black dotted lines). This kink is non-physical and is the result from a combination between the back-gate workfunction and the CVT model. We assume that the offset voltage $V_{off} = -0.45$ V completely compensates $\Delta\phi_2 = -0.45$ eV. However, if the workfunction difference is overcompensated with the offset voltage, we have a situation at $V_{GS} = 0$ where $\psi_{s2} < \psi_{s1}$. Increasing the gate-voltage with e.g. $k = 1.1$ then eventually results in $\psi_{s2} = \psi_{s1}$ at some value of V_{GS}. Further increasing the gate-source voltage results in $\psi_{s2} > \psi_{s1}$. We thus see a change in the sign of the transverse field, and apparently the CVT model cannot cope with this. Actually, the vertical dashed black lines thus indicate the gate-source voltage at which the surface potentials are equal. The situations for lower and higher gate-source voltages are also indicated (black arrows with respect to the vertical dashed black lines). It can be noted that the gate-source voltage at which the

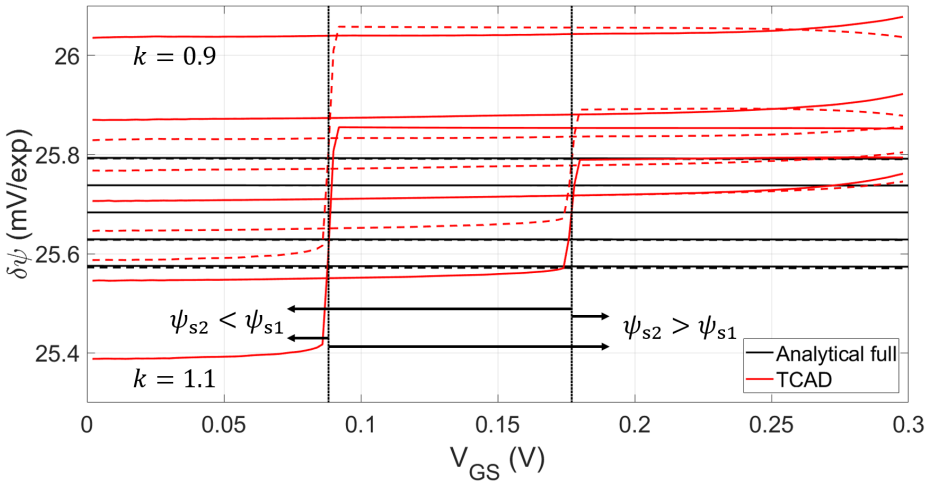


Figure 5.12: Transverse field contribution in mV per factor of e in drain current (mV/exp) as a function of the gate-source voltage for the analytical model and TCAD simulations (SOIFET). The results for $\delta\psi_{s1}$ (solid red/black))and $\delta\psi_{s2}$ (dashed red/black) are shown for $k = 0.9, 0.95, 1, 1.05$ and 1.1. The lowest and highest k are indicated. The TCAD simulation results for $k = 1.1$ and $k = 1.05$ show a kink at $\psi_{s1} = \psi_{s2}$, as indicated by the vertical dashed black lines. Left of this kink, $\psi_{s2} < \psi_{s1}$ and right of this kink $\psi_{s2} > \psi_{s1}$, as indicated (black arrows).

surface potentials are equal shifts to the left for increasing k. This is because the back surface potential increases more for a higher k, such that the situation of equal surface potentials is already obtained for a lower gate-source voltage. In case the k-value is so low that the back surface potential is still lower than the front surface potential at $V_{GS} = 0.3$ V, no kink is observed. This is the case for $k = 1.025$ for this TCAD simulation series (not shown). In general, for $k \leq 1$ no problems are encountered. Furthermore, in case the workfunction difference is not entirely compensated, we obtain a similar situation. In that case, $\psi_{s2} > \psi_{s1}$ at $V_{GS} = 0$ V and we obtain $\psi_{s2} < \psi_{s1}$ at some higher V_{GS}-value for $k < 1$. Then, for $k \geq 1$ no problems are encountered.

In conclusion, we cannot include a field-dependent mobility for an SOIFET deck where the workfunction difference is not exactly compensated by V_{off}. This means that our analytical model cannot be tuned for a field-dependent mobility, as we simply lack an accurate TCAD model to test against.

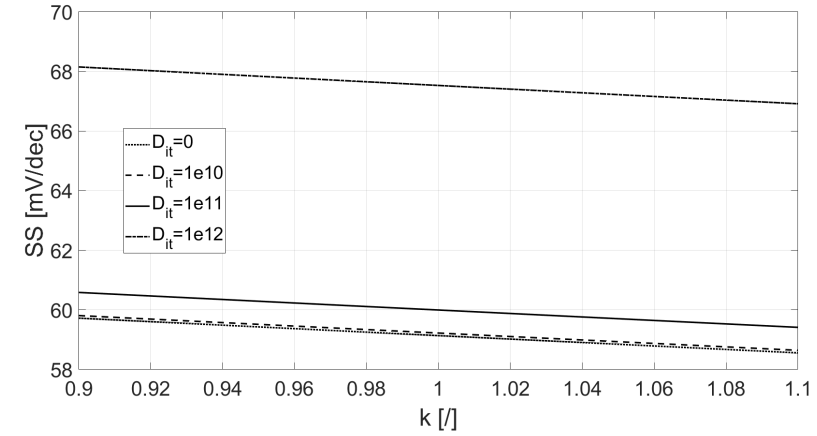
5.2.2 Analytical model and TCAD simulations with interface traps

We first discuss the influence of interface traps on the analytical model and then compare the analytical model (including traps) to TCAD simulations (including traps). Finally, we extract the interface trap densities from both interfaces separately from the TCAD simulations by fitting the analytical model to the results. We then thus effectively use the TCAD simulations as measurements (or "emulations") in order to validate the model, obtain possibly an estimate of the extracted D_{it}-functions, an estimate of the error of the fitting procedure and determine the limits of this fitting method.

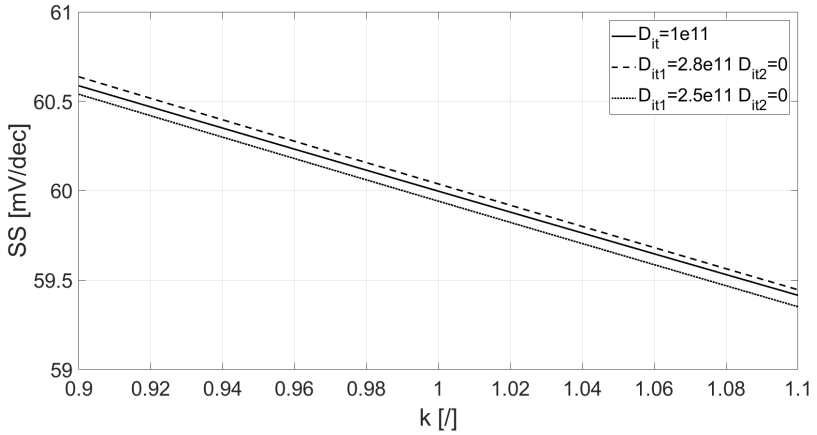
Analytical model including interface traps

For this part of the work we included interface traps in the analytical model. That is, so far we used $D_{it1} = D_{it2} = 0$ cm^{-2}eV^{-1} and next we changed this to non-zero values.

Figure 5.13(a) shows the subthreshold swing as a function of k for uniformly distributed symmetric interface trap density profiles, i.e. for $D_{it1} = D_{it2} = D_{it}$. The SS curves for $D_{it} = 0$ cm^{-2}eV^{-1} and $D_{it} = 1 \cdot 10^{10}$ cm^{-2}eV^{-1} are difficult to distinguish. For higher interface trap densities the subthreshold



(a)



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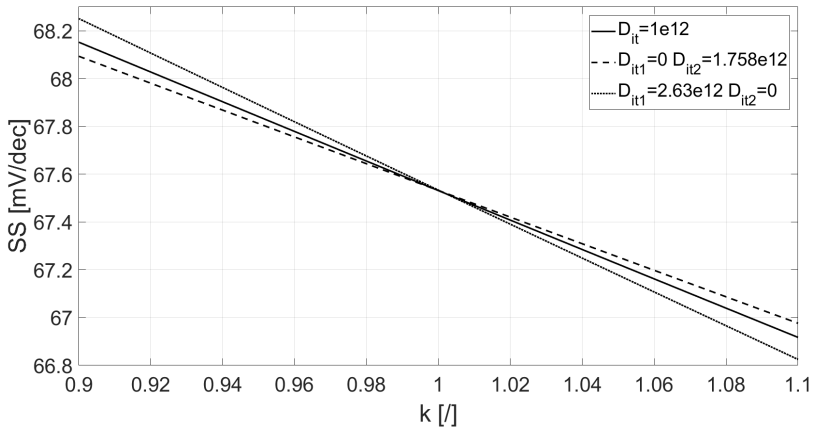


(c)

Figure 5.13: Subthreshold swing as a function of k for the analytical model (hence independent of V_{GS}) for (a) symmetric interface trap profiles, i.e. $D_{\mathrm{it1}} = D_{\mathrm{it2}} = D_{\mathrm{it}}$, (b) asymmetric interface trap profiles with only front interface traps, i.e. $D_{\mathrm{it2}} = 0$ cm^{-2}eV^{-1} as compared to a symmetric profile with $D_{\mathrm{it}} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1}, where we chose D_{it1} for asymmetric profiles such that the symmetric trap profile is well-approximated, and for (c) asymmetric interface trap profiles with either only front or back interface traps, i.e. $D_{\mathrm{it2}} = 0$ cm^{-2}eV^{-1} and $D_{\mathrm{it1}} = 0$ cm^{-2}eV^{-1}, respectively. In both cases we chose the trap profile of the other interface such that the symmetric profile with $D_{\mathrm{it}} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} is well-approximated. For all figures, the units of the indicated interface trap densities (in the legend) are cm^{-2}eV^{-1}.

swing clearly increases. For $D_{\text{it}} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1} the SS is approximately 1 mV/dec higher than for $D_{\text{it}} = 0$ cm^{-2}eV^{-1} and for $D_{\text{it}} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} the SS is approximately 8 mV/dec higher. We expect the lower limit of interface trap extraction to be around $D_{\text{it}} = 1 \cdot 10^{10}$ cm^{-2}eV^{-1}, as originally reported by Schmitz et al. [23], since smaller values would give an indistinguishable SS as compared to this.

Figure 5.13(b) compares the symmetric interface trap density profile (with $D_{\text{it}} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1}) with two asymmetric profiles. The asymmetric profiles only contain front interface traps, i.e. $D_{\text{it2}} = 0$ cm^{-2}eV^{-1}. The front interface trap density of the two curves is chosen such that it becomes clear that the symmetric profile can be well-approximate by an asymmetric profile for such a low interface trap density. The slope of the asymmetric profile curves is slightly different from the slope for the symmetric profile, but the curves would be hard to distinguish by trying to fit the curves. Especially when considering (more noisy) measurement data, the lower limit of extracting the interface trap densities for the two interfaces separately is expected to be at least $1 \cdot 10^{11}$ cm^{-2}eV^{-1}.

Figure 5.13(c) compares the symmetric interface trap density profile (with $D_{\text{it}} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1}) with two asymmetric profiles. One of the asymmetric profiles contains only front interface traps, i.e. $D_{\text{it2}} = 0$ cm^{-2}eV^{-1}, the other contains only back interface traps, i.e. $D_{\text{it1}} = 0$ cm^{-2}eV^{-1}. For these profiles with higher values for the interface trap density, the difference in slopes for the two asymmetric situations and the symmetric situation becomes clear.

Note also that the effect of back interface traps on the slope is similar to the effect of the depletion capacitance. This results in difficulties for the trap extraction if the effect of the depletion capacitance is not accurately known. Thus, for extracting the interface trap density from measurements we expect this to result in errors, next to the field-dependence of the mobility.

TCAD simulations including interface traps

We compare the SS for TCAD simulations (symmetric DGFET) with $D_{\text{it}} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1} and the analytical model for this same symmetric trap profile in figure 5.14. For comparison, the analytical model curves for $D_{\text{it}} = 0$ cm^{-2}eV^{-1} are also shown. In the figure, the subthreshold swing is shown as a function of the gate-source voltage for five k-values. The analytical model and TCAD curves match well

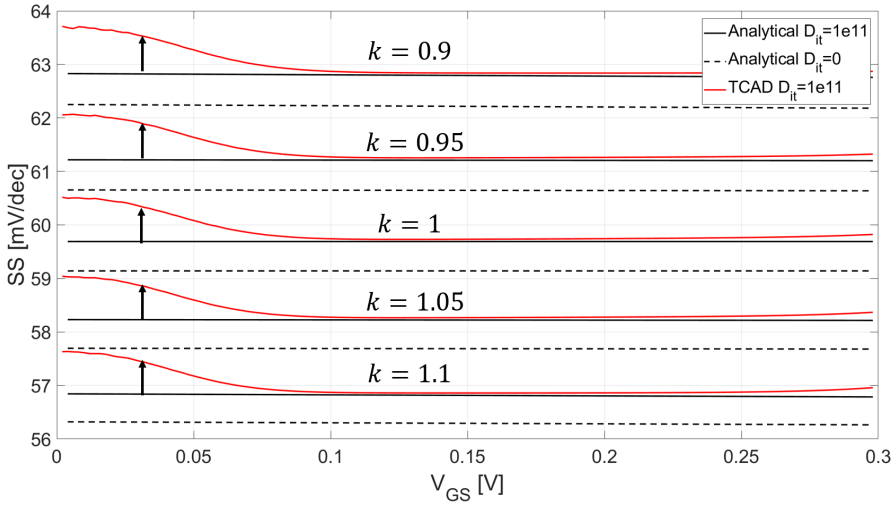


Figure 5.14: Subthreshold swing as a function of the gate-source voltage for $k = 0.9, 0.95, 1, 1.05$ and 1.1. Results shown for TCAD simulations (symmetric DGFET) and the analytical model, with a symmetric interface trap profile with $D_{\text{it}} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1}. The analytical model curves for $D_{\text{it}} = 0$ cm^{-2}eV^{-1} are shown for comparison. The difference between TCAD simulations and the analytical model (with traps) for low gate-source voltages is indicated (black arrows).

for $V_{GS} > 0.1$ V. The discrepancies between the analytical model and TCAD simulation results within this range ($0.1 < V_{GS} < 0.3$ V) are the same in magnitude as those observed for the situation without traps (see figure 5.6). This indicates that the model is valid both without and with traps.

However, incorporating traps in the TCAD simulations results in strange behaviour for both the transverse field contribution $\delta\psi_s$ and the electrostatics m for $V_{GS} < 0.1$ V. These effects propagate through in the subthreshold swing and are clearly shown (indicated by the black arrows). The reason for this behaviour at low voltages is due to the way in which Atlas incorporates the discrete traps. The discrete trap implementation as used here is compared to a continuous trap implementation in [50]. The conclusion is that a continuous C-interpreter function is preferred due to the discrepancies in the discrete trap implementation. One of the discrepancies shown in the article is a higher subthreshold swing for low gate-source voltages.

For the asymmetric DGFET (with $t_{ox1} = 1.3$ nm and $t_{ox2} = 20$ nm) we obtain qualitatively similar results. That is, the effect of k is smaller (more closely spaced curves) such that the effect of this erroneous discrete trap behaviour is more significant. Also, within the range of $0.1 < V_{GS} < 0.3$ V the discrepancies in the obtained subthreshold swing are equal in magnitude as was the case without traps.

In case of only front- or back interface traps, the slope of the TCAD simulation curve changes the same as was the case for the analytical model (see figure 5.13(a) and (b)).

If we use the CVT model we see the same trend as shown in figure 5.10(b), i.e. the TCAD simulation curve (for $D_{it} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1}) is tangential to the analytical curve (for $D_{it} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1}) at $k = 1$, and deviates for increasing or decreasing k.

5.2.3 Extracting interface traps from TCAD simulations with the analytical model

Trap extraction from TCAD without input interface traps

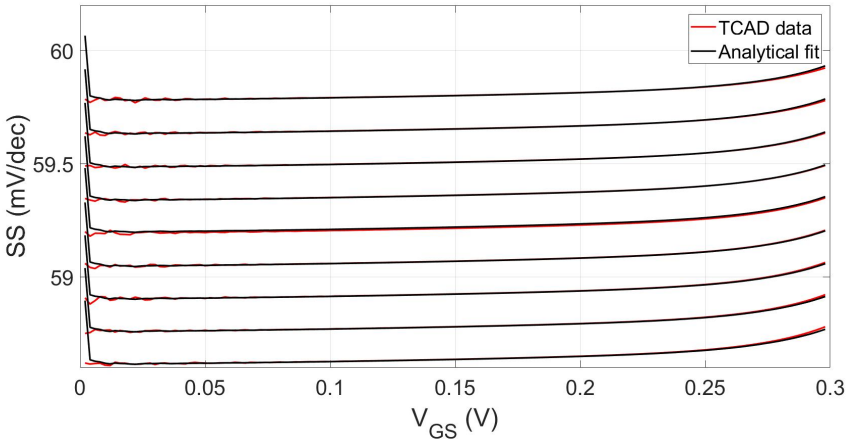
We discuss how we could fit the analytical model to "measurement" data for extracting the trap density at both interfaces separately. We used TCAD simulation data as "measurement" data and fit the total set of SS Vs. V_{GS} curves for all k. This way, we can investigate the validity of this method.

First the "apparent" interface trap density was extracted from TCAD simulation data (asymmetric DGFET, $t_{ox1} = 1.3$ nm and $t_{ox2} = 20$ nm) where the device actually contains no interface traps. We then obtained the limit of the accuracy of the analytical model for extracting interface traps. The analytical model was fitted to the TCAD curves as is shown in figure 5.15(a). In this figure, the subthreshold swing is shown as a function of the gate-source voltage for all nine k-values: $k = 0.9, 0.925, 0.95, 0.975, 1, 1.025, 1.05, 1.075$ and 1.1. The extracted interface trap densities corresponding to this fit are shown in figure 5.15(b), as a function of the gate-source voltage.

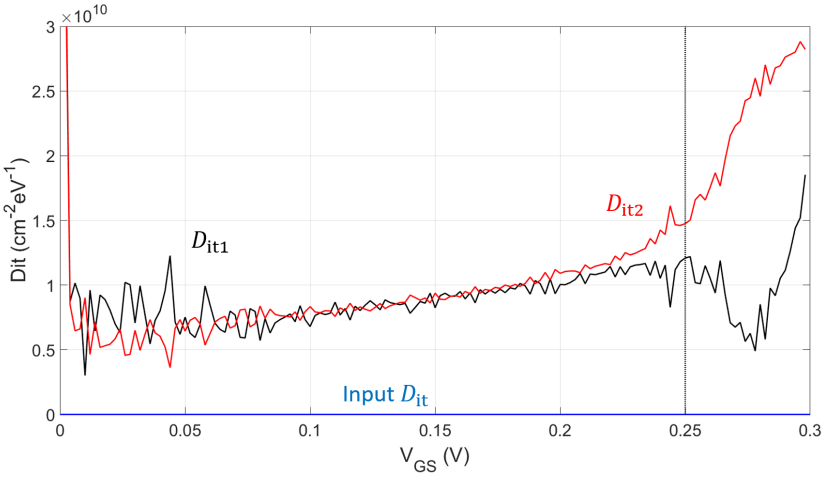
The extracted interface trap density is noisier for $V_{GS} < 0.05$ V as the TCAD simulation data is noisier. This even results in some "fitting artifact" for the first datapoint. Furthermore, the analytical model showed to be increasingly more inaccurate with increasing the gate-source voltage (see figure 5.6), due to the "apparent conduction band edge", which is not accounted for in the model. Here, the extracted interface trap density is significantly more erroneous for approximately $V_{GS} > 0.25$ V. At this V_{GS}-value we find that the difference between the TCAD and analytical subthreshold swing is approximately 0.2%, so apparently an error larger than this results in an increase in the error in interface trap density extraction. We therefore define the valid range of interface trap density extraction to be $0 < V_{GS} < 0.25$ V, where we neglect the first datapoint. We obtain a lower limit of the accuracy of approximately $1 \cdot 10^{10}$ cm^{-2}eV^{-1} for the interface trap density within this range.

Trap extraction from TCAD with symmetric input interface traps

We then extracted the interface trap density from TCAD simulation data (same asymmetric DGFET) where $D_{it1} = D_{it2} = D_{it} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1} is used as input for TCAD. Figure 5.16(a) shows the subthreshold swing as a function of the gate-source voltage for all nine k-values, for TCAD simulation



(a)

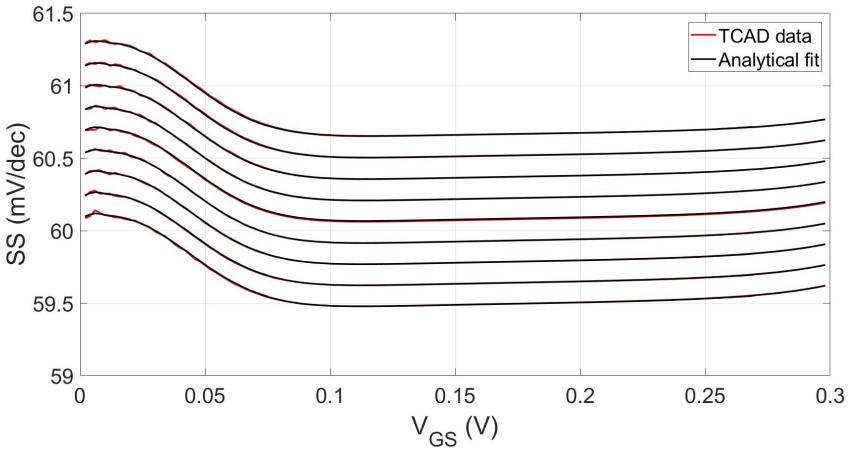


(b)

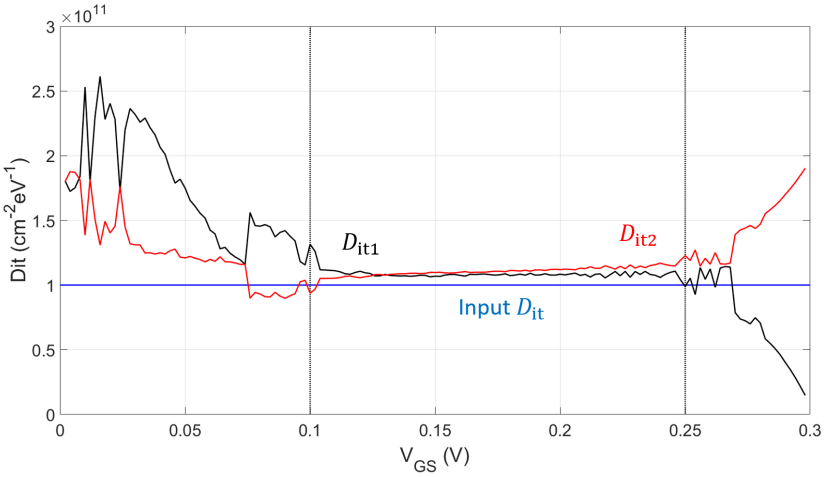
Figure 5.15: (a) Subthreshold swing as a function of the gate-source voltage for $k = 0.9, 0.9250.95, 0.975, 1, 1.025, 1.05, 1.075$ and 1.1. Results shown for TCAD simulations (asymmetric DGFET) and the analytical model as fitted to the TCAD results. An input interface trap density profile of $D_{\text{it}} = 0$ cm^{-2}eV^{-1} is used in TCAD. (b) Trap density of the front and back interfaces corresponding to (a). The input trap density profile is shown (solid blue line) and the valid range ($V_{\text{GS}} < 0.25$ V) is indicated (vertical dotted black line).

data and the fitted analytical model. The corresponding extracted interface trap densities are shown as a function of the gate-source voltage in figure 5.16(b).

Within the range of $0 < V_{\text{GS}} < 0.1$ V the discrete trap implementation results in errors. We therefore redefine the valid range of interface trap density extraction to be $0.1 < V_{\text{GS}} < 0.25$ V. Within this range, an approximately equal interface trap density is obtained for both interfaces, with a value of approximately $1.1 \cdot 10^{11}$. The errors introduced by the discrete trap implementation result in an extracted interface trap density of 1.5 to 2.5 times higher. For extracting the interface trap density in the apparent conduction band edge range, the main error is that the trap density is increasingly more attributed to the back interface. For example, at $V_{\text{GS}} = 0.3$ V we obtain approximately $D_{\text{it1}} = 0.2 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{\text{it2}} = 1.8 \cdot 10^{11}$ cm^{-2}eV^{-1}.



(a)



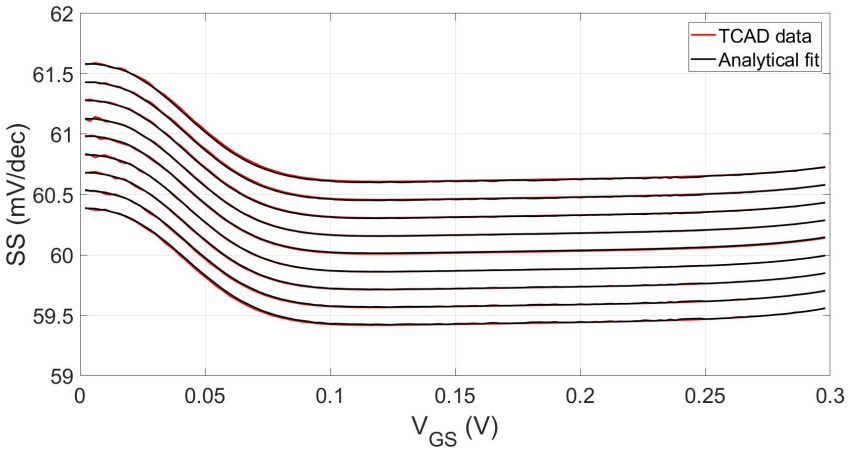
(b)

Figure 5.16: (a) Subthreshold swing as a function of the gate-source voltage for $k = 0.9, 0.9250.95, 0.975, 1, 1.025, 1.05, 1.075$ and 1.1. Results shown for TCAD simulations (asymmetric DGFET) and the analytical model as fitted to the TCAD results. A symmetric input interface trap density profile of $D_{\text{it}} = 1 \cdot 10^{11}$ cm^{-2}eV^{-1} was used in TCAD. (b) Trap density of the front and back interfaces corresponding to (a). The input trap density profile is shown (solid blue line) and the valid range ($0.1 < V_{\text{GS}} < 0.25$ V) is indicated (vertical dotted black lines).

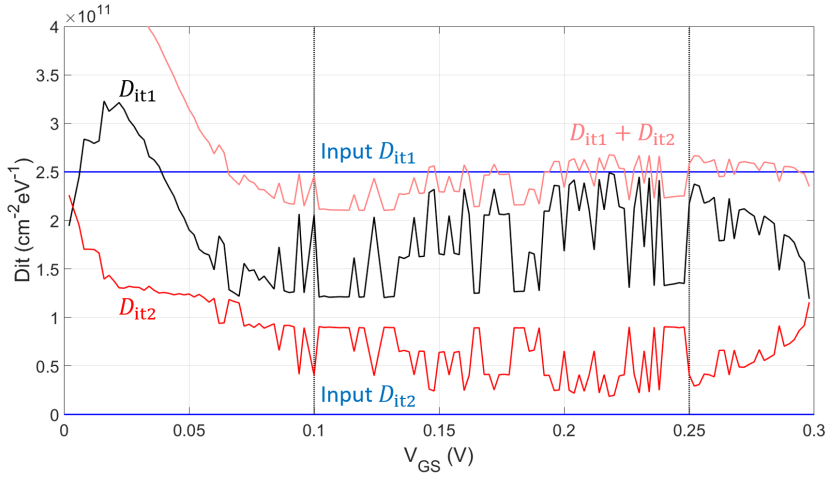
Trap extraction from TCAD with asymmetric input interface traps

We show the results for extracting traps from TCAD simulation data (same asymmetric DGFET) where $D_{\text{it1}} = 2.5 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{\text{it2}} = 0$ cm^{-2}eV^{-1} are used as input for TCAD. Figure 5.17(a) shows the subthreshold swing as a function of the gate-source voltage for all nine k-values, for TCAD simulation data and the fitted analytical model. The corresponding extracted interface trap densities are shown as a function of the gate-source voltage in figure 5.16(b).

Within the valid gate-source voltage range, we extracted a front interface trap density in the range of $1.3 \cdot 10^{11}$ to $2.5 \cdot 10^{11}$ cm^{-2}eV^{-1}, while the extracted back interface trap density is in the range of $3 \cdot 10^{10}$ to $8 \cdot 10^{10}$ cm^{-2}eV^{-1}. The total interface trap density $D_{\text{it1}} + D_{\text{it2}}$ is indicated in the figure (pink) and corresponds well to the total input interface trap density D_{it1} (since $D_{\text{it2}} = 0$ cm^{-2}eV^{-1}). However, attributing the traps to the correct interface is difficult. On average approximately $0.5 \cdot 10^{11}$ cm^{-2}eV^{-1} trap density is incorrectly attributed to the back interface. We thus have an error with respect to



(a)



(b)

Figure 5.17: (a) Subthreshold swing as a function of the gate-source voltage for $k = 0.9, 0.925...1.1$ for TCAD simulations (asymmetric DGFET) with an asymmetric input interface trap density profile of $D_{\text{it1}} = 2.5 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{\text{it2}} = 0$ cm^{-2}eV^{-1} and for the analytical model as fitted to the TCAD results. (b) Corresponding trap density of the front (black) and back (red) interfaces, as well as the total interface trap density $D_{\text{it1}} + D_{\text{it2}}$ (pink). The input trap density profile is shown (solid blue lines) and the valid range ($0.1 < V_{\text{GS}} < 0.25$ V) is indicated (dotted black lines).

the input front interface trap density of about 20% for a constant trap profile with a magnitude of $2.5 \cdot 10^{11}$ cm^{-2}eV^{-1}.

Without taking depletion and a field-dependent mobility into account, we can thus distinguish between front and back interface traps reasonably well. However, it is expected that taking a lower value (of the magnitude of the trap density) will result in a significantly increasing difficulty in splitting the interface trap contributions.

The results shown were for the asymmetric DGFET deck. Results obtained for the symmetric DGFET deck are similar.

Trap extraction from TCAD incorporating the CVT model and depletion effects

The effects of the CVT model (field-dependent mobility) and depletion capacitance (SOIFET deck) were also investigated. Both influenced the accuracy significantly.

From TCAD simulation data for which the CVT model was used, no accurate interface trap density can be extracted.

For TCAD data with depletion (SOIFET) we obtain approximately the same lower limit of the accuracy (tested for $N_{\text{well}} = 5 \cdot 10^{16}$ cm^{-3}, $N_{\text{well}} = 5 \cdot 10^{17}$ cm^{-3} (default) and $N_{\text{well}} = 5 \cdot 10^{18}$ cm^{-3}). However, for using an input profile with only front interface traps, fitting the analytical model to TCAD results in a high and incorrect back interface trap density (in the range of $D_{\text{it2}} = 6.0 \cdot 10^{10}$ cm^{-2}eV^{-1} as compared to $D_{\text{it1}} = 2.5 \cdot 10^{10}$ cm^{-2}eV^{-1}). This is due to the fact that the slope resulting from the depletion capacitance is similar to the effect of back interface traps.

Trap extraction from TCAD with δ-peak-like input interface traps

As a final test we investigated the effect of a δ-peak-like input interface trap profile. This input profile was investigated since the "spread" observed on the y-axis (extracted D_{it}) and x-axis (V_{GS} could be observed very locally (in V_{GS}). That is, extracting a profile from a δ-peak clearly indicates the "spreading" of the input profile. The interface trap density is extracted from TCAD simulation data (same asymmetric DGFET) where $D_{\text{it}} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} within the energy range of $E - E_{\text{V}} = 0.745$ to 0.755 eV and $D_{\text{it}} = 0$ cm^{-2}eV^{-1} for all other energies.

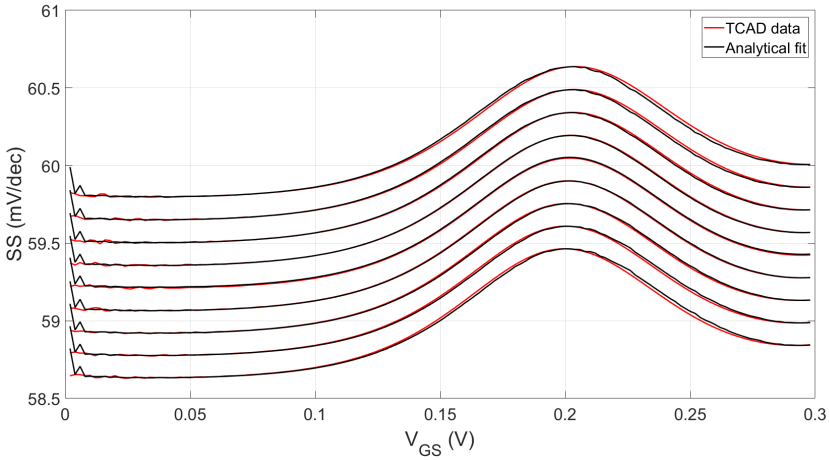
Figure 5.18(a) shows the subthreshold swing as a function of the gate-source voltage for all nine k-values, for TCAD simulation data and the fitted analytical model. The corresponding extracted interface trap densities are shown as a function of the gate-source voltage in figure 5.18(b). The mentioned energy range of the input interface trap profile is translated to a gate-source voltage range of $0.185 < V_{\text{GS}} < 0.195$ V (using $E - E_{\text{V}} = E_{\text{G}}/2 + q \cdot \psi_{\text{s}}$, see equation 2.6). The input interface trap density profile is shown for this translated range (solid blue line). From the figure it becomes clear that the input interface trap density is "smeared out" for the extracted profiles, as was also reported by Boksteen et al. [20]. That is, the maximum value decreases significantly but the area under the curve is the same.

We also obtained a maximum front and back interface trap density of $D_{\text{it1}} = 2.4 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{\text{it2}} = 1.6 \cdot 10^{11}$ cm^{-2}eV^{-1}. Integrating the input profile results in $1 \cdot 10^{10}$ cm^{-2} and integrating the extracted trap profiles (and correcting for the accuracy, the integral of the result shown in figure 5.15, approximately $3 \cdot 10^{9}$ cm^{-2}) results in $\int D_{\text{it1}} = 1.2 \cdot 10^{10}$ cm^{-2} and $\int D_{\text{it2}} = 8 \cdot 10^{9}$ cm^{-2}. Thus, adding the integrals of the extracted front and back interface trap densities (after correction) results in the same value as adding the integrals of the input front and back interface trap densities.

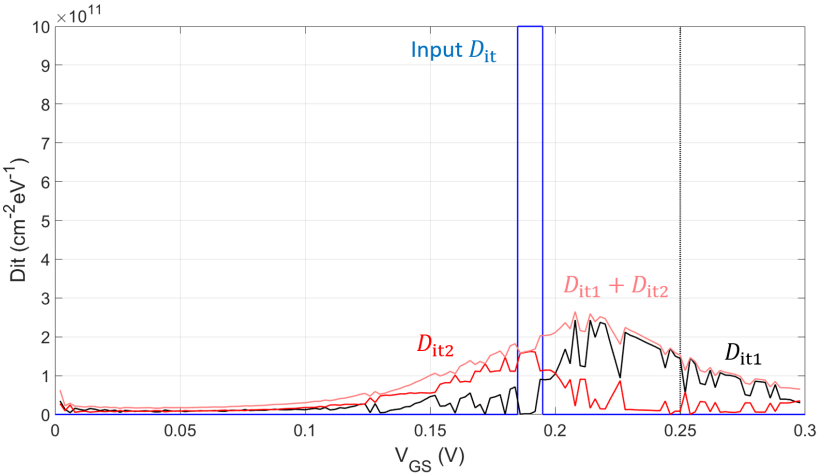
We also applied a δ-peak-like input trap profile (with the same magnitude and range as used for figure 5.18) to only the front interface, with no traps at the back interface. Then, the maximum front and back interface trap densities are $D_{\text{it1}} = 1.1 \cdot 10^{11}$ cm^{-2}eV^{-1} and $D_{\text{it2}} = 4.5 \cdot 10^{10}$ cm^{-2}eV^{-1}. The corrected front and back interface trap density integrals are $\int D_{\text{it1}} = 6.0 \cdot 10^{9}$ cm^{-2} and $\int D_{\text{it2}} = 2.5 \cdot 10^{9}$ cm^{-2}.

So, applying a δ-peak-like input trap profile to both interfaces or to only the front interface results qualitatively in the same "smeared out" trap profile. We note two interesting aspects of the curves: 1) the maximum of the total extracted interface trap density is shifted with respect to the input profile and 2) the extracted trap profile is "smeared out". For the first observation we need to investigate whether equation 2.6 is correct for asymmetric devices. We calculated the input profile from the input energy range, so in case the equation used for this is incorrect and the actual input profile is shifted to the right, there might not be a difference at all. A further investigation regarding this was not performed in this work. The second observation can partially be explained by thermal spread, which has a characteristic width of ≈ 25 mV. However, the bumps observed in figure 5.18 seem to be larger than the range explained by thermal spread. This could be further investigated by taking e.g. δ-like-input profiles at different energy locations and with different widths.

Thus, extracting a peak in the interface trap density is difficult. A "smeared out" trap density is obtained for both the front and back interface. The area under the curve is the same for the total input trap density as for the total extracted trap density, so we can determine the total trap density. The ratio between the maximum values or the integrals of the interface trap densities is different for a symmetric



(a)



(b)

Figure 5.18: (a) Subthreshold swing as a function of the gate-source voltage for $k = 0.9, 0.9250.95, 0.975, 1, 1.025, 1.05, 1.075$ and 1.1. Results shown for TCAD simulations (asymmetric DGFET) and the analytical model as fitted to the TCAD results. A δ-peak-like input interface trap density profile of $D_{\text{it}} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} within the energy range of $E - E_{\text{V}} = 0.745$ to 0.755 eV and $D_{\text{it}} = 0$ cm^{-2}eV^{-1} for all other energies is used in TCAD. (b) Corresponding trap density of the front (black) and back (red) interfaces, as well as the total interface trap density $D_{\text{it1}} + D_{\text{it2}}$ (pink). The input trap density profile is shown (solid blue line) and the valid range ($0 < V_{\text{GS}} < 0.25$ V) is indicated (vertical dotted black line).

trap profile and an asymmetric front interface trap profile. However, the difference between the two is so small that we cannot distinguish between the interfaces for the δ-peak-like interface trap density profiles. Furthermore, we observe an error in determining the energy of the traps. That is, the input and extracted profiles are shifted. Further research is needed to determine the reason for the mentioned inaccuracies.

5.2.4 Conclusion TCAD simulations

The TCAD simulations as obtained using Silvaco Atlas (with Deckbuild) have been compared to the analytical model, and to the separate contributions to the subthreshold swing of the analytical model. We showed that the analytical model matches the TCAD simulations well for a symmetric or asymmetric

DGFET, for all subthreshold swing contributions. Still, some small discrepancies were obtained and explained. We found that the subthreshold swing was slightly higher at $k = 1$ than expected due to short-channel effects. These same effects are expected to result in the observed small offset between the transverse field contribution to the subtreshold swing from TCAD as compared to the analytical model. Additionally, this offset changes for increasing the BOX layer thickness. It was demonstrated that the apparent conduction band edge observed for the electrostatics is not due to a chosen model, the drain-source voltage or a length-dependent effect. We expect that the apparent conduction band edge is caused by the inversion charge carriers, which are neglected in the model. The effect of the depletion capacitance were shown and the effect of a field-dependent mobility was demonstrated. For the latter, we encountered an error in the CVT model for simulations where the sign of the transverse field changes.

We compared the influence of traps for the analytical model and for TCAD simulations, and we found that an error is obtained for low gate-source voltages due to the discrete trap implementation used for this study. This limits the valid interface trap density extraction range. Then, the trap density was extracted from the two interfaces separately by fitting the analytical model to the TCAD data. We showed the lower limit of this extraction method, as well as the results for extracting traps for a symmetric and asymmetric input trap profile. Finally, we demonstrated how a δ-peak-like trap profile could not be extracted accurately, as was also reported for a symmetric (FinFET) device [20]. The total trap density could be extracted, but the interface at which the traps reside could not be determined accurately. Also, the extracted profiles clearly indicated an unexplained shift in energy of the input and extracted trap profiles with respect to each other.

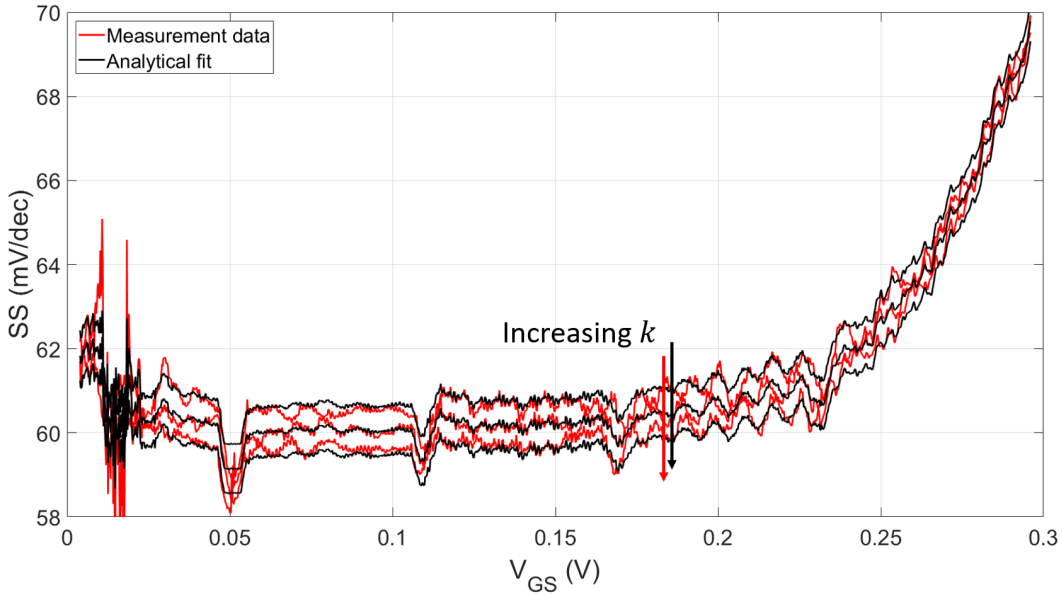
5.2.5 Extracting interface traps from measurements with the analytical model

We tested the analytical model by fitting it against TCAD results as if it were measurements in order to validate the analytical model. The goal was to use the analytical model as a "fitting tool" with which to fit the measurement results. We would like to end this study by fitting the analytical model to some actual measurement data. We show these results here, and not in the measurement chapter, since this better fits the story line of this report.

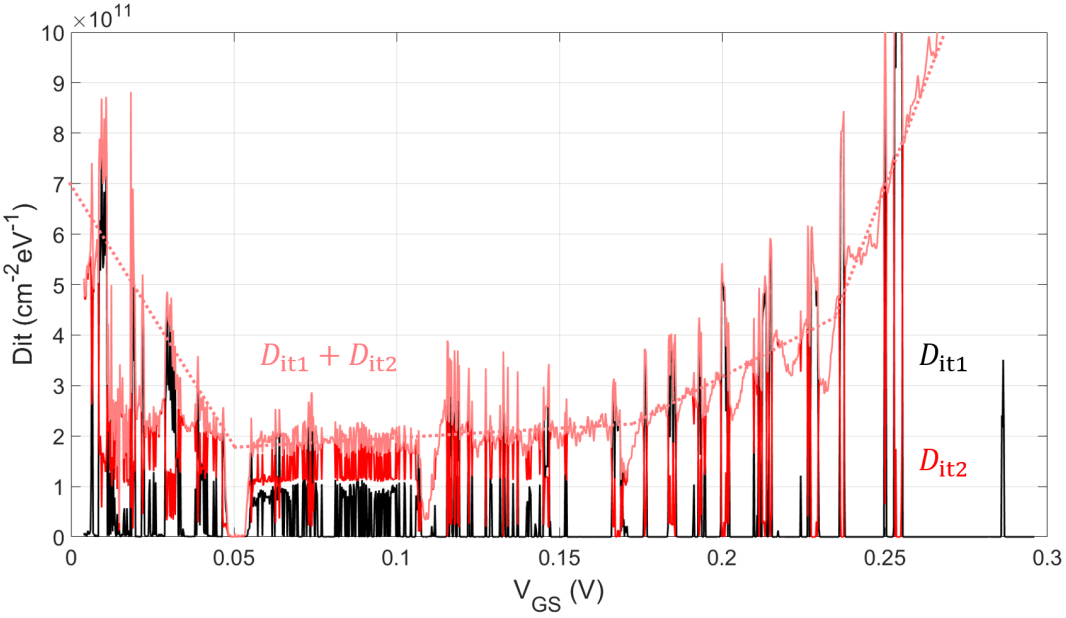
We show the fitted subthreshold swing for measurements together with the extracted trap density at the front and bottom interface in figure 5.19. In more detail, figure 5.19(a) shows the subthreshold swing as a function of the gate-source voltage for $k = 0.9, 1$ and 1.1, and figure 5.19(b) shows the corresponding interface trap profiles.

The obtained total interface trap density, $D_{\text{it1}} + D_{\text{it2}}$ (pink), corresponds well to the values obtained using the simplified k-sweep method (chapter 3) and the BSIM compact model (chapter 4). This extended analytical model can thus be used to extract the total interface trap density.

The measurement data is much noisier than the TCAD data previously shown, even with using the regression analysis. If we do not use this regression analysis or if we use a smaller regression window (which we would need to do in case we e.g. take a higher ΔV_{GS}) the results become even noisier. Therefore, the fitted analytical model results also look noisy. As a result, the extracted trap density of the back interface takes values that vary by at least $1 \cdot 10^{11}$ cm^{2}eV^{-1}, within a small gate-source voltage interval. The values of the front interface trap density vary even more. Therefore, the analytical model as it is cannot be used to extract the trap density from the front and back interfaces separately.



(a)



(b)

Figure 5.19: (a) Subthreshold swing as a function of the gate-source voltage for $k = 0.9, 1$ and 1.1 for measurements and for the analytical model as fitted to the measurement results. (b) Corresponding trap density of the front (black) and back (red) interfaces, as well as the total interface trap density $D_{\text{it1}} + D_{\text{it2}}$ (pink). A manually added trend line is shown for the total interface trap density (dotted pink line).

Chapter 6

Discussion & Future Research

The accuracy of the used extraction methods is discussed. Then, improvements to the TCAD decks are discussed, followed by the shortcomings of the analytical model, as well as possible model extensions for future research. Finally, we describe TCAD simulations that could be performed to validate some assumptions or hypotheses.

6.1 Accuracy of used methods

Several interface trap density extraction methods were used throughout this work. First, in the measurement chapter (3) we used the simplified k-sweep method (section 2.7) to attribute all interface traps to one of the two interfaces. Then, in the Compact Model Simulation chapter (4) we compared the BSIM simulation results to the measurement data. Finally, we then fitted the complete analytical model to TCAD simulations. As discussed, the first two methods can only be used to extract an averaged or total interface trap density, where we cannot distinguish between the top and bottom interface. The method of fitting the analytical model to the (TCAD) data can be used to distinguish between the interfaces, but the method does not seem to be applicable to measurement data. One of the main concerns is that no accurate prediction of the accuracy of all of these methods was given.

Accuracy of k-sweep method

For the simplified k-sweep method the authors in [21] indicated that the technique was sensitive to interface trap capacitance values as low as 1 nF/cm^2 (for devices with $t_{ox2} = 400$ nm). This effectively assumes an accuracy in extracting k_0 of approximately 0.1. For our devices ($t_{ox2} = 20$ nm) this would mean that the accuracy is around 20 nF/cm^2, which corresponds to an interface trap density extraction accuracy of $1 \cdot 10^{11}$ cm^{-2}eV^{-1}. Since we expect (and measured) values in this order of magnitude, the theoretical limit of this simplified k-sweep method has to be investigated in order to ensure that the extracted interface trap densities are valid. Also, the accuracy could then be improved upon by e.g. improving the accuracy of the k_0-extraction.

Accuracy of compact modeling simulations

The accuracy of the compact model simulations is difficult to assess. It depends on how well the compact model fits the measurement data and therefore this is hard to determine. For example, the description of the interface trap capacitance in BSIM is some averaged value, which might already give some error. Also, depletion is not accounted for in the model such that directly fitting the compact model curve to the measurement curve results in some depletion-related accuracy error. This is because the influence of back interface traps and depletion effects is similar, as was described and investigated in the TCAD

simulations chapter (5, section 5.2.2). Thus, better understanding the accuracy of the compact model extraction method is required in order to validate the results.

Accuracy of complete analytical model

The analytical model was fitted against TCAD simulation data. The goals was to validate whether the analytical model would be used for trap extraction of both interfaces separately and simultaneously. We determined the lower limit of accuracy (with simple symmetric or asymmetric DGFET decks) to be around $1 \cdot 10^{10}$ cm^{-2}eV^{-1}. However, it would be useful to determine the accuracy of the analytical model with respect to several parameters analytically, i.e. we would like to determine the theoretical accuracy of the analytical model. For example, we could determine the influence of temperature, a drain current measurement error, a transconductance extraction error and oxide thickness fluctuations, by deriving the error propagation of these parameters as performed in [23].

6.2 TCAD simulation improvements

Quantum-mechanical confinement

We tested the influence of the Hansch and Van Dort TCAD models to incorporate some Quantum-Mechanical confinement effects, and found that the results were not significantly different (for $k = 1$) as compared to the TCAD simulation results without these models. We only tested this for $k = 1$ and for the symmetric DGFET deck. Firstly, the results with and without these QM-models might become (significantly) different in case a transverse field is present across the body. Therefore, testing the effects for $k \neq 1$ is recommended. Secondly, the effects have to be tested for an asymmetric deck. Finally, it might be better to implement and test the density gradient model to account for QM confinement effects, as done by J. van der Steen [11]. This model then has to be tested for the same conditions as described for the Hansch and Van Dort models.

Interface trap implementation

We implemented the interface traps in TCAD using the *INTTRAP* statement. With this statement, discrete interface traps can be implemented at specific energies. Implementing the traps for multiple energies then results in a quasi-continuous trap distribution. As mentioned, the discrete implementation of interface traps has some known disadvantages [50]. The TCAD trap implementation could be improved by using a C-interpreter to define a continuous trap profile.

Field-dependent mobility

We implemented the CVT (field-dependent mobility) model in TCAD (section 5.2.1). It was found that the CVT model cannot cope with a sign change in transverse field, which occurs for TCAD simulations with the SOIFET deck. The reason for this was a combination between the workfunction difference and the k-sweep method. An improved TCAD model is needed to accurately describe the transverse field behaviour in thin-film devices around a transverse field of 0 V/cm. For this work it would be beneficial if also the effects of strain on the mobility could then be implemented in this model.

6.3 Analytical model extensions

Depletion effects

The effects of n-well depletion were examined (section 5.2.1) and it was concluded that the effect is similar to increasing the BOX layer thickness. Depletion effects could therefore be accounted for (in a first-order

approximation) by simply fitting the analytical model to the TCAD simulation results with t_{ox2} as fitting parameter. This way, the additional depletion oxide thickness, $t_{dep} = t_{ox2,0} - t_{ox2,well}$, can be obtained as a function of N_{well}. Then, we can use N_{well} as input parameter for the analytical model to account for (first-order) depletion effects. If a more accurate and more complete depletion model is desired, equations 2.62 and 2.63 can be implemented in the analytical model and tuned with TCAD simulations for several N_{well}- and k-values.

Field-dependent mobility

The effects of incorporating a field-dependent mobility were examined (section 5.2.1) by using the CVT model in TCAD. We concluded that the analytical model cannot describe the subthreshold behaviour in case the mobility depends on the transverse field. It would therefore be useful to incorporate the transverse field in the analytical model. However, the CVT model cannot cope with a sign change in transverse field (see section 6.2). An improved model is thus needed to the describe the effects of a (transverse) field-dependent mobility. This model can then be incorporated in the analytical model as explained in section 2.10. Additionally the effects of strain on the mobility have to be investigated in more detail. In case the mobility increase is field-dependent, we have to add this effect to the analytical model. In case (mainly) a constant increase in mobility results, the effect of strain on the mobility is not important for extracting interface traps. Then, we do not have to add this to the model.

Looking at the situation from a different perspective, we can also attempt to measure the mobility as a function of the gate-source voltage for several k-values. This way, we can check if the mobility in our FDSOI devices is significantly influenced by the transverse field. If this is not the case, assuming a constant mobility might still be valid.

Short channel effects

We attributed the offset between the analytical model and the TCAD results for the transverse field contribution ($\delta\psi_{sx}$, see section 5.2.1) to short channel effects. We have not validated this with TCAD simulations for devices with a longer channel, e.g. $L = 5$ μm. First of all, these simulations have to be performed in order to validate our findings. Secondly, in case we indeed find that SCE results in the discussed offset, the analytical model can be corrected for this. As a first-order approximation, we can simply add a constant by e.g. taking a higher value for u_T (as was also discussed in section 5.2.1).

Inversion charge

The difference between the analytical model for the electrostatics and the TCAD results were attributed to the inversion charge in the channel. We tested all other parameters that could result in the discussed trend, and expect that this trend results from the neglected inversion charge in the channel. However, we have not actually performed tests where the inversion charge is monitored, such that we did not fully validate our conclusion. Therefore, additional tests could be performed to establish if the discussed discrepancy between the analytical model and the TCAD results for the electrostatics is indeed inversion charge-related. In case it is, the inversion charge can be investigated and the behaviour can be added to the analytical model.

Interface between n-well and BOX layer

In the entire derivation for the electrostatics of an FDSOI device we only considered the FOX/channel and BOX/channel interfaces. However, the BOX/n-well interface is also of importance and might contain interface traps just as well as the other two interfaces. We therefore recommend adding this interface to the analytical model. It has to be noted that extracting the trap density of three interface simultaneously where the trap densities have to be distinguishable would be difficult. Therefore, it is advisable to assume

that the trap densities at the BOX/channel and BOX/n-well interfaces are the same. Although this is not necessarily true due to the different fabrication techniques for both interfaces, the assumption that the mentioned two interfaces are similar in trap profile as compared to the FOX/channel interface seems reasonable, considering that the BOX/channel and BOX/n-well interfaces contain the same materials.

6.4 TCAD simulation tests

Extracting interface traps as a function of energy

In this work we described that the trap density is desired as a function of energy for both interfaces separately. We showed results where the interface trap density is obtained as a function of the gate-source voltage. The translation between the gate-source voltage and energy is theoretically described (equation 2.6) and changes in this translation due to QM-effects and a strained channel are discussed (sections 2.11 and 2.12), but the results have not been obtained as a function of energy yet. The validity of equation 2.6 should be investigated for asymmetric devices. The correct relation between the surface potentials and the energy can then be used to obtain the interface trap density as a function of energy.

Effects of strain

We performed simulations for an undoped and unstrained silicon channel. However, strain affects the mobility in the channel (see section 6.3 for the discussion on this statement) and the apparant band gap. The change in the apparent band gap due to strain has only been investigated theoretically in this work. Checking the presented theoretical results (see section 2.12) using e.g. TCAD would give insight in the effects of strain on the energy landscape of an FDSOI device.

Testing the analytical model for workfunction differences

For the comparison between the analytical model and TCAD simulations, we used two cases with respect to the implemented workfunction. In the first case, as used for the DGFET deck, the workfunctions of the front and back gates are the same. Then, the workfunction has no influence on the electrostatics. In the second case, as used for the SOIFET deck, the workfunction of the back gate was compensated with V_{off}. The workfunction difference was not observed in our simulation results due to this. However, we have not tested the analytical model for a situation where a minor but significant workfunction difference is present. Examining this would give insight in the influence of different workfunctions on the obtained results. Effectively, an error in V_{off} is then investigated.

6.5 Extraction using TCAD

We mainly discussed how the analytical model can be improved such that it can be used to extract the interface trap density from measurements. However, after tuning the mobility model for TCAD such that it is correct, we can also simply use TCAD as "fitting tool" for extracting the interface trap density from the measurements. We have verified that this would be valid, since the analytical model explains all basic trends observed in the TCAD simulation results. This way, the (corrected) field-dependent mobility, the depletion effects and the inversion charge carrier contribution are automatically incorporated in the extraction method.

6.6 Extraction using BSIM model

We performed simulations with the BSIM model, where the drain current was obtained as a function of the gate-source voltage for a range of k-values, for several C_{it}. The measurement data was then visually

compared to the BSIM curves such that the interface trap density could be determined. An improvement would be to use a similar fitting algorithm as used for the analytical model with respect to TCAD. In this case, the BSIM model can be used as "fitting tool" instead of the analytical model. At each specific V_{GS} the drain current and transconductance could be obtained for severeal k-values. Then, the C_{it} is changed until the best fit is obtained. The procedure should be repeated for all desired V_{GS}, such that a result similar to figure 5.15 is obtained.

Chapter 7

Conclusion

We described how the interface trap density is theoretically linked to the relation between the surface potentials and gate voltages. The k-sweep method [21] was described (section 2.7) and improvements to this k-sweep method were explained (section 2.10), thus resulting in the improved k-sweep method. With these methods, the interface trap density can theoretically be extracted from the subthreshold swing, hence from the drain current as a function of the gate-source voltage. We studied whether or not these interface trap extraction methods can be used to accurately extract the interface trap density from asymmetric DGFET devices in practice.

For the measurements the drain current was obtained as a function of the gate-source voltage with $\Delta V_{\mathrm{GS}} = 0.2$ mV. From this, the subthreshold swing can be extracted using a regression analysis as described in [20], with a regression window of ≈ 8 mV. In order to demonstrate the (simplified) k-sweep method, we showed how to extract k_0 from measurements for several front to back gate voltage ratios $V_{\mathrm{BGS}}/V_{\mathrm{GS}} = k$. The interface trap capacitance and interface trap density were determined as a function of the gate-source voltage from k_0 for a single interface, assuming the other interface to not contain any traps. Effectively, the total interface trap density can thus be extracted at each gate-source voltage. For this extraction, we assume equal front and back gate workfunctions. Additionally, we assume SCE and depletion effects to be insignificant and we assume the mobility as a function of V_{GS} to be constant at k_0. We concluded that $D_{\mathrm{it1}} \approx 2 \cdot 10^{11}$ cm^{-2}eV^{-1}, away from the band edge (low V_{GS}), considering the back interface to be much better than the front interface.

We obtained simulation results of the drain current as a function of the gate-source voltage for several k-values using the BSIM compact model. The effect of interface traps in the BSIM model are demonstrated and the measured subthreshold swing is compared to that of simulations with several different interface trap capacitance inputs. Simulation results for $C_{\mathrm{it}} = 1 \cdot 10^{-8}$ F/cm^2 fit the measurement subthreshold swing best in the range of $0.05 < V_{\mathrm{GS}} < 0.15$ V. The corresponding interface trap density ($D_{\mathrm{it}} = 6.3 \cdot 10^{10}$ cm^{-2}eV^{-1}) corresponds well to that obtained using the simplified k-sweep method. From the BSIM model only a total (or an averaged) C_{it} or D_{it} can be obtained, just as for the measurements.

The TCAD simulations as obtained using Silvaco Atlas have been compared to an improved k-sweep analytical model, in order to investigate the validity of this new model. We showed that the analytical model matches the TCAD simulations well for a symmetric or asymmetric DGFET. Still, some discrepancies were obtained. We found that the subthreshold swing was slightly higher at $k = 1$ than expected, due to short-channel effects. The effects of back-gate depletion were shown and the effect of a field-dependent mobility was demonstrated. For the latter, we encountered an error in the CVT model for simulations where the sign of the transverse field changes.

For gate voltages in the range of $0.25 < V_{\mathrm{GS}} < 0.3$ V a higher interface trap density is obtained (as compared to low V_{GS}), corresponding to the apparent conduction band edge. This effect is attributed to the increasing number of inversion charge carriers in the channel.

We compared the influence of traps for the analytical model and for TCAD simulations. We found that an error is obtained for low gate-source voltages, due to the implementation of discrete traps in

TCAD as used for this study. This limits the valid interface trap density extraction range and should be improved upon by using a continuous trap implementation method. The trap density was extracted from the two interfaces of a DGFET separately by fitting the analytical model to the TCAD data. We showed the lower limit of this extraction method to be $1 \cdot 10^{10}$ cm^{2}eV^{-1}. Results for extracting traps for a symmetric and asymmetric input trap profile were promising. The total trap density could be extracted, and a first-order indication of the interface at which the traps reside could be given. However, this trap attribution to a specific interface could not be performed accurately. We demonstrated how a δ-peak-like trap profile is "smeared out". This could partially be explained by thermal spreading, but no complete description of the cause was given. Also, the extracted trap profiles clearly indicated an unexplained shift in energy of the input and extracted trap profiles with respect to each other.

From fitting the analytical model to measurement data a noisy interface trap density was obtained, with a total value of $D_{\text{it1}} + D_{\text{it2}} \approx 2 \cdot 10^{11}$ cm^{-2}eV^{-1} in the range of $0.05 < V_{\text{GS}} < 0.2$ V.

We conclude that fitting the BSIM model to the measurement data is the easiest method to accurately extract the total interface trap density. The improved k-sweep-based analytical model can be used to extract the total trap density with a reasonable accuracy, but that the method has to be improved upon in order to correctly attribute traps to specific interfaces. The anlytical model could be improved upon by incorporating the depletion capacitance and improving the relation for the transverse field contribution to the subthreshold swing. Another method would be to incorporate the continuous trap model in TCAD and then simply use TCAD for the trap extraction. This way, the inversion carrier and depletion effects are automatically accounted for.

Appendix A

Debye length and characteristic length

Debye Length

The Debye length defines the electrostatic screening effect of a charge resulting in thermodynamic equilibrium. The potential drops by $1/e$ for each Debye length such that surrounding charges are effectively electrically screened. For a device with a single gate, a fully depleted channel is obtained when the channel thickness is less than about the Debye length [20]:

$$t_{\mathrm{si}} \leq \eta \sqrt{\frac{\varepsilon_{\mathrm{si}} u_{\mathrm{T}}}{qN}}, \tag{A.1}$$

with t_{si} the silicon channel thickness, $\varepsilon_{\mathrm{si}}$ the silicon dielectric constant, q the elementary charge, N the channel doping and with $u_{\mathrm{T}} = k_{\mathrm{B}}T/q$ the thermal voltage, where k_{B} is Boltzmann's constant and T is the temperature. η has a value of 1 for single gate devices and a value of 2 for double gate devices. This is because for a device with two gates, the charge is screened from two sides and half the silicon channel thickness has to be less than about the Debye length. For example, for DG (SG) silicon devices with $N = 10^{15}$ cm^{-3}, the channel thickness should be less than ~ 250 nm (~ 125 nm).

Characteristic length

For a FD FET (such as a FinFET or FDSOI FET) in subthreshold mode operation we obtain [9]:

$$\nabla^2 \psi = -\frac{\rho}{\varepsilon_{\mathrm{si}}} \approx 0, \tag{A.2}$$

where ρ is the volume charge density. The surface potential following from this is

$$\psi_{\mathrm{s}} = \psi_0 \cdot \exp\left(\pm \frac{x}{\lambda}\right), \tag{A.3}$$

with a surface potential minimum ψ_0, x the confinement direction and with the characteristic or natural length given by

$$\lambda = \sqrt{\frac{1}{\eta} \frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}} t_{\mathrm{si}} t_{\mathrm{ox}}}. \tag{A.4}$$

The dielectric constants of silicon and the oxide are $\varepsilon_{\mathrm{si}}$ and $\varepsilon_{\mathrm{ox}}$, respectively, t_{si} and t_{ox} are the silicon and oxide thickness, respectively, and η is 1 for SG and 2 for DG control, i.e. η is the number of gates.

For example, a FinFET with $t_{\mathrm{si}} = 6$ nm and $t_{\mathrm{ox}} = 2$ nm has $\lambda \approx 4$ nm. Calculating the characteristic length of an asymmetric DG device is somewhat more difficult. We specify two oxide thicknesses, t_{ox1} and t_{ox2}, and calculate the characteristic length separately for both thicknesses to check for single gate

control. Also, we calculate the characteristic length for $t_{ox} = t_{ox1} + t_{ox2}$ for double gate control. The single gate control values can thus be viewed as limiting cases for the actual FDSOI characteristic length. We calculate two examples here. 1) Taking $t_{si} = 6$ nm, $t_{ox1} = 1.3$ nm and $t_{ox2} = 20$ nm we arrive at $\lambda_1 \approx 5$ nm and $\lambda_2 \approx 19$ nm for front and back gate control, respectively, and $\lambda \approx 14$ nm for double gate control. 2) Taking $t_{si} = 6$ nm, $t_{ox1} = 3.5$ nm and $t_{ox2} = 20$ nm we arrive at $\lambda_1 \approx 8$ nm and $\lambda_2 \approx 19$ nm for front and back gate control, respectively, and $\lambda \approx 14.5$ nm for double gate control. The first example will be explained to correspond to the SG devices and the second example corresponds to the EG devices.

The FET behaves as a long-channel device when the effective gate length is approximately a decade higher than the characteristic length [9]. For the obtained characteristic length of an FDSOI FET under DG operation the channel length thus has to be larger than ~ 140 nm for SG devices and larger than ~ 145 nm for EG devices.

Appendix B

Single gate sweep for asymmetric device

Back channel subthreshold slope for an asymmetric device

The same method can be applied to obtain the back channel current as a function of the back gate voltage for a fixed front gate voltage. We start with equation 2.19b) and set $V_{\mathrm{G1}} - \Delta\phi_1 = 0$. Taking the derivative with respect to the back gate voltage, the following is found for the ideality factor:

$$m_{2,2} = \frac{dV_{\mathrm{G2}}}{d\psi_{\mathrm{s2}}} = 1 + \frac{C_{\mathrm{it2}}}{C_{\mathrm{ox2}}} + \frac{C_{\mathrm{si}}(C_{\mathrm{ox1}} + C_{\mathrm{it1}})}{C_{\mathrm{ox2}}\left(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right)}, \tag{B.1}$$

which corresponds to the capacitor division scheme shown in figure 2.8b). The influence of the back gate voltage on the front surface potential is given as well:

$$m_{2,1} = \frac{dV_{\mathrm{G2}}}{d\psi_{\mathrm{s1}}} = \frac{\left(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right)\left(C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}}\right) - C_{\mathrm{si}}^2}{C_{\mathrm{si}}C_{\mathrm{ox2}}}. \tag{B.2}$$

The final equation would then be valid as long as the back surface potential is higher than the front surface potential (by at least the thermal voltage u_{T}) and as long as the front channel is not in accumulation. The obtained equation for the back channel subthreshold slope is:

$$\frac{\partial V_{\mathrm{GS2}}}{\partial \log_{10}(I_{\mathrm{D2}})} = u_{\mathrm{T}} \frac{(\psi_{\mathrm{s2}} - \psi_{\mathrm{s1}})(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}})}{(\psi_{\mathrm{s2}} - \psi_{\mathrm{s1}})(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}) - (C_{\mathrm{ox1}} + C_{\mathrm{it1}})} \left(1 + \frac{C_{\mathrm{it2}}}{C_{\mathrm{ox2}}} + \frac{C_{\mathrm{si}}(C_{\mathrm{ox1}} + C_{\mathrm{it1}})}{C_{\mathrm{ox2}}\left(C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}}\right)}\right) \ln(10). \tag{B.3}$$

Since the BOX layer is thicker than the front oxide layer, the correction term C is larger for back channel control (equation B.3) than for front channel control (equation 2.28), assuming similar interface trap densities and an equal surface potential difference. Also, the ideality factor is higher for back channel control, i.e. $m_{2,2} > m_{1,1}$. Therefore, controlling the current with the back gate results in a higher subthreshold swing, in comparison to controlling the current with the front gate.

Simplified model for subthreshold swing

A different model was proposed in [27]. The method is based on using the surface potential relations (equations 2.19) and the relation for the free carrier inversion charge (equation 2.10). The subthreshold swing is defined as $SS = dV_{\mathrm{GS1}}/d\ln\left(Q_{\mathrm{i}}\right) \cdot \ln(10)$ [27]. The exact calculation results in the subthreshold swing without approximations, since the LVP is considered to be exact in the subthreshold regime. However, no closed-form analytical expression can be obtained from this. The assumption that $\Delta\psi \equiv \psi_{\mathrm{s1}} - \psi_{\mathrm{s2}}$ is small is used in order to make a first-order Tayler expansion of the exact result around $\Delta\psi$, which results in:

$$\ln\left(Q_{\mathrm{i}}\right) = \ln\left(q n_{\mathrm{i}} t_{\mathrm{si}}\right) + \frac{\psi_{\mathrm{s1}}}{2u_{\mathrm{T}}} + \frac{\psi_{\mathrm{s2}}}{2u_{\mathrm{T}}}. \tag{B.4}$$

From this, the subthreshold swing can be expressed as:

$$SS = \ln(10) u_{\mathrm{T}} \frac{2}{\frac{\partial \psi_{\mathrm{s1}}}{\partial V_{\mathrm{GS1}}} + \frac{\partial \psi_{\mathrm{s2}}}{\partial V_{\mathrm{GS1}}}} = \ln(10) u_{\mathrm{T}} \left(1 + \frac{C_{\mathrm{it1}}}{C_{\mathrm{ox1}}} + \frac{(2C_{\mathrm{si}} + C_{\mathrm{ox1}} + C_{\mathrm{it1}})(C_{\mathrm{ox2}} + C_{\mathrm{it2}})}{C_{\mathrm{ox1}}(2C_{\mathrm{si}} + C_{\mathrm{ox2}} + C_{\mathrm{it2}})} \right). \tag{B.5}$$

Comparing equations 2.28 and B.5 can be insightful. The first equation contains only the influence of the front surface potential rate of change directly and incorporates the influence of the the back surface potential using a correction factor. The latter equation contains no explicit correction factor (C in equation 2.25) and incorporates the effects of both surface potential rates of change directly. Equation B.5 contains $2C_{\mathrm{si}}$ instead of the used C_{si} in equation 2.28. Except for this, the denominators of the two ideality factors are the same, while the numerator of the last term of equation B.5 contains the front oxide and interface trap capacitances additionally. These additional two terms in equation B.5 should thus result in an approximation of the behaviour described by the correction factor in equation 2.28. It should be mentioned that equation 2.28 shows the correct overall result, but that equation B.5 can be applied directly.

Appendix C

General and k-sweep electrostatics

The relations between the surface potentials ψ and the voltages as given by equations 2.19 are of the form:

$$\psi_{s1} = f_{11}(C) \cdot V_{GS} + f_{21}(C) \cdot V_{BGS} + g_1(\Delta\phi) \tag{C.1a}$$

and

$$\psi_{s2} = f_{12}(C) \cdot V_{GS} + f_{22}(C) \cdot V_{BGS} + g_2(\Delta\phi), \tag{C.1b}$$

with $f(C)$ the functions of all system capacitances that determine the electrostatic coupling and with $g(\Delta\phi)$ the functions that determine the offset voltage due to workfunction differences. We have:

$$f_{11}(C) = \frac{C_{ox1}(C_{si} + C_{ox2} + C_{it2})}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}, \tag{C.2}$$

$$f_{21}(C) = \frac{C_{ox2}C_{si}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}, \tag{C.3}$$

$$f_{12}(C) = \frac{C_{ox1}C_{si}}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}, \tag{C.4}$$

$$f_{22}(C) = \frac{C_{ox2}(C_{si} + C_{ox1} + C_{it1})}{(C_{si} + C_{ox1} + C_{it1})(C_{si} + C_{ox2} + C_{it2}) - C_{si}^2}. \tag{C.5}$$

For extraction of the wanted parameters from the simulations we use the central finite difference theorem. For the ideality factor we obtain:

$$m_{11} = \frac{V_{GS}(i+1) - V_{GS}(i-1)}{\psi_{s1}(i+1) - \psi_{s1}(i-1)} = \frac{dV_{GS}}{d\psi_{s1}}, \tag{C.6}$$

with index i indicating that the i-th numerical value should be used in case of (numerical) simulation or measurement data. Actually, this way we see the ratio between the front gate voltage and front surface potential, while the front surface potential is also influenced by the back gate voltage.

As explained, we use $k \cdot V_{GS} = V_{BGS}$. Thus, when comparing to the electrostatic equations:

$$m_{11} = \left(\frac{d\psi_{s1}}{dV_{GS}} + \frac{d\psi_{s1}}{dV_{BGS}}\frac{dV_{BGS}}{dV_{GS}}\right)^{-1} = (f_{11} + k \cdot f_{21})^{-1}. \tag{C.7}$$

The same way we can define the other m-parameters:

$$m_{21} = \frac{dV_{BGS}}{d\psi_{s1}} = \left(\frac{d\psi_{s1}}{dV_{BGS}} + \frac{d\psi_{s1}}{dV_{GS}}\frac{dV_{GS}}{dV_{BGS}}\right)^{-1} = \left(f_{21} + \frac{f_{11}}{k}\right)^{-1}, \tag{C.8}$$

$$m_{12} = \frac{dV_{GS}}{d\psi_{s2}} = \left(\frac{d\psi_{s2}}{dV_{GS}} + \frac{d\psi_{s2}}{dV_{BGS}} \frac{dV_{BGS}}{dV_{GS}} \right)^{-1} = (f_{12} + k \cdot f_{22})^{-1}, \tag{C.9}$$

$$m_{22} = \frac{dV_{BGS}}{d\psi_{s2}} = \left(\frac{d\psi_{s2}}{dV_{BGS}} + \frac{d\psi_{s2}}{dV_{GS}} \frac{dV_{GS}}{dV_{BGS}} \right)^{-1} = \left(f_{22} + \frac{f_{12}}{k} \right)^{-1}. \tag{C.10}$$

The given relations can be made more readily interpretative. Substitution of $V_{BGS} = k \cdot V_{GS}$ into equations C.1 results in equations 2.29 and these equations are of the form:

$$\psi_{s1} = f_1(C, k) \cdot V_{GS} + g_1(\Delta\phi), \tag{C.11a}$$

$$\psi_{s2} = f_2(C, k) \cdot V_{GS} + g_2(\Delta\phi). \tag{C.11b}$$

Where we then note that $f_1 = f_{11} + k \cdot f_{21}$ and that $f_2 = f_{12} + k \cdot f_{22}$. Thus, $m_{11} = f_1^{-1}$ and $m_{12} = f_2^{-1}$. m_{21} and m_{22} can be obtained by expressing equations C.11 in terms of V_{BGS} and following the same procedure. Rewriting equations 2.19 in the form of equations 2.29 thus allows for the simulation and measurement results to be directly comparable to the analytic results when using the k-sweep method.

Appendix D

Additional Compact Modeling

Drain-source voltage effect

Figure D.1 describes the influence of the drain-source voltage on the subthreshold swing and thus k_0 offset. Figure D.1(a) describes the drain current per unit width as a function of the gate-source voltage for BSIM simulations with two different V_{DS} and for the measurement. The corresponding subthreshold swing (expressed as m_1) is shown in figure D.1(b).

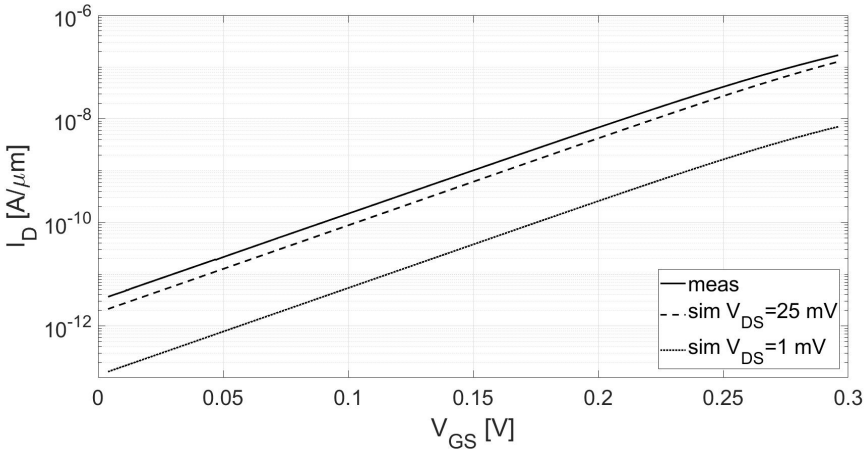
Oxide thickness effect

In figure D.2 the subthreshold swing expressed as m_1 is shown as a function of k at $V_{\mathrm{GS}} = 0.1$ V for the five given cases. At $k = 1$ we see that increasing the front oxide thickness reduces the subthreshold swing and that increasing the buried oxide thickness does not really have an influence. The slope of the subthreshold swing as a function of k clearly improves (becomes more negative) for an increasing front oxide and deteriorates for an increasing buried oxide thickness. Here it can be noted that the subthreshold swing for an increased buried oxide thickness at $k = 1$ is actually improved with respect to the default case. The reason for this is not yet understood and this does not follow from the described electrostatics in this report. Therefore, some additional effect which is unaccounted for in the electrostatics has to result in the mentioned discrepancy.

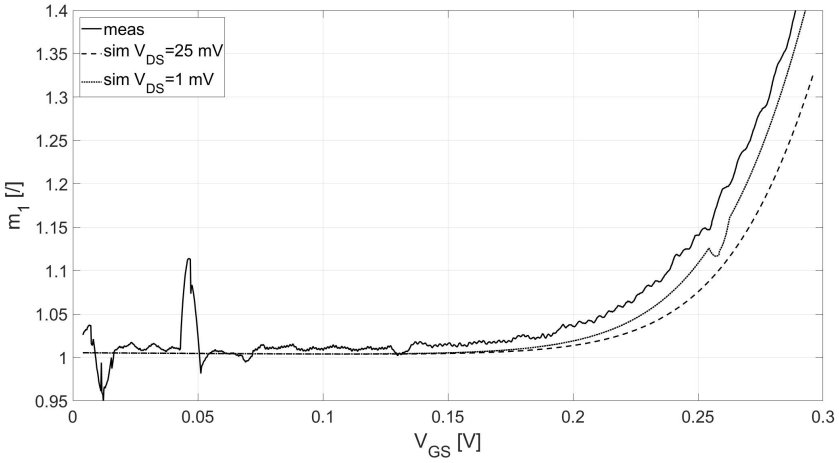
Oxide thickness effect; a symmetric device

Fig D.3 shows a comparison between the asymmetric case with $t_{\mathrm{ox1}}/t_{\mathrm{ox2}} = 1.3/20$ nm (corresponding to the measured devices) and two symmetric cases with $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = t_{\mathrm{ox}}$. For the symmetric cases we have $t_{\mathrm{ox}} = 1.33$ nm and $t_{\mathrm{ox}} = 2.66$ nm.

As the electrostatic total oxide thickness is higher for the asymmetric case, the current is expected to be lower. The current is expected to be better controlled for a thinner oxide with respect to the thicker oxide for the symmetric cases, because channel modulation effects play a smaller role for thinner oxides. Although this effect is expected to be small, a slightly higher current is expected for the symmetric case with thinner oxides. The BSIM simulations in figure D.3(a) show the drain current per unit width as a function of the gate-source voltage. The drain current for the asymmetric case is indeed lower than for the two symmetric cases, but the drain current for the symmetric case with thinner oxides is lower. This does not match with the described electrostatics in this report. Therefore, some additional effect which is unaccounted for in the electrostatics has to result in the mentioned discrepancy.



(a)



(b)

Figure D.1

Nwell doping concentration effect

The effect of the Nwell doping concentration is shown in figure D.4, where the drain current per unit width as a function of the gate source voltage and the corresponding subthreshold swing expressed as m_1 are shown.

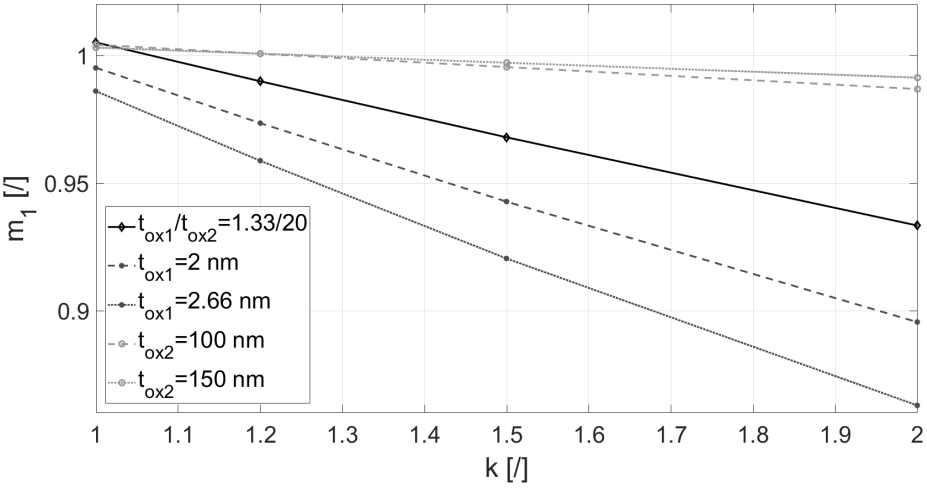
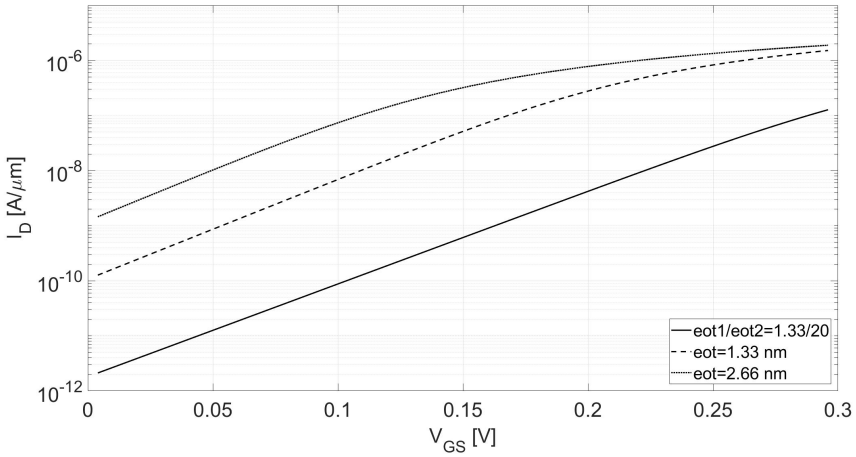
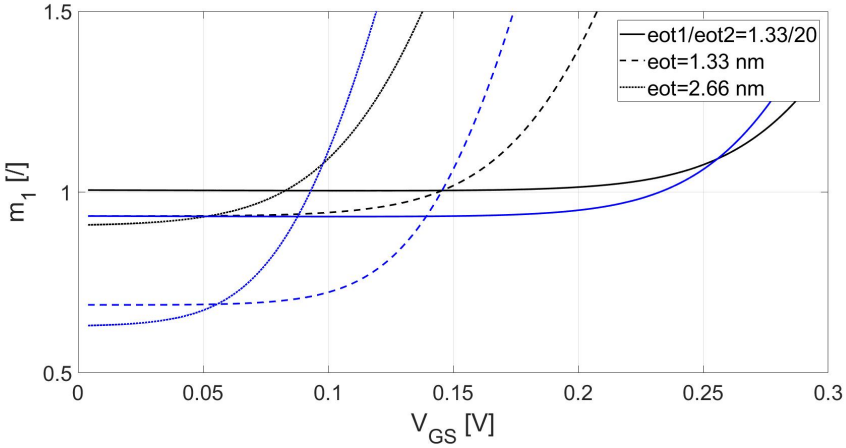


Figure D.2

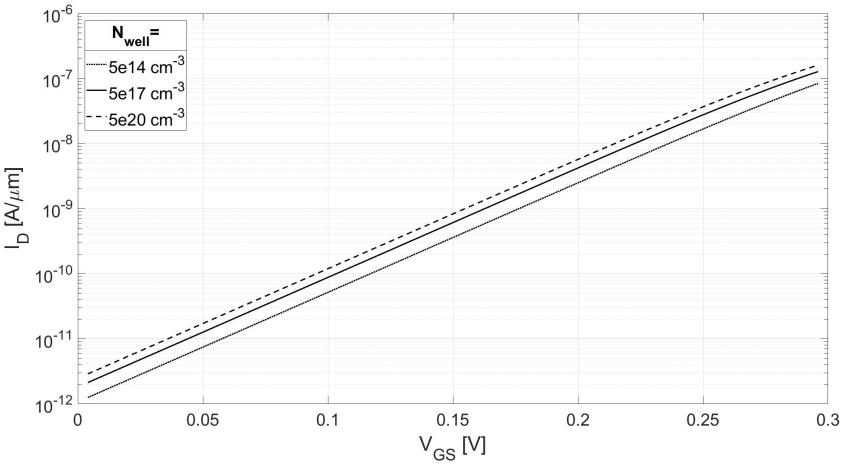


(a)

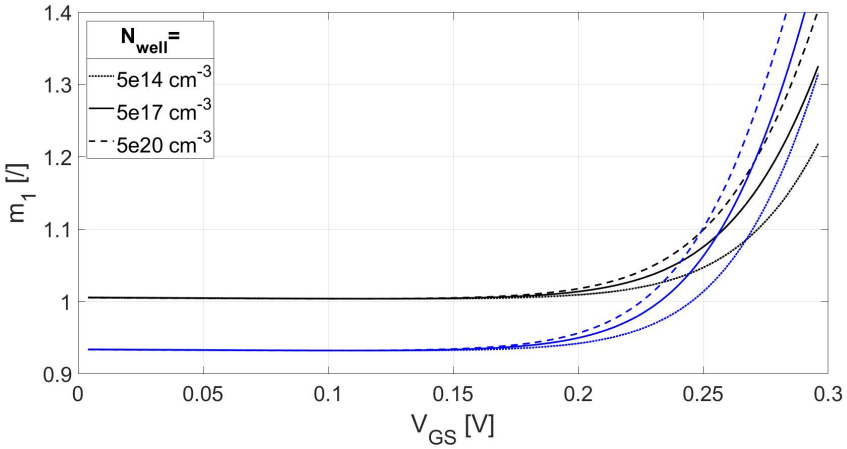


(b)

Figure D.3


N well=
5e14 cm-3
5e17 cm-3
5e20 cm-3
I D [A/μm]
V GS [V]

(a)


N well=
5e14 cm-3
5e17 cm-3
5e20 cm-3
m 1 [/]
V GS [V]

(b)

Figure D.4

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