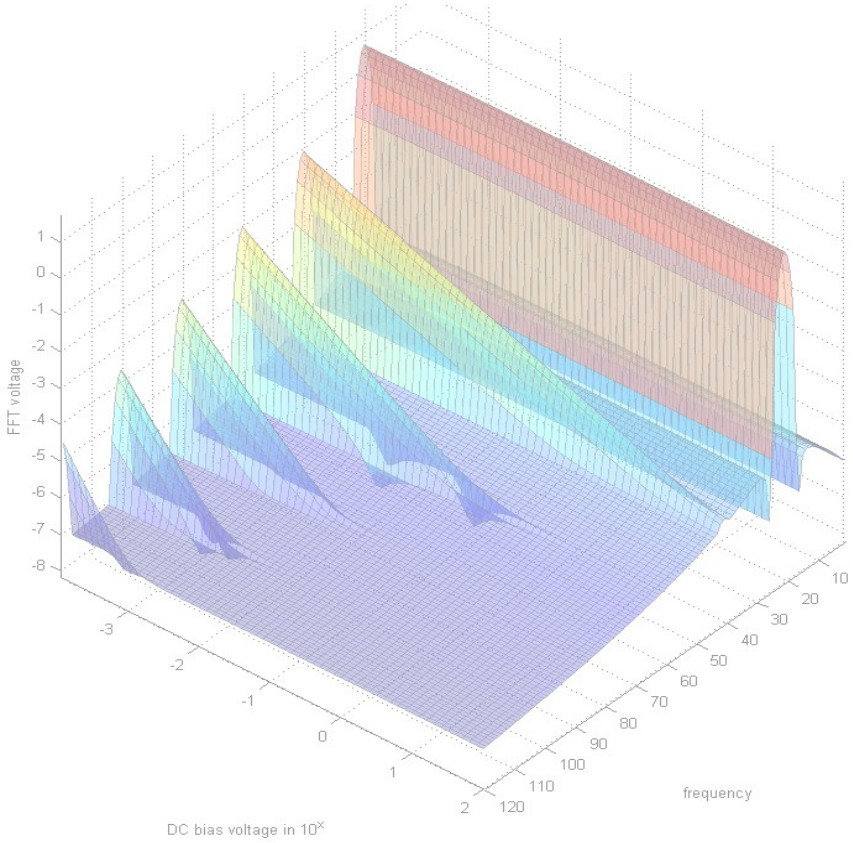
ADC buffer

with fast settling and lower power consumption

Thesis Report



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Abstract

An ADC input Buffer amplifier with load capacitor pre-charging technology is shown in this report. The amplifier has high slew rate (peak slew rate = 180 V/us) and consume less power compare to conventional implementation.

The conventional negative feedback amplifier under certain fixed load conditions, has its slew rate limited by its GBW and/or static power consumption. The GBW / feedback stability / power consumption are correlated, in case the amplifier under certain fixed load conditions. Not one of these three parameter can be made much better, and at same time not affect to other two parameters. In an application such large slew rate and relatively lower signal frequency is employed, a much larger GBW is need to fulfill the slew rate requirements.

Such problem can be solved by combining a fast but not very precise pre-charge amplifier and a slower and much more precise amplifier. The fast amplifier only active in the fast slew period, and the precision amplifier only is active in the tracking period. Both amplifiers can be built with low power consumption in this case.

The speed of the designed fast amplifier is maximized by utilizing one–shot nonlinear feedback technology. The effective gain window only open when the input signal around the determine voltage, such structure make the fast amplifier could operating over the unstable region without having oscillation problem.

The precision amplifier is operating to several MHz range which, stability will be a problem if more than 2 stages is apply in the feedback loop. This amplifier is optimized for highest open loop linearity, which enable use only 2 stages and minimum GBW to meet closed loop distortion requirements. The low GBW results a lower power consumption, as the precision amplifier occupies the most part of total system operating time. The low GBW also results a lower cutoff frequency for the output noise.

The final results of this project (circuit simulation) preview:

P(total) = 396 uW

Setting time (to 99%) = 40 ns;

Setting time (to 90%) = 2 ns;

THD = -59 dB;

SFDR = -65 dB;

Under conditions:

UMC 65nm MOSFET process; C(load) = 1 + 1 pF; Vout(differential, peak to peak) = 2 V; f(input)= 2 MHz; f(sample)= 10 MHz; Vdd= 1.2v

Preface

- What include in this report

This report is the sum of many small research parts through the project. Each research parts has targeted to a particular problem meet during the project. Both theory and technical problem appeared to be encountered (mixed) through the project time line. In this report, theory parts have been present at first and followed by the technical parts. There for, the arrangement of the content of this report may not meet the time sequence of these objects' emerge.

1 Introduction

Digital signal processing has more and more been used in many applications. The overall system performance is limited by the performance of the analog signal chain.

A typical analog signal digitizing chain contains an input driver and an analog to digital convertor (ADC).

Most ADC have a relatively large sample capacitor at the input. This sample capacitor will draw a large current at the sampling moment. Direct connect the signal source to ADC input may results large distortion of the input signal, in case the signal source has a high output impedance. (Figure 1)

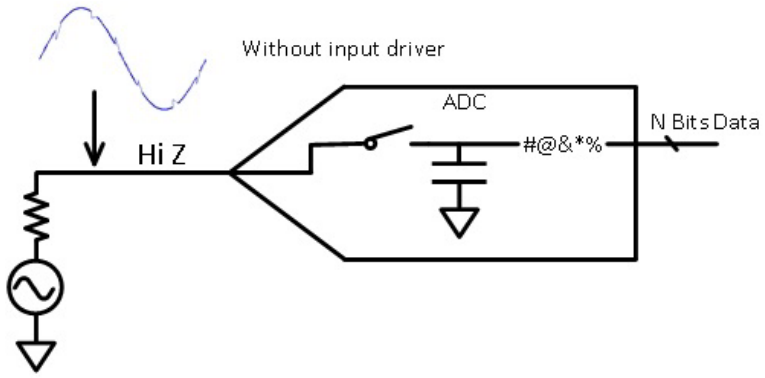


Figure 1 ADC input without driver

This problem can be solved by adding a driver amplifier in front of the ADC (Figure 2). This driver amplifier will give these benefits:

1. Create a low impedance source for the sample and hold circuit.

2. Create a high input impedance for the signal source.

3. Isolate the sampler from the signal source to prevent sampler kickback effects.

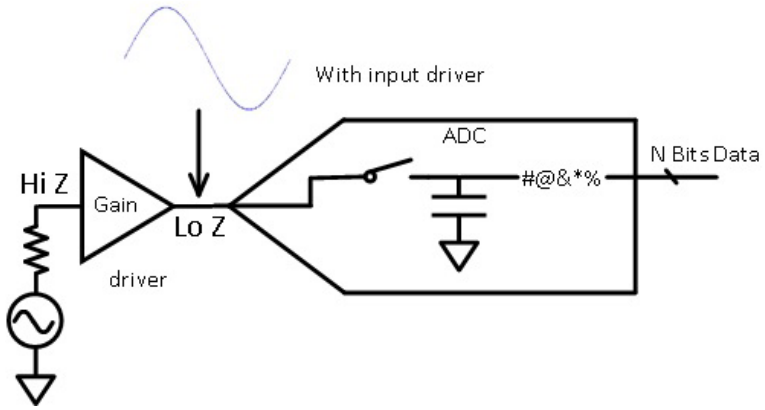


Figure 2 ADC input with driver

In this project, an ADC buffer amplifier will be designed. The major design challenges for such buffer are:

1. Low operating supply voltage. The requirement in this project is 1.2V.

2. Low power consumption. The average power consumption should as low as possible.

3. Rail to rail performance in both input and output.

4. Voltage on sampling capacitor settle to 11-bits precision in 50ns

The requirements for the final outcome are not clearly defined, but the optimization is towards low power consumption.

2 Theoretical limitation of system

In this chapter, the connection between circuit performance and power consumption will be shown. The theory calculation will give benchmark and guidance for circuit performance optimization.

2.1 Power use to charge the sampling capacitor

The driver amplifier must take at least the amount current from power supply to charge the sample capacitor. The amount charge into the capacitor is depend on the signal swing. The charge repeat rate (in 1s) is same as the signal frequency.

Define the sampling capacitor has value C_s . The sampling frequency is f_s.

Consider in the maximum signal swing, the voltage on the sampling capacitor is varying between V_{ss} and V_{dd}.

The average power used to charge the capacitor is:

$$\overline{P_{charging,MAX}} = \overline{I_{charging,MAX}} V_{dd} = \frac{1}{2} f_s (V_{dd} - V_{ss}) C_s V_{dd} \qquad \text{Eq. 1}$$

2.2 Minimum required gm

Minimum amount open loop gain is required to make a feedback system retain the expected closed loop gain. E.g. it require a minimum open loop voltage gain of 9 to make a unity gain buffer has its 90% designed closed loop voltage gain (1 x 90% = 0.9). The minimum power consumption to keep the sufficient amount of open loop gain will be calculated in this part. The amplifier here is an operational transconductance amplifier (OTA) with limited gm Figure 3, and its small signal equivalents Figure 4.

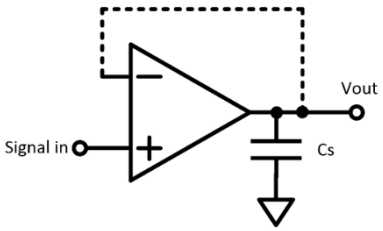


Figure 3 simple feedback amplifier

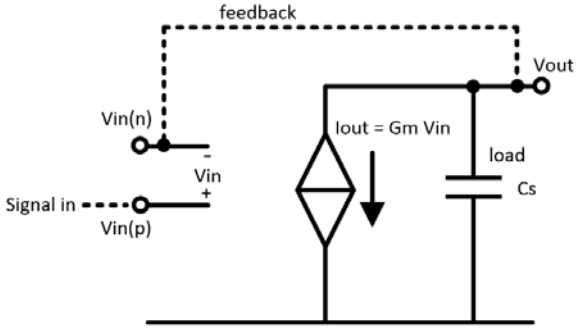


Figure 4 equivalent circuit of simple feedback amplifier

The amplifier (Figure 3) with limited transconductance gm (Figure 4) has its transfer function:

$$I_{out} = gm_{iopamp}(V_{in,p} - V_{in,n}) \quad \text{Eq. 2}$$

To keep the unity gain buffer working properly (closed loop gain ≃ 1), the requirements are:

For the negative feedback loop:

$$V_{out} = \frac{A}{A+1} V_{sig} \quad \text{Eq. 3}$$

And, the open loop gain is:

$$A = gm_{iopamp} Z_{load} \quad \text{Eq. 4}$$

The load impedance is known as:

$$Z_{load} = \frac{1}{j\omega C_s} \quad \text{Eq. 5}$$

The A will decrease with higher signal frequency ω. The gain bandwidth product is:

$$GBW = \frac{gm_{iopamp}}{2\pi C_s} \quad \text{Eq. 6}$$

Known a unity gain buffer has its K time designed closed loop voltage gain at:

$$\left| \frac{A}{A+1} \right| = K \quad \text{Eq. 7}$$

With Eq. 4 Eq. 5 Eq. 7, the minimum gm required to achieve K times voltage gain at frequency ω is:

$$gm_{min} = \frac{C_s K \omega \sqrt{1-K^2}}{1-K^2} \quad \text{Eq. 8}$$

Note, the Eq. 8 is under the condition: the amplifier has a constant gm over all input and output voltage, and no distortion.

The min gm required by amplifier determines the min bias voltage required by the amplifier. The minimum bias current can be calculated based on minimum bias voltage. Minimum theory power consumption so can be computed based on Eq. 8 . (circuit base on Figure 3 Figure 4)

2.3 Open loop gain limitation - by gm

The trans-conductance of a single transistor is limited by the size of that transistor and by its bias conditions. A single transistor amplifier with simple transistor model (Figure 5) is used to analysis the relation between gm and bias current / transistor size. Note, the voltage controlled current source (VCCS) here has variable gm.

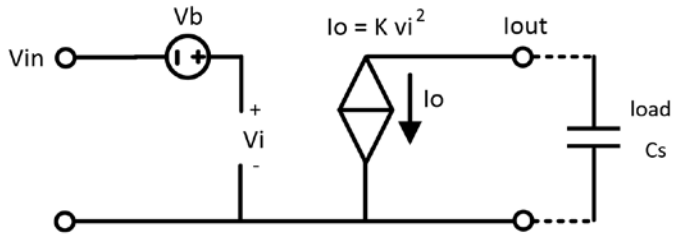


Figure 5 square law model

The gm of a transistor is related to the W/L and I_D. The simplified MOS-transistor (square-law) model known as:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{GT}^2 \qquad \text{Eq. 9}$$

The gm can be found as:

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GT}} \qquad \text{Eq. 10}$$

And, the transistor go into triode region when $V_{DS} < V_{SAT}$:

$$V_{SAT} = V_{GT} \qquad \text{Eq. 11}$$

There are three major way to increase gm (e.g. by factor of 2):

Type of modification	modification	results	
		gm	I_D
Increase W --- hold I_D	4 * W	2 * gm	1 * I_D
Hold W --- increase I_D	4 * I_D	2 * gm	4 * I_D
Parallel transistor (increase both W and I_D)	2 * multiplier	2 * gm	2 * I_D

Table 1 gm vs. W vs. Id

There are different drawback for these modifications.

1.. Increase W --- hold I_D : this way will be the most power saving way to gain gm, but paid with larger area and larger parasitic capacitance. The channel unity width current density is reduced in this case. The GBW will be reduced if the load is dominate by transistor's parasitic capacitor (see 3.3 Optimum unity width current density).

2.. Hold W --- increase I_D : this method consume 4 times power to gain 2 times gm. The drawback is obvious – higher power consumption, higher V_{SAT} , higher channel / junction temperature. The benefits is – higher gm, and (almost) no increase on transistor parasitic capacitors.

3.. Parallel transistor (increase both W and I_D): the output driving capacity is doubled, with two times power consumption. GBW increase when the load is dominate by external capacitor (Cs).

2.4 Open loop gain limitation - by μ

The channel modulation has effect on the voltage gain of transistor. The limited channel length will result in channel modulation. The effective amplification factor (μ) could below 10 for short channel device in sub-micron process (e.g. UMC65nm L=60nm; Vgt=300mV; Vds=1.2V; $\mu = 8.4$). The maximum voltage gain is limited by channel modulation incase $g_m Z_{load} \gg \mu$. The amplification factor μ describes the ratio of the drain current controllability between v_{gs} and v_{ds} .The μ is defined as:

$$\mu = \frac{\frac{\partial i_d}{\partial v_{gs}}}{\frac{\partial i_d}{\partial v_{ds}}} = \frac{\partial\, v_{ds}}{\partial\, v_{gs}} = g_m\, r_d \qquad \text{Eq. 12}$$

$$r_d = common\ source\ drain\ resistance$$

The simplified MOS transistor model including channel modulation is:

$$i_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{GT}^2(1 + \lambda V_{DS}) \qquad \text{Eq. 13}$$

With Eq. 12 Eq. 13, μ (in saturation region) is:

$$\mu = \frac{2(1 + \lambda V_{DS})}{V_{GT}\lambda} \qquad \text{Eq. 14}$$

Clearly from Eq. 14 μ is closely related with λ. At the same time, a transistor operating with lower V_{GT} I_D and higher V_{DS} should has higher μ. (Eq. 13 Eq. 14)

Overall, the analysis shows two basic limitation for the voltage gain. First is the $gm\ z_{load}$ product. Second is the transistor amplification constant μ. The voltage gain will be **dominated by the $gm\ z_{load}$ product** when the **load impedance is relatively low**. Or, **dominate by amplification constant μ** when the **load impedance is high**.

2.5 The relation between distortion / trans-conductance / power consumption

The distortion in this section is modeled with a "quasi large signal" model (Figure 6) which makes the analytical analysis possible. This model consist of a parameterized distortion generator and a small signal gain / feedback block.

The distortion generator creates distortion according to the input signal. An increase of input signal amplitude will increase distortion. Increase input bias voltage will decrease the distortion (Eq. 17; Eq. 18; Eq. 19).

The feedback reduces distortion. Higher loop gain results in lower closed loop distortion (Eq. 15).

The model show in Figure 6 does not contain the true feedback loop. No input signal related loop gain modulation happen, so, only 2nd harmonic exist in the system(Eq. 18). However, in a true circuit, the higher order harmonic is weak compare to the 2nd order harmonic. The loss of higher order harmonic will not strongly affect the THD value.

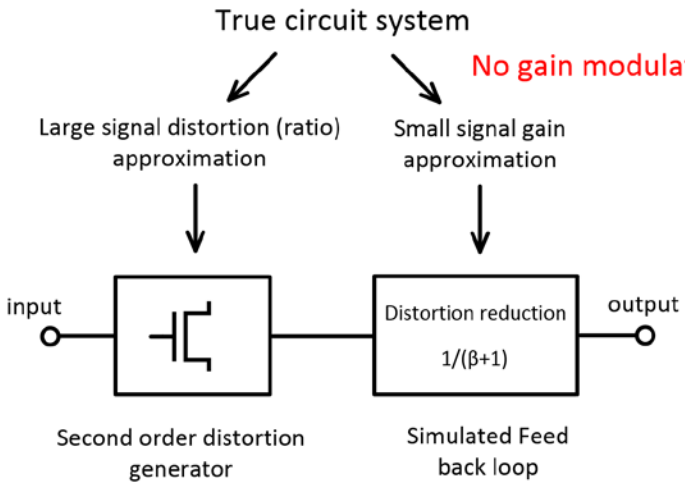


Figure 6 quasi large signal distortion model

The amplifier's distortion will decrease with negative feedback. Sufficient amount of loop gain is required to suppress the distortion under a certain level. The required open loop gain A is (see Appendix 5):

$$\frac{THD_{openLoop}}{THD_{closeLoop}} = A + 1 \qquad \text{Eq. 15}$$

With Eq. 4 : $A = gm_{iopamp} Z_{load}$

Eq. 5 : $Z_{load} = \frac{1}{j\omega C_s}$

Eq. 10 : $g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$

The relation between I_D and THD with normalized load is about:

$$I_D = \frac{\left[\left(\frac{THD_{openLoop}}{THD_{closeLoop}} - 1\right)|Z_{load}|^{-1}\right]^2}{2\mu C_{ox}\frac{W}{L}} \quad \text{Eq. 16}$$

Eq. 16 assume the gm is dominated by the bias current (Eq. 10), the (large) signal has no effect to the gm. The relation between the parameters in Eq. 16 are shown in

THD vs. power	2 * Open loop THD	4 * power
Transistor Width vs. power	2 * W	0.5 * power

Table 2

From Eq. 16, clearly, with a certain closed loop THD need to be achieved, the bias current increases with higher open loop distortion.

Increase transistor W supposed to increase the gm, so, lower bias current is required to keep the required gm.

Let's see the **open loop large signal (square law) model** with Figure 5 :

The input signal is: $V_A \sin x$

Input bias voltage is: V_b

The normalized (real value) load is: Z_L

The output voltage is:

$$V_{out} = 0.5\mu_n C_{ox}\frac{W}{L}Z_L(V_b + V_A \sin x)^2 \quad \text{Eq. 17}$$

Evaluate Eq. 17:

$$V_{out} = 0.5\mu_n C_{ox}\frac{W}{L}Z_L\left({V_b}^2 + 2V_bV_A \sin x + \frac{{V_A}^2 - {V_A}^2\cos 2x}{2}\right) \quad \text{Eq. 18}$$

Open loop THD (voltage ratio) to bias voltage is about :

$$THD_{openloop} = \frac{V_A}{4V_b} \quad \text{Eq. 19}$$

The open loop THD (voltage ratio) to bias current is:

$$THD_{openloop} = \frac{V_A}{4\sqrt{\frac{2I_{d,bias}L}{\mu_n C_{ox}W}}} = \sqrt{\mu_n C_{ox}\frac{W}{L}\frac{{V_A}^2}{32\,I_{d,bias}}} \quad \text{Eq. 20}$$

With Eq. 16 Eq. 19 and Eq. 20 the closed loop distortion and bias current has relation (Appendix 4):

$$I_d = \frac{1}{Z_L^2}\left(\frac{{V_A}^2}{64\,THD_{closeloop}^2 I_d} - \frac{V_A}{4\,THD_{closeloop}\sqrt{2\mu_n C_{ox}\frac{W}{L}I_d}} + \frac{1}{2u_n C_{ox}\frac{W}{L}}\right) \quad \text{Eq. 21}$$

With a known / fixed close loop THD requirement, the relation between transistor size and bias current can be found.

Numerical solution has been used to solve this problem.

The **equation residual error** is defined as the **absolute value** of the numerical difference between left side and right side of the equation.

The scale 10^x has been use in 3D plot. Because it is difficult to accept describe transistor width in dB scale.

The scale 10^x is defined as :

X=1	$10^x = 10$
X=2	$10^x = 100$
X=3	$10^x = 1000$
And so on …	

The equation has its solution when the “equation residual error” is sufficiently low. In other words, the equation has its solution sets right under the “valley” of the plotted surface.

2.5.1 Numerical solution – transistor width vs. bias current

With “numerical sweep solver”, Eq. 21 can be solved :

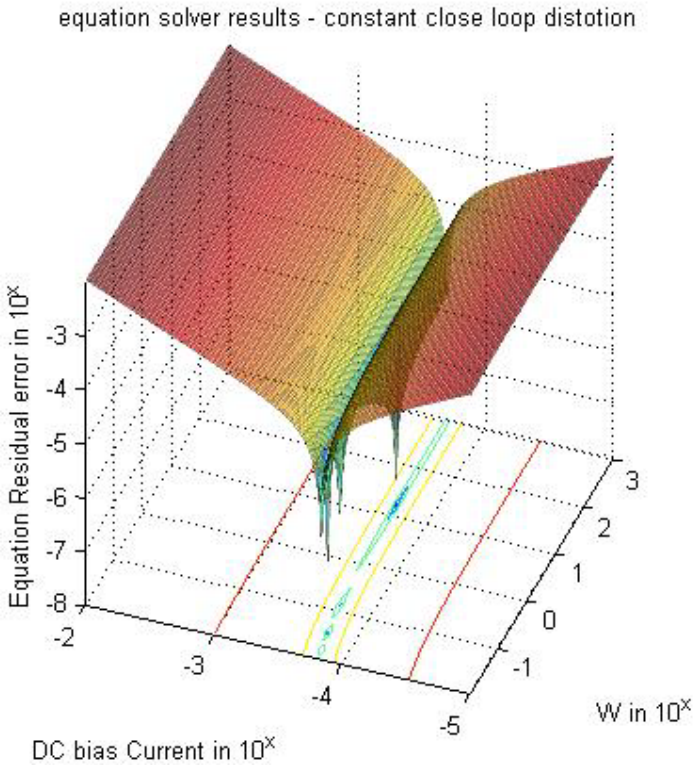


Figure 7 solving residual error vs. bias current vs. transistor width

The results shows, that under condition of a **fixed closed loop THD** (requirement), the **bias current is weakly influenced by the transistor width**. In other words, **hold** the **bias current** and **change** transistor **width**, the **closed loop distortion** remains **almost unchanged** (ignoring transistor parasitic, with simplified model).

The results shows above may looks strange at first look. In fact it is reasonable:

1.. With a larger transistor width and same bias voltage → bias current increase.

$$I_{D,bias}\uparrow = \frac{1}{2}\mu C_{ox}\frac{W\uparrow}{L}V_b^2 \qquad \text{Eq. 22}$$

2.. To keep the bias current unchanged → reduce bias voltage, but the input signal remaining unchanged → open loop distortion increase (Eq. 19).

$$THD_{openloop}\uparrow = \frac{V_A}{4V_b\downarrow}$$

3.. Now, the transistor width increase and bias current unchanged → higher gm → higher loop gain (Eq. 10).

$$g_m\uparrow = \sqrt{2\mu C_{ox}\frac{W\uparrow}{L}I_{D,bias}}$$

Over all, by increase transistor width and hold bias current, results **higher loop gain** and **higher open loop distortion**. The closed loop distortion, by coincidence, remaining unchanged (with the simplified model, in case the transistor parasitic effect are ignored) . For the circuit use actual transistors, the performance should decrease due to the increased parasitic in a larger transistor (in case sufficient Vds is always present on transistor).

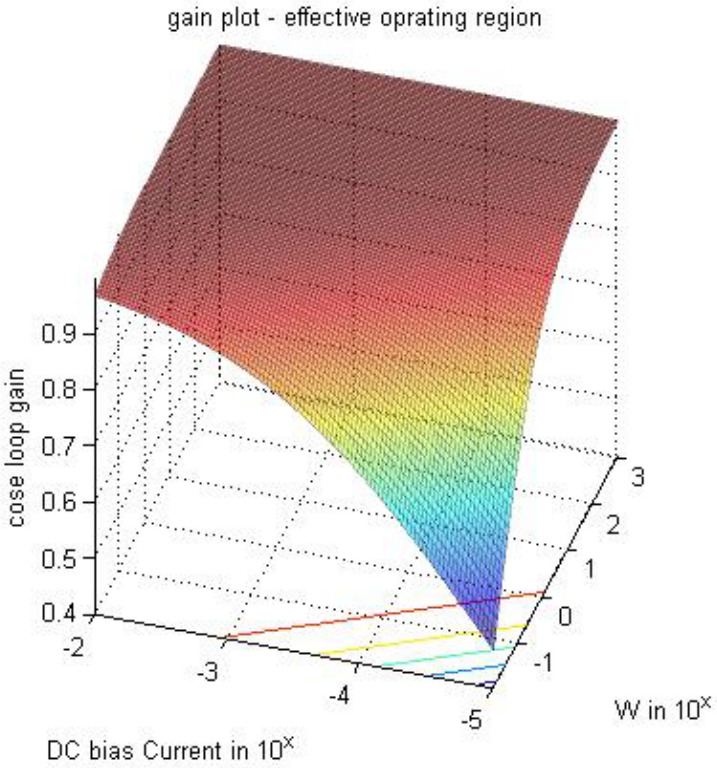


Figure 8 closed loop gain plot

The closed loop gain plot (Figure 8) indicates the useful operating region for different transistor width and bias current setting. Clearly, a closed loop gain close to 1 is only available with sufficient transistor size and bias current.

In case the transistor width does not affect the distortion a lot, the width should adjust to a larger value to give a more stable closed loop gain.

2.5.2 Numerical solution – load capacitor vs. bias current

By sweep the **load capacitor higher**, the **bias current** required to achieve certain closed loop distortion is clearly **increasing**.

In Eq. 16

$$I_D \uparrow = \frac{\left[\left(\frac{THD_{openLoop}}{THD_{closeLoop}} - 1\right)|Z_{load} \downarrow|^{-1}\right]^2}{2\mu C_{ox}\frac{W}{L}}$$

In other word, heavier load require more power to drive it.

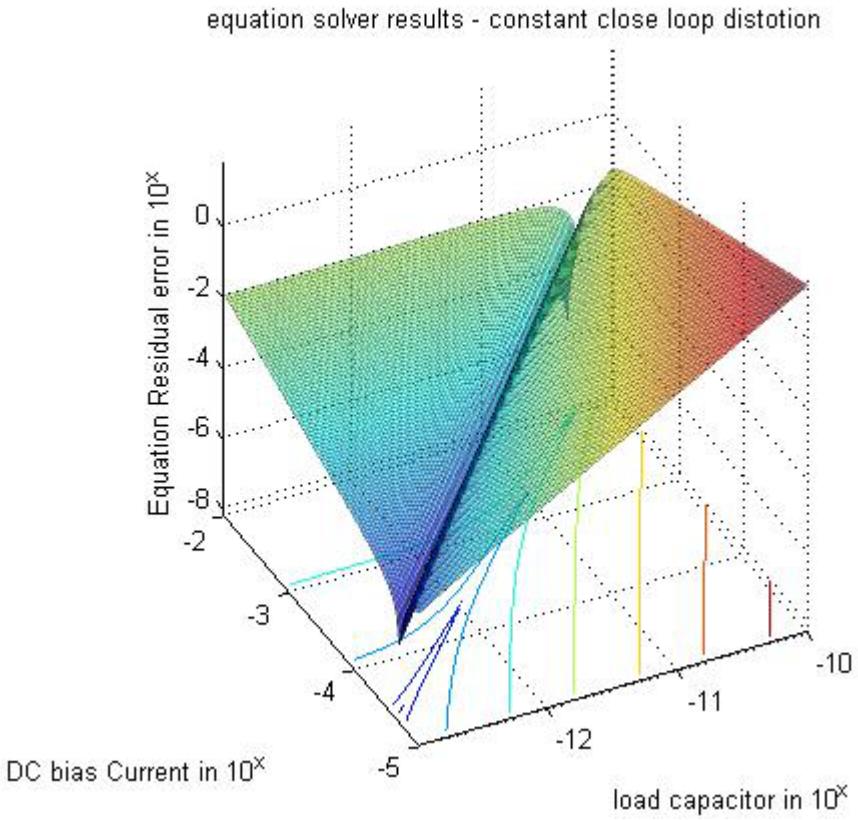


Figure 9 solving residual error vs. bias current vs. load capacitance

2.6 Numerical evaluation of power consumption and distortion

Full numerical method has been used in this part to evaluate the performance of a unity gain buffer. This model has not been simplified. The analytical results are not easy to interpret. However, the 3D plot will give some useful information to the performance evaluation.

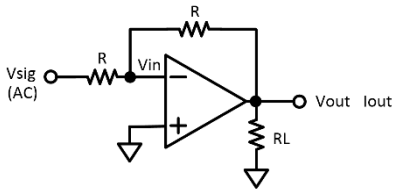


Figure 10 model circuit

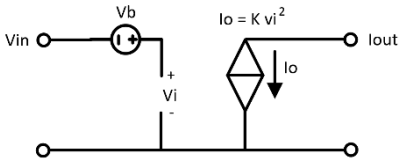


Figure 11 amplifier equivalent circuit

$V_b = bias\ voltage$

The circuit is modeled with Eq. 23.

$$\begin{cases} \dfrac{V_{out} - V_{in}}{R} + \dfrac{V_{sig} - V_{in}}{R} = 0 \\ K(V_{in} + V_b)^2 + \dfrac{V_{in} - V_{out}}{R} + \dfrac{0 - V_{out}}{R_L} = 0 \end{cases} \qquad \text{Eq. 23}$$

Solve Eq. 23 (for V_{out}) get:

$$V_{out} = -\frac{2\sqrt{RR_L + R^2 + \frac{R_L^2}{4} - KRR_L^2V_b - 2KR^2R_LV_b - KRR_L^2V_{sig} - KR^2R_LV_{sig}} - R_L - 2R + 2KRR_LV_b + KRR_LV_{sig}}{KRR_L} \qquad \text{Eq. 24}$$

Three types sweep were made from Eq. 24. These results show the performance trends with different variation on circuits parameter. The transistor parasitic effect are not count in this level's model, but the transistor indeed has a large signal model for its voltage to current transfer, so the distortion is purely created by the second order transfer function of the MOSFET.

One issue of square law model is : it do not allow a "reversed current" (Figure 12). Because from Eq. 9:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{GT}^2$$

I_D can never be a negative number. This limited the using of this model only with a positive V_{GT}.

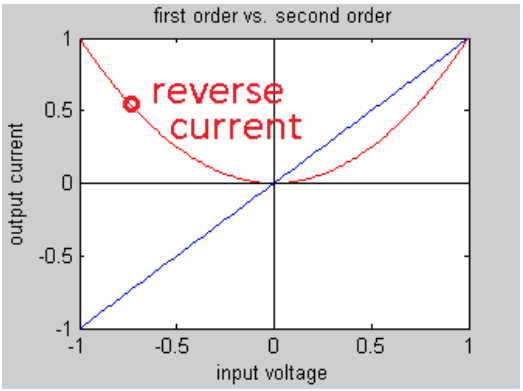


Figure 12 linear model vs. second order model

The second order model (Eq. 9) will not work properly when the signal amplitude larger than the bias voltage V_b. Fortunately, such situation only happen when the open (also closed) loop gain is very low. An additional closed loop gain plot has been added to identify whether the model is in the effective operating region.

2.6.1 Distortion vs. bias current

Figure 13 shows the output spectrum plot. The higher order harmonic clearly roll off faster. The distortion is mainly contribute by the 2nd harmonic. The distortion roll of at -15 dB per 10 times bias current (Figure 14).

Figure 15 shows the closed loop gain, the close loop gain is close to 1, which indicate the circuit operates normally.

The simulation results shows, with a less linear open loop transfer function, higher loop gain (bias current) is required to maintain the required closed loop gain.

E.g. assume use a class AB stage instead of class A stage increase large signal open loop distortion by 15dB, to solve this problem, it require increase bias current 10 times to meet the (original) distortion requirement.

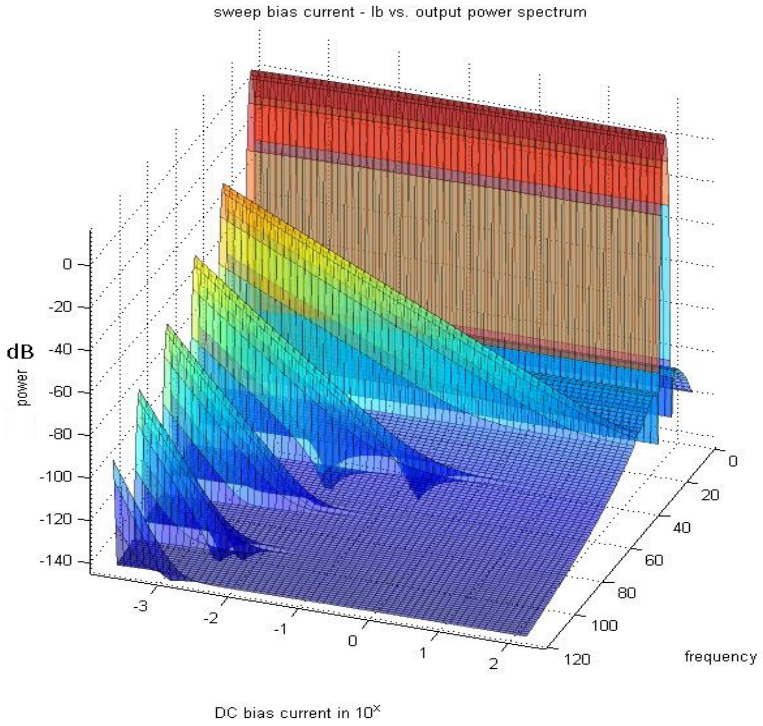


Figure 13 output power spectrum vs. bias current

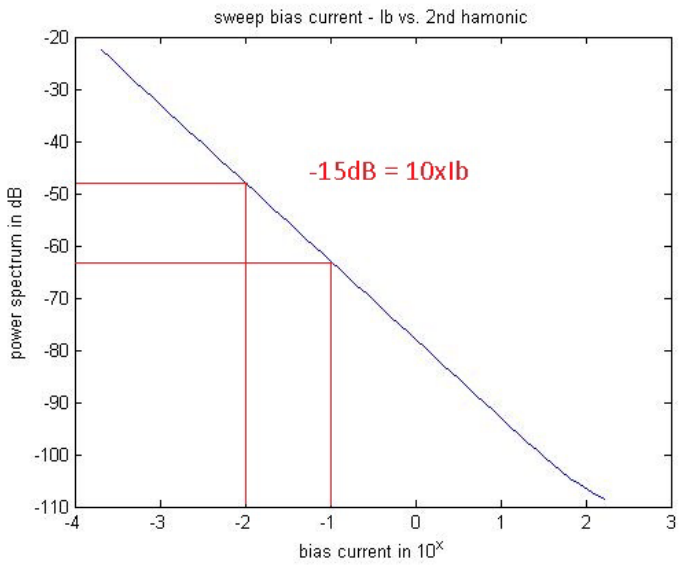


Figure 14 distortion (2nd + 3rd harmonic to fundamental) vs. bias current

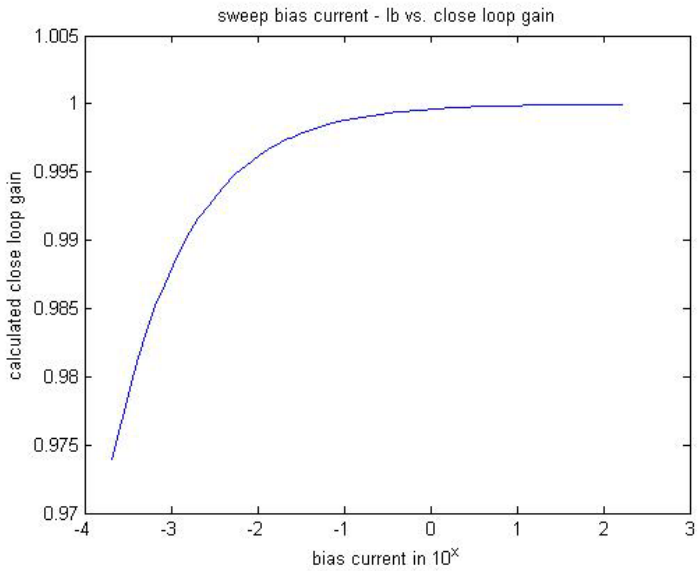


Figure 15 calculated closed loop gain vs. bias current

2.6.2 Distortion vs. input signal voltage

The input signal amplitude has been sweep in this part, with fixed bias condition. In Figure 16, it clearly shows an increasing of all harmonic power with higher input signal amplitude.

The total distortion (2^{nd} + 3^{rd} harmonic) increases about 20 dB for every 10x input signal amplitude. As the total distortion is domain by the second order distortion.

Simulation shows the distortion can be much lower with lower signal voltage swing. The performance improvement in here do not increase power consumption.

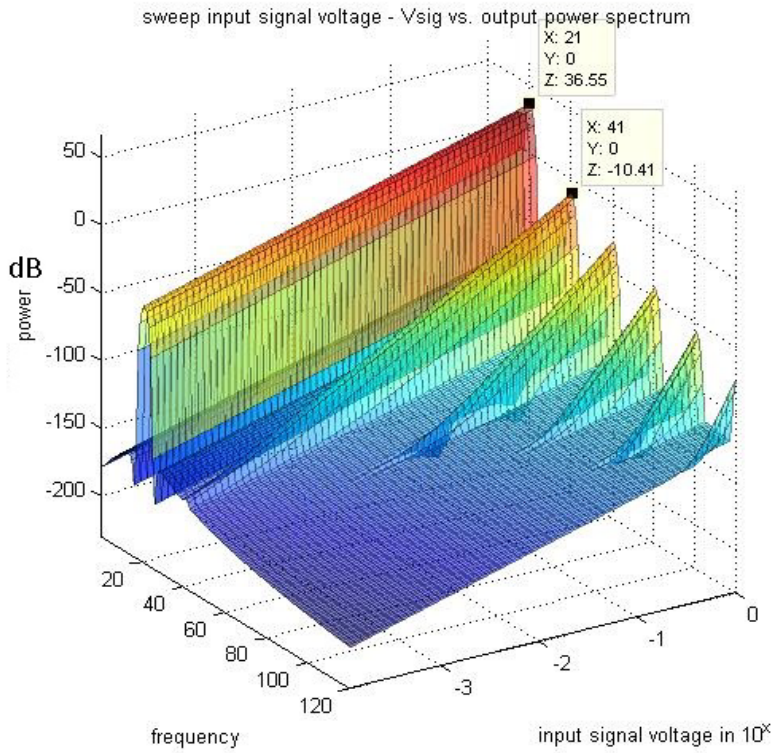


Figure 16 output power spectrum vs. input signal amplitude

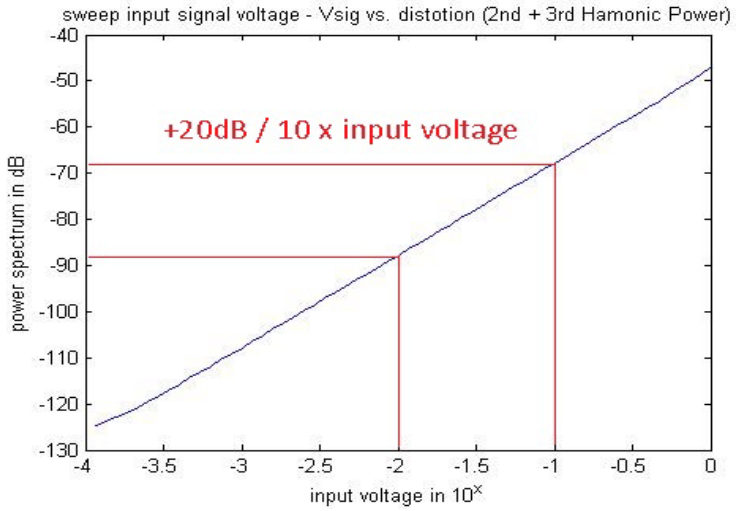


Figure 17 output distortion vs. input signal amplitude

2.6.3 Distortion vs. transistor width with fixed bias current

The transistor width has been sweep in this part, with a fixed bias current for all different transistor width. This part is set to determine whether the re-size of a circuit with fixed power consumption will affect the performance.

Figure 18 (surprised) shows the **distortion increase** with **larger transistor width**. However, the change is not strong as those shows in previous two sweeps. The distortion increase 5 dB every 10x transistor width.

The results in here is a surprise, because increase transistor width will increase the loop gain (Figure 20) which, naturally, will reduce the distortion. But, with a fixed power consumption or bias current, the **bias voltage on transistor gate will decrease**:

$$I_{d,bias} = 0.5\mu_n C_{ox} \frac{W}{L}\uparrow \; V_{gs,bias}^2 \downarrow \qquad \text{Eq. 25}$$

The reduce on gate bias voltage will increase the gate voltage variation (ratio), which equivalent to increase the input signal level. The loop gain variation is link to the gate voltage variation (ratio), and the variation on loop gain generate distortion.

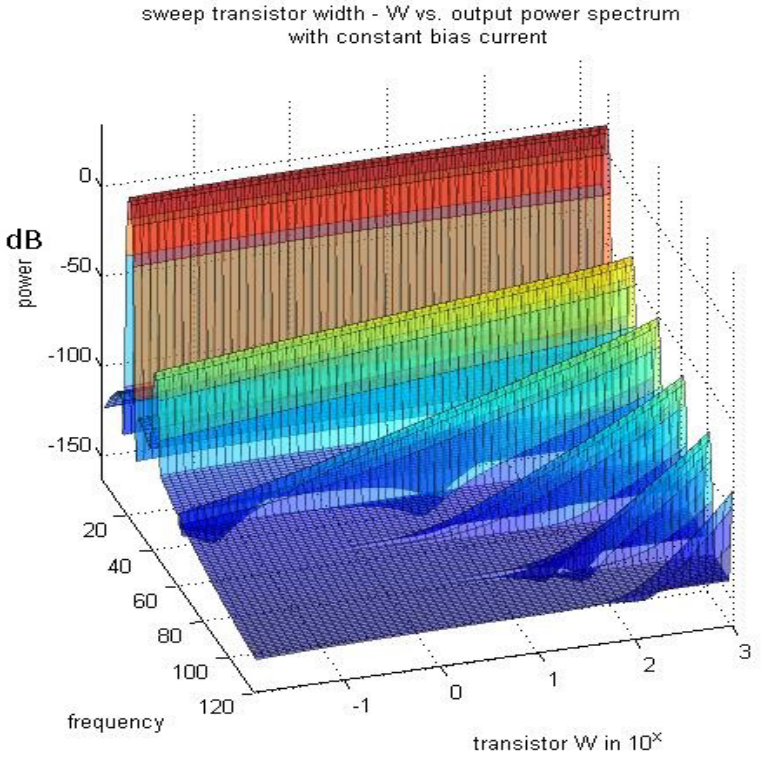


Figure 18 output power spectrum vs. transistor width - with constant bias current

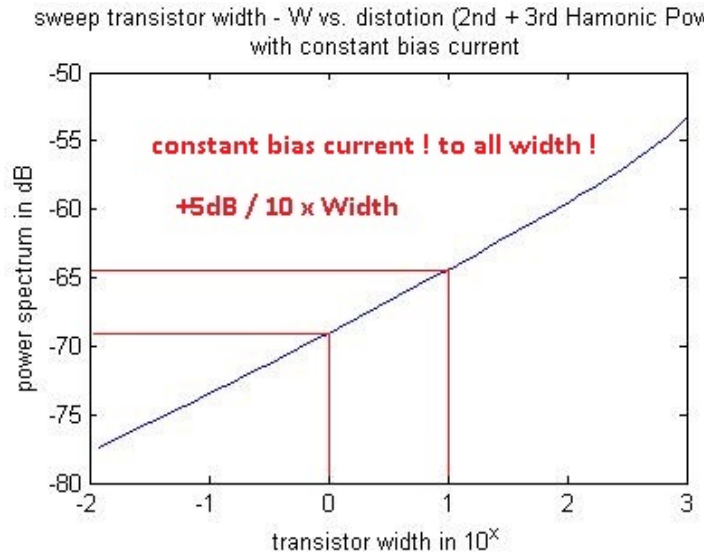


Figure 19 output distortion vs. transistor width - with constant bias current

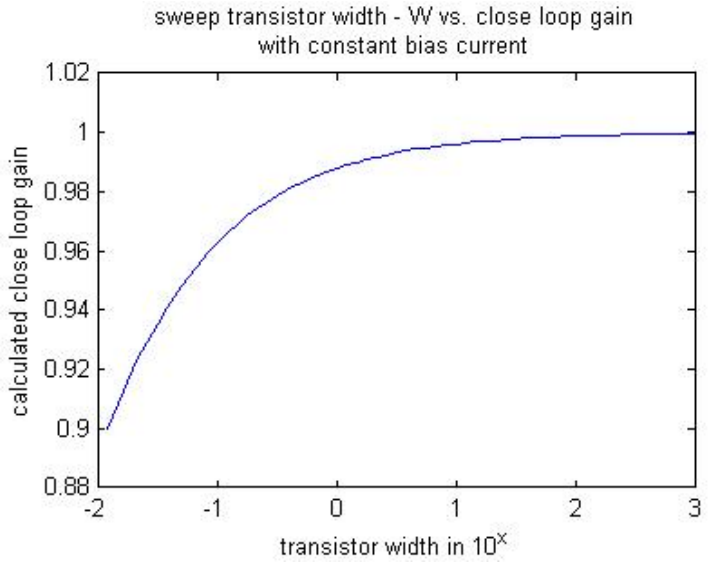


Figure 20 calculated closed loop gain vs. transistor width - with constant bias current

2.6.4 conclusions

The relation between distortion and circuit parameters is show in Table 3.

Relation	ratio
Distortion vs. Bias current	-15 dB per 10 x Ib
Distortion vs. Input signal voltage	-20 dB per 0.1 x Vin
Distortion vs. transistor Width with fixed bias current	-5 dB per 0.1 x W

Table 3 performance cost

The results shows increase bias current and /or decrease input voltage is the most effective way to reduce distortion. The drawback of these modification are obvious – higher power consumption and / or lower signal to noise ratio due to limited signal swing.

The first solution – increase bias current is less possible to fit the requirements of a low power circuit. So, the only solution left is to reduce the amplifier's signal swing and in the same time – the signal swing on sampling capacitor should remain unchanged (near rail to rail).

2.7 Class A output stage Large signal settling time vs. bias current analysis with Ideal linear amplifier

Two scenario have been evaluated in this part: amplifier settling with fixed slew rate, and amplifier settling with fixed output impedance. The amplifier is ideal, with limited slew rate.

Sampling capacitor average charging current is known as:

$$\overline{I_{charge,Cs}} = C_s V_{in,p-p} f_{in} \quad \text{Eq. 26}$$

Note, the average charging current shown here is the worst case prediction which, the voltage on sampling capacitor changing between$V_{dd}$and gnd .

In case the Class A output stage has constant current slewing, and class A amplifier has its bias current equal to the maximum output current. The charging current known as:

$$I_{charging} = C_s \frac{d\, V_{Cs}}{d\, t} \quad \text{Eq. 27}$$

e.g. C_s =1E-12; V_{Cs} =2; t_{charge} =20E-9; the charging current is 1E-4. The bias current of Class A amplifier should higher than **100uA**.

In case the Class A output stage has constant output impedance. The sampling capacitor voltage settled follows $1 - e^{-t/\tau}$. The settling residual is $e^{-t/\tau}$. The residual voltage slew rate is:

$$\frac{d\, e^{-t/\tau}}{d\, t} = -\frac{e^{-\frac{t}{\tau}}}{\tau} \quad \text{Eq. 28}$$

The initial (t=0) residual voltage slew rate is $-\frac{1}{\tau} V_{in}$. The initial charging current is:

$$I_{charge,init} = C_s \frac{1}{\tau} V_{in} \quad \text{Eq. 29}$$

From the requirements, the final setting error should less than 0.5 LSB (the full scare of ADC = 1). So,

$$\frac{2^{-N}}{2} \geq 1\, e^{-t/\tau} \quad \text{Eq. 30}$$

Overall, the initial current can be found as:

$$I_{charge,init} = \frac{ln\left(\frac{2^{-N}}{2}\right) C_s V_{in}}{-t_{charge}} \quad \text{Eq. 31}$$

e.g. C_s =1E-12; V_{Cs} =2; t_{charge} =20E-9; N=11; Initial charge current 8.317E-4. In this case, the Class A amplifier bias current should higher than **831.7uA**.

3 Two stage Operational Amplifier

A typical Operational amplifier consists 3 signal terminals : invert input (in-) / non-invert input (in+) / and output (out). The operational amplifier sense the voltage difference between invert input and non-invert input, amplify this difference, then show this difference by a voltage signal on output terminal. The relation between inputs and output is shown in Eq. 32

$$V_{out} = A_v(V_{in+} - V_{in-}) \qquad \text{Eq. 32}$$

An ideal operational amplifier should have the amplification or gain approaching to infinity.

3.1 Practical limitations of operational amplifier

There are many limitations on a practical operational amplifier. The major limitation are:

- Gain bandwidth product (GBW)

This limitation has been discussed in Eq. 6 and Eq. 42. Practically, transistor has limited gain and internal and external capacitor load. These loads and practices limit the voltage gain of the amplifier. In many case, power consumption cannot be reduced through scale down the transistor size because a large (dominated) external load.

- Slew rate

This limitation has been discussed in Eq. 27 and Eq. 31 for class A output stage. The slew rate also limited by the amplifiers bandwidth and input stage's bias current.

- Input / output voltage swing range

Obvious, transistor could only operating in a certain voltage range. The higher transistor unit width current density will give higher GBW and at same time give higher Vsat. The higher Vsat, the smaller drain voltage could swing through. (see chapter 3.3)

- Input offset

Increase the size of input differential transistor pair will reduce mismatch. This will payed with higher transistor parasitic capacitors.

- Noise

The MOSFET drain current noise is known as:

$$\overline{I_n^2} = 4kT\gamma gm \qquad \text{Eq. 33}$$

And the drain signal current can be:

$$I_{sig}^2 = V_{in}^2 \ gm^2 \qquad \text{Eq. 34}$$

From Eq. 33 Eq. 34, clearly, the signal power grow faster than noise power with higher gm. This indicates higher signal to noise ratio can be achieved with high gm, and higher gm in many case means "burn" more power.

3.2 Small signal stability analysis for typical 2-stage amplifier with miller compensation

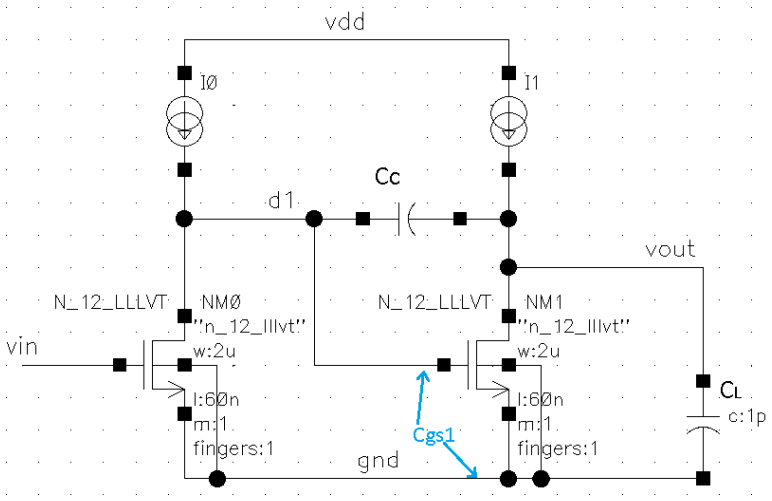


Figure 21 simplified 2-stage amplifier

Figure 21 shows a simplified 2- stage amplifier, one transistor for each stages. The output stage consists one transistor (NM0) and a current source I1. The load C_L here is the sampling capacitor (C0) only. All the gm have positive value.

With KCL on net v_{out} :

$$-gm_1V_{d1} + SC_c(V_{d1} - V_{out}) + SC_L(0 - V_{out}) = 0 \qquad \text{Eq. 35}$$

On net V_{d1} :

$$-gm_0V_{in} + SC_c(V_{out} - V_{d1}) + SC_{gs1}(0 - V_{d1}) = 0 \qquad \text{Eq. 36}$$

Solve Eq. 35 Eq. 36 get open loop transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{(-g_{m0}C_c)\left(S - \frac{g_{m1}}{C_c}\right)}{(C_cC_L + C_{gs1}C_c + C_{gs1}C_L)(S+0)\left(S + \frac{g_{m1}}{C_L + C_{gs1} + C_{gs1}\frac{C_L}{C_c}}\right)} \qquad \text{Eq. 37}$$

Two poles and one zero is shown in Eq. 37 :

$P_1 = 0$,or low frequency, due to μ limitation show in Eq. 14 Eq. 38

$$P_2 = -\frac{g_{m1}}{C_L + C_{gs1} + C_{gs1}\frac{C_L}{C_c}} \qquad \text{Eq. 39}$$

$$Z_1 = \frac{g_{m1}}{C_c} \qquad \text{Eq. 40}$$

From Eq. 39 clearly, the second pole P_2 move to higher frequency with larger compensation capacitor C_c . The drawback of increasing C_c is reduction of the open loop gain bandwidth product. This problem can be solved by increase gm_0 , and the first stage power consumption will increase.

Several facts have been observed with matlab simulation (Appendix).

1.. negative feedback stability requirements. In case the second stage input capacitance (Cgs1) is very small, increase output / input transistor size ratio (gm1/gm0) make loop more stable.

2.. the Cgs1 should well below the compensation capacitor Cc to keep Cc work properly.

3.. the compensation is dominate by ratio of C_c/C_L, sizing M0 and M1 with same ratio do not affect stability a lot. Only GBW increase with larger transistors.

4.. the reasonable value for Cc is 30% of CL, and reasonable value of M1 / M0 transistor width ratio is 3-6.

3.3 Optimum unity width current density for highest small signal gain

The optimum transistor operating condition for the highest small signal gain is evaluated in this chapter. **Transistor's parasitic effect has been take into count.**

With Eq. 10

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_d}$$

And assume drain capacitance has linear relationship with transistor width:

$$C_d = K_{cd,w}\,W \qquad \text{Eq. 41}$$

with Eq. 6, the small signal gain bandwidth Product (GBW) will be:

$$GBW = \frac{gm}{2\pi C_d} = \frac{\sqrt{2\mu C_{ox}\frac{W}{L}I_d}}{2\pi K_{cd,w}W} = \sqrt{\frac{2\mu C_{ox}I_d}{4\pi^2 K_{cd,w}^2\,WL}} = \sqrt{\frac{2\mu C_{ox}}{4\pi^2 K_{cd,w}^2 L}}\sqrt{\frac{I_d}{W}} \qquad \text{Eq. 42}$$

Unity width current density

Clearly, a transistor load by a current source, its **GBW increases** with **higher unity width current density**. Such relation will **hold until** the transistor operating into **triode region**. The small signal GBW curve of a transistor biased at a fixed current can be found with simulation sweep.

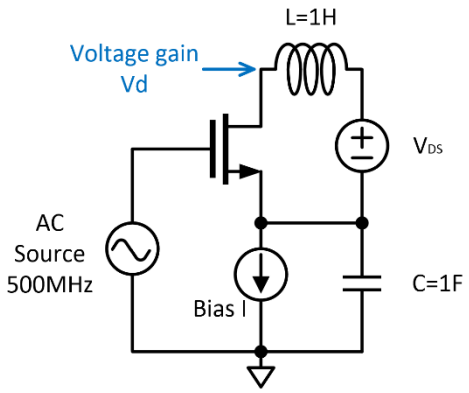


Figure 22 simplified simulation circuit

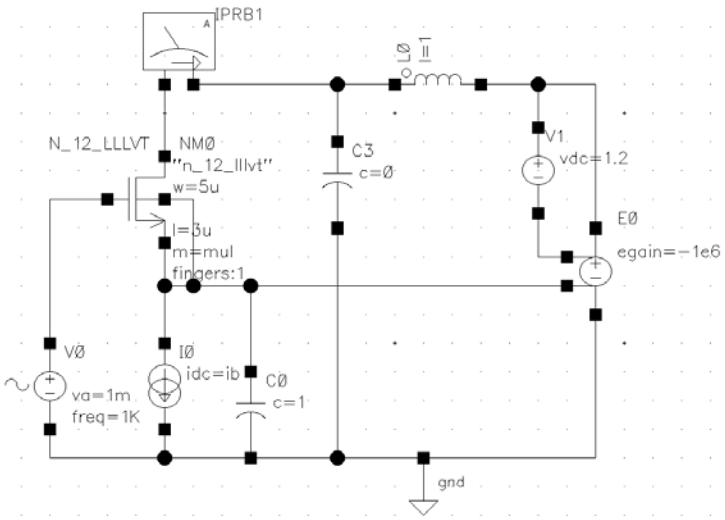


Figure 23 constant bias current / Vds, trans-conductance / bandwidth test circuit

The circuit shown in Figure 23 give transistor a fixed bias current, and regulated Vds. The transistor width is sweep through different values by changing the multiplier during the simulation, and the drain voltage gain is simulated by small signal AC simulation as:

Drain voltage gain G_d or "gain" in Figure 24 :

$$G_{d,v} = \frac{v_{ds}}{v_{gs}} \qquad \text{Eq. 43}$$

The gain peaking is clearly visible in the simulation results (in Figure 24, $V_{DS} = 1.2V, V_{GS} =$ value in plot) .

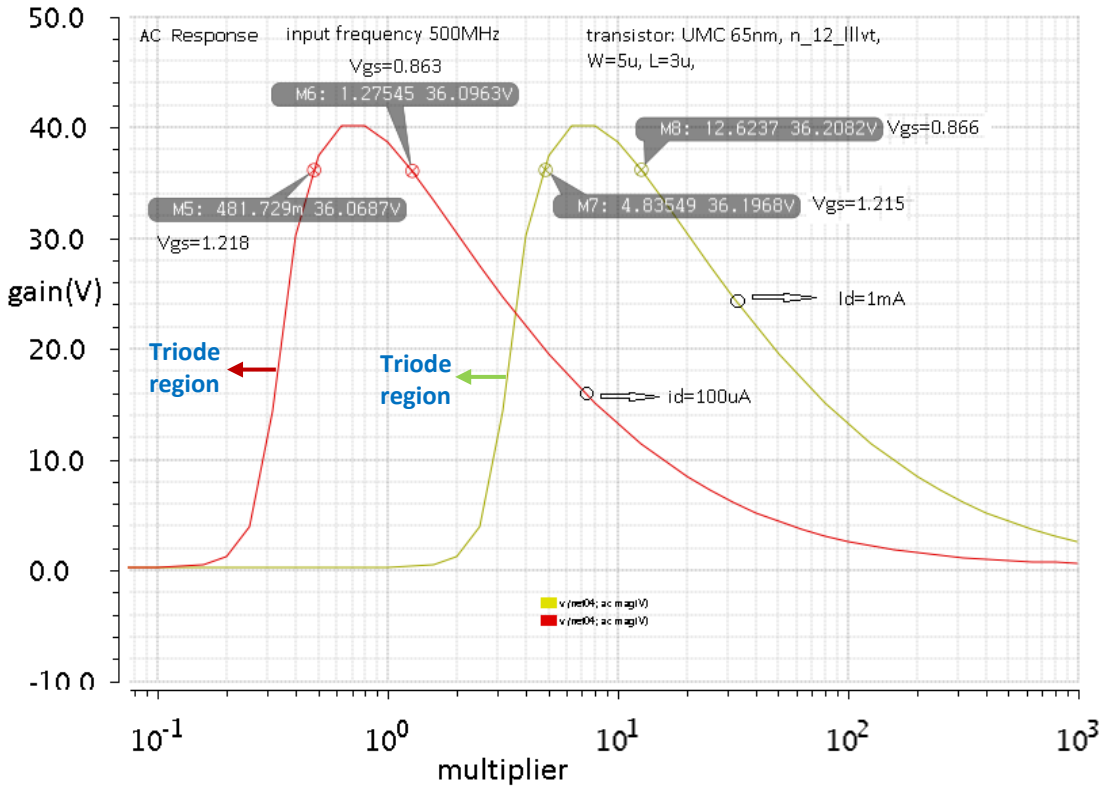


Figure 24 maximum common source drain voltage gain vs. width at fixed bias current

For two stage amplifier, the first stage load is dominate by the C_{gs} of second stage. Typically, the optimum unity width current density reduced when the load capacitance is dominated by external capacitor.

Note, when a transistor work at gain peak, and with a small load capacitance, the operating point of this transistor will be very close to the triode region. The high V_{sat} (or large voltage headroom) made the rail to rail operation of these transistors are not possible.

4 circuit design

In previous chapters, the researches show several different factors will affect the circuit performance. The performance priority are :

Low distortion > Maximize signal swing > Power consumption

Performance (distortion) cost is shown below:

Possible Modification	Cost
Distortion vs. Bias current	-15 dB per 10 x Ib
Distortion vs. Input signal voltage	+20 dB per 10 x Vin
Distortion vs. transistor Width with fixed bias current	+5 dB per 10 x W

Table 4 performance cost

From Table 4, reduce input signal level give best results on reduce distortion, and it do not increase power consumption. The drawback of this method is obvious – either the maximum signal swing is reduced or, the power supply voltage need to be increased. Clearly, both these problem cannot be easily solved with conventional system structure.

4.1 Pre-charging circuit

The proposed solution is show in Figure 25 and Figure 26. The sampling capacitor Cs and offset capacitor has been charged (with control) in phase 1, then linear amplifier taking the tracking process in phase 2.

Such configuration has improved the circuit performance on:

1. Extremely high initial slew rete.
2. Rail to rail voltage swing on sampling capacitor voltage.
3. Lower voltage swing on amplifier output voltage.
4. Fixed amplifier output initial voltage (initial condition) for tracking process.
5. Less power consumption compare to conventional implementation.

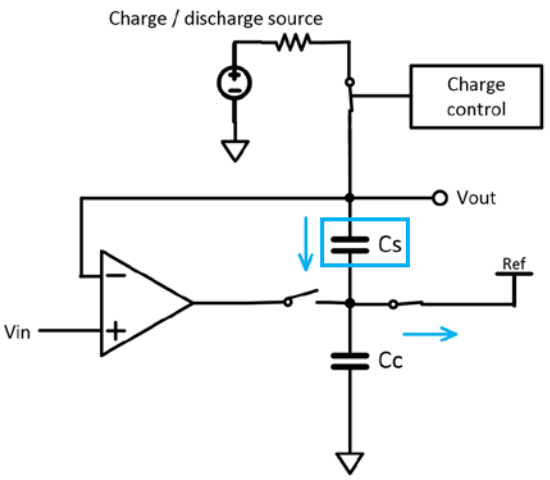


Figure 25 phase 1 --- Pre-charging

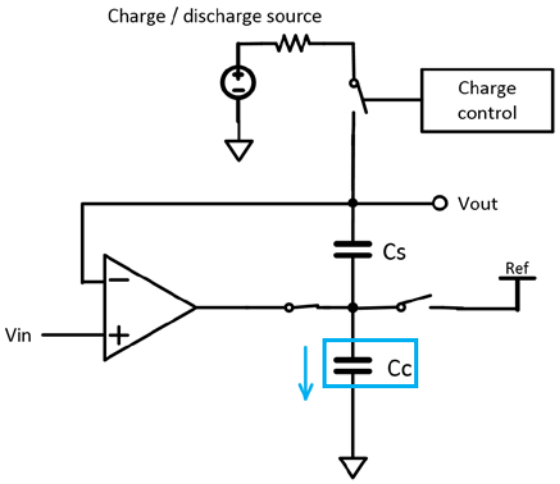


Figure 26 phase 2 --- tracking

4.2 Pre-charging control circuit

The pre-charging control circuit will determine:

- The charging polarity (charge or discharge).
- The moment to stop.

The functional diagram of the charging controller is shown in Figure 27. The first comparator Comp1 enable at first, and will determine the charging polarity by compare the voltage in sampling capacitor Cs and input voltage. The compare result will decide the Cs should be charge or discharge, and the comparator Comp2 cut off polarity. The second comparator enabled after the output of first comparator is stable. It will determine the moment that charging process should been stopped. The switch connect to XOR gate will cutoff at Comp2 zero crossing point.

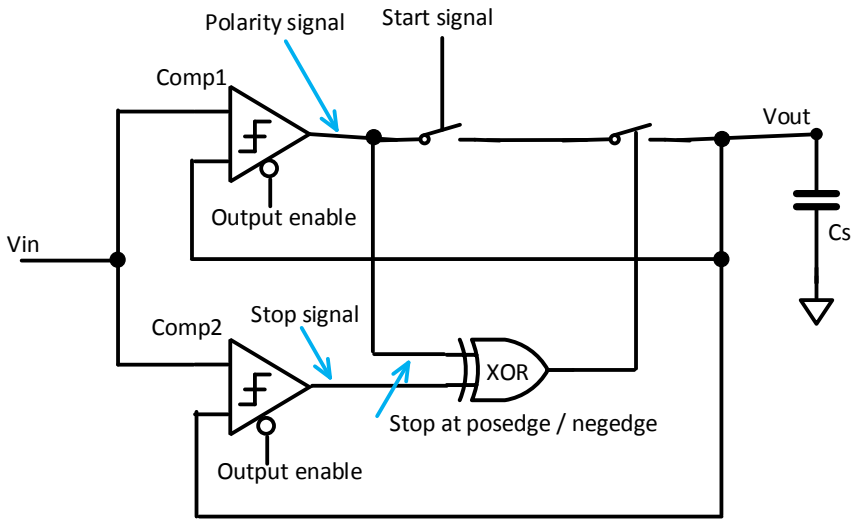


Figure 27 pre-charging / charge controller

4.3 Implementation of charge control

The charge controller consists two major parts. The first part is the charging polarity comparator (function as Comp1). The second part is the stop trigger (function as Comp2).

4.4 Comparator

The comparator here will determine the charging polarity before the charging begin. The input signal is continuously changing during this process. Minimize setting time of the comparator is critical to making the right charge / discharge decisions.

The schematic is shown in Figure 30. This is a CMOS “push-pull” comparator. The CMOS pair has been connect to Vdd and Gnd (via reset switch NM7). Such configuration enable supply high current to CMOS pair at determine period, so the setting time is minimized.

The input differential pair are NM0 NM3. One noticeable problem for this configuration is the reverse leakage through differential pair (see Figure 30). The leakage current at certain input voltage could high as 80% total average operation current of the comparator. To solve this problem, diode connected NM12 NM13 (in Figure 30) is used to prevent the reverse current flow through transistor NM0 or NM3 (in Figure 30).

Noise and mismatch is not the major problem in this circuit, due to it served in a less precision pre-charge circuit.

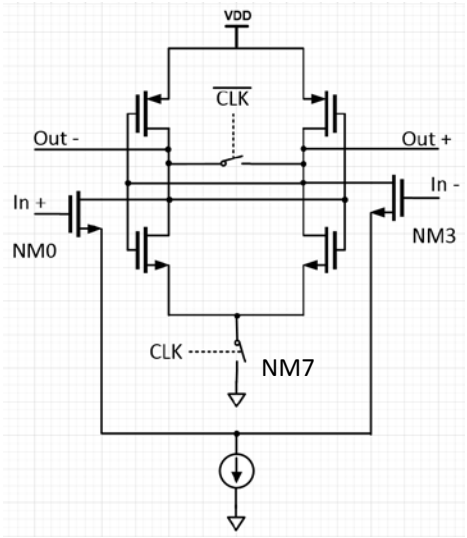


Figure 28 simplified comparator diagram

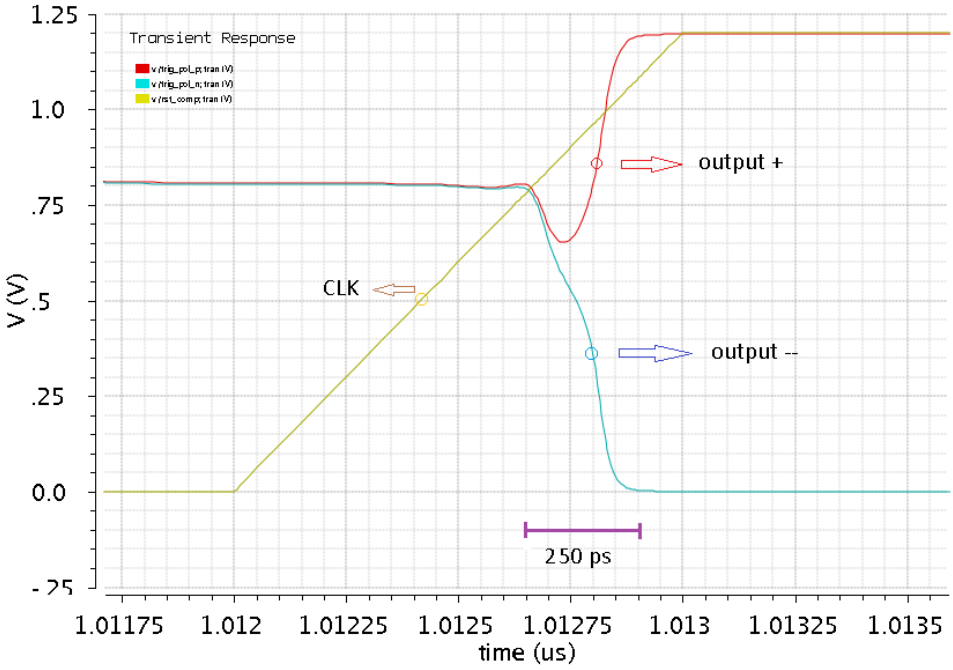


Figure 29 comparator output setting

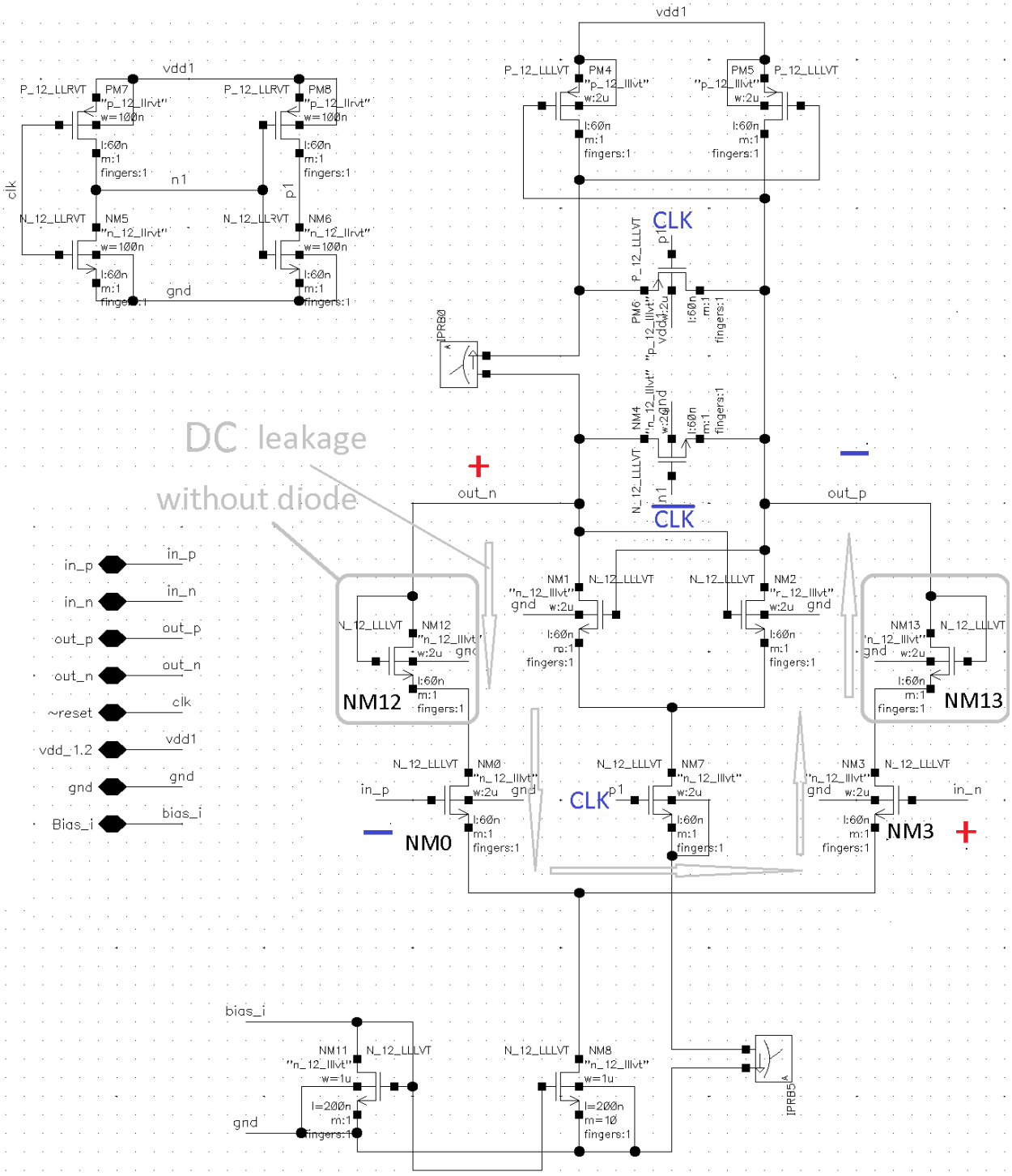


Figure 30 charge control. comparator

4.5 Stop trigger

The core of the trigger circuit is the negative resistor pair consists PM0 and NM2. The negative resistor generated by these two transistors only exist when these transistors are biased, as their drain current higher than the leak current source (PM3 PM2 / NM5 NM6). Once the transistor current over the critical point, both transistor will fully turn on within 1~2 ns. The transistor pair PM0 NM2 practically equivalent to a tunnel diode, which widely be used in oscilloscope trigger system before high performance MOSFET are available.

The differential amplifier / polarity switch in the left part is used to compare the IN+ and IN- voltage, and generate proper (polarity) driving current to negative resistor pair. The polarity switch act as the XOR gate shown in Figure 27.

The trigger is reset by cut off NM4. Transistor switch NM16 also been switch off to keep voltage on net “t_out_n” at Vdd. (Figure 33)

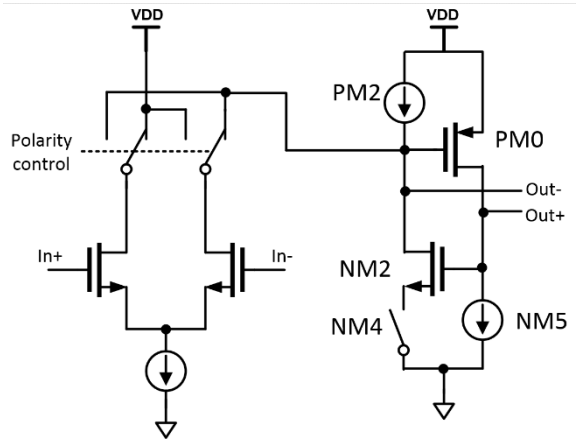


Figure 31 simplified trigger diagram

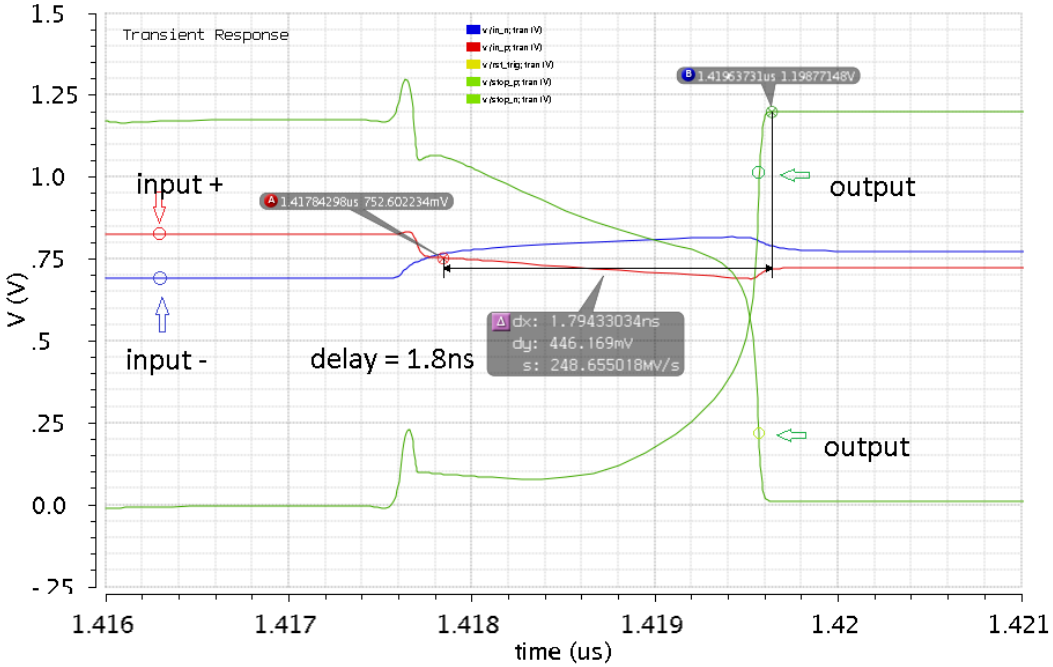


Figure 32 trigger transient response

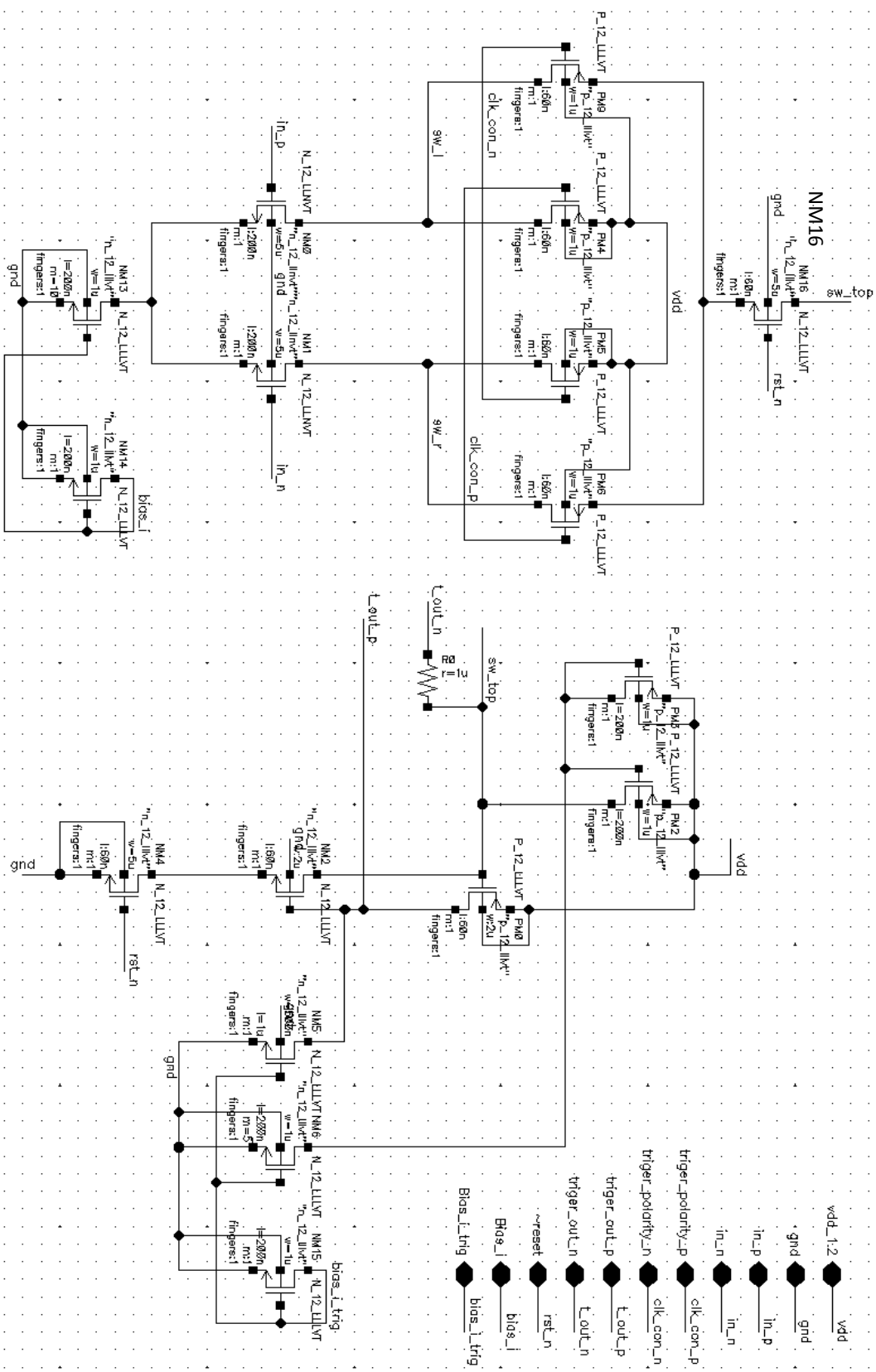


Figure 33 charge control. stop trigger

4.6 Charging control gate

The charging gate is use to switch on / off charging current. Typical gate involve only one switch and a control logic (Figure 34). The problem of such configuration is, the control logic created a relatively large delay between start / stop signal and switch. This delay results large charging error.

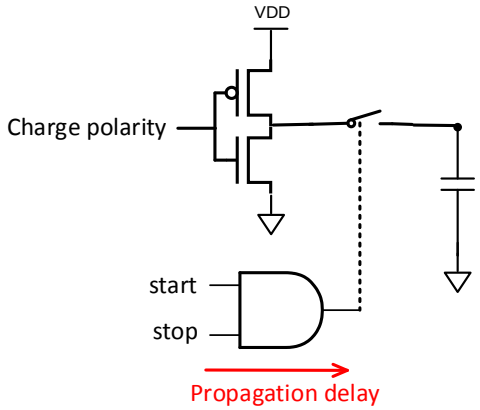


Figure 34 gate with control logic

The circuit show in Figure 35 and Figure 36 has same function as the one in Figure 34. The difference is, it has two gates, one connect to start signal, another to stop signal. Such configuration eliminates the requirement for control logic, and minimize the propagation delay. Such two gate configuration has been used in many mechanical cameras.

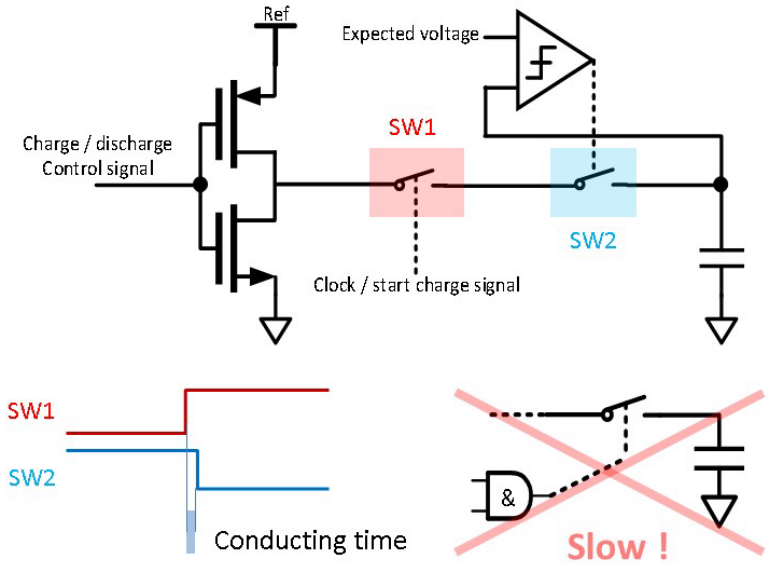


Figure 35 double gate function diagram

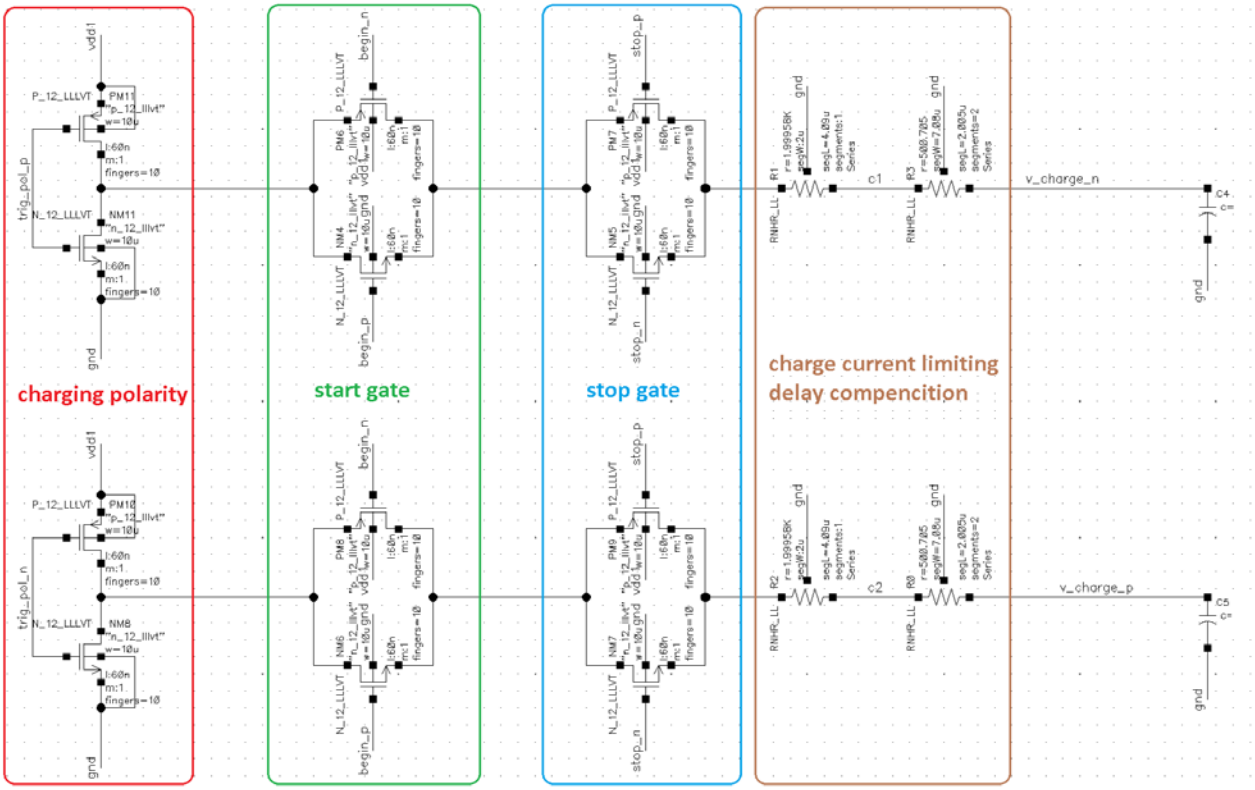


Figure 36 charging gate

4.7 Gate delay compensation

Although the gate has been designed to minimize on / off delay, there still some delay exist (~1ns). Small mount delay could results large charging error when the voltage rising / falling speed is very high on sampling capacitor. Excessive overshoot / undershoot results oscillation (show in Figure 38, red trace).

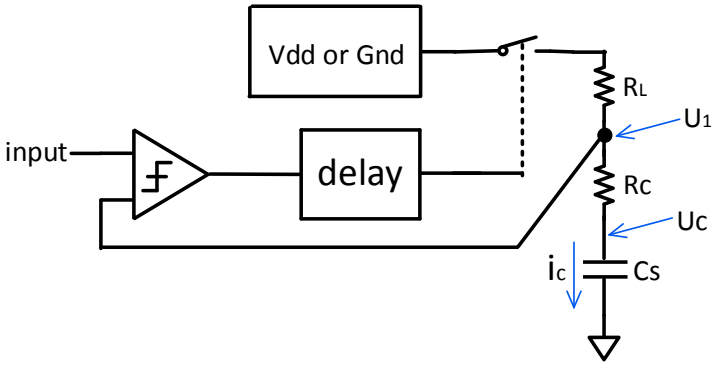


Figure 37 simplified delay compensation schematic

The delay – overshoot problem can be solved by adding a resistor Rc between sampling capacitor Cs and charging current limiter R_L (show in Figure 37).

Assume the charging current i_c is constant during the time $[t_{cutoff} - t_{delay}, t_{cutoff}]$.

The voltage error on sampling capacitor is:

$$\Delta u_{c,error} = \frac{\Delta q}{C_s} = \frac{i_c \Delta t}{C_s} \qquad \text{Eq. 44}$$

With R_c, the voltage at u_1 will higher than u_c. The compensate voltage is:

$$\Delta u_{compen} = u_1 - u_c = i_c R_c \qquad \text{Eq. 45}$$

The charge error will be canceled if:

$$\Delta u_{compen} = \Delta u_{c,error}$$

$$i_c R_c = \frac{i_c \Delta t}{C_s}$$

$$R_c = \frac{\Delta t}{C_s} \qquad \text{Eq. 46}$$

The mathematic shows a fix relation between delay and compensation resistor R_c .

The delay induced overshoot has been significantly reduced, after adding R_c into circuit (show in Figure 38, orange trace).

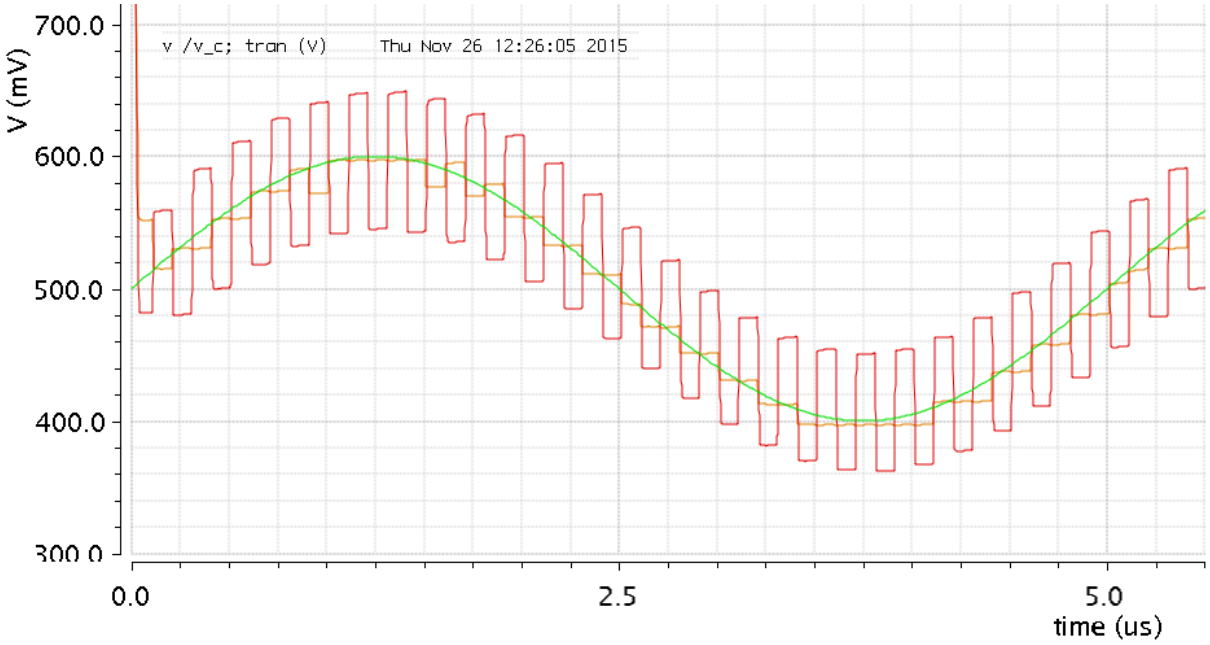


Figure 38 control delay compensation
red - without compensation / orange - with compensation

4.8 Pre-charge controller input offset control

The controller input offset control presets the input common mode voltage for the comparator and trigger inputs. The differential voltage come from inputs and sampling capacitor connect to capacitor network. Normally, the comparator / trigger inputs is balanced when input voltage equal to sampling capacitor voltage. The stop trigger cutoff the charging current when the comparator / trigger inputs voltage cross zero.

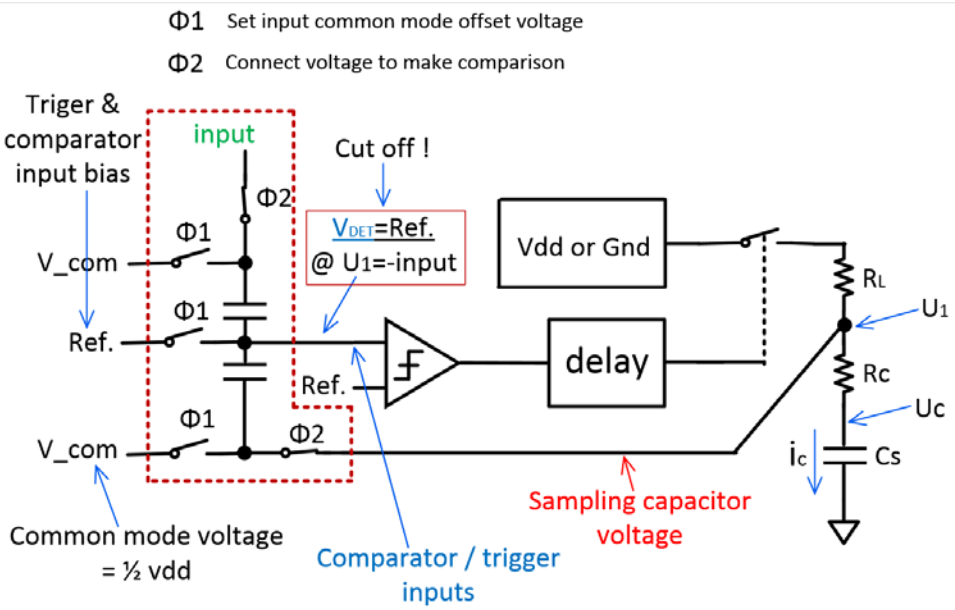


Figure 39 simplified trigger / comparator input common mode bias circuit

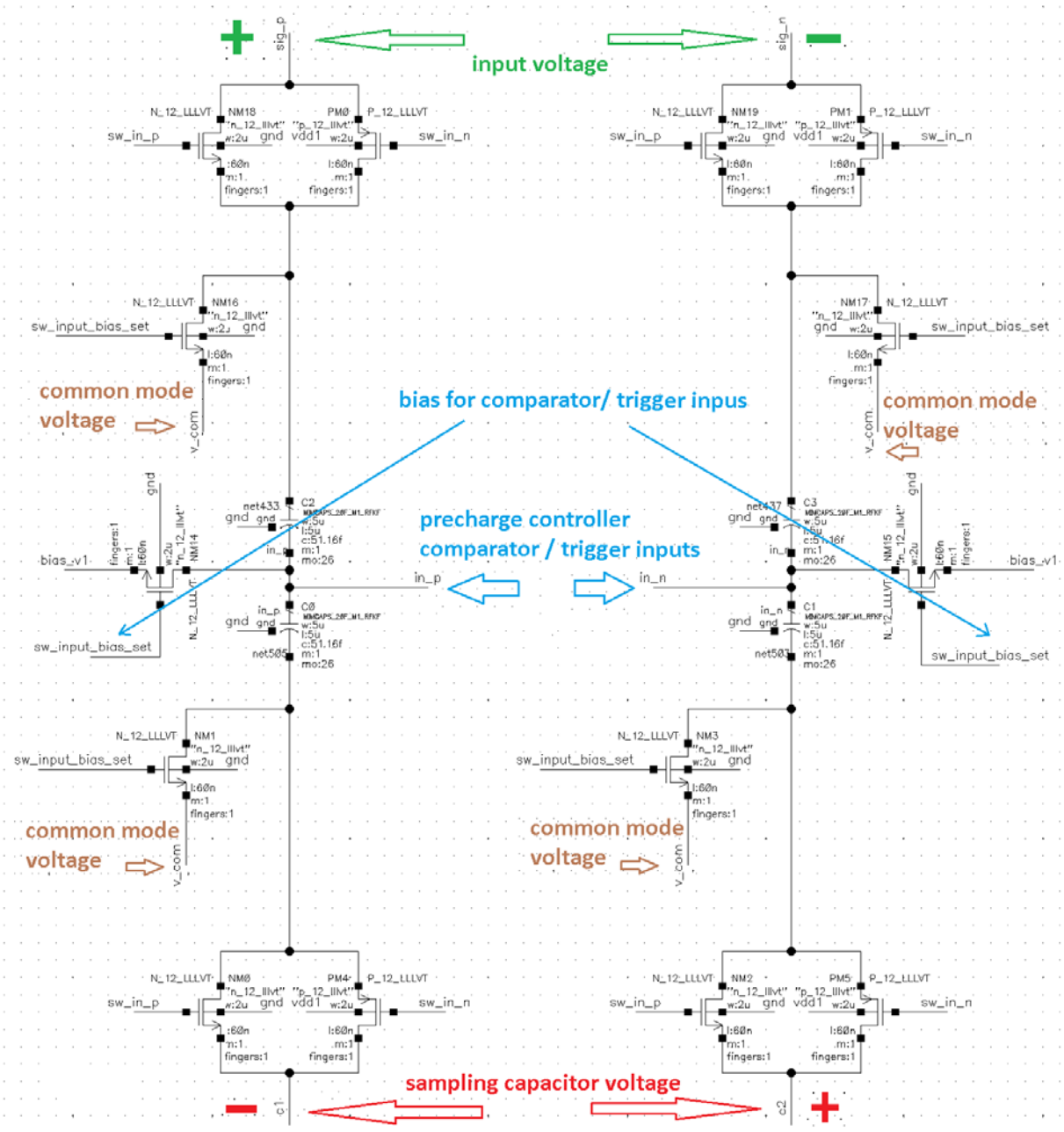


Figure 40 comparator / trigger input offset

4.9 Operational Amplifier

The operational amplifier will continuous the work done by pre-charging circuit. It will drive the sampling capacitor to track the input voltage, and in the same time – give a much lower voltage error compare to pre-charge circuit can do.

Use previous results, the amplifier's open loop distortion should made as low as possible to minimum power consumption. The low distortion require the amplifier has a constant open loop gain.

The opamp schematic (common mode voltage control not shown) is shown in Figure 43. This is a typical two stage amplifier. The input stage is folded cascode. The output stage is biased in class A. The overall open loop gain is very stable in the effective output swing range (about 800mv p-p). The output swing range is limited by the minimum Vsat required by the output stage transistors, but such drawback is overcome by the pre-charge process.

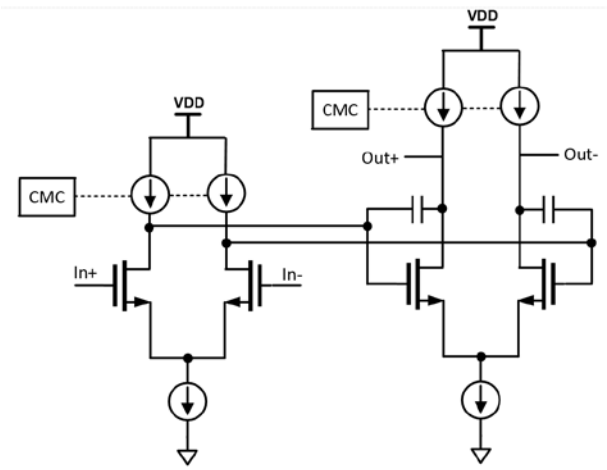


Figure 41 simplified operational amplifier schematic

Figure 42 shows the full schematic of the operational amplifier. Two common mode voltage control is used to regulating the output common mode voltage of first and second stage. Additional source followers have been insert in the miller compensation loop in first stage's common mode control circuit to reduce additional capacitor loading on first stage's output and stabilize the feedback loop.

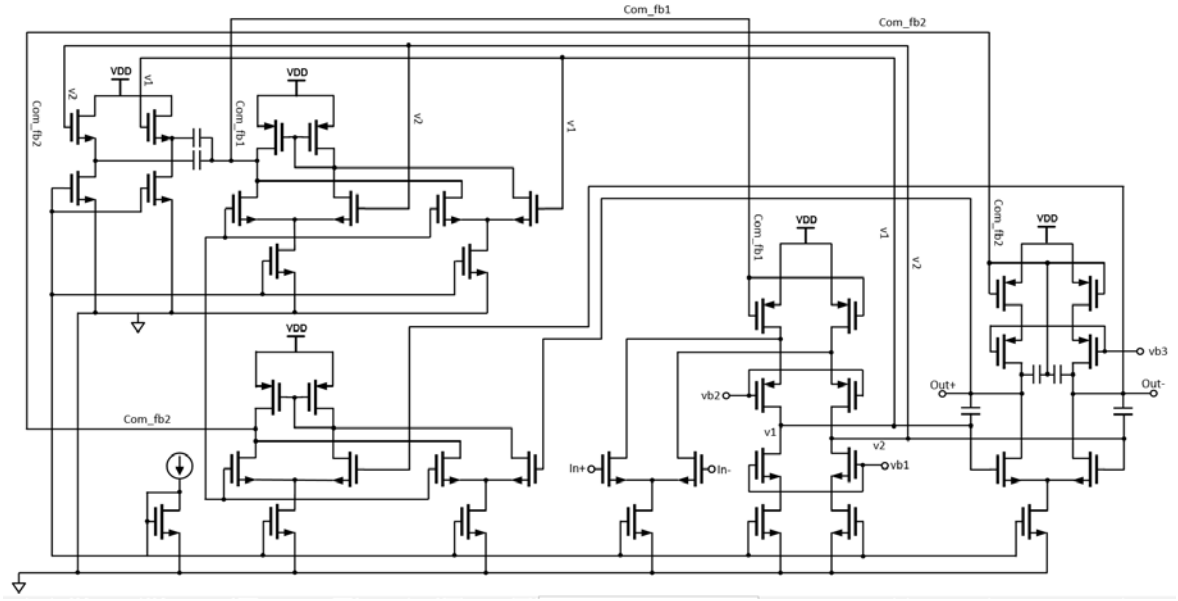


Figure 42 full schematic operational amplifier

The Opamp consume current 216uA to satisfy the distortion requirements with SFDR = -63dB at input signal frequency 2MHz; differential Vout = 600mVp-p; Vdd=1.2V; load capacitor 1+1pF; The amount of bias current is essential to keep distortion low.

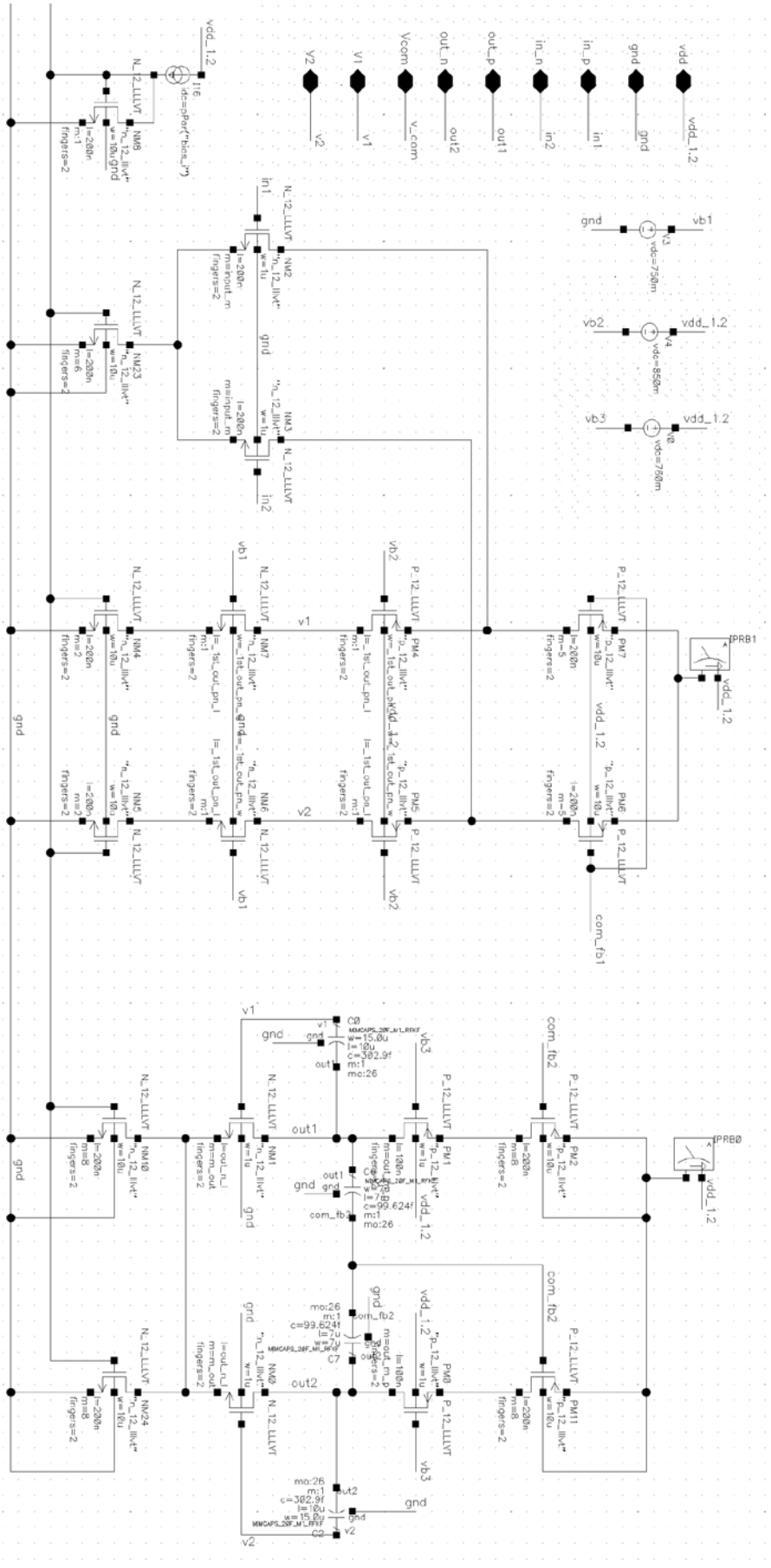


Figure 43 operational amplifier schematic

Figure 44 shows the opamp open loop small signal Gain-phase plot. The phase margin is about 51.48 degree. The GBW is about 50MHz. under conditions Vdd=1.2V; load capacitor 1+1pF;

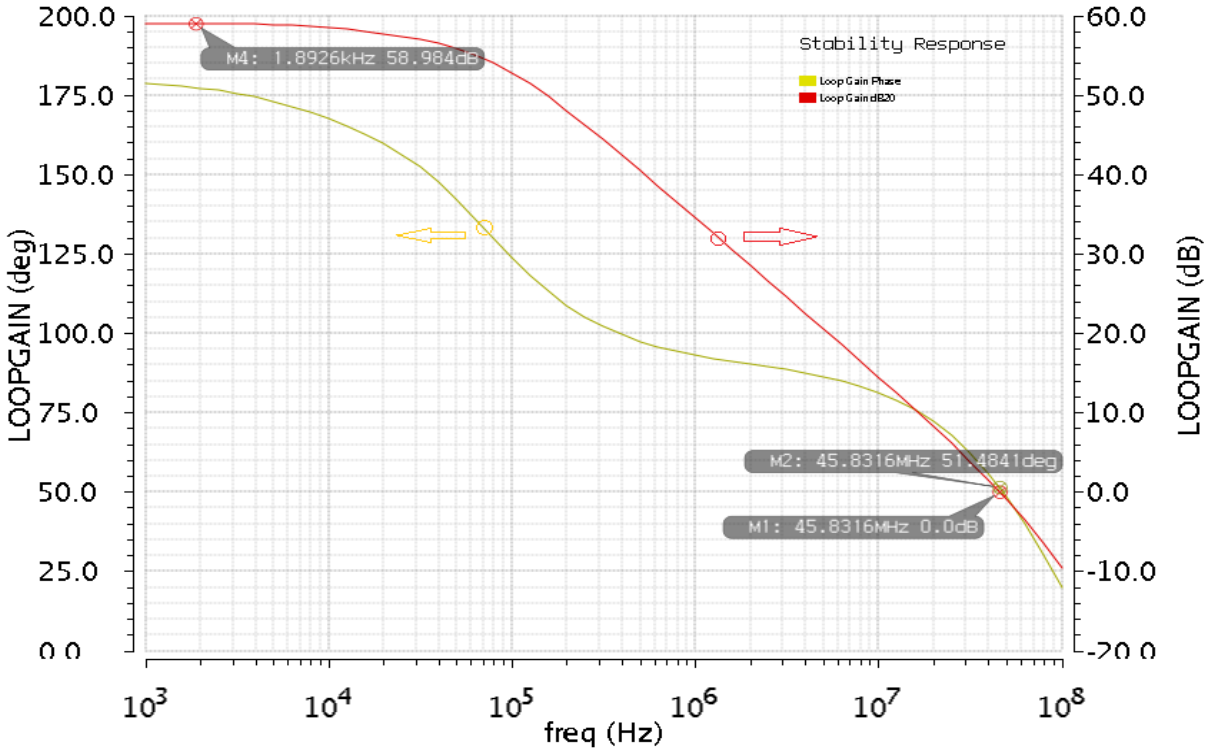


Figure 44 operational amplifier Gain-Phase plot

Figure 45 shows the large signal output power spectrum. The opamp has lower distortion (SFDR -63dB) at 800mV output voltage swing, and much higher distortion (SFDR -45dB) at 1000mV output voltage swing, due to the output transistors operating into triode region. The largest spur is identified as 3rd harmonic folded back.

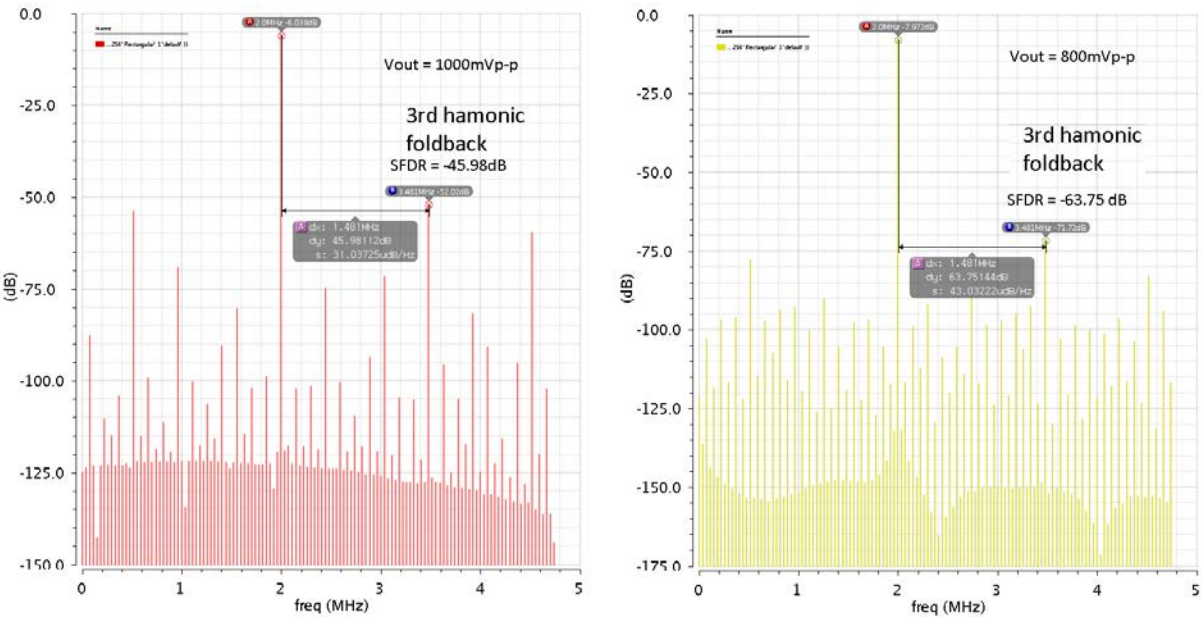


Figure 45 operational amplifier THD plot

4.10 operational amplifier in pre-charge configuration

The external circuit surround the operational amplifier includes the feedback capacitor Cfb, pre-charge capacitor Cs and fine adjust capacitor Ca, and necessary switches for the operation configuration control.

The operation starts from connect only Φ1 switches. The differential voltage stored in capacitor Ca will be discharged, and the Cs and Cfb will be connected in pre-charge mode. Next, connect Φ_{charge} switches and start pre-charge process (Φ1 switches remain connected during this process). After the pre-charge done, disconnect all switches and connect only Φ2 switches, and enable operational amplifier to finish the precision settling and tracking process. Disconnect all switches to hold the voltage on net Out_n and Out_p.

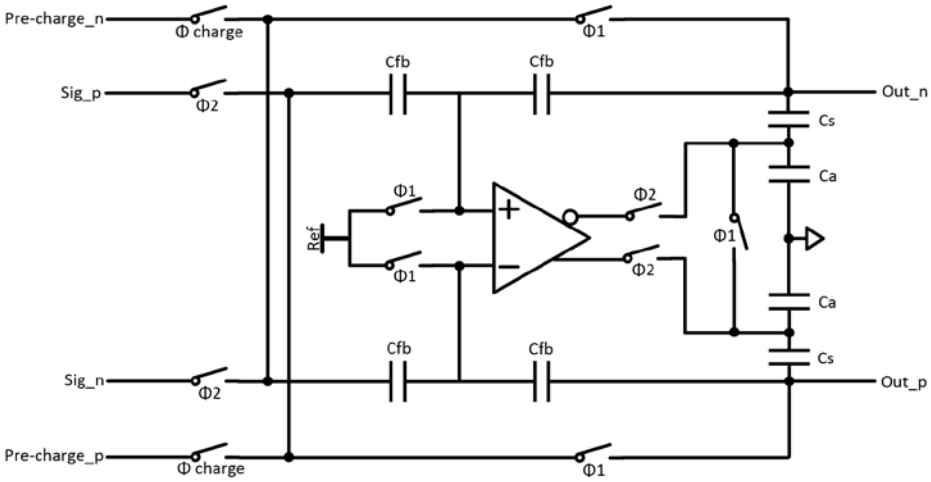


Figure 46 amplifier with pre-charging configuration

Figure 47 (left) shows the power spectrum of sampled signal between out_n and out_p (Figure 46). The spur at around 4.2 MHz is the fold-backed 3rd harmonic, and the 5th harmonic see around 0.2 MHz.

Figure 47 (right) is the time domain plot of the input and output signal. The initial fast setting and tracking process is clearly seen.

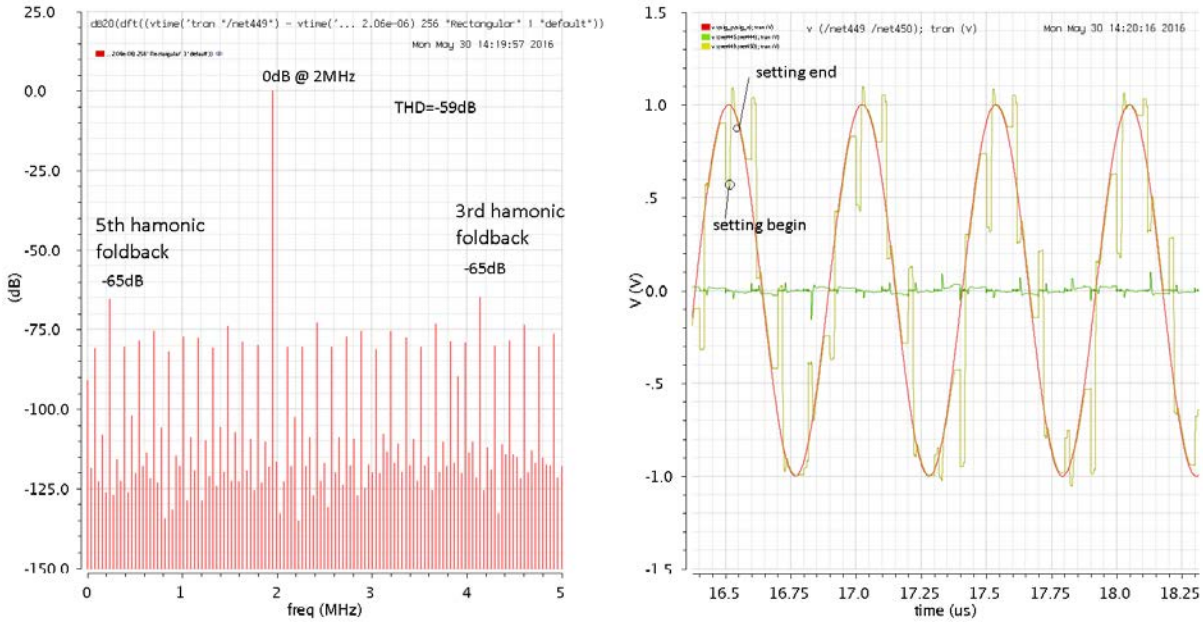


Figure 47 output spectrum; transient voltage (red – input; yellow - output)

Figure 48 shows the input signal voltage (red), voltage at opamp output (green), and voltage at sampling capacitor output (yellow). The voltage swing on opamp output is about 0.4Vp-p, and yet the voltage swing on sampling capacitor is nearly rail to rail at 2Vp-p. The higher sampling frequency / input signal frequency ratio, the lower opamp output swing is required to archive rail to rail output on sampling capacitor.

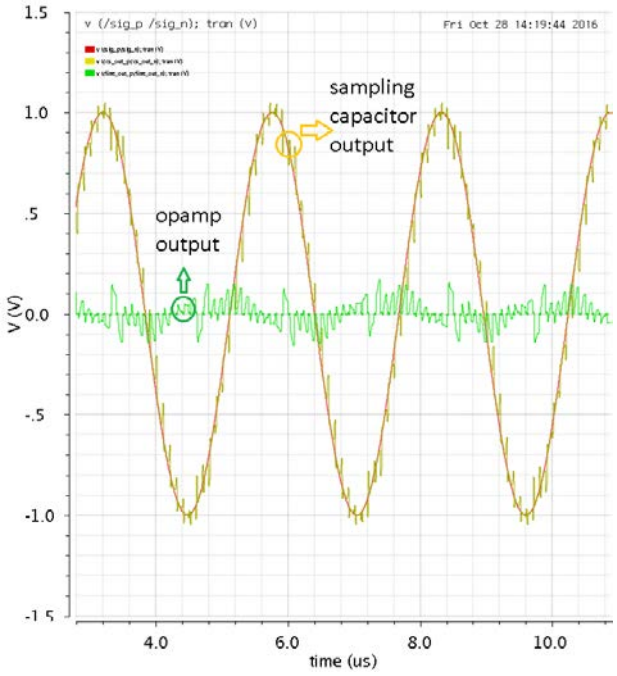


Figure 48 opamp output swing reduction at lower input frequency

Figure 49 shows the opamp input referred noise. The 1/f noise power density is clearly higher than the thermo-noise. The total noise in the frequency span from 1Hz to 100MHz is about 0.57mVrms.

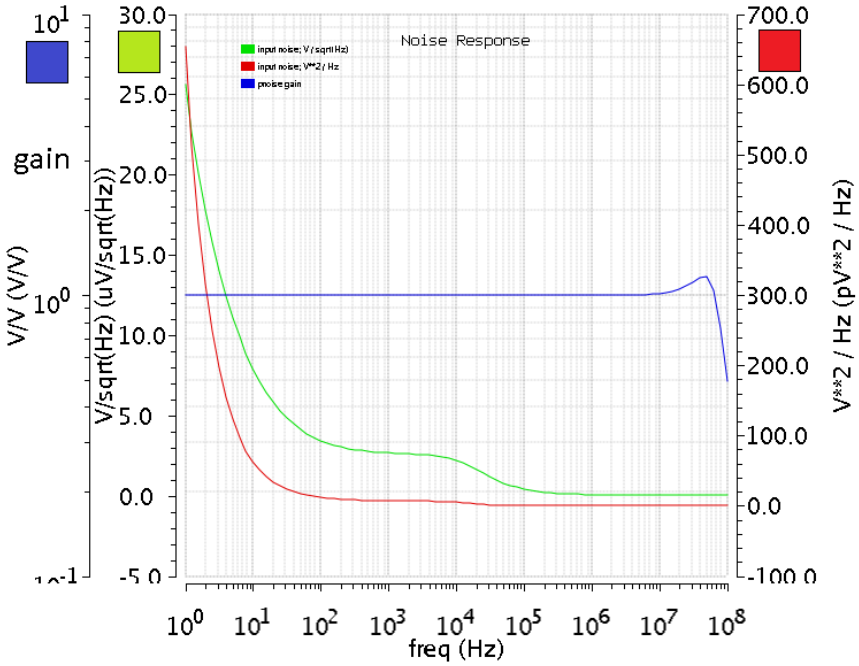


Figure 49 unit gain opamp buffer input referred noise vs. frequency

The overall simulated performance show in below:

P_{total}	$396\ \mu W$	Under conditions: UMC 65nm MOSFET process; C(load) = 1 + 1 pF; Vout(differential, peak to peak) = 2 V; f(input)= 2 MHz; f(sample)= 10 MHz; Vdd= 1.2v Noise integration span = 1Hz ~ 100MHz Offset in 1 sigma (standard deviation) by Promost
I_{total}	$339\ \mu A$	
t_{set}	$40\ ns$	
$t_{set,90\%}$	$2\ ns$	
$peak\ slew\ rate$	$180\ V/\mu s$	
$THD + N$	$-59\ dB$	
$SFDR$	$-65\ dB$	
$opamp\ input\ noise$	$0.57mV$	
$opamp\ input\ offset$	$2.68mV$	

Table 5 overall performance

5 future work

This project is intend to find out the performance and usability of new amplifier structure. The circuit implementation is limited to give sufficient performance support only. Several modification could been performed to give better overall system performance.

1.. The bias current of charge controller and amplifier can be switch off to save power during the hold period.

2.. The charging time is signal dependent during pre-charging process. The charging slow down when the voltage on sampling capacitor close to Vdd or Gnd. This problem result uncertainty on the time gap between the end of pre-charge and begin of fine settling. Such uncertainty made each fine settling process has different initial error. Further, the time gap has to be longer to make sure all pre-charging process could end normally, this also larger the fine settling initial error.

A different pre-charging circuit can be used to solve the problem. E.g. source follower combined with power supply voltage boost. Such circuit enable sampling capacitor voltage to track the input signal voltage continuously with a less precision compare to the fine settling amplifier. The price is higher power consumption.

3.. Better opamp (precision amplifier) can be used to get better performance.

Appendix 1

% please aware some codes are wrapped ! Direct copy this code into matlab may not work.

```
%{
report 4th order equation solver

performance at certain required closed loop distotion level
%}



%close all;
clear;
clc;
%-------------------------parameters
log_id_begin = -50;        % id sweep
log_id_end = -20;
log_id_points = 100;
log_id = log_id_begin : (log_id_end - log_id_begin)./log_id_points :
log_id_end;
id = 10.^(log_id./10);  % calculate lin Id

sweep_length=100;        % parameter sweep points
sweep_begin_log_W = -20;
sweep_end_log_W = 30;
sweep_step_size_W = (sweep_end_log_W - sweep_begin_log_W)./ sweep_length;

THD = 0.01;     % required closed loop THD
un =1;
cox =3.33e-4;    % umc65 N UnCox = 3.3e-4
W =10;
L =0.1;
w =5e6*2*pi;    % signal frequency
cl = 1e-12;     % load Cap
vin=0.5;  % input signal amplitude
%---------------------------------------- init memory
save_log_id_idd = zeros(length(log_id),sweep_length);
save_W = zeros(1,sweep_length);
save_cl = zeros(1,sweep_length);
save_gain = zeros(length(log_id),sweep_length);

%----------------------------------sweep loop start here
for sweep_index=1:sweep_length

%cl=10.^((sweep_index-20)./10) .*cl0;
W=10.^((sweep_begin_log_W + sweep_index .* sweep_step_size_W)./10);
A=2*un.*cox.*W./L;
idd =w.^2.*cl.^2.*(vin.^2./(64*THD.^2.*id)-
vin./(4*THD.*(A.*id).^0.5)+1./A)-id;
% the load has its absolute value use here

save_log_id_idd(:,sweep_index)=log10(abs(idd));
%save_cl(sweep_index) = log10(cl);
save_W(sweep_index) = log10(W);

gain_op= (2*un.*cox.*W./L.*id).^0.5 ./(w.*cl);
save_gain(:,sweep_index)= gain_op./(gain_op+1);
```

```
end
 %{
figure(1)
cla;
loglog(id,idd)
%axis([-1 1 -100 10])
%}

plot_sweep_index=1:sweep_length;
%---------------------------------- give the solution of id
figure(3)
cla;
surfc(save_W,log10(id),save_log_id_idd,...   %power spectrum in db vs ib in
10^x
'FaceAlpha',0.5,'EdgeAlpha',0.3)

axis('vis3d');

%xlabel('transistor width in 10^x');
%xlabel('load capacitor in 10^x');
xlabel('W in 10^x');
ylabel('DC bias Current in 10^x');
zlabel('Equation Residual error in 10^x');
title('equation solver results - constant closed loop distotion');

%-------------------------------show the closed loop gain at certain id

figure(4)
cla;
surfc(save_W,log10(id),save_gain,...   %power spectrum in db vs ib in 10^x
'FaceAlpha',0.5,'EdgeAlpha',0.3)

axis('vis3d');

%xlabel('transistor width in 10^x');
%xlabel('load capacitor in 10^x');
xlabel('W in 10^x');
ylabel('DC bias Current in 10^x');
zlabel('cose loop gain');
title('gain plot - effective oprating region');
```

Appendix 2

% please aware some codes are wrapped ! Direct copy this code into matlab may not work.

```
%{
3D plot for the numerical solution

!!! Vin (in this program) = Vsig (in report) !!!

default input signal sampling points :
ph=0:0.1*pi:(40*pi-0.1*pi);
% modify input signal will affect hamonic calculation !!!
*fundmental = 21 **2nd Hamonic = 41 ***3rd Hamonic = 61 ...and so on.


%}
%close all;
clc;
clear;

%------------------------------- plot control /
% data capture at <plotATindex> sweepindex
plo_en = 1;
plotATindex = 50;


% -------------------- top sweep control
sweep_size=60;
spct_k=0.3;
% FFT plot frequency range from (0Hz) to (spct_k * full_span)

%------------------------------ vb sweep control
sweep_vb = 0;   % ************** !!! sweep Bias Voltage !!!
vb_sweep_log_begin = -10;
vb_sweep_log_end = 20;
vb_sweep_log_step_size =...
 (vb_sweep_log_end - vb_sweep_log_begin)/sweep_size;
vb = 1;

% ---------------------------- Vin sweep control
sweep_input_v = 0;  % ************ !!! sweep Vsig amplitude !!! %
%1=sweep input amplitude; 0=fixed input
vin_sweep_log_begin = -40;
vin_sweep_log_end = 0;
vin_sweep_log_step_size =...
 (vin_sweep_log_end - vin_sweep_log_begin)/sweep_size;
fix_Vin = 0.1;

% ---------------------------- W sweep control (with CONSTANT BIAS CURRENT)
sweep_W = 1;    % ************* !!! sweep transistor Width !!!
W_sweep_log_begin = -20;
W_sweep_log_end = 30;
W_sweep_log_step_size =...
 (W_sweep_log_end - W_sweep_log_begin)/sweep_size;
const_ib=-10e-3; % bias current; must be a negtive number !!!

%----------------------------------------- constants Gen. Inital Memory
r=100e3;    % feedback resistor
```

```
rl=10e3;    % output load resistor
%vb=1;
ucox=3.33e-4;
W= 10;
L= 0.1;
K=-0.5*ucox.*W./L;   % transistor constant = 0.5 u0 Cox W/L

ph=0:0.1*pi:(40*pi-0.1*pi);
% modify input signal will affect hamonic calculation !!!
len_ph=length(ph);
%win=(flattopwin(len_ph)).';
win=(blackmanharris(len_ph)).';
%win=(chebwin(len_ph)).';
%win=1;

if sweep_input_v == 0
vs=fix_Vin *sin(ph);         % fixed input signal
end

save_spectrum = zeros(sweep_size,len_ph*spct_k);
save_ib = zeros(sweep_size,1);
save_W = zeros(sweep_size,1);
save_gain = zeros(sweep_size,1);
save_vin = zeros(sweep_size,1);

indexx=(1:(len_ph*spct_k)).';
%----------------------------------------

for index = 1:sweep_size

if sweep_input_v == 1   % input signal amplitude log sweep
vs=10^(0.1*(vin_sweep_log_begin + vin_sweep_log_step_size*index)) *sin(ph);
end

if sweep_vb == 1
vb=10^(0.1*(vb_sweep_log_begin + vb_sweep_log_step_size*index));
%vb= 0.05*(index);
end

if sweep_W == 1
W= 10^(0.1*(W_sweep_log_begin + W_sweep_log_step_size*index));
K=-0.5*ucox.*W./L;
vb= (const_ib./K).^0.5;
end

%%{
vo=-(2*(r*rl + r.^2 + rl.^2/4 - K*r*rl.^2*vb - 2*K*r.^2*rl*vb...
- K*r*rl.^2*vs - K*r.^2*rl*vs).^(1/2) - rl - 2*r + 2*K*r*rl*vb...
 + K*r*rl*vs)/(K*r*rl);

im= sum(abs(imag(vo)));
if im ~= 0
fprintf('out put voltage image part detected at index %d, W= %f, vb= %f
\n',index,K,vb);
end
%%}
%{
vo=(2*r + rl + 2*(r.*rl + r.^2 + rl.^2/4 - K.*r.*rl.^2.*vb -
2*K.*r.^2.*rl.*vb - K.*r.*rl.^2.*vs...
```

```
 - K.*r.^2.*rl.*vs).^(1/2) - 2*K.*r.*rl.*vb - K.*r.*rl.*vs)/(K.*r.*rl);
%}
vo_ac=-vo+mean(vo);

vo_no_neg= 0.5*(vo - abs(vo));
vo_no_neg_ac=vo_no_neg - mean(vo_no_neg);

if (plo_en ~= 0) && (index == plotATindex)
figure(1)
hold off;
cla;
plot(vs,'-r')
hold on;
plot(vo,'-b')
plot(vo_no_neg_ac,'-g')
str=sprintf('Plot at index = %d', index);
title({str ;'red = input';'blue = output with DC';'green = output AC'});
end

% choose FFT from normal <vo_ac>, or cliped (no reverse current on Id)
<vo_no_neg_ac>
vo_ft=abs(fft(vo_no_neg_ac.*win));

if (plo_en ~= 0) && (index == plotATindex)
figure(2)
hold off;
cla;
semilogy(vo_ft)
str=sprintf('Plot at index = %d', index);
title({str; 'output spectrum'});
end


save_spectrum (index , :) = 20*log10(vo_ft(1:(len_ph*spct_k)));     % power
spectrum in dBV

save_ib(index) = K*(vb).^2;

save_vin(index) = 10^(0.1*(vin_sweep_log_begin +
vin_sweep_log_step_size*index));

save_W(index) = W;

gain_openloop = ucox.*W./L.*vb.*rl;
save_gain(index)= gain_openloop./(gain_openloop +1);
end

log_save_ib=log10(abs(save_ib));
log_save_W = log10(abs(save_W));
log_save_vin = log10(save_vin);


% ------------------------------------------------------ plot sweep Vb
if sweep_vb==1
figure(3)
surf(indexx,log_save_ib,save_spectrum,...   %power spectrum in db vs ib in
10^x
'FaceAlpha',0.5,'EdgeAlpha',0.5)
```

```
1
2   xlabel('frequency');
3   ylabel('DC bias current in 10^x');
4   zlabel('FFT power');
5   title('sweep bias current - Ib vs. output power spectrum');
6
7   %zoom on;    % fix the figure window distotion for 3D plot
8   %zoom(0.8);
9   %zoom off;
10  axis('vis3d') % better way to fix the figure window distotion for 3D plot
11
12  figure(5)
13  distotion = (10.^save_spectrum(:,41)+ 10.^save_spectrum(:,61))./
14  (10.^save_spectrum(:,21));
15  plot(log_save_ib,log10(distotion));  % ib vs 2nd + 3rd hamonic power
16  xlabel('bias current in 10^x');
17  ylabel('power spectrum in dB');
18  title('sweep bias current - Ib vs. distotion (2nd + 3rd Hamonic Power)');
19
20  figure(6)
21  plot(log_save_ib,save_gain);
22  xlabel('bias current in 10^x');
23  ylabel('calculated closed loop gain');
24  title('sweep bias current - Ib vs. closed loop gain');
25  end
26
27
28  %-----------------------------------------------------------plot sweep Vsig
29  if sweep_input_v==1
30  figure(3)
31  surf(indexx,log_save_vin,save_spectrum,...   %power spectrum in db vs ib in
32  10^x
33  'FaceAlpha',0.5,'EdgeAlpha',0.5)
34
35  xlabel('frequency');
36  ylabel('input signal voltage in 10^x');
37  zlabel('FFT power');
38  title('sweep input signal voltage - Vsig vs. output power spectrum');
39
40  %zoom on;    % fix the figure window distotion for 3D plot
41  %zoom(0.8);
42  %zoom off;
43  axis('vis3d') % better way to fix the figure window distotion for 3D plot
44
45  figure(5)
46  distotion = (10.^save_spectrum(:,41)+ 10.^save_spectrum(:,61))./
47  (10.^save_spectrum(:,21));
48  plot(log_save_vin,log10(distotion));  % ib vs 2nd hamonic power
49  xlabel('input voltage in 10^x');
50  ylabel('power spectrum in dB');
51  title('sweep input signal voltage - Vsig vs. distotion (2nd + 3rd Hamonic
52  Power)');
53
54  end
55
56  % ------------------------------------------------- plot sweep W
57  if sweep_W==1
58  figure(3)
```

```
surf(indexx,log_save_W,save_spectrum,...   %power spectrum in db vs ib in
10^x
'FaceAlpha',0.5,'EdgeAlpha',0.5)

xlabel('frequency');
ylabel('transistor W in 10^x');
zlabel('FFT power');
% !!! this make a two line title !!! ---------v
title({'sweep transistor width - W vs. output power spectrum ';'with
constant bias current'});
%zoom on;    % fix the figure window distotion for 3D plot
%zoom(0.8);
%zoom off;
axis('vis3d') % better way to fix the figure window distotion for 3D plot

figure(5)
distotion = (10.^save_spectrum(:,41)+ 10.^save_spectrum(:,61))./
(10.^save_spectrum(:,21));
plot(log_save_W,log10(distotion));  % ib vs 2nd + 3rd hamonic power
xlabel('transistor width in 10^x');
ylabel('power spectrum in dB');
title({'sweep transistor width - W vs. distotion (2nd + 3rd Hamonic
Power)';'with constant bias current'});

figure(6)
plot(log_save_W,save_gain);
xlabel('transistor width in 10^x');
ylabel('calculated closed loop gain');
title({'sweep transistor width - W vs. closed loop gain';'with constant
bias current'});
end









% figure(4)
% %plot(save_ib);
% semilogy(save_ib);  % ib vs sweep index
```

Appendix 3

```
% work on matlab 2013 and on wards
clc;
cla;

syms  w;
gm0=1e-3;
gm1=10e-3;
cgs=0.02e-12;
cl=1e-12;
cc=0.3e-12;

PM(1:20)=0;
PMR(1:20)=0;
cc_rec(1:20)=0;

for index=1:20  %number of sweep points
NO_=index
cc=0.0e-12+0.01e-12.*index  %calculate Cc
%{
s=solve(abs((gm0.*gm1.*cl+gm0.*gm1.*cgs+gm0.*gm1.*cgs.*cl./...
cc-gm0.*cc.*1i.*w.*cl-gm0.*cc.*1i.*w.*cgs-gm0.*cc.*1i.*w.*cgs.*cl./cc)...
 ./ (-w.^2.*cc.*cl.^2-w.^2.*cc.*cl.*cgs-w.^2.*cc.*cl.*cgs.*cl./...
cc-w.^2.*cgs.*cc.*cl-w.^2.*cgs.*cc.*cgs-w.^2.*cgs.*cc.*cgs.*cl./...
cc-w.^2.*cgs.*cl.^2-w.^2.*cgs.*cl.*cgs-w.^2.*cgs.*cl.*cgs.*cl./...
cc+gm1.*1i.*w.*cc.*cl+gm1.*1i.*w.*cgs.*cc+gm1.*1i.*w.*cgs.*cl))==1,w);
% absolute gain vout/vin
%}

s=vpasolve(abs((-gm0.*cc).*(1i.*real(w)-
gm1./cc)./((cc.*cl+cgs.*cc+cgs.*cl).*...
1i.*real(w).*(1i.*real(w)+gm1./(cl+cgs+cgs.*cl./cc))))==1,w,1e9);

p2=gm1./(cl+cgs+cgs.*cl./cc)    %calculate second pole
omiga=double(s)
omiga_abs=real(omiga)

% frequency difference between 0dB point and second Pole
w0dBToP2=p2-omiga_abs

% frequency marging ratio
w0dBToP2_ra=w0dBToP2./p2

PM(index)=w0dBToP2;
PMR(index)=w0dBToP2_ra;
cc_rec(index)=cc;

end

figure(1);
hold off;
cla;
plotyy(cc_rec,PM,cc_rec,PMR);
legend('frequency of (pole 2 - 0dB point)','frequency of (pole 2 - 0dB
point) / pole 2',2);
xlabel('frequency');

```

Appendix 4

eq. 15 :

$$I_d = \frac{\left[\left(\frac{THD_o}{THD_c} - 1\right) Z_L^{-1}\right]^2}{2 u C_{ox} \frac{W}{L}}$$

eq. 18 :

$$THD_o = \frac{A}{4 V_b}$$ → Signal Amplitude

↓

eq. 19 :

$$THD_o = \sqrt{u C_{ox} \frac{W}{L} \frac{A^2}{32 I_d}}$$

eq. 15 + eq. 19 :

$$I_d = \frac{\left[\left(\frac{\sqrt{u_n C_{ox} \frac{W}{L}} \sqrt{\frac{A^2}{32 I_d}}}{THD_c} - 1\right) Z_L^{-1}\right]^2}{2 u C_{ox} \frac{W}{L}}$$

$$= \frac{Z_L^{-2}\left[\left(\frac{\sqrt{u_n C_{ox} \frac{W}{L} A^2/32 I_d}}{THD_c}\right)^2 - 2\left(\frac{4 \cdot \sqrt{u_n C_{ox} \frac{W}{L} \frac{A^2}{32 I_d}}}{THD_c}\right) + 1\right]}{2 u C_{ox} \frac{W}{L}}$$

$$= \frac{Z_L^{-2}\left[\left(\frac{u_n C_{ox} \frac{W}{L} \frac{A^2}{32 I_d}}{THD_c^2}\right) - \frac{2 \sqrt{u_n C_{ox} \frac{W}{L} \frac{A^2}{32 I_d}}}{THD_c} + 1\right]}{2 u C_{ox} \frac{W}{L}}$$

$$= Z_L^{-2}\left[\frac{\frac{A^2}{64 I_d}}{THD_c^2} - \frac{2 \sqrt{u_n C_{ox} \frac{W}{L} A^2/32 I_d}}{2\, THD_c \left(\sqrt{u C_{ox} \frac{W}{L}}\right)^2} + \frac{1}{2 u C_{ox} \frac{W}{L}}\right]$$

$$= Z_L^{-2}\left[\frac{A^2}{64 I_d THD_c^2} - \frac{\cancel{2} \sqrt{A^2/32 I_d}}{\sqrt{u C_{ox} \frac{W}{L}}\ THD_c} + \frac{1}{2 u C_{ox} \frac{W}{L}}\right]$$

$$= Z_L^{-2}\left[\frac{A^2}{64 I_d THD_c^2} - \frac{A}{4 \cdot \sqrt{u C_{ox} \frac{W}{L} I_d \cdot 2}\ THD_c} + \frac{1}{2 u C_{ox} \frac{W}{L}}\right]$$

Appendix 5

Relation between open loop / closed loop distortion

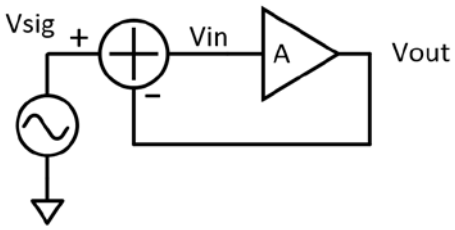
With equation Eq. 17 Eq. 18 Eq. 19 we know:

$$THD_{openloop} = \frac{V_A}{4V_b} \qquad \text{Eq. 19}$$

The open loop distortion is related to the input signal (V_A) level. The distortion level depend on the transfer function of the amplifier. Eq. 19 shows the relation between distortion and the input signal / bias voltage ratio, for a single transistor common source class A amplifier.

Clearly, distortion reduced with lower input signal level.

For a unity gain buffer amplifier, the feedback gain is 1. The amplifier gain is A.



The Vin is:

$$V_{in} = V_{sig}\frac{1}{1+A} \qquad \text{Eq. 47}$$

With a fixed input signal V_{sig} and $V_A = V_{in}$, the relation between open loop distortion and closed loop distortion is:

$$\frac{THD_{openLoop}}{THD_{closeLoop}} = A + 1 \qquad \text{Eq. 15}$$