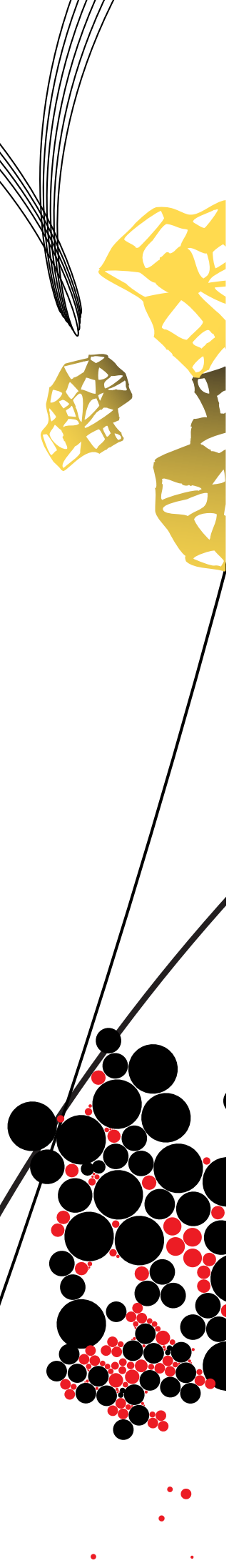

UNIVERSITY OF TWENTE.

Faculty of Electrical Engineering, Mathematics & Computer Science

Master Thesis

The relation between TLP and VSWR to improve the ruggedness of LDMOS transistors

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Abstract

An analysis is presented to the behavior of laterally diffused metal oxide semiconductor (LDMOS) transistors under normal and mismatch conditions. Mismatch conditions are loads applied to the output of the radio frequency (RF) power amplifier which are not nominal loads, 50 ohms. The mismatch is measured using a voltage standing wave ratio (VSWR) measurement at product level. The robustness to a mismatch is often denoted as the ruggedness of the transistor. Insight of the behavior of the LDMOS transistor under mismatch conditions is used to find a relation between an on-wafer measurement, transmission line pulse (TLP), and the VSWR measurement on product level. A relation between the on-wafer measurement and the measurement on product level will lead to a faster development cycle and will save money and time since a design of the packaged transistor and RF circuit can be avoided.

A detailed model of the die, matching, packaging and the RF circuit is created to evaluate the current flows inside the transistor together with the voltages at different nodes. The model can be used to simulate the behavior of the transistor under nominal conditions, 50 ohms, and under mismatch conditions.

The failure mode during VSWR measurements at product level is founded to be related to the current flow in breakdown of the transistor. A maximum current flow is reached when a maximum inductive load is applied to the die of the transistor. All measured devices failed in the region were the transistor is in breakdown. The current flow in breakdown is measured on-wafer by TLP and can therefore be used as a measure to determine the ruggedness of the transistors.

Further investigations needs to be done to find a clear relation between the on-wafer TLP measurements and the VSWR at product level/ A relation is not achieved because the current levels in breakdown of the TLP were too small to find a proper relation. A clear relation is not achieved, although a trend between TLP and VSWR is visible. The VSWR increases when the maximum current in TLP also increases.

Acknowledgements

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Acronyms

CW	Continuous Wave
LDMOS	laterally diffused metal oxide semiconductor
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier
TLP	Transmission Line Pulse
VSWR	Voltage Standing Wave Ratio

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Chapter 1

Introduction

This thesis project is part of the master program at the Electrical Engineering department of the University of Twente. The project is conducted internally at the company Ampleon. Ampleon is specialized in radio frequency (RF) power and it offers a broad range of transistors, Monolithic Microwave Integrated Circuits (MMICs), pallets and modules in laterally diffused metal oxide semiconductor (LDMOS) and galliumn nitride (GaN) technology.

A typical RF transistor consists of a package with a semiconductor die and possibly internal matching. The main part of the transistor is the die. On-wafer measurements such as loadpull or DC are used as an indication of the final performance in application. These on-wafer measurements are therefore an essential measure for technical development.

An important element within the overall performance is the capability to withstand a mismatched load, not 50 Ohms, to the output of an amplifier which includes the transistor. This performance is typical determined by the transistor and is called ruggedness. A rugged transistor can withstand large mismatched load conditions applied to the output of the amplifier. Improving the ruggedness of the transistors is therefore important because this will allow a wider application range.

Presently, technologists do not have a clear on-wafer transistor parameter to predict the ruggedness of the transistors. The ruggedness of the transistors is obtained by measuring the packaged transistors. Before these packaged transistors can be measured, a designer should design a packaged transistor and a circuit to measure the ruggedness of the transistors. When wafer level measurements would be available, money and time could be saved since the matching steps of the package and RF circuit could be avoided.

Until now it is not certain which failure mechanism determines the ruggedness and what is happening during a ruggedness measurement. There are predictions that there is a correlation between the ruggedness and the IV-characteristics, figure 1.1. A dedicated study is needed to confirm this prediction.

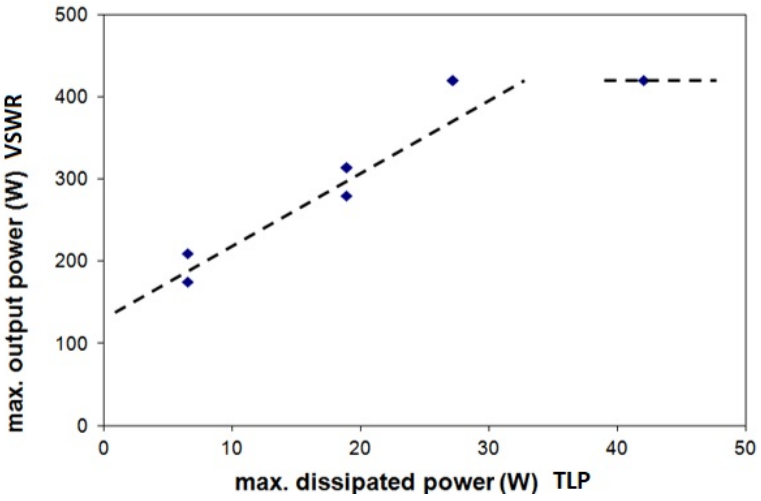

Figure 1.1: Relation between the maximum output power measured during VSWR and maximum dissipated power measured using TLP [1]

The goal of this study is to investigate the relation between the ruggedness of the transistors and the on-wafer IV-characteristics. Furthermore, understanding the failure mechanism during a voltage standing wave ratio (VSWR) measurement and the on-wafer transmission line pulse (TLP) test will be examined in this study. This study will provide guidance to technologists, to improve the ruggedness of the dies, but also to transistor and circuit designers to indicate the effects of matching on the ruggedness performance. This report starts with theory of an LDMOS transistor, ruggedness and DC measurements and some background on RF in chapter 2. The theory will be used as background information for the steps taken in this report. In Chapter 3, the used materials and measurement setups will be described. The modelling needed for the analysis of the ruggedness measurements is described in Chapter 4. The results are described in Chapter 5. The results are discussed in chapter 6. Chapter 7 concludes the results and gives recommendations for further research.

Chapter 2

Theory

This section outlines the background theory. First the LDMOS transistor is introduced. Next, the importance of matching is described. The ruggedness of LDMOS transistors is treated together with the measurement for defining the ruggedness. An introduction to the Smith chart together with its Z and S parameters is treated in section 2.2. The background information will be used throughout the report.

2.1 LDMOS transistor

The laterally diffused metal oxide semiconductor, LDMOS, is specially developed for high frequency and high power applications. The LDMOS is derived from the VDMOS where the source wire inductance of the VDMOS, to connect the source with the ground of the package, is replaced by a P+-sinker and a highly conducting P-substrate. This improvement will increase the frequency range of the transistor [2], [3]. The LDMOS transitor became widely accepted in the beginning of the 90's. It has replaced bipolar transistors for high power applications. The LDMOS has several advantages compared to bipolar transistors. The LDMOS transistor has a better linearity and has a positive temperature coefficient which is beneficial for ruggedness.

A cross-section of the LDMOS die is shown in figure 2.1. The operation principle is equal to a standard NMOS. A channel is induced by applying a positive voltage to the gate. A current starts to flow when a voltage is applied to the drain. The drain is extended to increase the breakdown voltage of the transistor. The breakdown voltage is the voltage where the leakage current starts to increase exponentially. An increased breakdown voltage allows a higher supply voltage. A higher supply voltage is desired to increase the power levels by an increased output voltage swing. The on-resistance increases due to the extension of the drain. The created space between the drain and the gate is called the drain extension or DEX. Supply voltages of V=28 to V=65 V can be reached. The function of the shields is to reduce high

electric field peaks and to reduce the feedback capacitance [4], [5].

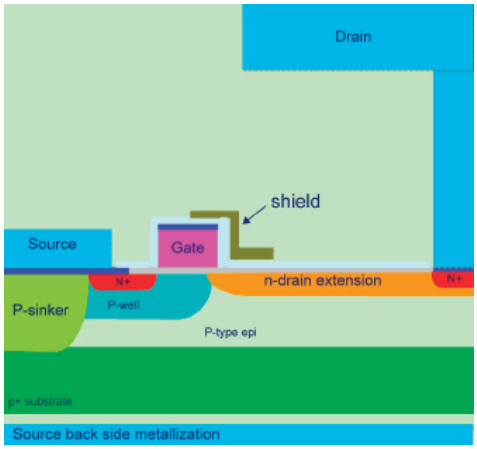

Figure 2.1: Cross-section of the die of a transistor [6]

The schematic displays a cross section of a single transistor, increasing the gate width (multiple fingers parallel) increases the total output power of the transistor.

As in any CMOS device, parasitic elements are present in the LDMOS. The parasitic capacities are displayed in the small signal model in figure 2.2. The transistor can be replaced by a voltage dependent current source. The capacities and resistances are induced by the technology of the transistor. These parasitics are undesired because they will reduce the efficiency, complicate the matching of the transistor and reduce the frequency band of the LDMOS.

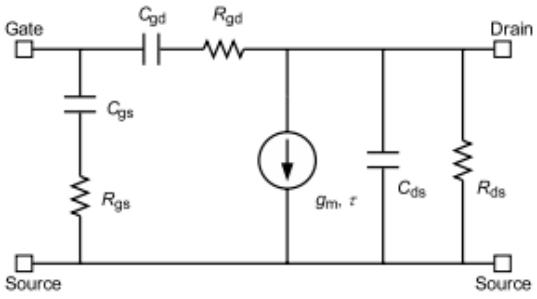

Figure 2.2: Small signal model of the LDMOS transistor including the parasitic capacities [7]

Next to the parasitic capacities, also a body diode and bipolar junction transistor (BJT) are present in the LDMOS transistor. These parasitics play an important role when the transistor is exposed to extreme conditions. The voltage can increase even above the breakdown voltage during these extreme conditions.

2.1.1 LDMOS operating in class AB

The transistor can be set to operate in different classes. Commonly used classes are class A, B and AB. Class AB is a compromise between the high linearity of class A and the high efficiency of class B. The transistor can be set to operate in a certain class by setting the Q-point of the transistor. The Q-point is set by the drain current I_{dq} at a certain drain voltage. Figure 2.3 displays the loadline in a typical class AB configuration. The grey curves are the DC IV curves. The ideal loadline is connected to the knee voltage and the set I_{dq}. The LDMOS voltage will vary between the knee voltage and about 60 V. The current flow through the LDMOS together with the gate voltage are also shown in figure 2.3. The transistor only operates half of the wave. The complete wave is formed by the transistor in combination with the LC circuit. The LC circuit is used to resonate at the work frequency of the transistor.

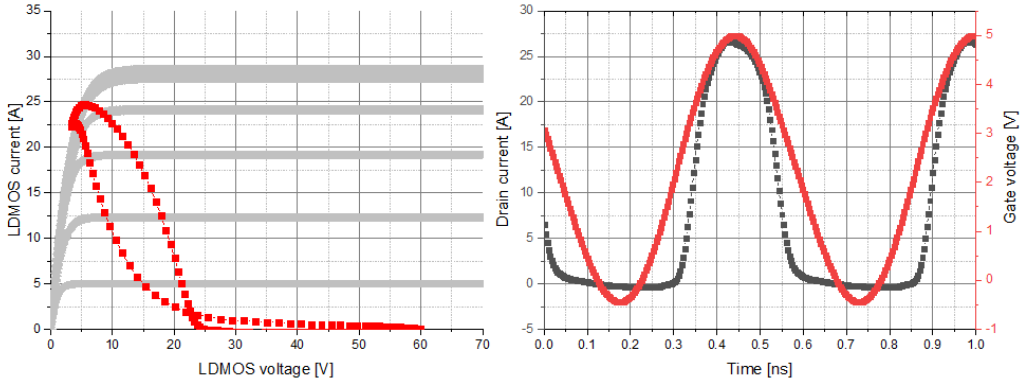

Figure 2.3: Loadline and waveforms of the transistor in a matched AB configuration

When the transistor is exposed to extreme conditions, the current and voltage waveforms together with the loadline will change. Figure 2.4 displays the loadline and corresponding waveforms at extreme load conditions.

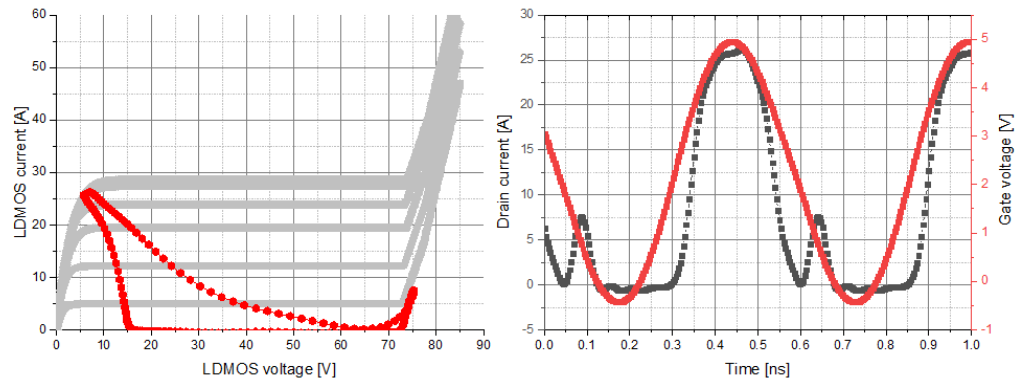

Figure 2.4: Loadline and waveforms of the transistor in an unmatched class AB

The voltage is increased even above the breakdown voltage. A current starts to flow through the LDMOS at these extreme load conditions. The current flow is displayed by the small peak at $0.6ns$.

2.1.2 Transistor ruggedness

The breakdown voltage which is determined by the epi-thickness and the DEX, is typically 70 and 120 V for the LM8+ and LM8HV process. Above breakdown, a current starts to flow through the LDMOS transistor. The current can flow vertically or horizontally through the device. The vertical current flow can be adjusted by increasing or decreasing the epi thickness of the LDMOS transistor. A vertical current flow, through the epi, is a stable current flow which will not damage the LDMOS transistor. The epi-thickness can be modelled by a diode. The current will start to flow if the voltage reaches the breakdown voltage of the diode. The elements playing a role in breakdown are displayed in figure 2.5.

If the current increases further, a horizontal current flow can be established. A failure mode of the LDMOS transistor can be triggered by thermal heating, electric field modulation due to charge buildup or the turn on of the BJT. The BJT has a negative temperature coefficient. The triggering of the parasitic BJT causes a catastropic failure of the LDMOS transistor. A current flow due to triggering of the BJT will increase the temperature locally and therefore decreases the impedance. Due to the decreased impedance, more current starts to flow through the BJT until a catastrophic failure occurs. Two conditions must be met to trigger the BJT. The first condition is that base must be forwarded by the charge carriers (holes) flowing from the source of the LDMOS. The second condition is that the common-emitter current gain should be larger than 1. The BJT will become unstable if both conditions are met. The point where an increased current starts to flow and a failure occurs is called the snapback point. The corresponding voltage is called the snapback voltage [8]–[10].

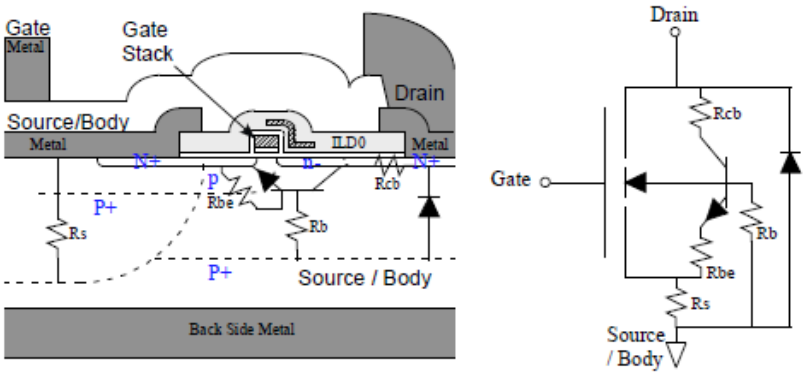

Figure 2.5: Cross-section of the LDMOS transistor including the parasitic elements

2.2 LDMOS transistor model

A transistor consists of a package including a die, bondwires and internal matching, figure 2.6. Bondwires are the metal connections between the active and passive parts of the transistor. The optimal output impedance for optimal performance of the die is called R_{opt}. Load line theory can be used to match the R_{opt} of the transistor [11]. The bondwires needed for connection introduce an undesired inductance which should be compensated by matching. A complete model of the LDMOS transistor consists of the die, internal matching and circuit matching. These matching steps are needed to match the R_{opt} to 50 Ohms. Figure 2.6 displays a packaged transistor including internal matching.

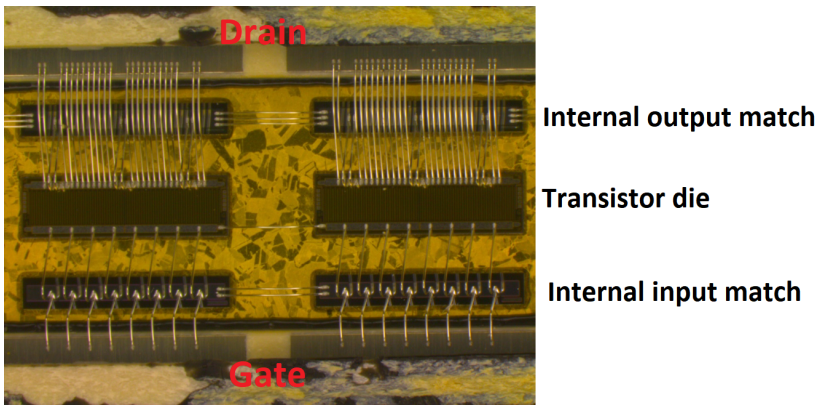

Figure 2.6: Inside a packaged transistor with the die, internal matching and the bondwires

Two silicon dies are placed in the middle of figure 2.6. The two bars below the die are the internal input match, the internal output match is above the die.

2.2.1 Matching of LDMOS transistor

An optimal matching of the LDMOS will result in the best performance that can be achieved by the transistor. Both, the input and output of the transistor should be matched. The output is more critical than the input because larger currents will flow at the output of the transistor.

Internal input matching

The input match is achieved by an inductor L1, parallel capacitance C1 and series inductor L2. The inductors L1 and L2 are bondwires. These are connected to the MOS capacitor which is positioned next to the die. The inductance can be varied by changing the length and height of the bondwire [12].

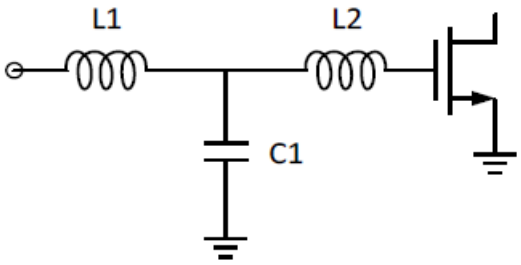

Figure 2.7: Input matching of the LDMOS transistor [13]

Internal output matching

The effects of the drain-source capacitance can be reduced by a shunt-L network.

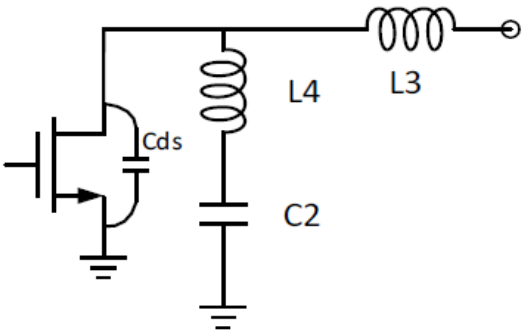

Figure 2.8: Internal output matching of the LDMOS transistor with shunt-L network [13]

The shunt-L network consists of an inductor (bondwire), L4, connected to a capacitance C2. The inductance L4 together with the drain-source capacitance result in a shunt-resonant circuit at the fundamental frequency. The shunt-resonant circuit has an open state at the resonant point. The capacitance C2 must be large enough that the inductance L4 is shorted to ground at the fundamental frequency while blocking any DC current. The inductance L3 is the connection between the die and the package and will increase the imaginary part of the impedance [12], [13].

2.2.2 Circuit matching

The output of the LDMOS is far from matched to 50 ohms. An additional matching circuit is needed on board level to match the impedance of the LDMOS transistor to 50 ohms and to add the bias lines for the supply voltages. Figure 2.9 displays a matching circuit with the bias lines of the in and output, red boxes, and the matching to 50 ohms.

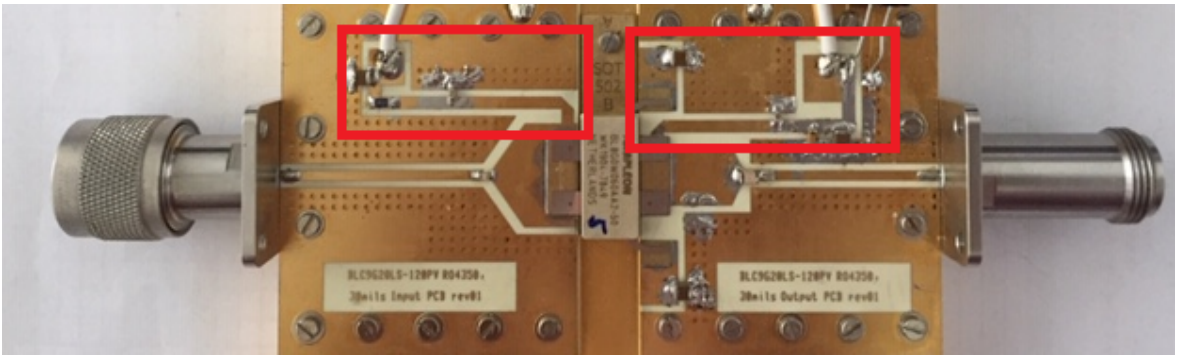

Figure 2.9: Circuit to match the output impedance of the transistor to 50 ohms.

Harmonic content will influence the performance of the power amplifier (PA). Harmonic content can be used to improve the efficiency of PA but it can also cause ruggedness issues. The voltage due to even harmonics is added to the fundamental voltage, this will result in less headroom of the fundamental. Less headroom for the fundamental voltage will limit the RF output power. The impedance of the even harmonics are therefore shorted at the internal current source of the transistor. The harmonics can be suppressed by using a quarter-wave short-circuited stub (SCSS) at the fundamental frequency. A quarter lambda will transform to an open at the fundamental frequency. At the second harmonic, the quarter lambda will transform to an half lambda. An half lambda will be a short so a quarter lamda will transform to a short for the even harmonics [11].

A complete amplifier with all the components is described in figure 2.10. All steps are needed to match the die of the transistor to a load of 50 ohms and to reduce the effects of harmonics. The different boxes indicate the different parts of a power amplifier.

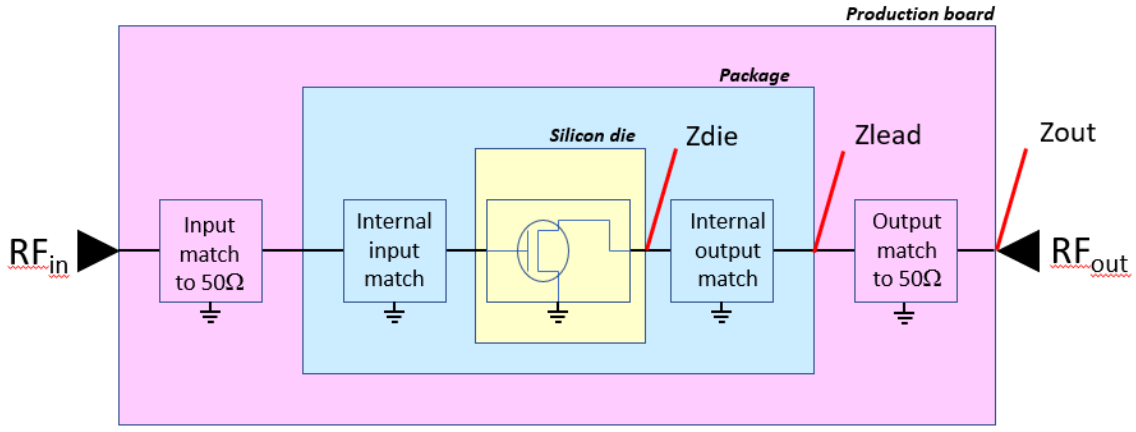

Figure 2.10: Schematic representation of the different parts of a RF power amplifier.

2.3 Ruggedness

The ruggedness of the transistor is the least well defined parameter. The ruggedness of the transistor depends strongly on the application and PA design. The definition of ruggedness as stated by Burdeaux and Burger is ”the ability of a device to withstand unusual electrical conditions on the input or output section of a PA without degrading the RF performance when conditions return to normal” [14]. The unusual electrical conditions are quantified by a Voltage Standing Wave Ratio, VSWR, measurement. The ruggedness of the device is determined at the output of the production board, Zout in figure 2.10. The impedance at the output is, during a VSWR measurement, deliberately not 50 ohms. The mismatch can be explained using the Smith chart, figure 2.11.

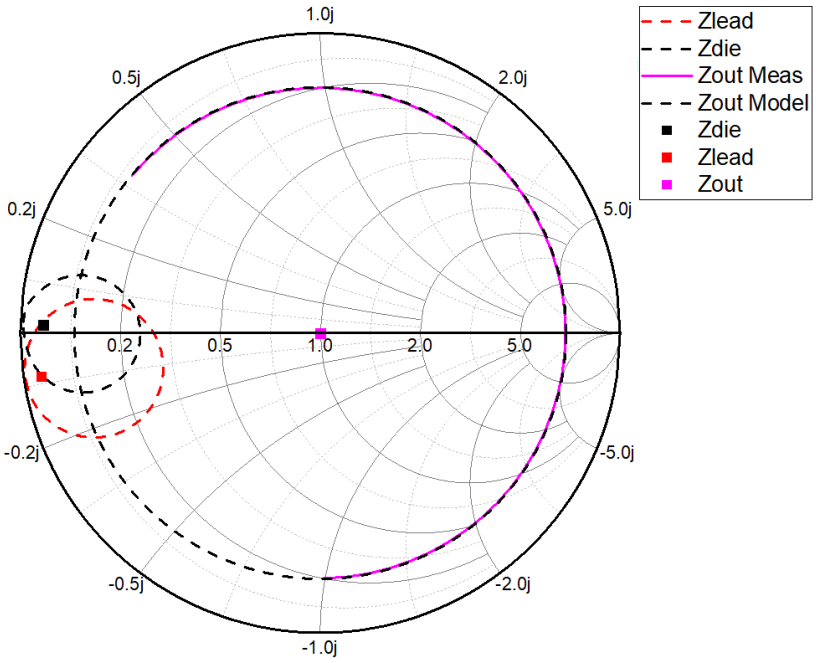

Figure 2.11: Smith chart with the mismatch impedances at the transistor, lead of the package and the output of the amplifier.

The Smith chart is used for plotting reflections in an impedance or admittance coordinate system. The impedance is the reciprocal of the admittance. The impedance is a complex number, including a resistive component R and an imaginary reactance jX. The admittance is represented by Y and the impedance by Z. The power is optimally transferred from the transistor to the circuit when the impedance's are their complex conjugate. The impedance changes over the frequency because the reactance is frequency dependent.

A Smith chart is typically normalized. The pink point in the middle of figure 2.11 is 50 ohms, the smith chart is in this case normalized. The horizontal line in the

Smith chart is the resistive line. The area above this line is the inductive state and the area below is the capacitive state of the Smith chart. The resistance ranges from zero, the left side of the Smith chart, to infinity, the right side. The circles crossing the resistive line have a constant resistance. The lines of constant reactance are connected to the values around the Smith chart [13].

The reflections are represented by the greek letter gamma, Γ. The reflection is the root of the incident power divided by the root of the reflected power.

$$\Gamma = \frac{\sqrt{W_r}}{\sqrt{W_i}} \tag{2.1}$$

Where W_r is the reflected power and W_i is the incident power. The gamma is also related to the magnitude of the Voltage Standing Wave Ratio, VSWR.

$$VSWR = \frac{1+ \mid \Gamma \mid}{1- \mid \Gamma \mid} \tag{2.2}$$

The VSWR is the ratio of the peak amplitude of the voltage of a standing wave to the minimum amplitude of a standing wave. When the reflection coefficient has a non-zero value, when the output is not perfectly matched, power will be reflected from the load back to the power amplifier. The reflected voltage wave will interfere with the transmitted wave along the transmission line, this will create the peaks and valleys in the voltage. A VSWR of 1 means that no power is reflected from the load. When the VSWR is 5, the reflection coefficient is 0.667 and 44% of the power is reflected [13].

The VSWR is measured at the output of the amplifier, Zout in figure 2.10. The VSWR is changed at Zlead and Zdie due to the matching circuit of the production board and the internal matching of the transistor. The change of VSWR is shown in figure 2.11. The impedance at Zdie, Zlead and Zout are the bold points in the Smith chart when the output of the amplifier is perfectely matched to 50 ohms. The striped contours are the impedance's due to a mismatch applied at the output of the amplifier. The striped contours are not centered around the corresponding bold point because of the scale of the axes.

Chapter 3

Methodology

This chapter describes the technologies which are used in this project along with the measurement equipment and protocols.

3.1 Technologies

Two different technologies are used within Ampleon's products, respectively based on Si and GaN technology. The technologies have different flavours consisting of different supply voltages of 30, 50 and 65 V. This research study focuses on the 30 V LDMOS technology because of the availability of the parts needed for experiments. For experimental purposes, six different variants of the technology are investigated to explore the impact on ruggedness. The variants have differences in the epi-thickness and ED2 dose. The ED2 dose is an implant in the DEX. Each variant has a thick and thin wafer. The thick wafers are used for measuring on-wafer where the thin wafers are sawn and assembled. The packaged transistors consists of 2 dies, each $60mm$, to form a total gate width of $120mm$. An assembly schematic and packaged transistor are shown in figure 3.1.

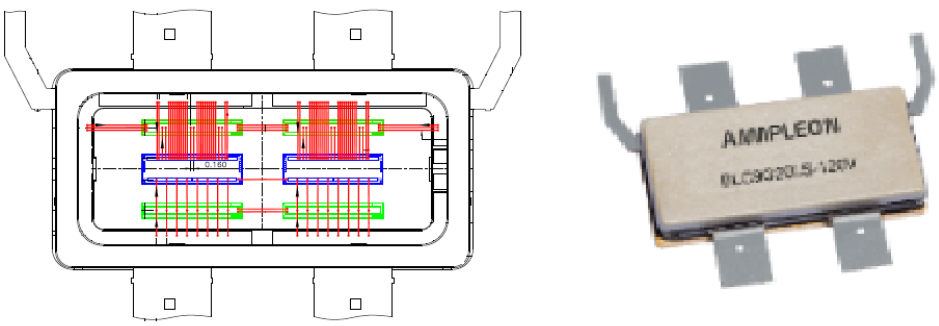

Figure 3.1: Assembly drawing and packaged product of the 30V process with in- and output matching.

The top part of the packaged transistor is the drain and the bottom is the gate, the source is connected with the backside of the package. The blue rectangle in the schematic represents the die, the green rectangles represents the input and output matching capacitance. The red lines are the bondwires. The large amount of bondwires at the drain side is needed to support the high current levels.

3.2 RF Production circuit

The LM8+, 30 volt, process already has a production circuit which can be used for powersweeps and VSWR measurements. The availability of the production circuit was the reason for starting with the LM8+ process. The production RF circuit, N2385, is a gold plated base plate. The connector is 50 ohm and the strip lines are used to match the input and output impedance to the in- and output respectively. A series capacitance in the in- and output is used for DC filtering. The red boxes are the DC bias lines. The videoleads are connected with a capacitor to ground in the blue boxes. The videoleads are used for lowpass filtering. The packaged transistors will operate in class AB with an Idq of 700 mA. The operation frequency of the transistors is at 1.8GHz.

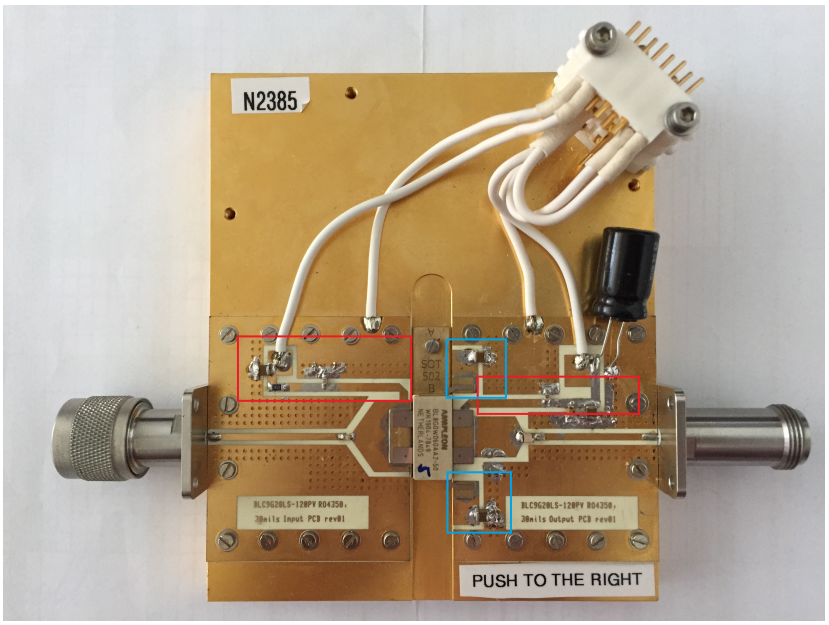

Figure 3.2: RF Production circuit with a LM8+ die with in- and output matching.

3.3 Measurement setup

This section describes the measurement setups and protocols. DC, TLP, VSWR and Power sweep measurements are needed for developing a model of the transistors.

3.3.1 DC

Basic $I_d - V_d$ characteristics of the transistors are measured by DC measurements. DC parameters such as breakdown voltage, maximum current, on-resistance and thermal resistance are measured. A test program specific for each process is available. The setup consist of an Itec μPARSET and a test fixture T211 for the LM8+ process. The packaged transistors are manually placed in the test fixture and measured via a test plan. The setup will indicate if the transistor has passed the test or if a failure occurs. A failure occurred when the specification of a parameter is not within the set margin. A failure can occur when the die is not attached properly to the package during fabrication. $I_d - V_d$-Curves are measured after each single transistor is tested. The transistor is, again, placed in the test fixture for measuring the IV-curves. The drain voltage will be increased from 0 V to 20 V. The gate voltage will be increased with 0.2 V from 2 V up to and including 6 V after each drain voltage sweep. The pulse-width of the drain voltage is $450\mu s$ with $25ms$ delay. The data is saved and analyzed afterwards. The $I_d - V_g$ curves are taken from the $I_d - V_d$ data. The drain current is taken at a drain voltage of 10 V for each gate voltage ranging from 2 up to and including 6 V.

3.3.2 TLP

The TLP measurement is currently used to give insight in the device's ability to handle high currents under breakdown conditions. Main objective of this study is to find a relation between TLP and VSWR measured at product level. For this purpose, the IV curves measured by TLP are therefore included in the model. The TLP measurement is a DC measurement were very short, 100 ns, pulses are used to minimize self-heating. TLP measurements are executed on dedicated TLP test structures. These structures have less fingers which limits the total current and can therefore be measured with the TLP setup. The total length of the fingers is 3.712 mm. The gate is shorted with the source to prevent instabilities during the measurement. If the gate is not shorted, the gate can be lifted due to the high drain pulse. When the gate is lifted, the channel could be opened which will influence the TLP characteristics.

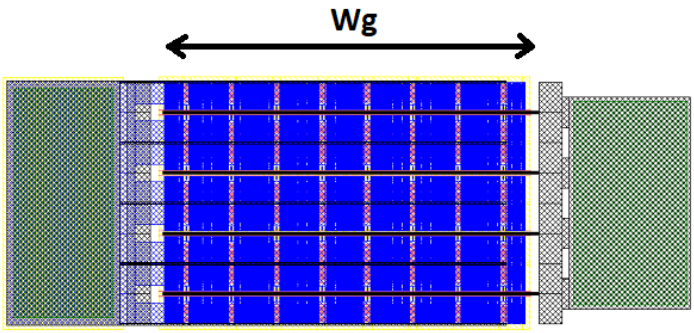

Figure 3.3: TLP test structure for measuring the breakdown region. The gate is shorted to the source. The left connection pad is the gate and the right pad is the drain.

The setup consists of a probe station, high current and voltage prober and a pulse generator, figure 3.4. A pulse is generated by the pulse generator by charging a coax cable. The coax cable will be discharged when the voltage pulse is applied to the drain of the die. The two needles of TLP probe, which can handle large voltages and currents are placed at the drain and gate side of the transistor. A voltage pulse of 100 ns with a rise-time of 10 ns will be applied to the drain of the TLP structure. The current which flows due to the applied voltage is measured. The voltage pulse will increase until the device fails. The voltage applied is half of the voltage at the drain, this is because the voltage will be reflected and will add up to the existing pulse. All TLP measurements are measured at ambient temperature.

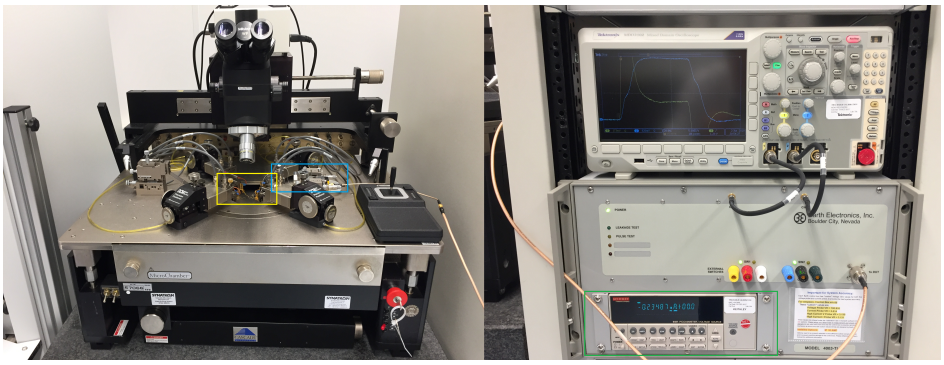

Figure 3.4: TLP test setup for measuring the TLP curves in breakdown. Left figure displays the probe station and the right figure the pulse generator

3.3.3 S-parameters

The reflection coefficients are measured by S-parameters. The open-circuit in- and output can be extracted from these reflections. The network analyzer is calibrated using calibration kit 85031B. The calibrated network analyzer, green box in figure

3.5, is connected to the test circuit, blue box, via limiters. The limiters are used to protect the network analyzer if the transistor starts to oscillate. The test circuit consists of an input and output, A01, and is already de-embedded to obtain the S-parameter values of the transistor. The output is connected to an attenuator for measuring on-state, purple box. The transistors are measured off- and on-state. A drain voltage of 28 V is applied during off-state analysis, red box in figure 3.5. During on-state, the gate voltage is increased until a drain current of 700mA is established. An Idq of 700mA is used because the transistor will be used in class AB with an identical Idq. The data is saved and analyzed afterwards using software program ADS 2019.

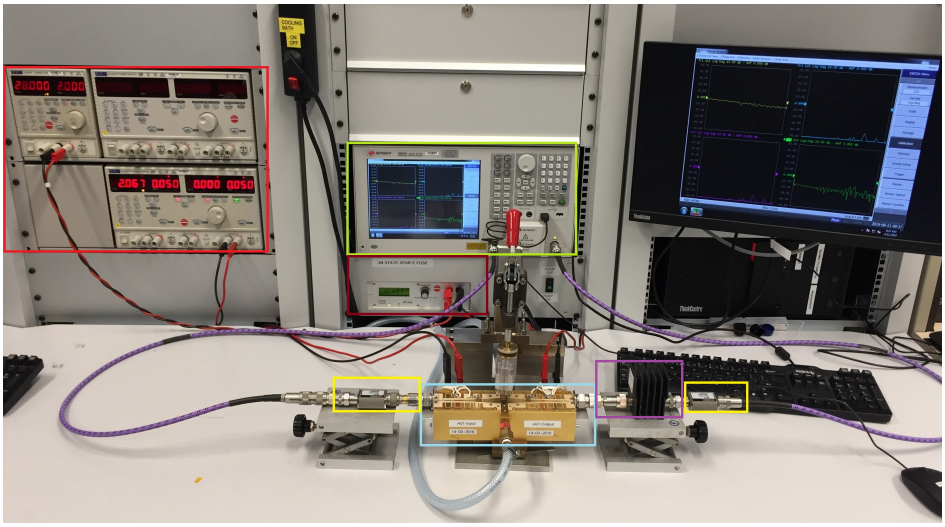

Figure 3.5: Setup for measuring on- and off-state S-parameters

3.3.4 RF Power sweeps

RF Power sweeps provide insight of the LDMOS and board under actual (pulsed CW) RF conditions. In this study, the power sweeps are used for verification of the model and to determine the P1dB point of the transistor. The P1dB point is the point were the gain drops with 1 dB. A signal generator, yellow box in 3.6, is connected to a signal amplifier, red box. The output of the signal amplifier is connected via a coax cable to the circulator, green box. The circulator is a 3-port device with one port connected to 50 ohm. The signal generator/amplifier is protected from the circuit during mismatch because of the circulator. The purple box in the figure is the coupler. The coupler is used to measure the input and reflected power via power sensors. The input coupler is connected to the measurement circuit, N2385. A pressing probe is used to fix the transistor. The transistor is cooled with water to a temperature of 25 degrees. The output of the circuit is connected to the Maury tuner, pink box, which will be used for VSWR measurements. The tuner is hidden inside

the setup in the pink box. The Maury tuner is set to a 50 ohm line condition, which makes it transparent. The output of the Maury tuner is connected to an attenuator, blue box, which will be used for dissipating the power. The output of the attenuator is connected to a power meter, brown box, which will measure the output power. A bias connector is connected to the circuit which applies the drain voltage and controls the DC gate voltage.

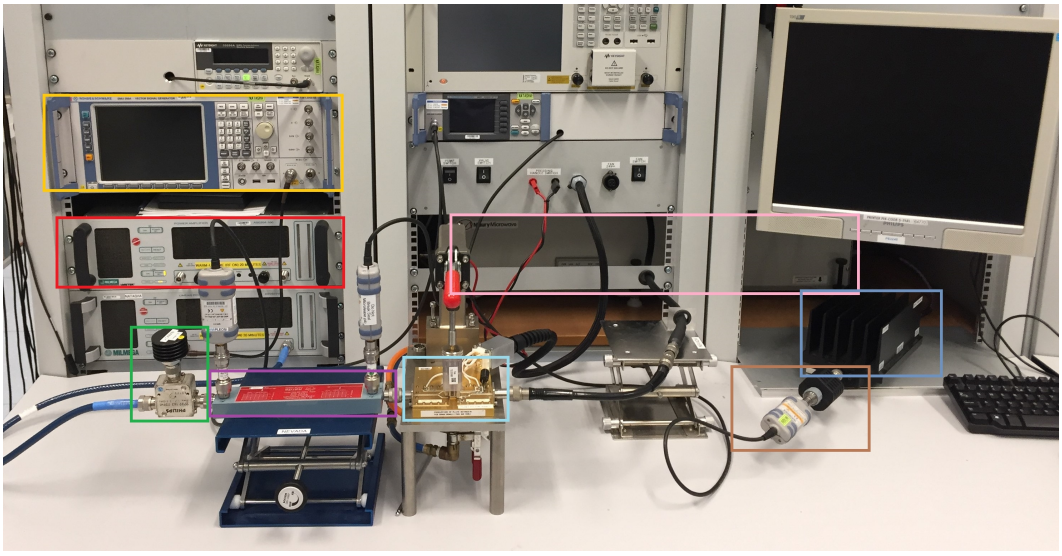

Figure 3.6: Setup for measuring the ruggedness of the packaged transistors

A testplan is executed during the powersweep measurements. The DC bias settings with a drain voltage of 28 V and a drain current of 700 mA are set in the testplan. A drain current of 700 mA is used for operation in class AB. The transistor are measured with a continuous wave (CW) pulsed signal. A CW-pulsed signal is used to reduce the influence of temperature. A pulse-width of $100us$ with a dutycycle of 10% is used for measuring the powersweeps.

3.3.5 VSWR

The VSWR measurements are a key element to find the desired relation between TLP and VSWR. The packaged transistors are measured at the P1dB points measured during by powersweep. The VSWR measurements are also executed with a CW-pulsed signal to minimize the influence of the temperature on the results.

The setup is almost identical to the setup used for measuring the power sweeps. The Maury tuner is in this case not shorted during the VSWR measurement. The Maury tuner is capable of applying different load impedances to the output. Maury tuner is calibrated at a certain frequency. A testplan is needed to set the magnitude of the mismatch. The Maury tuner will rotate through all the phases at this magnitude. The maximum mismatch which can be achieved by the Maury tuner is 15:1.

All measurements are executed with a mismatch of 10:1. Instead of increasing the mismatch, the supply voltage is increased starting at $28V$ for the LM8+ process. The P1dB points were determined at each supply voltage starting at 28 V and increasing with 2 V.

The testplan consists of four sequences. The first sequence, DC sequence, regulates the biasing of the transistor and the supply voltage. The second sequence is a powersweep. The third sequence is the mismatch sequence. The mismatch magnitude can be controlled and the pulse width and length. The pulse width is set to $100us$ with a dutycycle of 10%. The input power is the power needed to get an output power at 1 dB compression. The input power is constant during the mismatch sequence. The last sequence, sequence four, is a powersweep. The powersweep can be compared with the power sweep before the mismatch to see whether the device is degradated. A device passed the mismatch sequence if the deviation of the performance after the mismatch sequence is less than 10%. The supply voltage is increased and the transistor is remeasured at a new supply voltage.

Figure 3.7: Maury tuner used for VSWR measurements

Chapter 4

Transistor model

This chapter presents the modelling of the LDMOS transistor. A model which describes the the full circuit under both normal RF operation as well as VSWR conditions will give more insight in the current flows and voltages inside the transistor which cannot be measured directly. The matching steps inside the transistor and at the RF production board were already designed. The measurements, as indicated in figure 4.1, are executed to build up the model from the die to a complete transistor. The described method in this chapter is applied to the LM8+ process but can also be used for other technologies and processes.

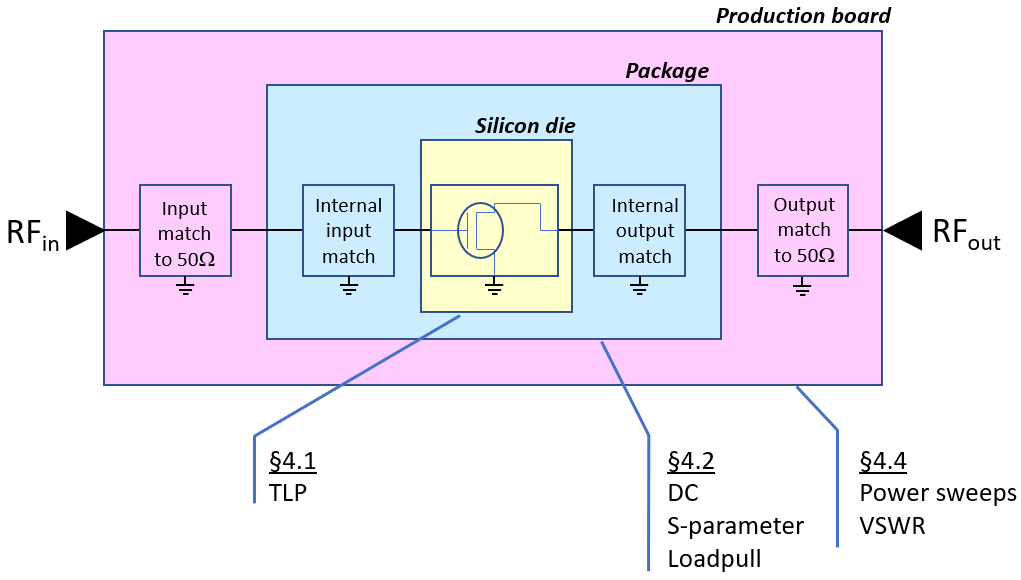

Figure 4.1: Overview of the executed measurements to model the transistor

4.1 Transistor die characteristics

The starting point of the model are the DC parameters. These parameters are the transconductance (g_m), maximum current (I_{dsx}), knee-voltage (V_{knee}) and threshold voltage (V_{th}). The parameters are measured at the transistor using the μParset as described in Chapter 3. A mathematical model consisting of formula's describing the parameters of the transistor is used to fit the DC measurements [7]. The g_m and the $I_d - V_d$ characteristics can be almost perfectly fitted to the measurements, figure 4.2. The I_{dsx} sets the maximum current in the $I_d - V_d$ curve. Both curvatures will be shifted when the threshold increases or decreases. The slope can be changed by changing the transconductance of the transistor. The values of the threshold voltage and the transconductance deviates from the typical values of a $120mm$ W_g transistor, as listed in [15]. The deviations are probably caused by simplifications of the formula's of the transistor in the model.

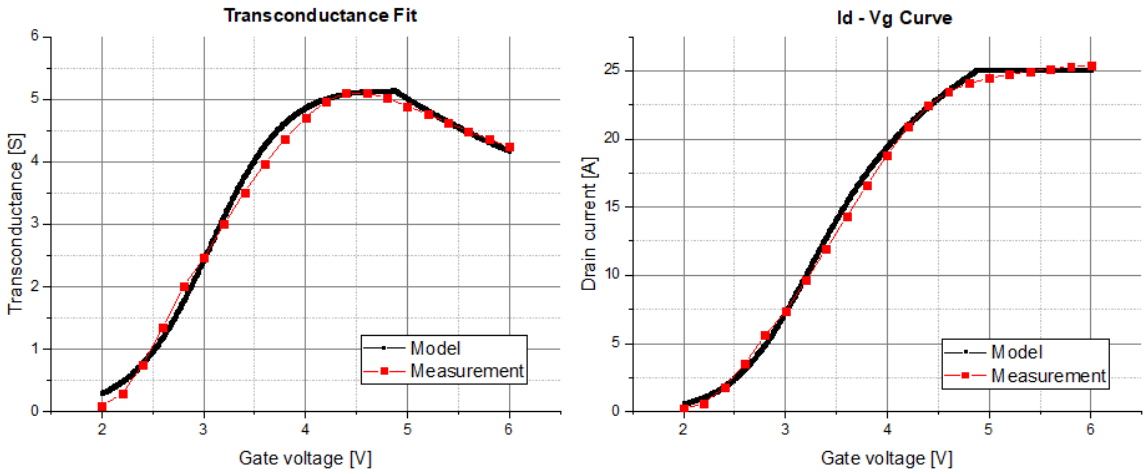

Figure 4.2: DC Fit of the g_m and the $I_d - V_d$ characteristic for the LM8+ process

The IV characteristics are used to fit the knee voltage of the transistor. The IV curves of the measurements and the model are shown in figure 4.3. The IV curves of the model correspond with the IV curves of the measurements.

An important part of the model are the characteristics above the breakdown voltage. The characteristics are measured by TLP measurements on a TLP structure. This structure has a W_g of $3.712mm$, the transistors for the VSWR measurements have a W_g of $120mm$. The $I_d - V_d$ curves of the TLP structures are scaled to the products by scaling of the current. The model includes the $I_d - V_d$ characteristics by addition of a linear equation to the model which can be fitted to the $I_d - V_d$ curves above breakdown. The slope of the equation can be fitted to the measurement.

The snapback point, maximum current and voltage before a failure occurred, has not been added to the model because this will cause convergences issues. The

snapback point has to be taken into account at the VSWR simulation manually by plotting the die voltage. The $I_d - V_d$ curves above breakdown are measured at zero gate voltage. The model will not include the complete $I_d - V_d$ curves with a biased transistor. A simplification is made by assuming that the $I_d - V_d$ curves above breakdown does not depend on the biasing of the transistor.

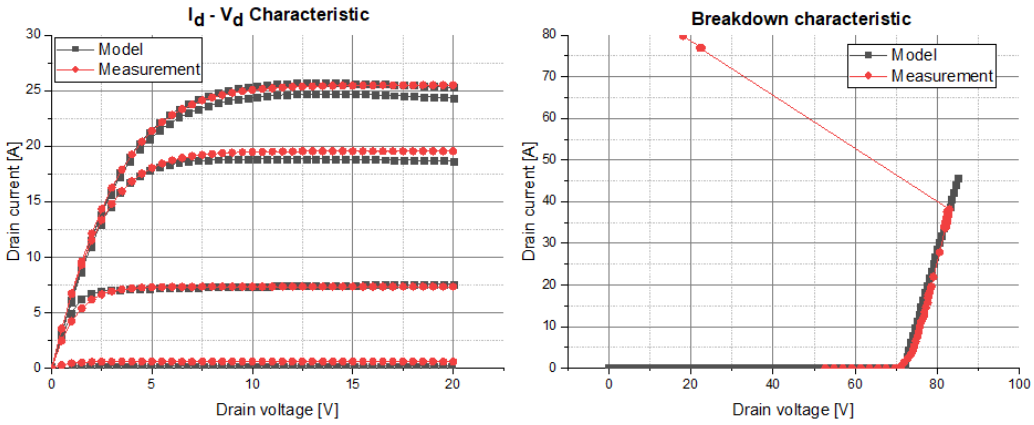

Figure 4.3: DC Fit of the $I_d - V_d$ curves for a V_{gs} of 2,3,4,5 and 6 V in the left figure and in the right figure the $I_d - V_g$ fit for the LM8+ process

The parasitic capacities are added to the model of the silicon die because these are intrinsically present in the die and will influence the matching of the transistor. The capacities have typical values for each technology, [15]. The values are evaluated by on-wafer capacitance measurements. The voltage dependence of the feedback capacitance is small. The feedback capacitance and the gate-source capacitance are modelled without a voltage dependency because the voltage dependency will have little influence on the VSWR simulations. The output capacitance is replaced by a voltage dependent capacitance because it strongly depends on the output voltage and will therefore influence the matching and VSWR. The capacities will have losses due to non-idealities and are modelled by resistances, figure 4.4

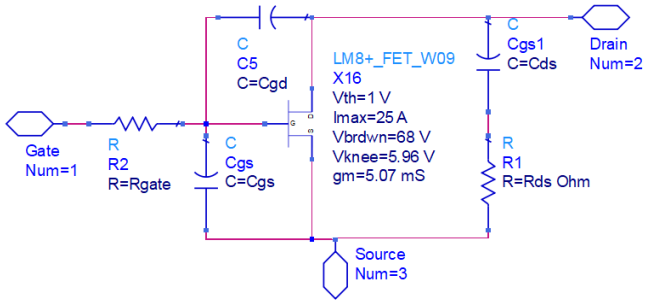

Figure 4.4: Schematic of the transistor die with input, output and feedback capacities

4.2 Characteristics of the packaged transistor

The die of the transistor is placed inside a package with internal in- and output matching. The matching steps are important for VSWR measurements because they will transform the mismatch at the output to a mismatch at the die. It is therefore important to include the matching steps and parasitics of the package to the model. The impedance of the in- and output over the frequency is measured by S-parameters. The S-parameters are used to match the impedance of the model with the measurements. Figure 4.5 displays the components needed to model the packaged transistor. An LC-network at the input is used as a first matching step. The inshin inductance at the output is included to create the shunt-resonant circuit at the fundamental frequency.

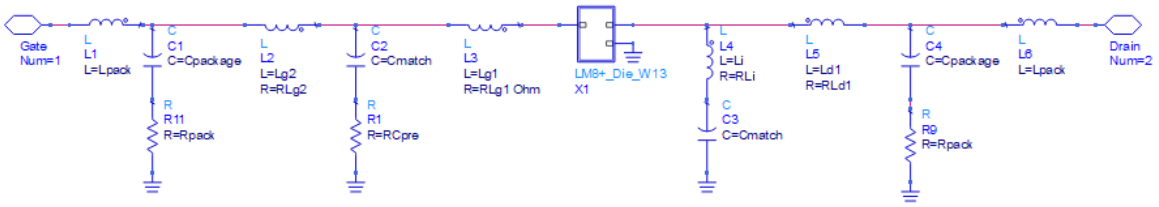

Figure 4.5: Schematic of the transistor model including the packaging, internal matching and the bondwires. The transistor die is shown in figure 4.4

The magnitude of the open-circuit in- and output impedance of the model are fitted over the frequency, figure 4.6. The values of the matching capacitance at the in- and output were already known. First, the bondwires at the in- and output are matched. At the input, the inductance L_{g1} will change the peak horizontally at about 2 GHz, the curvature can be lifted vertically by changing the inductance L_{g2}. Changing the inductance of the Inshin at the output will shift the peak at about 1.8 GHz horizontally. The complete curve can be shifted vertically by changing the inductance L_{d1}. The packaging parasitics at the in- and output influences the peak at 8 GHz. The gate and drain resistances are modelled by fitting the heights of the peaks at 2 GHz.

The curvature of the model fits perfectly with the curvature of the measurement except at the input below 1 GHz, this is probably due to imperfections of the measurement setup. The work frequency of the transistor is at 1.805 GHz, deviations below 1 GHz will not affect the the results of the model.

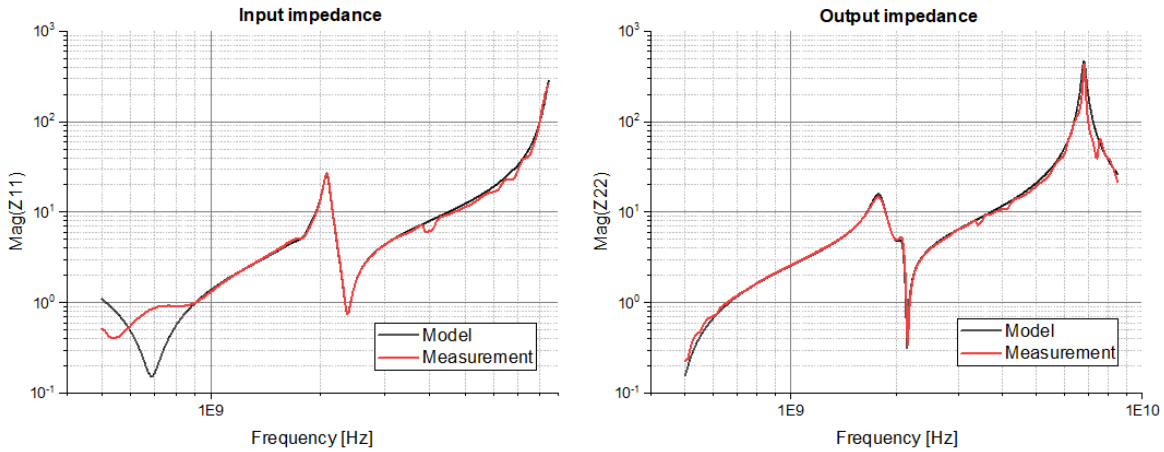

Figure 4.6: Matching of the open-circuit input and output of the transistor

The bondwires are coupled via an electromagnetic field with each other. The coupling of the bondwires is modelled after fitting of the inductances and parasitics. The open-circuit transfer impedance from port 1 to 2 (Z_{12}) is plotted in a polar plot in figure 4.7. The model can be fitted to the measurement by changing the coupling of the bondwires. The fit of Z_{12} does not match completely with the measurement but the coupling between the bondwires is a second order effect and will therefore not influence the VSWR results drastically.

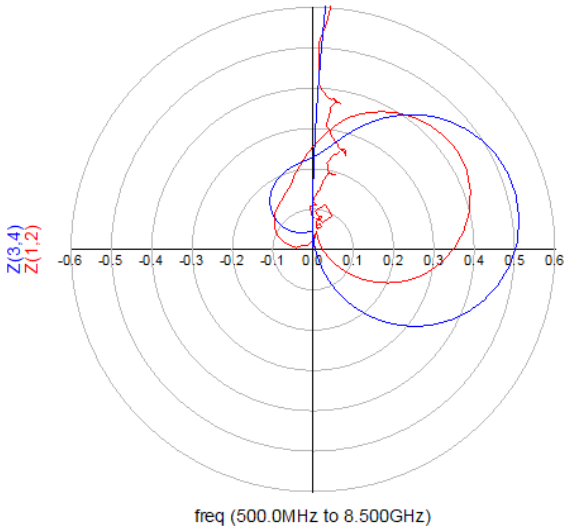

Figure 4.7: Polar plot of the open-circuit transfer impedance Z_{12}

4.3 Verification of the transistor model

A complete model of the transistor is build up from the die to the package. Load-pull measurements will give insight into the performance of the transistor. During

loadpull, powersweeps are measured/simulated at the selected load impedances. The efficiency, gain and output power can be extracted from these power sweeps. A correct model will obtain equal performances at an equally impedance. The loadpull measurements was already executed and is now compared with the loadpull simulations of the transistor model.

The efficiency and gain at 3 dB compression of the powersweeps simulations are shown in figure 4.8. Each single point represents the 3 dB compression point of a powersweep at a certain load impedance measured at a single transistor. The graphs shows that there is a trade-off between the maximum power and maximum efficiency. Both maximums can not be achieved at a single impedance.

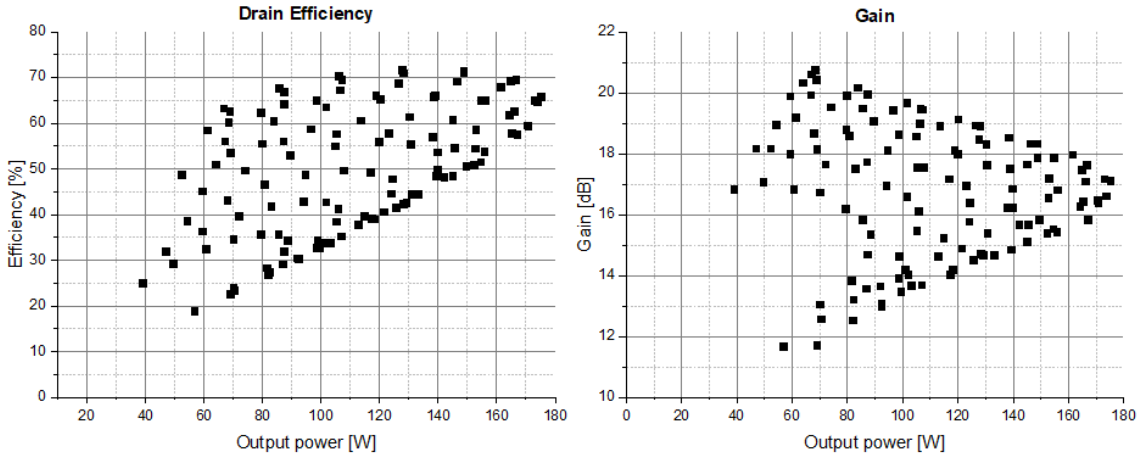

Figure 4.8: Maximum efficiency and gain at 3 dB compression

The graph is used to find the impedance at the maximum power and efficiency. The parameters of the loadpull measurements and simulations at 1 and 3 dB compression are listed in table 4.1 and 4.2 respectively.

Table 4.1: Comparison loadpull simulation and measurement at P1dB

	Gain (dB)	Eff (%)	Power (W)	Zload
Peak efficiency				
Model	21.41	71.7	111.3	2.4 - j2.9
Measurement	22.1	70.5	87.8	3.5 - j2.1
Peak Power				
Model	19.65	64.8	154.3	1.4 - j3.6
Measurement	19.3	60.1	149.2	1.7 - j4.0

Table 4.2: Comparison loadpull simulation and measurement at P3dB

	Gain (dB)	Eff (%)	Power (W)	Zload
Peak efficiency				
Model	21.4	71.7	127.5	2.4 -j2.9
Measurement	21.7	72.2	114.9	3.2 - j2.7
Peak Power				
Model	20.0	65.9	175.2	1.5 - j3.9
Measurement	18.9	59.7	177.9	1.5 - j4.2

The load impedance at the maximum power point matches the measured load impedance. There are small deviations at the maximum efficiency but these are due to a flat maximum efficiency line, figure 4.8. The maximum efficiency is almost a flat line over the output power, small deviations in the maximum efficiency point will result in large corresponding output powers. The impedance of the maximum power is therefore more important and these fits nicely with the measurements. Deviations of 10 to 20 % are acceptable. The efficiency, gain and power are all within this margin. The input impedance of the model is $1.45 + j5.88$, there was no data to compare the input impedance of the model with the measurements.

The loadpull data of the model corresponds with the measured loadpull data. The model can now be used to display the current waveforms inside the transistor and the voltages at different nodes.

4.4 RF production board modelling

Harmonics will influence the behavior of the LDMOS during normal operation and during mismatch. The production board takes care of the harmonic content by including a quarter-wave short-circuited stub in combination with a capacitance to short the even harmonics. The part of harmonic content in a circuit cannot be easily measured. The amount of harmonics during simulations should correspond with the measurements because harmonics can cause large voltage swings even above breakdown. The RF production board is therefore modelled to create a complete PA.

The PA used for measuring the transistors was already designed but a model was not available. The dimensions of the striplines at the production board are measured and added to the model. The ideal capacities are replaced by non-ideal capacities. The complete model of the PA including the transistor is shown in figure 4.9.

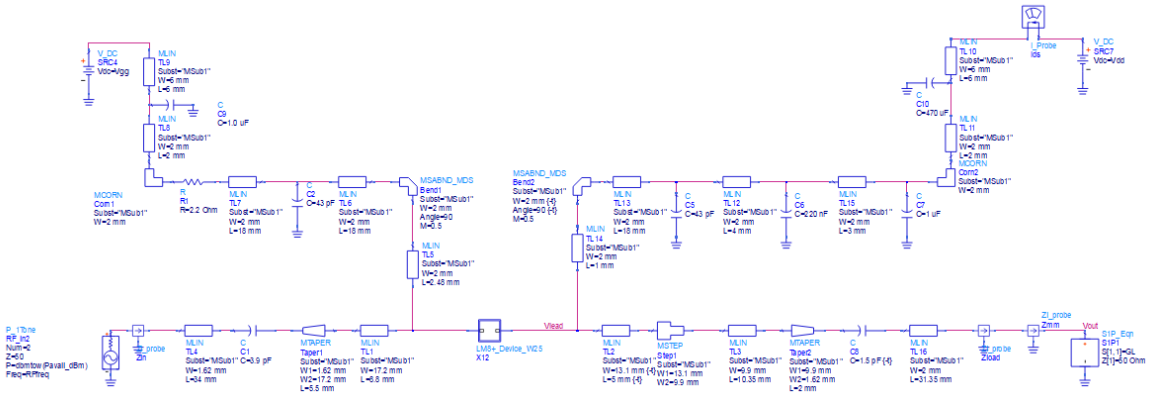

Figure 4.9: Complete model of the RF production board including the transistor model

Impedance probes are added to the model to simulate the impedance at the lead of the in- and output circuit which is transferred to 50 ohms. The impedance at the in- and output should correspond with the desired impedance extracted from the loadpull data. The input impedance at the lead of the production board is $2.24 - j5.8$. The input impedance of the transsitor at the die is $1.45 + j5.88$. The resistive part does not perfectly match. The reactance of the impedance does fit nicely and are their complex conjugates which is needed for optimal power transport.

4.5 VSWR simulations & measurements

A complete model of the transistor including the production board is created and can be used to simulate VSWR conditions. Only a few parameters such as the output power, dissipated power, supply current and phase are logged during VSWR measurements. The logged parameters of the VSWR measurements are compared with the simulations. The model should describe an equal behavior of the parameters at an equal phase of the mismatch.

The supply current and the output power are plotted versus the phase of the mismatch in figure 4.10. The phase of the simulation is shifted to fit the simulation to the measurements. In certain phases, below 35 and above 200 degrees, the supply current of the model has an offset of about 1A compared with the measurement. This offset could be due to simplifications of the IV curves of the model. The model can be improved by including the complete IV curves but it turned out that for the relation between VSWR and TLP these deviations at these phases are not important.

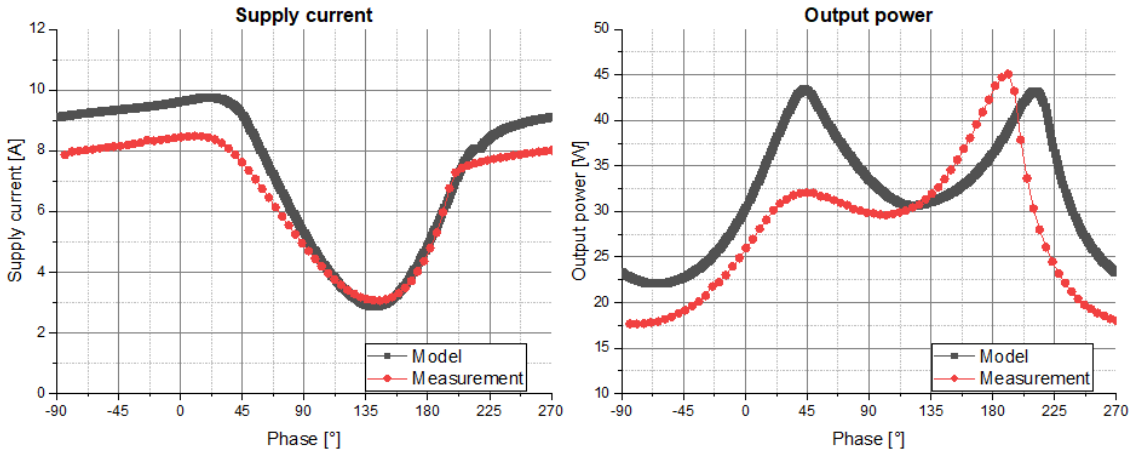

Figure 4.10: Comparison of the logged supply current and output power versus mismatch phase at a supply voltage of 28 V

Although there is a small deviation of the current at certain phases, the magnitude of the model does correspond with the measurements. An equal shape of the graph at an equally phase is also obtained. The model can therefore be used to give insight into the current flows and voltage inside the transistor and on the production board at matched and mismatched conditions.

Chapter 5

Results

This chapter presents the results of the measurements and simulations. First the IV characteristics in breakdown measured using TLP are analyzed. The model is used to display the current flows and voltages at different nodes inside the transistor. These currents and voltages are compared with the IV characteristics to find a relation between VSWR and TLP.

5.1 IV characteristics in breakdown

The IV characteristics in breakdown are measured by TLP as described in chapter 3. Three transistors of each variant, as listed in Appendix A, are measured. The IV characteristics of the transistors of the same wafer are perfectly on top of each other. The curves in breakdown are displayed in figure 5.1.

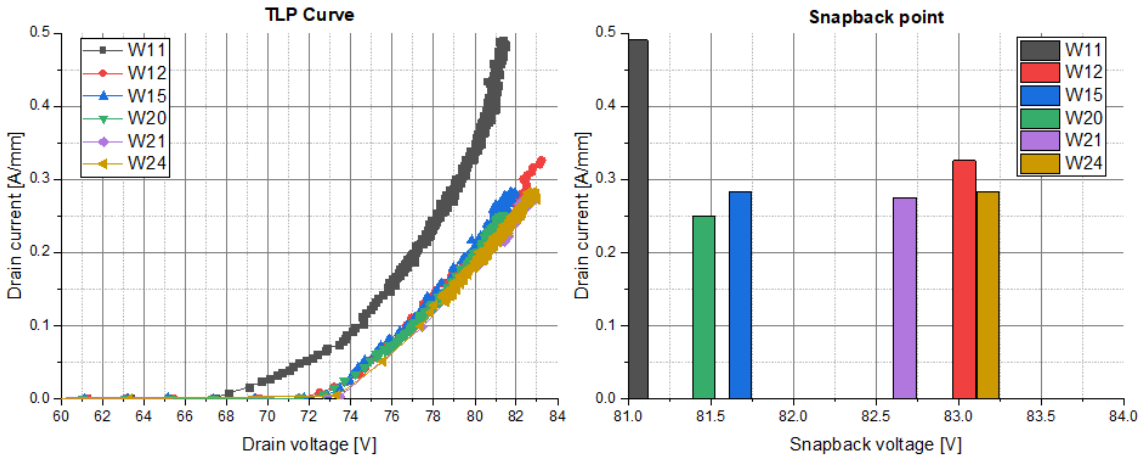

Figure 5.1: IV curves of the different variants of the LM8+ process

The differences in the maximum current in breakdown between the variants with an epi-thickness of 2.9 and 3.3 μm are very small. These small difference will make it more difficult to find a proper relation. A relation between the maximum current

through the die and the epi-thickness can be observed. A smaller epi will result in a larger current. The amount of current which is sinked by the body diode can be controlled by varying the epi-thickness. The sinking of the current vertically through the epi diode is more controlled. A smaller epi can sink more current before the internal BJT is triggered which will result in a larger maximum current. The variant with the smallest epi, W11, shows a double slope instead of a single slope for the other variants. Probably, the current will start to flow vertically through the epi until a certain voltage is reached. Above this voltage the current will also starts to flow horizontally through the LDMOS.

5.2 VSWR measurements & simulations

The designed model can be used to simulate the current flows inside the transistor during normal operation (50 ohm load) and during mismatch conditions. The VSWR measurements are executed as described in chapter 3. The load, applied to the RF production board, is varied from capacitive to inductive when going through all the phases with a constant VSWR of 10:1. The resistance and reactance of the impedance versus the mismatch phase are shown in figure 5.2.

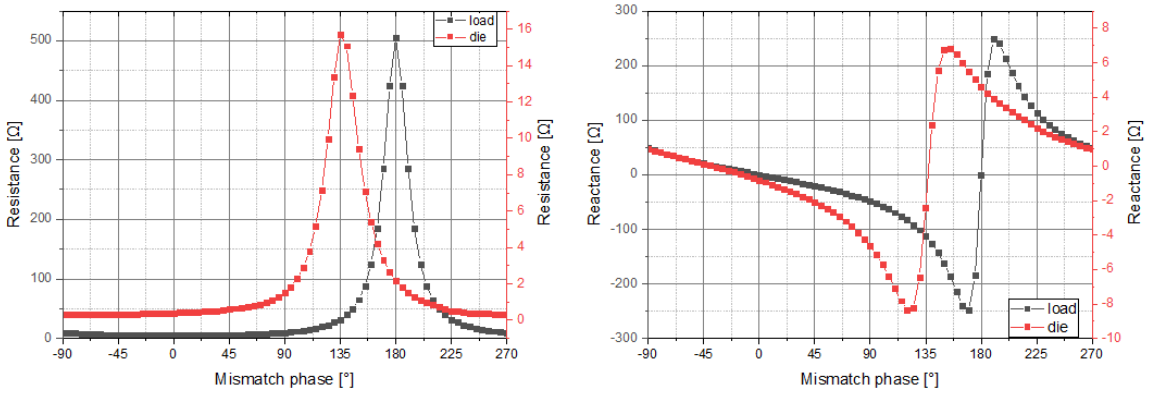

Figure 5.2: Plot of the real and imaginary part of the impedance at the load and the die of the transistor

The mismatch impedance changes due to the matching steps of the circuit and the internal matching. The phase is about 45 degrees shifted due to these matching steps. The amplitude has reduced drastically for both the resistance and the reactance at the die compared with the load. The inductive and capacitive region are visible in the graphs. The reactance is positive in the inductive region and negative in the capacitive region. A constant VSWR of 10:1 is applied to the output, the VSWR at the die is reduced to 1:7. The VSWR is calculated at four different points in the Smith chart.

The transistors are measured as described in chapter 3. The supply voltage is increased until a failure of the transistor occurred. The supply voltages at which a failure of the transistor occurred is shown in table 5.1.

Table 5.1: The supply voltages of the VSWR measurements at a failure of the transistor

Wafer	VSWR supply voltage [V]	epi thickness [μm]	ED2 implant
09	44	2.5	1.6
13	38	2.9	1.6
16	36	2.9	2.0
18	34	3.3	2.0
22	34	3.3	1.6
25	40	3.3	1.2

There is not a clear relation between the epi thickness or ED2 dose and the VSWR results. A trend between the epi thickness and the VSWR supply voltage seemed to be there but W25 with the thickest epi does not follow that trend. The phase of the mismatch is logged during the measurements. The mismatch phases at which a failure occurred is shown in figure 5.3. A failure of the transistor occur between the 60 en 180 degrees. The reactance and resistance of the impedance at the die changes drastically. A failure of the transistor is therefore related to these changes.

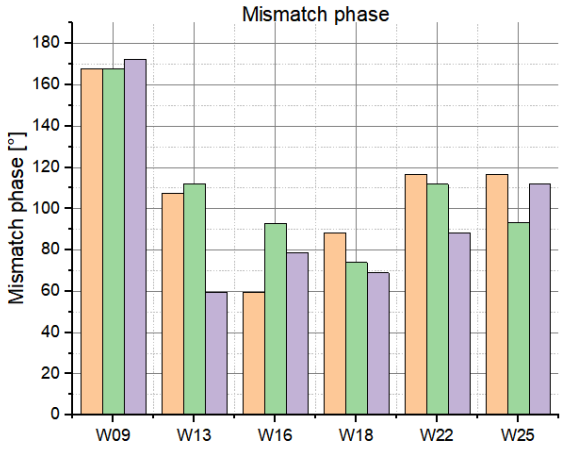

Figure 5.3: Plot of the mismatch phase were a failure of the transistor occurred for the different variants

A similar phase range can be observed at the supply current versus the mismatch phase, figure 5.4. The graph displays the drain current versus mismatch phase at

different supply voltages. The lowest supply current curve has a supply voltage of 34 volt. The highest curve is the curve were a mismatch occurred at a supply voltage of 42 volt. The red curves are the measurements and the blue curves the model.

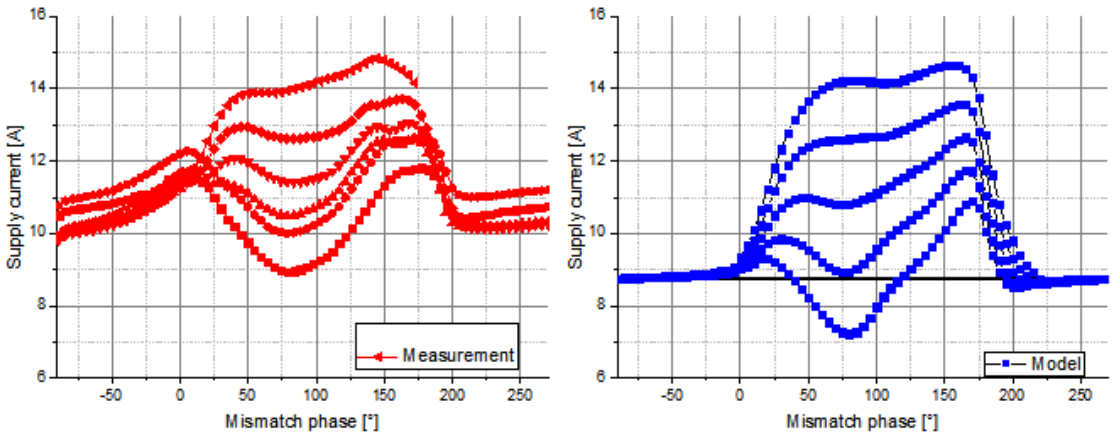

Figure 5.4: Supply current versus the mismatch phase, the red line displays the measurements and the blue line is obtained by simulations

The model will give more information about the current flows and voltages inside the transistor. The loadlines for a mismatch of 0, 135 and 200 degrees are shown in figure 5.5. The loadlines at 0 and 200 degrees are completely open and the voltage does not reach above the breakdown voltage. The loadlines closes gradually when the mismatch increases from 0 to 135 degrees. The loadline is closed at 135 degrees and gradually opens. During closing of the loadline, the voltage increases and follows the IV characteristics in breakdown. When the loadline opens, the voltage and maximum current decreases.

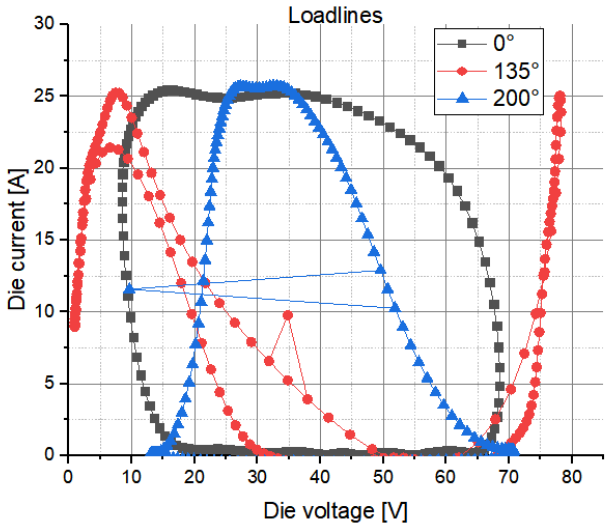

Figure 5.5: The loadlines at different mismatch phases

The maximum current is reached at a mismatch of 160 degrees. The phase at a maximum mismatch corresponds with the maximum reactance of the impedance at the die, figure 5.2. The maximum current is also visible in figure 5.6. The maximum current is the current in breakdown between the mismatch phase of 135 and 200 degrees. Below and above the 200 degrees, the loadline is open and the maximum current through the transistor is the I_{dsx}. The breakdown curve is also added in the figure of the die voltage. The voltage at the die is above breakdown between 0 and 200 degrees which corresponds with the variation in the supply current in figure 5.4.

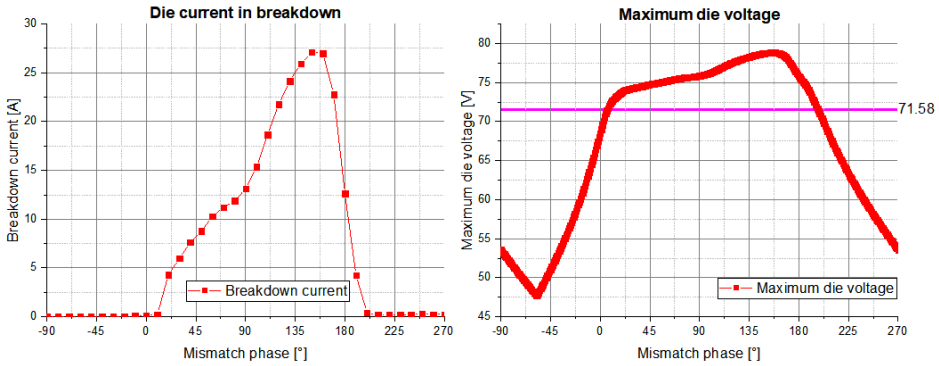

Figure 5.6: The maximum current through the transistor and the voltage at the die versus the mismatch phase

A transient analysis of the current through the transistor displays the breakdown region. Figure 5.7 shows the current through the transistor. The mismatch phase is fixed at 160 degrees, the current through the transistor is maximal. The supply voltage is increased from 28 to 38 V. 38 V is the supply voltage were a failure of the device occurred.

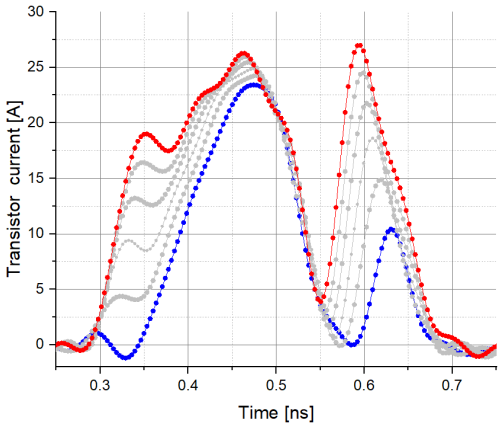

Figure 5.7: Transient simulation of the current through the transistor. Two regions are visible which are the normal region during normal operation and the breakdown region which appears during VSWR

The on-state and of-state of the transistor are visible in the graph. The I_{dsx} is reached during on-state of the transistor. The breakdown region appears when the gate voltage decreases. The maximum current increases drastically but also shifts horizontally. The shift of the maximum current in breakdown can be related to clipping of the die voltage. The die voltage for a supply voltage of 28 and 38 V is shown in figure 5.8. The breakdown voltage is also depicted in the figure. The die voltage is, at higher supply voltages, longer in breakdown. The die voltage is not a sinusoidal function anymore when the die voltage is above the breakdown voltage.

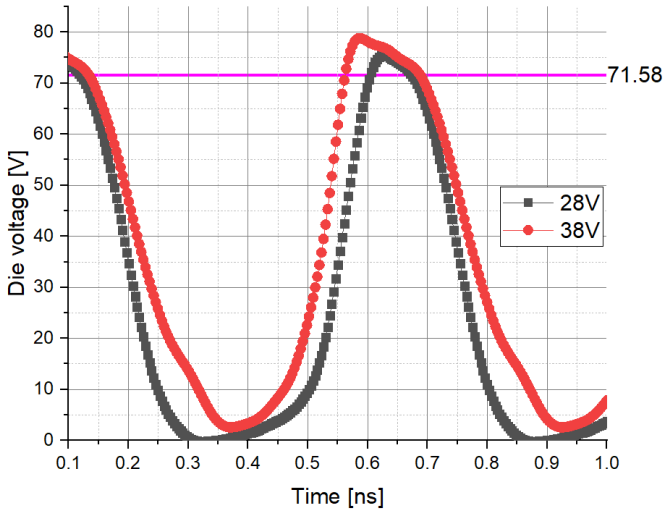

Figure 5.8: Transient simulation of the die voltage at a supply voltage of 28 and 38V

The die voltage is flattened above the breakdown voltage. The current through the drain-source capacitance is the derivative of the voltage across the capacitance. Due to the flattenning of the die voltage, no current will flow in the drain-source capacitance, figure 5.9.

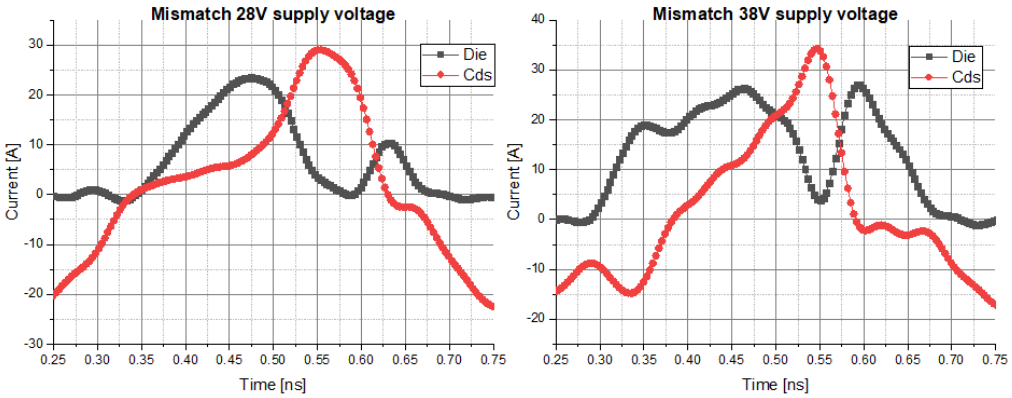

Figure 5.9: The current through the transistor together with the current of the drain-source capacitance at a supply voltage of 28 and 38 V

The current which should flow from the inshin inductor to the drain-source capacitance is flowing through the transistor. The current flowing through the transistor consists of the current flowing through the mismatch applied at the output and of the current of the inshin inductor which is not tuned out anymore due to the clipping of the die voltage above breakdown.

The breakdown region determines the ruggedness of the transistors. The maximum current in breakdown is reached when a maximum inductive load is applied to the die of the transistor. The current through the transistor consists of the current due to the applied load and the current due to the mismatch of the inshin inductor and drain-source capacitance.

The objective of this study was to find a relation between TLP and VSWR to predict the ruggedness of LDMOS transistors. Figure 5.10 displays the relation between VSWR and TLP. The maximum current capability of a transistor can be used as an indication of the VSWR. The supply voltage were a failure of the transistor occurred is plotted against the maximum current measured by TLP of the corresponding variants, red line. The VSWR model, blue line, displays the maximum simulated current through the transistor at breakdown at an equally supply voltage. An equal trend can be seen from the graphs. When the current capability increases, the VSWR supply voltage also increases which equals a more rugged transistor

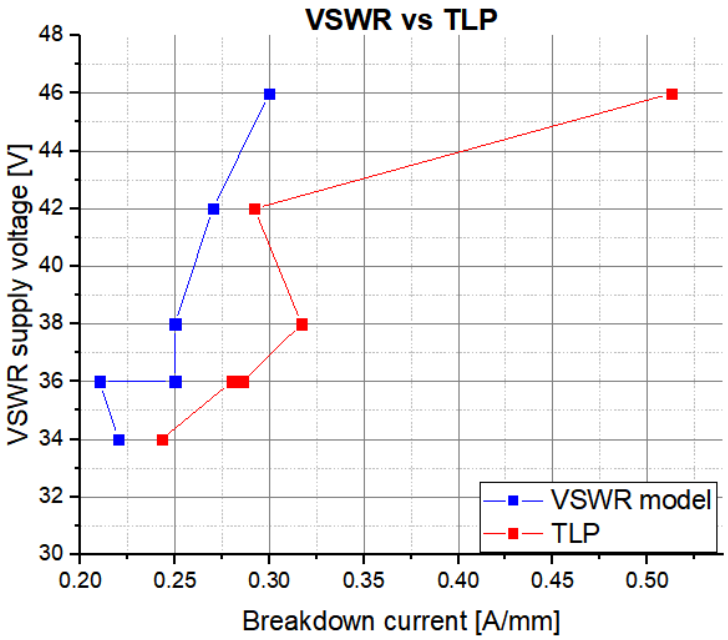

Figure 5.10: Relation between the supply voltage of the VSWR measurements and the maximum current in breakdown

A direct relation between the current through the LDMOS and the breakdown current measured by TLP can not be achieved. The breakdown currents measured

by TLP are within the uncertainty of the breakdown currents of the simulations. A uncertainty of 10% will give a VSWR supply voltage deviation of about 10 volt.

Chapter 6

Conclusion & Recommendations

A detailed model which could describe the operation of the LDMOS transistor in normal and mismatch conditions is created. The model is used to display the current flows and voltages at different nodes inside the transistor which could not be measured directly.

The model gave some interesting findings. All devices fail the mismatch measurement at a phase which corresponds with an operation in breakdown. The maximum breakdown current is achieved when the load is maximal inductive at the die of the transistor. Matching will transform the load from the output to the die. The load-line is closing when the load transfers from a capacitive load to an inductive load. An inductive load, which can be represented by an inductor, will try to keep the current flow constant. The current will therefore flow through the LDMOS. The voltage at the die will increase above breakdown which results in clipping. The output capacitance will not be matched with the Inshin inductance due to clipping. The current of the Inshin will not flow from the inshin inductance to the output capacitance anymore. The LDMOS will therefore sink the current. The total current through the LDMOS consists of the current due to a mismatch at the output and due to an unmatched inshin conductance.

A direct relation between the on-wafer TLP measurement and the VSWR measurement at the transistors could not be obtained. The variants in the breakdown current were too small to find a proper relation. A trend between the on-wafer TLP measurements and the VSWR measurements at product level is visible. Improving the current capability in breakdown will improve the ruggedness of the transistors. A maximum can be set to the current capability of the LDMOS. Increasing the current capability even further will not result in a more rugged transistor. Other failure modes as due to temperature effects could be triggered.

It is recommended to continue the examination of the LM8HV (50V) process in a follow up. This process has larger variations in the breakdown current and will give therefore more information for the relation between TLP and VSWR. Temperature

effects are not considered during VSWR measurements. The pulse-width can be changed to see whether the temperature does effect the VSWR results.

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Appendix A

Overview of variants

An overview of the different technologies are listed in A.1 and A.2. For the LM8^{+} technology, the thickness of the epi has been varied together with the drain extension implant. For the LM8HV technology, the drain extension implant has been varied.

LM8+ - CRA855 (30V)							
Wafer	Thick	Epi thickness			ED2 implant		
		2.5	2.9	3.3	1.2	1.6	2.0
11	x	x				x	
12	x		x			x	
15	x		x				x
20	x			x			x
21	x			x		x	
24	x			x	x		
9		x				x	
13			x			x	
16			x				x
17			x				x
18				x			x
19				x			x
22				x		x	
23				x		x	
25				x	x		

Figure A.1: Overview of variants of LM8^{+} technology with differences in epi-thickness and drain extension doping

LM8HV - F3CP10 (50V)						
Wafer		EDT				
	Thick	0.91	3.20	4.60	5.50	0.64
1	x	x				
2	x		x			
3	x			x		
4	x				x	
5	x					x
11		x				
12			x			
13				x		
14					x	
15						x

Figure A.2: Overview of variant of LM8HV technology with differences in drain extension doping