Design of a Current-Controllable AC Load for Static Energy Meter Testing

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***Abstract*—Today, no relatively cheap AC load exists which can purely arbitrarily draw current from an AC voltage source. A few exist on the market which, in general, are expensive and limited in the way current can be drawn. The need for this custom testing device, which needs to imitate waveforms from one or multiple appliances, arose to test static energy meters for measurement errors without swapping cables and devices. Additional waveforms can be generated to further test static meters, which enables the cause of error to be found more easily. The goal of this paper is to design a testing device on a conceptual level which meets these requirements. Simulations with actual waveforms are used to optimize and verify the conceptual design. Lastly, recommendations for the the physical design are given.**

I. Introduction

STATIC energy meters are continuously replacing their mechanical counterparts, which gave rise to erroneous readings and resulted in a higher electricity bill for consumers and companies. The University of Twente, together with Universitat Politècnica de Catalunya, companies and institutes, researches the reason behind these measurement inaccuracies. Recent studies [1][2][3][4] have shown that certain appliances will cause some static meters to show significant errors in their readings, despite them fulfilling harmonised standards [5]. Some meters show errors of up to 342%, depending on the appliance attached to it. These appliances all exhibit a non-linear way of drawing current, where errors have been correlated to parameters like current slope and phase firing angle. Measurements have been performed on these appliances, but so far no option exists to replicate these waveforms without actually attaching the appliance. Also, there is a need to arbitrarily draw current to see what causes the static meter to give erroneous readings, by generating current waveforms. This will enable a quantitative analysis on what current waveform parameters cause measurement errors, such that consumers and companies may be billed properly in the future. The design of this device follows from parameters of waveforms which are known to cause faulty readings, thus these parameters form a basis for the requirements of the device. The extraction of the relevant parameters will be done with Matlab. Then the technical background of a basic DC load, and why this circuit does not work for AC, will be discussed. Next to that, a more in depth look is taken at the design of a load and its design difficulties. The prototype design will then follow from this technical foundation and the circuit will then be simulated in LTspice. Afterwards, verification of the design will then be done with actual measured waveforms and is then coupled back to the Matlab script to verify the performance and requirements set by the parameters. Further development and realisation is out of scope for this paper, but all information given should give the reader enough details for the design of such a device. In the end, it enables an easier and a more structured approach on finding the cause of measurement errors in static meters.

II. Technical Background

The conceptual design will be made according to parameters of the current waveforms of appliances. These will set the requirements of the device, thus giving an indication the maximum voltage, current, power, etc. A basic load circuit will be discussed and an in-depth look is taken at individual components, such that suitable components can be chosen to form the AC load circuit. The impact of external parameters, like parasitic inductances, is analyzed as well, as it influences the slope of the current.

A. Requirements

Waveform data of problematic appliances has been used to set the requirements of the design. Researchers at the University of Twente provided this data, which contains the voltage between line and neutral and the differential mode current. The measurement equipment used are: a mains voltage monitor, the Pico TA189 and Pico PS4824 [6][7][8]. The bandwidth of the current probe is $100\,\mathrm{kHz}$, which means any frequency component above this frequency is attenuated and its impact therefore can not be determined. Table I shows the important waveform parameters and their extreme values, which a Matlab script has extracted from 61 different measurement data. These measurements come from appliances like water pumps, heaters or CFL/LED lamps and can be combined with a dimmer. Note that these values do not correspond to a single appliance, but are the maxima/minima of all the extracted parameters.

Voltage and current are trivial physical quantities for the design. These could have also been derived from the standard mains voltage level and maximum current, which are $230\,\mathrm{V_{RMS}}$ ($325\,\mathrm{V_{peak}}$) at $50\,\mathrm{Hz}$ and $16\,\mathrm{A}$ in the Netherlands [9]. However, the measurements show a higher peak voltage and current larger than a $16\,\mathrm{A}$. Other parameters are the crest factor (CF), power factor (PF), slew rate and power. The CF gives insight in how much the peak current deviates from the RMS value (1) and a higher value usually corresponds to narrower current pulses [10].

$$CF = \frac{I_{peak}}{I_{RMS}} \tag{1}$$

TABLE I
MEASURED WAVEFORM PARAMETERS

Voltage	Current	Pos. slew rate	Neg. slew rate	Crest Factor	Power factor	Average power	Peak Power
359.3 V	21.06 A	12.5 A/µs	−8.85 A/µs	13.58	0.061	821 W	5421 W

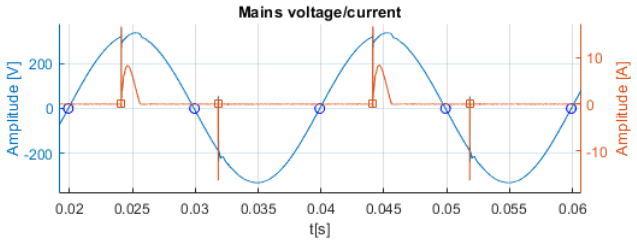

Fig. 1. Waveforms of a water pump in combination with a dimmer. This appliance has a highly non-linear way of drawing current.

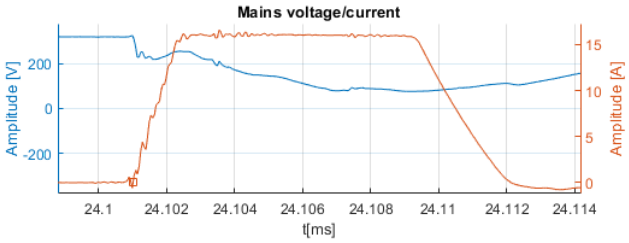

Fig. 2. Magnification of the first peak. Timescale of 2 µs/div.

Since the current waveforms of non-linear appliances are generally not a scaled, phase-shifted version of the voltage, a different definition of power factor is used [11]. This is given in equation (2).

$$PF = \frac{P_{active}}{V_{RMS} \cdot I_{RMS}} = \frac{\frac{1}{T}\int_0^T v(t) \cdot i(t)dt}{\frac{1}{T}\int_0^T |v(t)|dt \cdot \frac{1}{T}\int_0^T |i(t)|dt} \quad (2)$$

Together, the PF and CF can be used to give an indication of the location of a current pulse relative to the voltage and its narrowness. Slew rate is another important parameter, as it is a measure on how fast the device changes current in a certain amount of time. A higher slew rate makes it harder to design the circuit due to series inductance and resistance preventing a fast change in current. Slew rate is measured between 10 and 90% of a current pulse, so it does not give insight on what the waveform does between these levels, except for its average steepness. High frequency components can be superposed on top of the transition, which might actually result in the slew rate being smaller than the local dI/dt. It will be shown later on that current waveforms generally do not have a 'clean' edge. Average and peak power are mainly important for the selection of the transistor and the method of keeping it cool, since a load can be seen as a variable resistor where power is dissipated as heat.

Fig. 1 shows the voltage and current waveforms of a water pump in combination with a dimmer which has the largest slew rate of all appliances: 12.5 A/µs. This slew rate makes the waveform suitable for verifying the circuit in the end. It can be seen that the first period is similar to the second, but the current is not mirrored within the same period. Both the positive and negative cycle have a peak in current where the large slew rate is present. The first peak is enlarged and shown in Fig. 2. The width of the pulse is around 9 µs and peaks at almost 16 A. This relatively high current pulse can be problematic to replicate, due to parasitics in cables and in the circuit itself. Next to that, rising edge is not 'smooth', which requires a high bandwidth control loop. Other waveforms will be used as well for verification, but once the extreme case can be replicated, it can be assumed that other waveforms, with lower parameters, can be replicated as well.

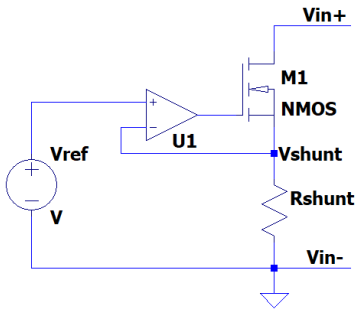

Fig. 3. Basic DC load circuit.

B. Basic load circuit

A basic constant-current DC load does not require a lot of components, but does not work for AC without modifications. However, this circuit, given in Fig. 3, still forms a basis for the rest of the design. A reference voltage is fed into the non-inverting input of the operational amplifier (op amp), which adjusts the output such that the voltage of the inverting input is equal to the non-inverting input. The transistor will be driven as a variable resistor by the op amp, such that the voltage at node V_{shunt}, which is $I_{shunt} \cdot R_{shunt}$, will be forced to be equal to the reference voltage [12]. Care must be taken that the gate voltage is high enough, because the shunt adds a voltage which needs to be overcome by the op amp.

This circuit only works for positive voltages, but mains voltage changes sign every half period. A diode bridge, placed at the input of the load circuit, solves this problem, but introduces a minimal voltage where current can be drawn. The total minimal voltage is dependent on circuit parameters and is a function of current through the shunt (3). For a relatively high current around zero crossings, low resistance components and low forward voltage diode must be chosen. Next to that, the reference voltage must be zero around the zero crossings to prevent the output of the op amp from clipping to the positive supply rail.

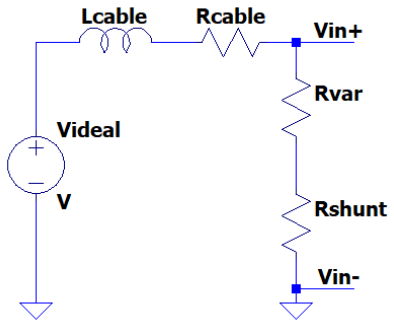

Fig. 4. Equivalent load circuit including cable parasitics.

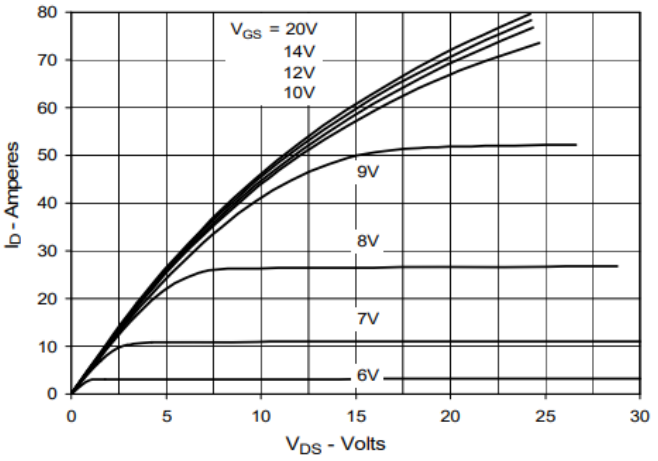

Fig. 5. Drain current vs drain-source voltage for different gate voltages for the IXTH30N60L2.

$$V_{min}(I_{shunt}) = 2V_f + I_{shunt}R_{DS(on)} + I_{shunt}R_{shunt} \quad (3)$$

C. Parasitic inductance

The cable going to the device contains parasitic inductances, which limits the current slew rate. An equivalent circuit is given in Fig. 4 and includes cable parasitics, transistor as variable resistor and a current shunt. The circuit equation is given by (4), and its time constant can be easily derived: $\tau = L_{cable}/R_{eq}$, where the equivalent resistance is given by: $R_{eq} = R_{cable} + R_{var} + R_{shunt}$.

$$I_{shunt} = \frac{V_{ideal}}{R_{eq}} - \frac{L_{cable}}{R_{eq}}\frac{dI_{shunt}}{dt} \quad (4)$$

The time constant can be used to derive an expression of the current slew rate, which is taken as an average over 0.5τ. During this time the current rises from 0 to $39\,\%$ of the steady-state current. Taking a relatively small fraction of τ gives the maximum current slew rate, but the average over a longer period gives a better approximation.

$$\frac{dI_{shunt}}{dt} = \frac{0.39I_{max}}{0.5\tau} = \frac{0.78\frac{V_{ideal}}{R_{eq}}}{\frac{L_{cable}}{R_{eq}}} = \frac{0.78V_{ideal}}{L_{cable}} \quad (5)$$

As can be seen, slew rate is now purely a function of input voltage and L_{cable}. Relatively low voltages prevent fast current changes, as well as a large cable inductance.

D. Power transistors

The main two functions of the transistor in a load circuit are to act as a variable resistance (i.e. voltage controlled resistor) and to dissipate the major part of the power. Due to the high voltage required and high slew rate, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are preferred. These days, most power MOSFETs are designed for switching applications where the main power dissipation takes place during transitions. Special transistors exist which are designed for linear operation where focus is laid on parameters like Forward-Bias Safe Operating Area (FBSOA) and thermal resistance.

MOSFETs for load applications are operated in the saturation region where the drain current (I_D) is almost independent on the drain-source voltage (V_{DS}). An example from the datasheet of the IXTH30N60L2 by IXYS [13], a MOSFET specifically designed for linear operation, can be seen in Fig. 5. A vertical line can be drawn for a fixed V_{DS} and it can be seen that the drain current increases in a non-linear fashion with the gate-source voltage (V_{GS}). This behavior is modeled by equation (6). A minimal gate voltage, the threshold voltage (V_{TH}), is required to turn on the device [14]. Therefore it is desired to force an offset voltage on the gate to enable a fast response.

$$I_{D,sat} = \mu C_{OX}\frac{W}{L}\frac{(V_{GS} - V_{TH})^2}{2} \quad (6)$$

In the ohmic region, where I_D is a function of V_{DS}, the drain-source resistance mainly determines the amount of current flowing through the transistor. Thus, there is less control over the MOSFET when large currents are required at low drain-source voltages.

The power dissipation can be relatively high, which can destroy a MOSFET if not handled correctly, even if cooled properly. Multiple transistors can be set in parallel, where each transistor shares a part of the current and power, but requires a separate control voltage due to manufacturing tolerances. Next to that, temperature differences will change MOSFET parameters like V_{TH} and the ON-resistance ($R_{DS(on)}$). The FBSOA diagram is important to verify a transistor's behavior for a certain amount of power [15]. The FBSOA in Fig. 6 of the MOSFET previously mentioned will again be used as an example. It shows the drain current vs the drain-source voltage, where a single point in the graph represents the power dissipated in the transistor. Three limits are present within this graph: the limit set by $R_{DS(on)}$, the DC line and the maximum voltage line. $R_{DS(on)}$ limits the amount of current at lower drain-source voltages, thus limiting the power. The DC line is given by the maximum power dissipation of the transistor and moves down with an increase temperature. The maximum voltage is set by the breakdown voltage of the transistor.

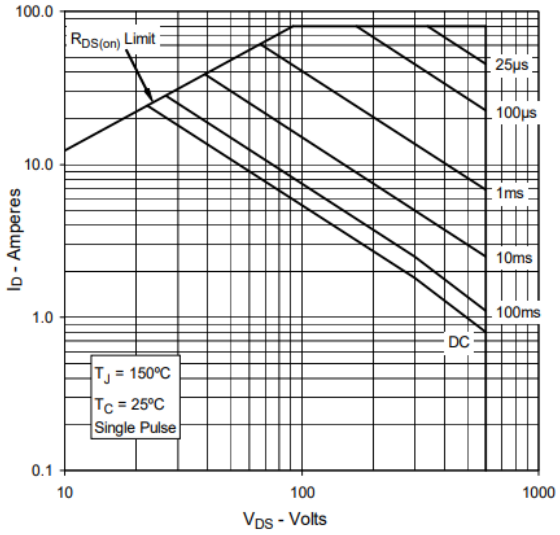

Fig. 6. Forward-Bias Safe Operating diagram of the IXTH30N60L2.

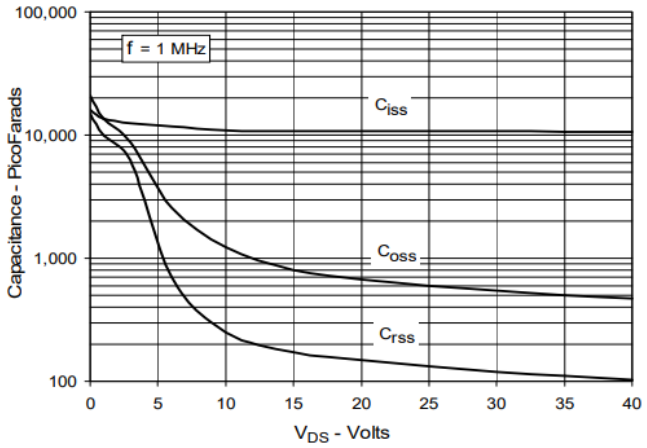

Fig. 7. Capacitances vs drain-source voltage of the IXTH30N60L2.

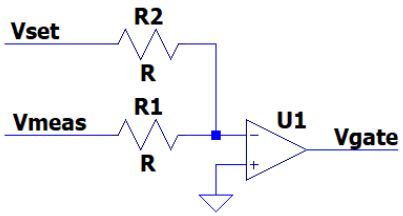

Fig. 8. Variant of a summing amplifier used to drive the MOSFET.

Shorter power pulses enable a higher power dissipation, but the DC line can assumed to be the worst case scenario for this application. Next to that, local temperature differences may cause the transistor to fail, even if operated inside the the specifications of this diagram.

The MOSFET input capacitance is the last parameter which is important in the design of a load. Higher capacitances slow down the responsiveness of the transistor, due to the charge that must be inserted at the gate to change V_{GS}. The input capacitance of a MOSFET is determined by the capacitance between gate-source and gate-drain and is given by: $C_{ISS} = C_{GS} + C_{GD}$ [16]. The gate-source capacitance barely changes with operating conditions, but C_{GD} becomes smaller with a higher V_{DS} [17]. This results in a lower input capacitance, as can be seen in Fig. 7. Less charge needs to be inserted for the same change in V_{GS}, making transistor more responsive at higher drain-source voltages. Fast current slew rates can only be achieved when the required charge is pumped into the gate in a relatively short time, i.e. the drive circuitry must be able to provide a relatively large amount of current.

E. Operational amplifiers

Op amps ease the design of analog electronics due to their linearity when run inside specifications. Two main op amp circuits are important for the design of a load: a variant on the summing amplifier and a differential amplifier [18].

The circuit given in Fig. 8 is used to drive the transistor, where its output is dependent on the set and measured currents, which are voltages. Note that there is no 'direct' feedback path between the output and inputs, as there is a transistor in the feedback path. The output does not change when the voltages at the inputs of the op amp are equal, which is at 0V. This is achieved with a negative V_{set}, such that the sum $V_{set} + V_{meas}$ is equal to zero. This only holds when $R_1, R_2 << R_{in}$, where R_{in} is the input resistance of the op amp. Resistors in series with the input voltages are mandatory to prevent a short and the resistors must be of equal size for the voltages to have equal weight. The output voltage of this circuit is described with $V_{out} = A_{OL}(-V_{set} - V_{meas})$, where A_{OL} is the open-loop gain of the op amp. This gain will be lower once the feedback loop is closed via the MOSFET and current shunt. It can be seen that the output voltage increases when $-V_{set} > V_{meas}$, which in other words means that V_{out} rises, thus increasing the gate voltage when the measured current is lower than the set current.

A differential amplifier is used to monitor the voltage across the current shunt. Parasitic resistance inside the circuit will raise the local ground potential at the shunt, resulting in a higher current reading. Therefore, the circuit in Fig. 9 is used to accurately measure the voltage over the current shunt. Its output voltage is given by equation (7) and is a scaled version of the difference between the input voltage, where the resistors determine the gain.

$$V_{out} = (V_{shunt+} - V_{shunt-})\frac{R_4}{R_3}, \text{ if } R_1 = R_3,\ R_2 = R_4 \quad (7)$$

As mentioned in the previous section, a large amount of current is needed to change V_{GS} in a relatively short amount of time. The output current of an op amp is therefore an important parameter, next to its ability to change the output voltage to at least reach V_{GS} in this time period. This is described with the slew rate of the output. Thus, a change in gate voltage is limited by the output current and slew rate. The response of the op amp is formed with the slew rate in combination with its bandwidth. A higher bandwidth results in a smaller settling time and the bandwidth is inversely proportional to

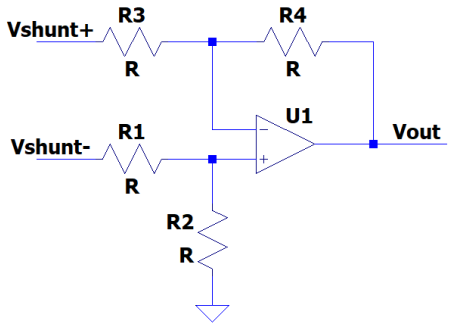

Fig. 9. Differential amplifier for shunt voltage monitoring.

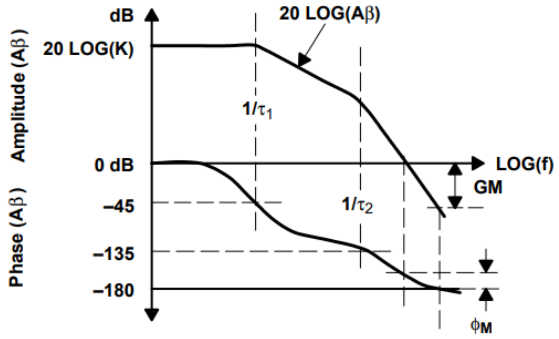

Fig. 10. Example of open-loop gain with added pole [18].

the gain. Determining the gain of the differential amplifier is very straightforward, but the gain of the circuit in Fig. 3 is more complex due to non-linearities in the feedback loop.

Instability issues may occur when an op amp is used to directly drive a capacitive load, e.g. C_{ISS} of the MOSFET. The op amp's output resistance (R_O) will form a pole in the transfer function, where its location is given by: $f_p = 1/(2\pi R_O C_{ISS})$. This pole will add $-20\,\mathrm{dB/decade}$ to the slope of bode plot, thus increasing the rate-of-closure. As a result, it moves the $0\,\mathrm{dB}$ intersection further to the DC point, as well as adding an additional $90°$ of phase shift around f_p. This can be seen in Fig. 10, where the open-loop gain of a generic, capacitively loaded op amp is plotted. The first bend point (at $-45°$) is due to the internals of the op amp, whereas the second bend point (at $-135°$) is at the location of the f_p. The phase margin (ϕ_M), also given in this figure, is reduced due to the extra phase shift created by the pole. A phase margin of $< 0°$ causes oscillations, whereas a phase margin between 0 and $90°$ causes overshoot and the percent overshoot decreases with ϕ_M [18]. The pole can be moved to a larger frequency by using a discrete or op amp buffer, due to a smaller R_O.

Compensation techniques exist where a zero, with the same frequency as f_p, is added in the transfer function such that it cancels the pole created by the capacitive load. However these techniques are not very practical when there is no fixed value for R_O and C_{ISS}, due to them varying over the operating range of the circuit.

TABLE II
CIRCUIT REQUIREMENTS

Operating voltage	$3.5 - 500\,\mathrm{V}$
Current range	$0 - 25\,\mathrm{A}$
Nominal power	$1\,\mathrm{kW}$
Peak power	$6\,\mathrm{kW}$
Current slew rate	$15\,\mathrm{A/\mu s}$ minimal
Bandwidth	$1\,\mathrm{MHz}$
Current control voltage	$-10\,\mathrm{A/V}$

III. PROTOTYPE DESIGN

Before the designing can begin, a list with requirements must be made. These will mainly follow from the requirements retrieved with the Matlab script. A list has been made with these requirements and is given in Table II, which will form the operating conditions of the device.

A. Design decisions

The device is limited in the way it can draw current, due to the workings of the load circuit. Operation is only possible in the first and third quadrant, where the sign of voltage and current is equal. Sourcing current requires an energy source inside the device and makes the design of such an AC load too complex. Replicating waveforms where power is sent back to the source is thus not possible with this device.

The operating voltage consists of an upper and lower limit. The lower limit has been previously defined in equation (3). With a diode forward voltage drop of $V_f = 0.7\,\mathrm{V}$, the budget voltage drop for the MOSFET and current shunt is $2.1\,\mathrm{V}$. At a maximum current of $25\,\mathrm{A}$, $R_{DS(on)} + R_{shunt}$ must be less than $84\,\mathrm{m\Omega}$ to stay within this budget. The upper limit is $500\,\mathrm{V}$ to allow for a safety margin to deal with parasitic inductance in the circuit inducing a high voltage during a fast negative slew rate.

The nominal power of the device is relatively high, and cooling is required as a result. Dissipating $1\,\mathrm{kW}$ in one transistor is generally quite difficult when it must be operated according to the FBSOA specification. Hence, the power will be shared among N load circuits, each drawing $1/N^{th}$ of the total current. In turn, this enables a higher $R_{DS(on)} + R_{shunt}$, because these components are essentially placed in parallel. Each MOSFET must still have its own driving circuit for multiple reasons. Firstly, it reduces the amount of current required to drive the gate, which will allow for a lower output current op amp. Secondly, it increases the robustness of the load circuitry by mitigating the effects of manufacturing variations and temperature differences between transistors. Thirdly, the capacitance seen by the op amp is also less, thus moving the pole created by the output resistance and gate capacitance to a higher frequency. This in turn increases stability due to an increased phase margin. The slew rate per circuit is now only $1/N^{th}$ of the required slew rate, as it is shared among the transistors, and therefore becomes more manageable. A higher shunt resistance can be chosen, which lowers the noise created by the differential amplifier, because a lower gain is required.

The minimal current slew rate is dependent on the parameters of the MOSFET, op amp and also the inductance

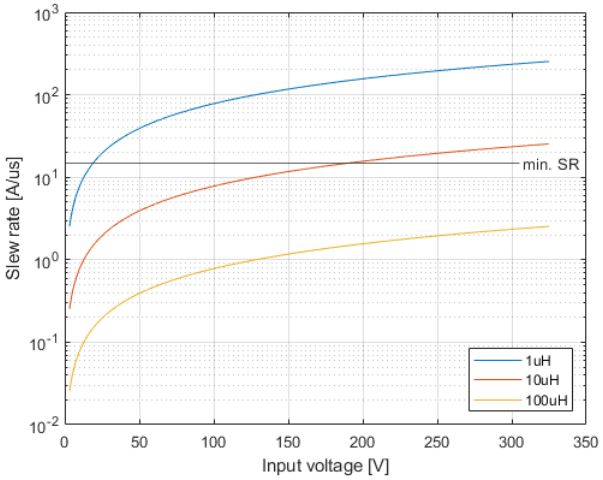

Fig. 11. Maximum slew rate for different parasitic cable inductances.

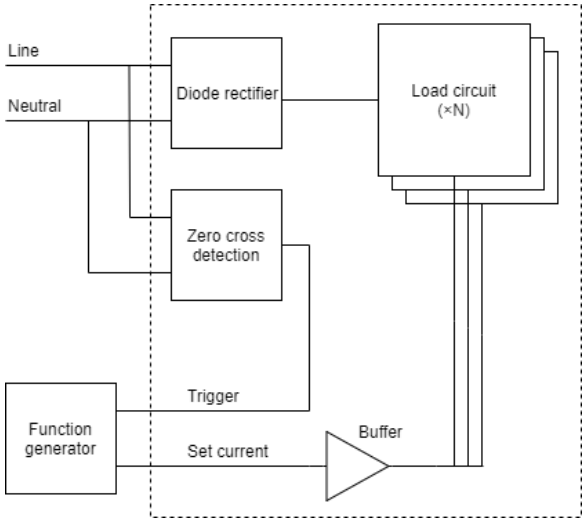

Fig. 12. Simplified functional block diagram.

of the line and neutral wires of the mains. For a certain current through the transistor, the threshold voltage must first be reached and the speed at which this is possible is mainly limited by the slew rate of the op amp and its output current. It is therefor necessary to bias the circuit with a relatively small amount of current such that V_{GS} is forced above V_{th}. This not only enables a faster slew rate, but also increases the bandwidth of the system due to the smaller voltage change required for the same change in current without the bias. In addition to that, the charge which needs to be injected in the gate is also lower for the same change in current. This lowers the minimal output current requirement of the op amp, as: $I_G = Q_G/\Delta t$ [19].

Using equation (5), a plot has been made with the maximum slew rate achievable for a certain parasitic cable inductance. This is shown for three different values in Fig. 11, where the minimal slew rate requirement of $15\,\mathrm{A/\mu s}$ is given as a horizontal line. The relation between input voltage, L_{cable} and slew rate can be clearly seen. The minimum slew rate is never reached for $100\,\mu\mathrm{H}$, whereas this requirement is only reached at around $200\,\mathrm{V}$ at one tenth of this inductance, emphasizing the effect L_{cable} has on the rest of the circuit.

The device will have a circuit which disables the load circuit if $|V_{in}|$ is under $3.5\,\mathrm{V}$ to prevent the user from drawing current at lower voltages. This is done by measuring the voltage input via a resistive divider and feeding this voltage into a comparator with Schmitt trigger which will pull down the inverting input of the op amp, disabling the circuit. The current is controlled via a voltage from a function generator, which makes the design easier. The current is set with $-10\,\mathrm{A/V}$, giving a maximum control voltage of $-2.5\,\mathrm{V}$. Since the input voltage is AC with a fixed frequency, the current waveform must be synchronized with this sinusoidal wave. This can be done with a zero cross detection circuit, including a Schmitt trigger to deal with multiple zero crossings caused by noise, that will send a trigger pulse to the function generator to start the waveform sequence. Preferably this is done once every period, because the current waveform may be different for the positive cycle, compared to the negative.

B. Block Diagram

Before a closer look is taken at the circuit diagram, the block diagram of the device is given in Fig. 12 to get a better understanding of the signal flows. The device is hooked up to an AC source with the line and neutral wires. This voltage is first rectified and then fed into the load circuits. The zero crossings of the AC source are detected using a Zero Crossing Detecion (ZCD) circuit, which sends a trigger pulse to the function generator. The function generator then supplies the current waveform and this is buffered and distributed among the load circuits. These will then draw current according to the waveform received by the function generator.

Linear Technology has published an application note on a high performance load, which has been used as a basis for the conceptual AC load circuit given in Fig. 13 [20]. The ZCD circuit has not been added, since triggering a waveform is not needed in a simulation. Next to that, parasitics have not been included in this circuit.

C. Component selection

Before components can be selected, the amount of load circuits must be determined. Parameters like current slew rate and power become smaller per load circuit as the amount of load circuits increases. This was chosen to be 10 to divide the power, current and slew rate by this amount and to ease the selection of a MOSFET, as more transistors will then fit the requirements. The resulting nominal power with 10 load circuits will thus be $100\,\mathrm{W}$ per stage with a maximum current of $2.5\,\mathrm{A}$. Now a transistor can be selected with the voltage, current and power parameters in mind. The previously mentioned MOSFET (IXTH30N60L2) has been selected for its maximum voltage, power, FBSOA and availability of a SPICE model. A few important parameters are given in Table III.

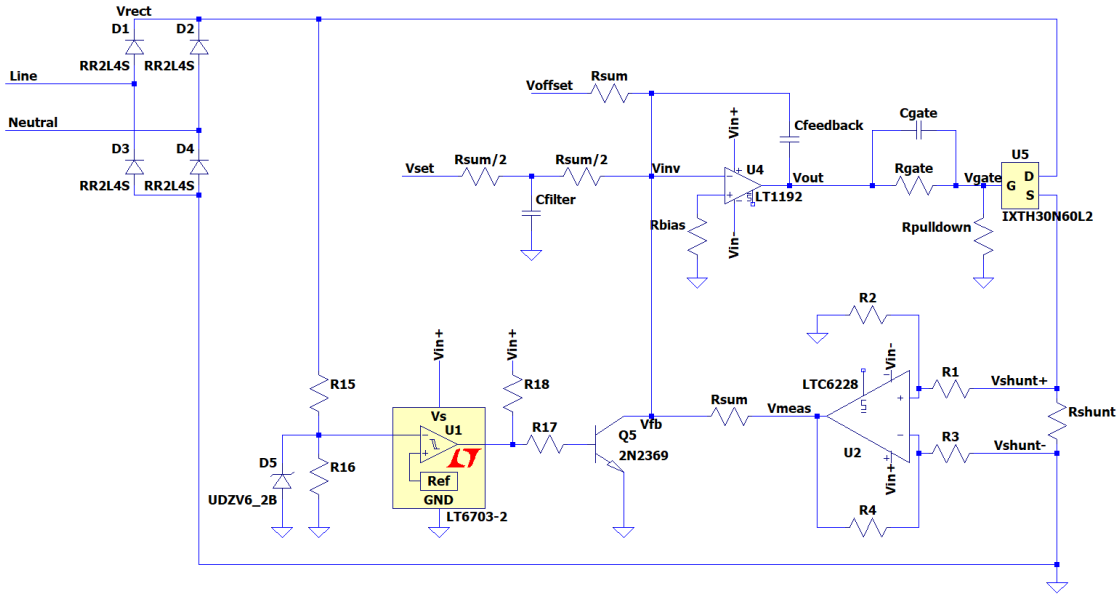

Fig. 13. Complete circuit diagram of the current-controllable AC load.

TABLE III
IXTH30N60L2 PARAMETERS

$V_{DS,max}$	$I_{D,max}$	$P_{D,max}$	V_{TH}	$R_{DS(on)}$	C_{ISS}
600 V	30 A	540 W	2.5 – 4.5 V	240 mΩ	10.7 nF

The requirements for voltage and current are easily met, but a closer look must be taken at the FBSOA diagram given in Fig. 14 for the power requirement. The transistor must be able to handle a peak power of 600 W, since the power is shared among 10 MOSFETs. This amount of power can only be delivered for $W_{nom}/W_{peak} = 1/6$ of the time to meet the nominal power requirement. When power is modeled as a pulse, its duration for a certain input frequency can be calculated with equation (8).

$$t_{pulse} = \frac{W_{nom}}{W_{peak}} \frac{1}{2f_v} = 1.67\,\text{ms} \tag{8}$$

The blue area in Fig. 14 corresponds to the W_{nom} requirement and the red area to W_{peak}. The horizontal line is defined I_{max}/N, the vertical line by $V_{in,max}$ and the connecting line by the power. It can be seen that the nominal power never reaches the DC line and the peak power stays well below the 10 ms line, indicating a safe operation of the MOSFET. The same can be done for the higher operating temperature FBSOA given in the datasheet [13]. Here the requirements are met as well, but the safety margin is lowered. Thus, proper cooling is needed but this will not be discussed in this paper.

Input admittance and gate charge depict the specifications of the op amp driving the transistor and the graphs of these parameters are given in Fig. 15 and Fig. 16. First, a total bias current of 50 mA was selected (5 mA per transistor), which makes sure the threshold voltage is reached. This sets V_{GS} at around 3.5 V, where the charge at the gate (Q_G) is just over 30 nC. Then V_{GS} and Q_G are determined for a current of 1.5 A

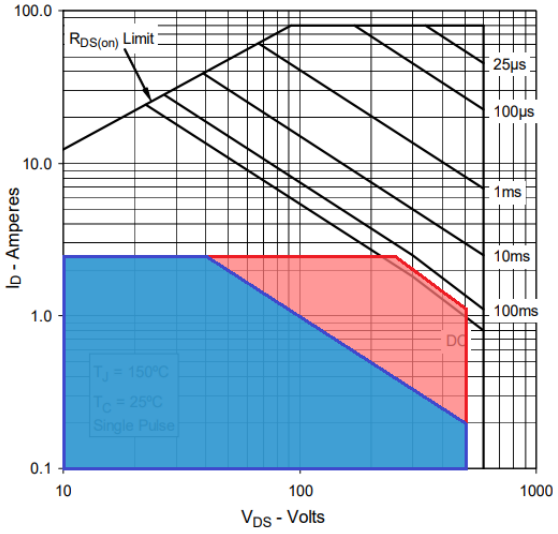

Fig. 14. Forward-Bias Safe Operating diagram including limitations set by the requirements.

per MOSFET, such that the slew rate is the change in current over 1 µs. These values are 6 V and 50 nC, read conservatively from the two previously mentioned figures. Thus, a change of 15 A/µs requires the gate voltage to rise at a rate of $6 - 3.5 = 2.5$ V/µs and the minimal gate current required is calculated in equation (9). Note that these values are the very bare minimum and a large margin is required to ensure that the requirements will be met.

$$I_{G,min} = \frac{\Delta Q_G}{t} = 20\,\text{mA} \tag{9}$$

The transistors will have a total resistance of $R_{DS(on)}/N = 24\,\text{m}\Omega$ and using the earlier calculated resistance budget

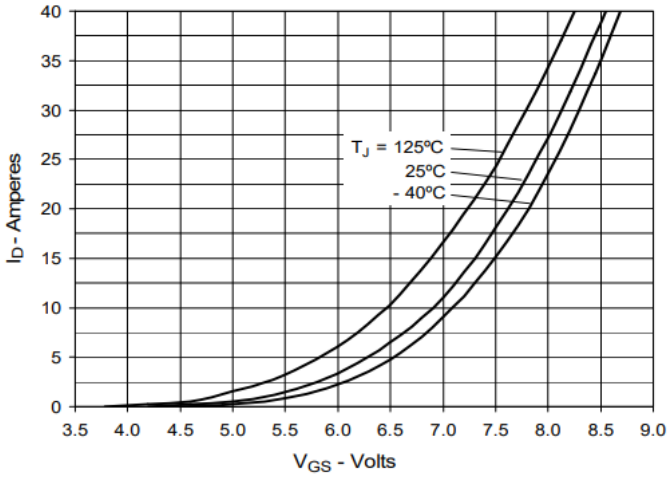

Fig. 15. Input admittance of the IXTH30N60L2.

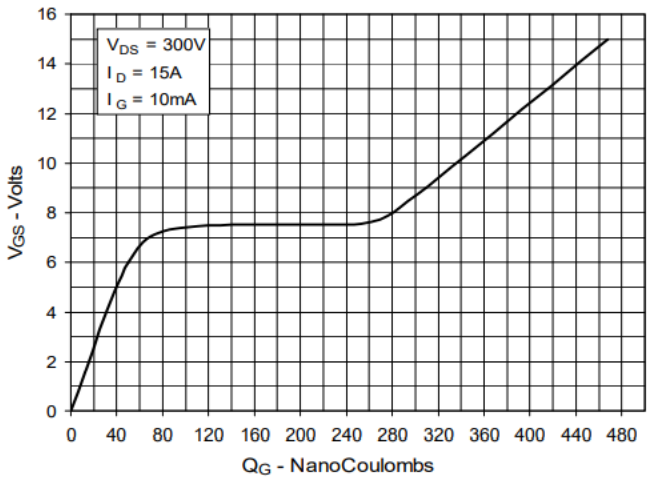

Fig. 16. Gate charge graph of the IXTH30N60L2.

allows for a current shunt resistor with a maximum resistance of $84-24=60\,\mathrm{m\Omega}$. A parallel resistance of $50\,\mathrm{m\Omega}$ results in a resistance of $50 \cdot N = 500\,\mathrm{m\Omega}$ per shunt. At a maximum current of $2.5\,\mathrm{A}$, the total voltage drop over the shunt is $(I_{max}/N)R_{shunt} = 1.25\,\mathrm{V}$. This voltage raises the source voltage of the MOSFET, which increases the maximum threshold voltage to $V_{shunt} + V_{TH,max} = 5.75\,\mathrm{V}$. Thus, the op amp must at least be able to reach this output voltage. Additionally, the shunt forms a negative feedback mechanism, where V_{GS} decreases with an increase in current through the shunt.

The current shunt resistor voltage is then amplified with a gain of 2 to have the voltage correspond to the function generator's output voltage. Using equation 7, the resistors can be determined for a ratio of 2:1. R_4 is set at $200\,\mathrm{k\Omega}$ and $R_3 = 100\,\mathrm{k\Omega}$. The op amp chosen for this application is the LTC6228 [21], which is a high speed op amp to reduce the phase delay caused by the current monitoring circuit. The bandwidth at a gain of 2 is $200\,\mathrm{MHz}$, which is considerably larger than the bandwidth requirement. Other than that, it is able to follow fast changes in current with an output slew rate of $500\,\mathrm{V/\mu s}$.

A high slew rate, output current and bandwidth op amp is needed for controlling the transistor, so the LT1192 [22] has been selected for this task. It features an output current of $\pm 50\,\mathrm{mA}$, a slew rate of $450\,\mathrm{V/\mu s}$, a gain bandwidth product (GBW) of $350\,\mathrm{MHz}$ and a 0.1% settling time of $90\,\mathrm{ns}$. It can be seen that the minimum output current and slew rate requirements set by the MOSFET have been met. It is hard to determine the exact bandwidth of the circuit, since the gain of the transistor, i.e. input admittance, can only be linearized around a relatively high bias current. The output impedance of the op amp goes up with frequency, which means the pole created by R_O and C_{ISS} moves around in frequency. To ensure stability of the op amp, a feedback capacitor has been placed between its output and inverting input. It is hard to determine the exact effect this capacitor has on the phase margin, thus optimization of the exact value is done in simulations.

The op amp is powered with $\pm 9\,\mathrm{V}$, which is enough to overcome $V_{TH} + V_{shunt}$. The non-inverting input of the op amp has been grounded via a resistor to cancel the effects of input bias current [23]. The resistors around summing node V_{inv} must be of equal size to minimize deviation in the current. The input is filtered with a RC circuit with a cutoff frequency at $10\,\mathrm{MHz}$ to smoothen the discrete steps of the measurement waveforms. A $1\,\Omega$ resistor has been placed in series with the gate to dampen the voltage overshoot effect caused by inductance at the gate [17] and a parallel capacitor increases the high frequency control of the op amp on the transistor.

D. Simulation

LTspice has been used for the circuit simulation and the circuit diagram, including component values, is given in Appendix A. A parasitic inductance of $1\,\mu\mathrm{H}$ has been chosen to still reach the desired current slew rate, since this slew rate was also achievable according to the measurements. The maximum current slew rate for a given voltage and this inductance can be read from Fig. 11. This inductor was placed in series with the AC voltage source and a $0.1\,\Omega$ resistor to imitate cable resistance. The current waveforms have been converted to a Piecewise Linear Function (PWL) file with a Matlab script and have been synchronized around the zero crossings in LTspice. The simulation data was then imported in Matlab for further processing and verification of the design. Note that the current through the AC voltage source has been used for verification, since this gives the best indication of the total current draw of the AC load.

IV. Verification

The design is verified with two methods. The first method involves a current step function where a look can be taken at the response of the circuit. The second method inserts current waveforms of measurements in the circuit, such that a real-life scenario can be tested. The feedback capacitor is varied in the simulation to determine the effect it has in the circuit. A quantitative analysis is done by means of waveform parameters and error between input and output, which will enable the selection of an optimal capacitor value.

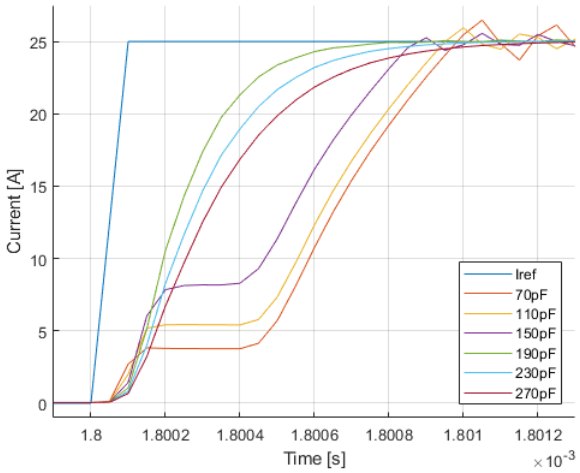

Fig. 17. Step response of the circuit for different capacitor values.

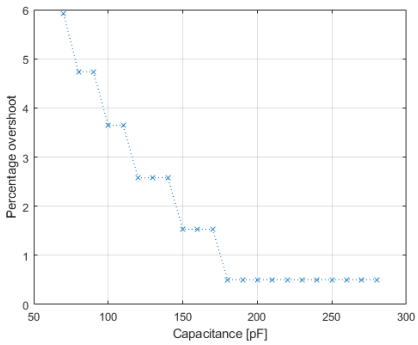

Fig. 18. Percent overshoot for different capacitor values.

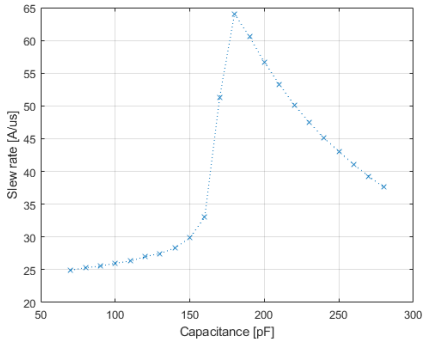

Fig. 19. Slew rate for different capacitor values.

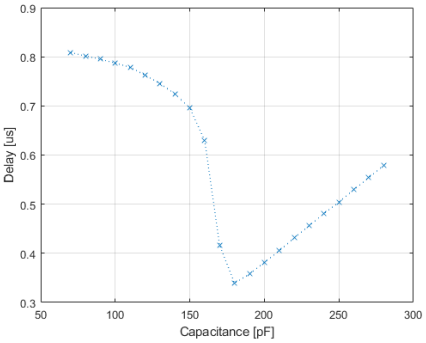

Fig. 20. Delay between input and output for different capacitor values.

A. Circuit response

Important parameters like delay, slew rate, settling time, rise time and percent overshoot have been used to determine instability issues and how well the circuit is designed. A $100\,\mathrm{ns}$, $25\,\mathrm{A}$ step function is fed into the circuit and its response can be seen in Fig. 17. The response of lower capacitor values are not plotted, due to oscillations caused by instability. It can be seen that overshoot and ringing occurs with a lower capacitance, and this relation has been plotted in Fig. 18. This implies that the stability of the circuit increases with capacitance. There is a plateau where the current stays constant for a short time at lower capacitor values. The exact reason for this is not clear, but it might have to do with the Miller plateau seen in Fig 16, even though V_{GS} is not sufficiently high for this. The slew rate is lower due to this 'plateau' and increases until the optimum point of $180\,\mathrm{pF}$ in Fig. 19. This is the best capacitor value for a parasitic inductance of $1\,\mu\mathrm{H}$ and a lower inductance usually has a lower capacitor for the optimal performance. The delay between the set and measured current is given in Fig. 20. The same optimum point can be seen here, due to this capacitance having the fastest rise time and slew rate.

The phase firing angle of the current pulse with respect to the voltage waveform also determines the response, since a lower voltage results in a lower slew rate. Demanding a high slew rate at a low voltage is another cause for instability and oscillations. The current filtering effect of the parasitic inductance and resistance is the cause for this. A pole is added in the control loop with $f_p = (R_{cable} + R_{DS(on)} + R_{shunt})/(2\pi L_{cable})$. This implies that a larger shunt resistor would increase the stability of the circuit, but this would also increase the minimum voltage for a certain amount of current.

B. Verification using measurement data

Now that it has been proven that the minimal slew rate requirement can be met, the circuit is verified with two current waveforms from the measurements. One is given in Fig. 1 and has been selected due to it having the highest slew rate. The response of the circuit to the first pulse of this waveform is given in Fig. 21. It can be seen that the circuit is less responsive for a larger capacitance, i.e. the bandwidth decreases with capacitance and a phase shift is introduced. The error between the set and measured waveforms was determined using the root-mean-square error (RMSE) method [24]. Here, the absolute current deviation is averaged over all samples and the resulting error per capacitor value is given in Fig. 22. There is a standard error due to the biasing of the MOSFET, which is $50\,\mathrm{mA}$. The optimum capacitor value is $90\,\mathrm{pF}$ when the deviation error needs to be minimized for this waveform.

Next, the simulated waveform parameters are being compared to the parameters of the measured waveform. A table,

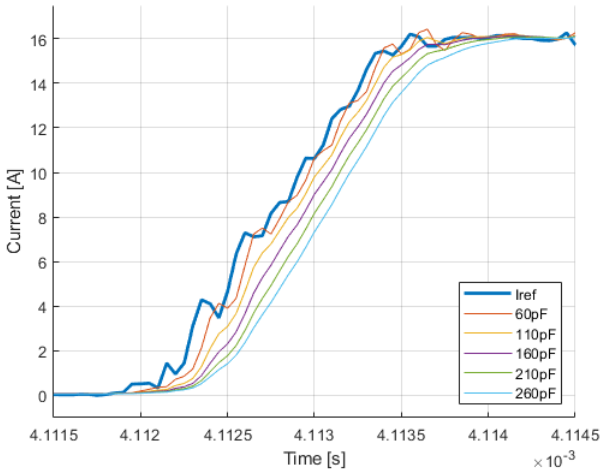

Fig. 21. Response of the circuit with different capacitor values.

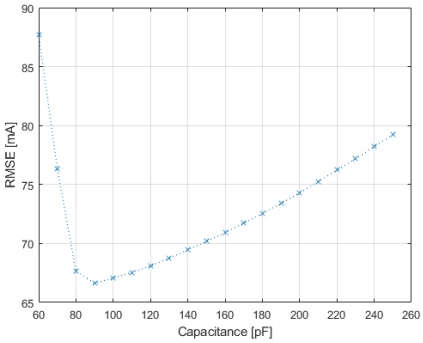

Fig. 22. Root mean square error of the first test waveform vs capacitance.

given in Table IV, has been made with the absolute percentage error to give an indication of the performance per capacitor value. A green color has been assigned to errors of less than 1%, red to errors above 5% and yellow to errors in between these percentages. A capacitor can be chosen according to which errors must be minimized, which seems to be between 140 pF and 190 pF for a minimum rise time and slew rate deviation.

The same is done for the waveform given in Fig. 23. This current waveform has been chosen for its low power factor and relatively high crest factor, but the maximum slew rate and minimum working voltage requirements are still met. The RMSE and percent errors for the waveform parameters are given in Fig. 24 and Table V. It can be seen that any capacitor value above 100 pF will minimize any error. This results from the fact that a relatively high current is drawn around the zero crossing, which is a source of instability at a relatively low feedback. The waveform has a lower slew rate and bandwidth, thus making it easier to imitate. This can be seen when comparing the error tables of the two waveforms.

Depending on which parameter is most important, as well as what type of waveform needs to be replicated, a capacitor value can be chosen. A trade-off is made between error and

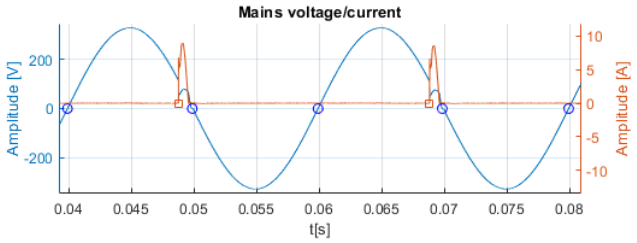

Fig. 23. Waveforms of a remote control water pump [25].

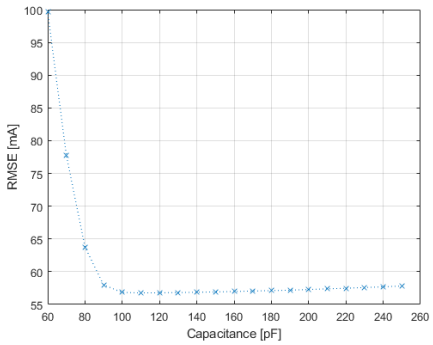

Fig. 24. Root mean square error of the second test waveform vs capacitance.

stability, as a higher capacitance increases stability, at a cost of an increase in certain errors.

V. Conclusion

A conceptual design has been proposed and it has been verified that the current waveforms can be imitated up to a certain degree. Errors may still occur when a signal has relatively high frequency components, slew rate or rise time. Custom current waveforms can be generated to test parameters like slew rate and phase firing angle, which relates to the CF and PF. A feedback capacitor should be chosen tailored to which parameter is most important and must not be too small when stability is key. The parasitic inductance of the source dictates the current slew rate, thus not every current waveform can be accurately made with the AC load. Next to that, a low power factor waveform with a relatively high current crest factor also causes issues, due to the instability and lower current slew rate around zero crossings of the voltage waveforms. The conceptual design proposed in this paper should be able to imitate waveforms which cause erroneous static energy meter readings and custom made waveforms can be easily tested, as long as the device is used within specifications. This includes a minimal voltage at which a certain amount of current can be drawn, due to components like diodes and resistors included in the design and parasitic inductances that limit the current slope, especially at lower voltages. This device will speed up and hopefully enable more research on the accuracy of static energy meters, next to it being useful to other AC applications.

TABLE IV
PERCENTAGE ERRORS VS FEEDBACK CAPACITANCE FOR THE REPLICATED CURRENT WAVEFORM GIVEN IN FIG. 1.

	60pF	70pF	80pF	90pF	100pF	110pF	120pF	130pF	140pF	150pF	160pF	170pF	180pF	190pF	200pF	210pF	220pF	230pF	240pF	250pF
Rise time error	1.5299	2.0975	2.6569	2.9554	3.0976	3.1382	2.8294	2.5877	2.3933	2.2949	1.5703	0.8335	0.2497	0.2775	0.4921	0.6539	0.7370	0.7924	1.2107	1.6297
Fall time error	3.1546	2.7562	2.5481	2.5365	2.5916	2.6957	2.8497	3.0281	3.2470	3.4863	3.7388	4.0263	4.3315	4.6610	4.9945	5.3531	5.7089	6.0666	6.4625	6.8570
Slew rate error	2.8604	2.5513	2.5229	2.3906	2.2011	1.9782	1.4413	1.0163	0.6723	0.4517	0.3875	1.2131	1.8650	2.4184	2.6599	2.8475	2.9553	3.0344	3.4595	3.8796
Max current error	1.2867	0.4003	0.2010	0.6355	0.9647	1.2221	1.4289	1.5977	1.7371	1.8535	1.9517	2.0365	2.1101	2.1476	2.1809	2.2122	2.2401	2.2661	2.2907	2.3131
Min pulse width error	0.4794	0.4089	0.3175	0.2353	0.1555	0.0828	0.0138	0.0746	0.1668	0.2611	0.3587	0.4503	0.5429	0.6382	0.7269	0.8235	0.9264	1.0246	1.1545	1.2831
Max pulse width error	0.3477	0.3465	0.3709	0.3440	0.3427	0.3430	0.3608	0.3599	0.3574	0.3564	0.3554	0.3549	0.3546	0.3552	0.3546	0.3536	0.3341	0.3530	0.3524	0.3523

TABLE V
PERCENTAGE ERRORS VS FEEDBACK CAPACITANCE FOR THE REPLICATED CURRENT WAVEFORM GIVEN IN FIG. 23.

	60pF	70pF	80pF	90pF	100pF	110pF	120pF	130pF	140pF	150pF	160pF	170pF	180pF	190pF	200pF	210pF	220pF	230pF	240pF	250pF
Rise time error	2.9284	0.0202	0.0273	0.0445	0.0616	0.0764	0.1831	0.1930	0.1100	0.1209	0.2379	0.2458	0.2538	0.2623	0.2094	0.2169	0.2242	0.2304	0.2377	0.2441
Fall time error	0.8397	0.1549	0.4998	0.5531	0.5540	0.5541	0.5545	0.5629	0.5627	0.5663	0.5706	0.5955	0.5928	0.7574	0.6023	0.6169	0.6236	0.6323	0.6354	0.6379
Slew rate error	0.5794	0.5309	0.4486	0.4808	0.4658	0.4562	0.5476	0.5482	0.4582	0.4629	0.5725	0.5769	0.5802	0.5809	0.5273	0.5319	0.5362	0.5397	0.5450	0.5492
Max current error	2.3320	0.5106	0.4760	0.4361	0.4039	0.3794	0.3635	0.3542	0.3477	0.3415	0.3333	0.3297	0.3250	0.3170	0.3168	0.3138	0.3108	0.3081	0.3060	0.3038
Min pulse width error	0.2192	0.2181	0.2237	0.2204	0.2168	0.2131	0.2102	0.2108	0.2235	0.2214	0.2200	0.2236	0.2170	0.2306	0.2145	0.2287	0.2273	0.2259	0.2248	0.2233
Max pulse width error	0.2192	0.2181	0.2237	0.2204	0.2168	0.2131	0.2102	0.2108	0.2235	0.2214	0.2200	0.2236	0.2170	0.2306	0.2145	0.2287	0.2273	0.2259	0.2248	0.2233

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APPENDIX

A. *Simulation circuit diagram*