Linearization techniques for CMOS Switched-Capacitor Power Amplifiers

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***Abstract*—This paper compares two different linearization techniques for CMOS Switched-Capacitor Power Amplifiers (SCPA), the Clock-overlap method and the Constant Resistance Inverters. The two techniques are compared based on their effect on the output conductance and on the input capacity of the CMOS switches. They are also compared based on their effect on the SCPA AM-AM and AM-PM distortion. An analytical model of the output conductance is derived, which is verified by performing simulations on 130 nm CMOS transistor models in LTspiceXVII. The analytical model is used to analyze the effect of the linearization techniques on the linearity of the SCPA, by analyzing the effect on the AM-AM and AM-PM distortion. It is shown that the Constant Resistance Inverters are more linear than the Clock-overlap method. The maximum deviation of the output conductance is reduced from 15.53 to 4.74 and from 15.53 to 1.1 for the Clock-overlap method and Constant Resistance Inverters, respectively. The input capacity of the Constant Resistance Inverters is 9.7 times higher than the input capacity of the Clock-overlap method. The AM-AM distortion is for both techniques the same and the AM-PM distortions are 4.4 degree and 0.4 degree for the Clock-overlap method and Constant Resistance Inverters, respectively.**

***Index Terms*—SCPA, CMOS Inverter, Constant Resistance Inverters, Clock-Overlap Method, Output Conductance, AM-AM, AM-PM, Input Capacity.**

I. Introduction

Direct-digital to RF transmitters show promising results for highly versatile and linear transmitter architectures. The RF-DAC is realized as a Switched-Capacitor Power Amplifier (SCPA) [1]. Capacitors can be very linear, but the linearity is limited by the nonlinearity in the switch-transistors that are used to control the capacitors and the gain compression that occurs at high power output. Figure 1 indicates a Switched-Capacitor Power Amplifier that uses quadrature modulation with a clock duty cycle of 25% [2].

The switches are constructed as CMOS Inverters, which consist of a NMOS and PMOS transistor. The CMOS Inverter has a high output when the input is low and vice versa. The nonlinearity is a result of a significantly lower output conductance while the switch is transitioning between the low and high state. The nonlinearity of the CMOS Inverter has been analyzed in depth in [3].

There are different linearization techniques that can be used to reduce the nonlinearity in the CMOS Inverter. The techniques that will be focused on in this paper are the Clock-overlap method [4] and Constant Resistance Inverters.

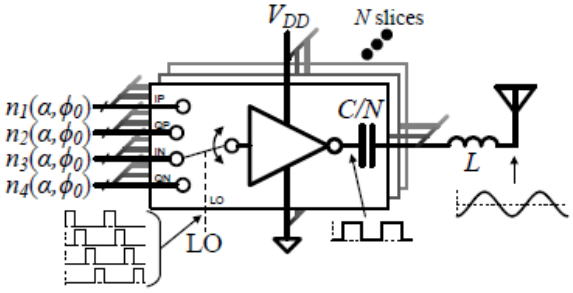


Fig. 1: Q25 SCPA, picture from [2].

The Clock-overlap method uses two separate clocks as input for the transistors, instead of one clock for both transistors. A time delay between both input clocks is used to increase the low output conductance that occurs during switching. The Constant Resistance Inverters is a novel technique, the inverters have a constant output impedance over input voltage. The constant output impedance is achieved by using two additional resistors connected between the drains of the transistors.

Both techniques improve the linearity of the circuit and therefore reduce the intermodulation distortion. The nonlinearity of the SCPA at a specific frequency will be quantified with the AM-AM and AM-PM distortion. According to [1] it is expected to have good AM-AM modulation, because of excellent capacitor matching. However, due to the nonlinearity of the switches it is expected to have bad AM-PM modulation.

The objective of this paper is to compare the Clock-overlap method and the Constant Resistance Inverters. The two techniques will be compared based on their effect on the linearity and their effect on the input capacity of the transistors. An analytic model will be derived to predict the output conductance for the two linearization techniques, which will be verified by doing transistor level simulations of the AM-AM and AM-PM distortion.

Section II explains the operation of the CMOS Inverter without the use of the two linearization techniques. It also explains the operation of the Switched-Capacitor Power Amplifier. Section III analyzes the operation of the Clock-overlap method. Section IV analyzes the operation of the Constant Resistance Inverters. Section V gives the simulation results and section VI gives a conclusion.

II. Theory of Operation

Section II-A covers the operation of the CMOS Inverter without the use of the two linearization techniques. It explains the operation of the CMOS Inverter and some important design choices. A model of the output conductance will be derived by analyzing different input states. Section II-B gives an overview of the operation of the SCPA.

A. CMOS Inverter

The CMOS Inverter consists of a N-MOSFET and a P-MOSFET, the design of a CMOS Inverter can be seen in figure 2. The transistors have both drains and gates connected. The source of the PMOS is connected to the supply voltage V_{DD} and the source of the NMOS to ground. The NMOS and PMOS operate similar, however, the PMOS is opposite in polarity compared to the NMOS.

The transistors can operate in three regions: cut-off, triode and saturation. The region of operation depends on the voltages V_{ds} and V_{gs}. The assumption will be made that there is no leakage current when the PMOS and NMOS are operating in the cut-off region. The drain currents in the triode and saturation region for the NMOS and PMOS respectively are given by [5]

$$I_{dn,tri} = \mu_n C_{ox} \frac{W_n}{L_n} \left[(V_{gsn} - V_{thn}) V_{dsn} - \frac{V_{dsn}^2}{2} \right] \quad (1)$$

$$I_{dn,sat} = \frac{1}{2} \mu_n C_{ox} \frac{W_n}{L_n} (V_{gsn} - V_{thn})^2 [1 + \lambda V_{dsn}] \quad (2)$$

$$I_{dp,tri} = -\mu_p C_{ox} \frac{W_p}{L_p} \left[(V_{gsp} - V_{thp}) V_{dsp} - \frac{V_{dsp}^2}{2} \right] \quad (3)$$

$$I_{dp,sat} = -\frac{1}{2} \mu_p C_{ox} \frac{W_p}{L_p} (V_{gsp} - V_{thp})^2 [1 - \lambda V_{dsp}] \quad (4)$$

When $V_{ds} \ll 2(V_{gs} - V_{th})$ it can be said that the transistors operate in the deep triode region [5]. The drain currents in the deep triode region for the PMOS and NMOS are respectively given by

$$I_{dn,dt} = \mu_n C_{ox} \frac{W_n}{L_n} (V_{gsn} - V_{thn}) V_{dsn} \quad (5)$$

$$I_{dp,dt} = -\mu_p C_{ox} \frac{W_p}{L_p} (V_{gsp} - V_{thp}) V_{dsp} \quad (6)$$

As already mentioned in section I, the CMOS Inverter has a low input state and a high input state. While it is in either one of those two states there is always one transistor closed and the other transistor is open. While switching between these states there is a moment that both are closed and as a result the output conductance drops to almost zero. This effect is explained in [3]. The low output conductance occurs when the input voltage is equal to the output voltage, also known as the midpoint $V_{in} \approx \frac{1}{2} V_{DD}$ [6]. A symmetric CMOS Inverter has the midpoint at exactly half the supply voltage.

There is a trade-off between the position of the midpoint and the output conductance for the low and high input state. It is not possible to get equal output conductance in both states and at the same time have the midpoint at exactly $\frac{1}{2} V_{DD}$. The PMOS and NMOS do not have the same μC_{ox} and V_{th}. The differences between the transistors are only partially compensated for when the width and length are scaled. The goal is to get equal output conductance in both states; therefore, the midpoint will not be exactly at $\frac{1}{2} V_{DD}$. However, for simplicity the assumption is made in the analytical model that the midpoint is at exactly $\frac{1}{2} V_{DD}$.

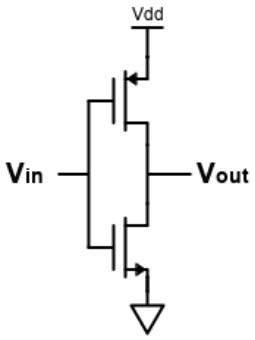


Fig. 2: Circuit of CMOS Inverter.

Equal output conductance for the low and high input state can be achieved by scaling the width and the length of the PMOS and NMOS. It is important to note that the on-resistance of a transistor scales with a factor $\frac{W}{L}$ and the input capacity scales with WL [5]. Ideally both the on-resistance and input capacity are as low as possible to achieve fast switching and low power consumption. The minimum length L is used to keep the input capacity as low as possible. A lower input capacity results in faster charging, hence it can handle a higher input frequency. Therefore, only the widths will be scaled.

TABLE I: Node voltages for different V_{in}.

Node	$\mathbf{V_{in} = 0V}$	$\mathbf{V_{in} = V_{DD}}$	$\mathbf{V_{in} = \frac{1}{2} V_{DD}}$
$V_{dsp} (= V_{out} - V_{DD})$	0V	$-V_{DD}$	$-\frac{1}{2} V_{DD}$
$V_{gsp} (= V_{in} - V_{DD})$	$-V_{DD}$	0V	$-\frac{1}{2} V_{DD}$
$V_{dsn} (= V_{out})$	V_{DD}	0V	$\frac{1}{2} V_{DD}$
$V_{gsn} (= V_{in})$	0V	V_{DD}	$\frac{1}{2} V_{DD}$

The low, high and midpoint input state will be analyzed by using the node voltages that are given in Table I. The output conductance for each state will be derived by using the corresponding drain current eq. 1 to eq. 6 and taking the derivative of I_d with respect to V_{ds}.

1) Input voltage $V_{in} = 0V$: The NMOS is open, because $V_{gsn} < V_{thn}$ and the PMOS is closed, because $V_{gsp} < V_{thp}$. There is no current flowing between V_{DD} and ground, because the NMOS is open. Since there is no current flowing and the leakage current is neglected the voltage V_{dsp} is zero. As a result, $V_{dsp} > V_{gsp} - V_{thp}$ and the PMOS operates in the deep triode region. The output conductance of the PMOS is derived from eq. 6 and is given by eq. 7. The NMOS is not conducting.

Therefore, the output conductance is $g_{d,out} = g_{dp,dt}$ and is given by

$$g_{dp,dt} = \mu_p C_{ox} \frac{W_p}{L_p}(V_{DD} + V_{thp}) \tag{7}$$

The $g_{dp,dt}$ is the output conductance of the PMOS in the deep triode region.

2) Input voltage $V_{in} = V_{DD}$: The NMOS is closed, because $V_{gsn} > V_{thn}$ and the PMOS is open, because $V_{gsp} > V_{thp}$. The output voltage is equal to zero, because there is a direct path between the output and the ground. The voltage V_{dsn} is equal to zero, because there is no current flowing between V_{DD} and ground. As a result, $V_{dsn} < V_{gsn} - V_{thn}$ and the NMOS is operating in the deep triode region. The output conductance $g_{d,out} = g_{dn,dt}$ is derived from eq. 5 and is given by

$$g_{dn,dt} = \mu_n C_{ox} \frac{W_n}{L_n}(V_{DD} - V_{thn}) \tag{8}$$

3) Input voltage $V_{in} = \frac{1}{2}V_{DD}$: The NMOS and PMOS are both closed, because $V_{gsn} > V_{thn}$ and $V_{gsp} < V_{thp}$. A result of symmetry is that for $V_{in} = \frac{1}{2}V_{DD}$ the output voltage is equal to $V_{out} = \frac{1}{2}V_{DD}$. For the NMOS $V_{dsn} = V_{gsn} = \frac{1}{2}V_{DD}$, hence $V_{dsn} > V_{gsn} - V_{thn}$ and the NMOS is operating in the saturation region. For the PMOS $V_{dsp} = V_{gsp} = -\frac{1}{2}V_{DD}$, hence $V_{dsp} < V_{gsp} - V_{thp}$ and the PMOS is operating in the saturation region. Both transistors are closed, therefore the output conductance is given by $g_{d,out} = g_{dn,sat} + g_{dp,sat}$. The output conductances are respectively derived from eq. 2 and eq. 4 and are given by eq. 9 and eq. 10.

$$g_{dn,sat} = \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n}(V_{gsn} - V_{thn})^2 \lambda \tag{9}$$

$$g_{dp,sat} = \frac{1}{2}\mu_p C_{ox} \frac{W_p}{L_p}(V_{gsp} - V_{thp})^2 \lambda \tag{10}$$

It can be concluded that the output conductance for the CMOS Inverter is significantly lower when both transistors are closed and are operating in the saturation region. Compared to when one transistor is closed and operates in the deep triode region.

B. SCPA

The Switched-Capacitor Power Amplifier consist of N unit cells, which are CMOS Inverters followed by a capacitor, as can be seen in figure 1. The top plates of the capacitors are connected in parallel and the bottom plates are connected to their CMOS Inverter. The top plate capacitance is constant; therefore, the bandpass matching network only needs to be tuned for a fixed frequency and capacitance [1]. The SCPA shown in figure 1 uses a four-phase mixer and a single sub-SCPA. According to [2] it is referred to as a quadrature modulation SCPA with a clock duty cycle of 25%. Based on a digital input an amount of unit cells is selected. The total capacitance is given by C_s and the unit capacitance is $\frac{C_s}{N}$ The inductor used in the matching network is according to [3] defined as $L = (\omega_0^2 C_s)^{-1}$. The impedance of the load is 50Ω. The output impedance of the SCPA depends on the total amount of unit cells, since all of them are connected in parallel the output impedance of the SCPA is equal to

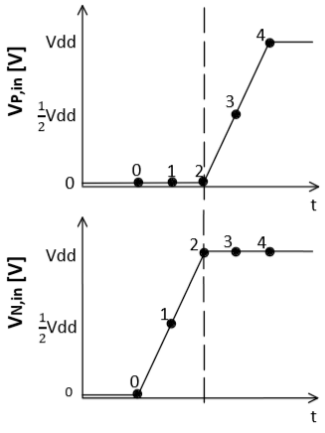
$$R_{out} = \frac{impedance\ unit\ cell\ [\Omega]}{N} \tag{11}$$

The efficiency of the SCPA is high when the output impedance of the SCPA is low. However, a low output impedance would mean that the input capacity is high. A good balance between the output impedance and the input capacity is achieved when $R_{out} = \frac{50}{10} = 5\Omega$.

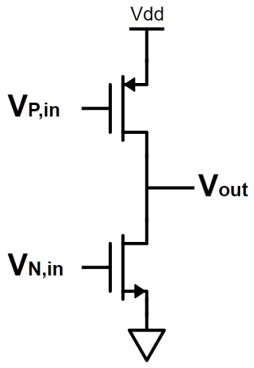
As already mentioned in section I it is expected that the SCPA has low AM-AM distortion, and high AM-PM distortion. A perfect linear amplifier would have zero AM-AM and zero AM-PM distortion [7]. By using the two linearization techniques it is expected that the AM-AM and AM-PM distortion are decreased and are closer to zero.

III. Clock-Overlap Method

The Clock-overlap method has been presented in [4] and is shown in figure 3b. The gates of the PMOS and NMOS are separated compared to the CMOS Inverter that is explained in section II-A. The inputs $V_{N,in}$ and $V_{P,in}$ are used to control the NMOS and PMOS. A time delay between the input voltages $V_{N,in}$ and $V_{P,in}$ is added, which makes the input clocks partially overlapping. The time delay that is used in [4] is equal to the rise and fall time T_{rf} of the input voltages. Which results in the input voltages that can be seen in figure 3a.



(a) Separated input voltages.



(b) Circuit Clock-Overlap method, picture adapted from [4].

Fig. 3: Clock-overlap Method

As explained in section II-A the output conductance drops significantly when both transistors are operating in the saturation region. In order to say something about the regions in which the transistors are operating it is necessary to analyze five combinations of the input voltages $V_{N,in}$ and $V_{P,in}$. The five combinations can be seen in figure 3a. The first and the last combination behave the same as for the CMOS Inverter and are already explained in section II-A. The other combinations will be explained respectively below.

1) Input voltage $V_{N,in} = \frac{1}{2}V_{DD}$ & $V_{P,in} = 0V$: The PMOS is closed and in the triode region. The NMOS is closed and operates in the saturation region, due to the low input voltage. The NMOS pulls the output voltage down and therefore V_{dsp} is no longer equal to zero and cannot be neglected in the derivation of the output conductance. Which means that the output conductance of the PMOS is derived from eq. 3 and is given by

$$g_{dp,tri} = \mu_p C_{ox} \frac{W_p}{L_p}(-V_{gsp} + V_{thp} + V_{dsp}) \qquad (12)$$

The total output conductance is $g_{d,out,c1} = g_{dp,tri} + g_{dn,sat}$ and can be found by adding eq. 12 and eq. 9.

2) Input voltage $V_{N,in} = V_{DD}$ & $V_{P,in} = 0V$: The PMOS and NMOS remain closed. Both transistors have the same input voltage, however, one is negative and one is positive. Since the CMOS Inverter is approximated to be perfectly symmetrical and both transistors have the same input voltage is the output voltage equal to $\frac{1}{2}V_{DD}$. The PMOS is operating in the triode region, because $V_{dsp} = -\frac{1}{2}V_{DD}$ and $V_{gsp} = -V_{DD}$ hence $V_{dsp} > V_{gsp} - V_{thp}$. The NMOS is operating in the triode region, because $V_{dsn} = \frac{1}{2}V_{DD}$ and $V_{gsn} = V_{DD}$ hence $V_{dsn} < V_{gsn} - V_{thn}$. Since both transistors are closed is the total output conductance $g_{d,out,c2} = g_{dp,tri} + g_{dn,tri}$. It can be found by adding eq. 12 and eq. 13.

$$g_{dn,tri} = \mu_n C_{ox} \frac{W_n}{L_n}(V_{gsn} - V_{thn} - V_{dsn}) \qquad (13)$$

This case can be compared to the case explained in section II-A3, because for both cases the output voltage is equal to $V_{out} = \frac{1}{2}V_{DD}$. It had been explained that for the CMOS Inverter both transistors are operating in the saturation region and that it results in the lowest output conductance. For the Clock-overlap method both are no longer operating in saturation region, but in the triode region. It is expected that by using the Clock-overlap method the maximum deviation of the output conductance is decreased.

3) Input voltage $V_{N,in} = V_{DD}$ & $V_{P,in} = \frac{1}{2}V_{DD}$: The PMOS and NMOS remain closed. The PMOS has less pulling power due to the lower overdrive voltage and hence the output voltage is less, compared to section III-2. The PMOS is in the saturation region and the NMOS remains in the triode region. The total output conductance is $g_{d,out,c3} = g_{dp,sat} + g_{dn,tri}$ and can be found by adding eq. 10 and eq. 13.

A longer time delay than T_{rf} would only result in a longer switching time and does not further decrease the maximum deviation of the output conductance. A shorter time delay than T_{rf} would only result in the transistors operating closer to the saturation region or even in the saturation region again.

IV. Constant Resistance Inverters

The Constant Resistance Inverter is a novel technique which uses two additional resistors between the drains of both transistors, as can be seen in figure 4. The drain resistors are used to increase the output impedance of the CMOS Inverter. A higher output impedance has as results that the fluctuating impedance of the transistors is less noticed at the output.

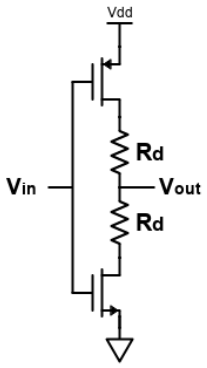


Fig. 4: Circuit Constant Resistance Inverter.

This linearization technique will be analyzed based on the input voltages $V_{in} = 0V, V_{in} = \frac{1}{2}V_{DD}$ and $V_{in} = V_{DD}$, which are the same as for the CMOS Inverter of section II-A.

1) Input voltage $V_{in} = 0V$: The PMOS is closed and the NMOS is open. The drain resistors do not change the fact that there is no current flowing between V_{DD} and ground, because the NMOS is open. As a result, the output voltage is still equal to V_{DD} and the voltages across V_{dsp} and V_{Rd} remain close to zero. The drain resistor is in series with the transistors and the output conductance is given by

$$g_{d,out} = \frac{1}{R_d + g_{dp,dt}^{-1}} \qquad (14)$$

2) Input voltage $V_{in} = V_{DD}$: The NMOS is closed and the PMOS is open. It behaves the same as the low input state explained above. The output conductance is given by

$$g_{d,out} = \frac{1}{R_d + g_{dn,dt}^{-1}} \qquad (15)$$

3) Input voltage $V_{in} = \frac{1}{2}V_{DD}$: There is a direct path between V_{DD} and ground. Therefore, the drain resistors influence the output conductance more than for the low and high input state. When $R_d \ll R_{on}$ the drain resistor can be neglected and the circuit behaves the same as explained in section II-A3. When $R_d \gg R_{on}$ the on-resistance can be neglected. The circuit is a voltage divider and the output impedance can be found by taking both resistors in parallel. The output conductance is than given by

$$g_{d,out} = \frac{2}{R_d} \qquad (16)$$

The interesting behavior occurs when R_d is between the two extremes that are explained above. It can be seen that when $R_d \gg R_{on}$ that the output conductance for $V_{in} = \frac{1}{2}V_{DD}$ is higher than the output conductance for the low and high input state. This is exactly the opposite of what has been explained in section II-A. By setting a certain value for R_d between the two extremes, it seems possible to get a constant output conductance over input voltage. This behavior is rather difficult to analyze theoretically and will therefore be analyzed in section V by using simulations.

V. Simulations

The simulations will be performed in LTspiceXVII on 130 nm transistor level models. The output conductance of the CMOS Inverter, Clock-overlap method and Constant Resistance Inverters will be analyzed and were possible verified with the derived analytical model. Simulations on a 8-bit SCPA will be performed to analyze the effects on the linearity. The 8-bit SCPA consist of 5 unary bits (31 unary cells) and 3 binary bits. Table II is created by performing simulations on the used 130 nm transistor technology. The characteristics have been derived by using first order approximations given by Razavi in [5]. They only describe the behavior of the transistors with a limited accuracy and will result in deviations between the theoretical and simulated output conductance.

TABLE II: Characteristics of the used 130nm PMOS and NMOS technology

MOSFET	L	W	Vth	μC_{ox}	λ
PMOS	130nm	2.845um	-0.25V	$65.51\frac{\mu A}{V^2}$	$0.708V^{-1}$
NMOS	130nm	0.6484um	0.3V	$196.8\frac{\mu A}{V^2}$	$0.728V^{-1}$

A. CMOS Inverter

Simulations on the CMOS Inverter without the use of one of the two linearization techniques function as base reference.

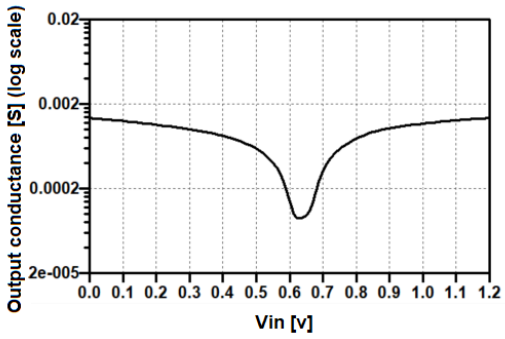


Fig. 5: Output conductance for CMOS Inverter

The output conductance of the CMOS Inverter over input voltage is shown in figure 5. The widths of the NMOS and PMOS are scaled to get equal output conductance for the low and high input state. The scaling ratio has been found by performing simulations and is given in table II. The CMOS Inverter is asymmetric, as explained in section II-A. A result of the asymmetry is that the lowest output conductance is given for $V_{in} = 0.63V$.

It can be seen in figure 5, that the simulated output conductance for the low and high input state are equal to $g_{d,out} = 1.37mS$. By using table II, eq. 7 and eq. 8 is the theoretical output conductance for the low input and high input state respectively given by

$$g_{dp,dt} = -6.551 \cdot 10^{-5}\frac{2.845}{0.13}(-1.2 + 0.25) = 1.36mS \quad (17)$$

$$g_{dn,dt} = 1.968 \cdot 10^{-4}\frac{0.6484}{0.13}(1.2 - 0.3) = 0.88mS \quad (18)$$

The theoretical output conductances are different than the simulated output conductances. This is expected, because the midpoint is not at exactly $\frac{1}{2}V_{DD}$, which has been approximated in section II-A. The simulated output conductance for $V_{in} = 0.63V$ is equal to $g_{d,out} = 88.2\mu S$. The theoretical output conductance for $V_{in} = 0.63V$ is given by eq. 9 + eq. 10.

$$\begin{aligned} g_{d,out} &= g_{dn,sat} + g_{dp,sat} \\ &= \frac{1}{2} \cdot 1.968 \cdot 10^{-4}\frac{0.6484}{0.13}(0.63 - 0.3)^2 \cdot 0.728 \\ &+ \frac{1}{2} \cdot 6.551 \cdot 10^{-5}\frac{2.845}{0.13}(-0.57 + 0.25)^2 \cdot 0.708 \\ &= 90.9\mu S \end{aligned} \quad (19)$$

The maximum deviation in output conductance for the CMOS Inverter without the use of one of the two linearization techniques is given by

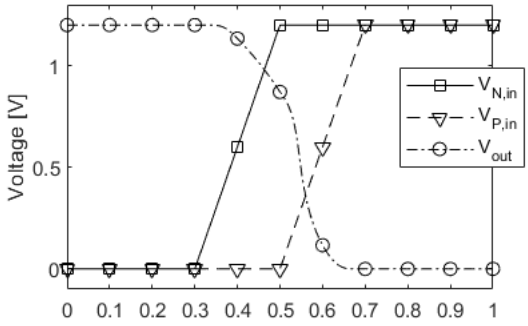
$$max_{dev} = \frac{1.37 \cdot 10^{-3}}{88.2 \cdot 10^{-6}} = 15.53 \quad (20)$$

For the CMOS Inverter the simulated output impedance for the low and high input state is equal to $R_{out} = \frac{1}{1.37 \cdot 10^{-3}} = 730\Omega$. The SCPA model that is used consist of 34 unit cells; 31 unary cells and 3 binary cells. By using eq. 11 the output impedance for the SCPA is equal to $730/34 = 21.5\Omega$. However, as explained in section II-A the output impedance of the SCPA should be equal to 5Ω. Impedance scaling with a factor of $\frac{21.5}{5} = 4.3$ is necessary to get the required output impedance for the SCPA. A result of impedance scaling as explained in section II-A is that the input capacity increases with a factor 4.3. The output impedance of the SCPA is thus given by

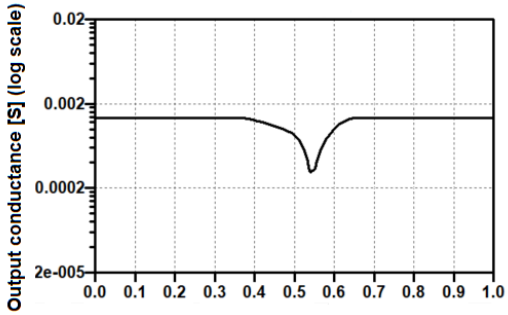
$$R_{out,SCPA} = \frac{730}{34 \cdot 4.3} = 5.0\Omega \quad (21)$$

B. Clock-Overlap Method

The simulations on the Clock-Overlap method are performed by stepping the input voltages. Since it is not possible in LTspiceXVII to step two variables at the same time, a not ideal solution has been used. The input voltages are created by using two equations, which depend on a variable that is stepped. The input voltages and output voltage that are a result of this can be seen in figure 6a. This solution has as consequence that the output conductance in figure 6a cannot be compared directly to figure 5. The output conductance for a delay equal to the transition width can be seen in figure 6b.



(a)



(b)

Fig. 6: (a) Input and output voltages for $\Delta t = T_{rf}$ (b) Output conductance for $\Delta t = T_{rf}$.

It was expected in section III-2 that the output conductance would be at its lowest for $V_{N,in} = 1.2V$ and $V_{P,in} = 0V$. However, the inverter is not perfectly symmetrical and therefore the simulated output conductance is the lowest for $V_{N,in} = 1.2V$ and $V_{P,in} = 0.27V$ and is equal to $g_{d,out} = 283.9\mu S$. The theoretical output conductance is derived by using $V_{N,in} = 1.2V$, $V_{P,in} = 0.27V$ and $V_{out} = 0.56V$ and is given by

$$\begin{aligned} g_{d,out,c2} &= 1.968 \cdot 10^{-4} \frac{0.6484}{0.13}(1.2 - 0.3 - 0.56) \\ &\quad - 6.551 \cdot 10^{-5} \frac{2.845}{0.13}(-0.93 + 0.25 + 0.64) \\ &= 391.1\mu S \end{aligned} \tag{22}$$

The theoretical output conductance is slightly higher than the output conductance seen in the simulations. However, this is probably due to the approximation of V_{th} and μC_{ox}.

For the case explained in section III-1, the simulated output conductance is equal to $g_{d,out,c1} = 1.28mS$. For the case explained in section III-3, the simulated output conductance is equal to $g_{d,out,c3} = 1.00mS$. By using the corresponding output voltage given in figure 6a the theoretical output conductance for the two cases respectively is given by

$$\begin{aligned} g_{d,out,c1} &= -6.551 \cdot 10^{-5} \frac{2.845}{0.13}(-1.2 + 0.25 + 0.07) \\ &\quad + \frac{1}{2} \cdot 1.968 \cdot 10^{-4} \frac{0.6484}{0.13}(0.6 - 0.3)^2 \cdot 0.728 \\ &= 1.29mS \end{aligned} \tag{23}$$

$$\begin{aligned} g_{d,out,c3} &= \frac{1}{2} \cdot 6.551 \cdot 10^{-5} \frac{2.845}{0.13}(-0.6 + 0.25)^2 \cdot 0.708 \\ &\quad + 1.968 \cdot 10^{-4} \frac{0.6484}{0.13}(1.2 - 0.3 - 0.12) \\ &= 0.84mS \end{aligned} \tag{24}$$

The simulated and theoretical output conductance are slightly off due to the used approximations of V_{th} and μC_{ox}.

The output impedance for the low and high input state is the same as for the CMOS Inverter that is explained in section V-A, therefore the maximum deviation in output conductance for the Clock-overlap method is given by

$$max_{dev,Co} = \frac{1.37 \cdot 10^{-3}}{0.289 \cdot 10^{-3}} = 4.74 \tag{25}$$

The output impedance for the low and high input state are the same as for the CMOS Inverter. Therefore, the impedances are also scaled with a factor 4.3, to get the desired output impedance for the SCPA. Since the impedance are scaled with a factor 4.3 the input capacity is also scaled with a factor 4.3. The input capacity for the Clock-overlap method is thus the same as for the CMOS Inverter.

C. Constant Resistance Inverters

The output conductance for the Constant Resistance Inverters will be analyzed based on different values for R_d. The behavior for $R_d \ll R_{on}$ is the same as for $R_d = 0\Omega$, hence the same as for the CMOS Inverter and can be seen in figure 5. As explained for $R_d \gg R_{on}$, the on-resistance of the transistors can be neglected. Figure 7 gives the output conductance for $R_d = 100k\Omega$, it can be seen that the parabola has a concave shape. The simulated output conductance for the low and high input state is equal to $g_{d,out} = 10\mu\Omega$ and for the midpoint its almost equal to $g_{d,out} = 20\mu\Omega$. The theoretical output conductance for the low and high input state is given by

$$g_{d,out} = \frac{1}{1 \cdot 10^5} = 10\mu\Omega \tag{26}$$

The theoretical output conductance for the midpoint state is given by

$$g_{d,out} = \frac{2}{1 \cdot 10^5} = 20\mu\Omega \tag{27}$$

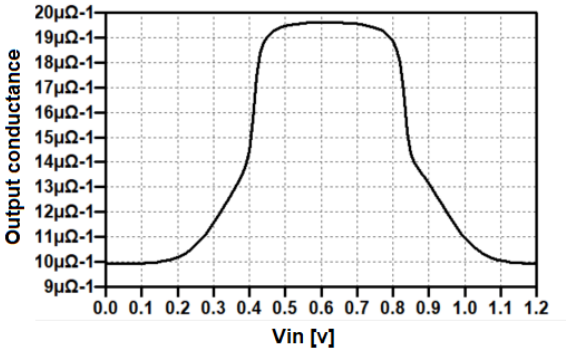


Fig. 7: Output conductance for $R_d = 100k\Omega$

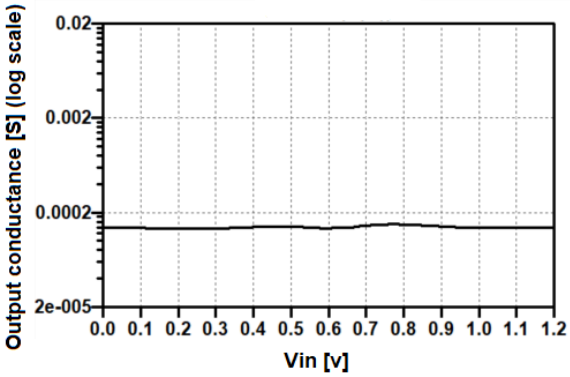


Fig. 8: Output conductance for $R_d = 6.5k\Omega$

By comparing figure 5 and figure 7 it seems possible to find a value for R_d that results in constant output conductance over input voltage. An almost constant output conductance is achieved for $R_d = 6.5k\Omega$, as can be seen in figure 8. A small ripple in the output conductance is present, but in general the simulated output conductance is equal to $g_{d,out} = 0.14mS$. The theoretical output conductance for the low and high input state is derived by using eq. 14 and is given by

$$g_{d,out} = \frac{1}{1.37mS^{-1} + 6.5 \cdot 10^3} = 0.14mS \tag{28}$$

The theoretical output conductance and the simulated output conductance for the low and high input state are the same.

It is necessary to understand in which regions the transistors are operating to say something about the theoretical output conductance for $V_{in} \approx \frac{1}{2}V_{DD}$. For $R_d = 6.5k\Omega$ the voltage V_{ds} for both transistors is equal to 0.2V and the voltage V_{Rd} for both resistors is equal to 0.4V. This means that both transistors are operating in the triode region. By using these voltages across the transistors and eq. 12 and eq. 13 is respectively the output conductance of the transistors given by

$$\begin{aligned} g_{dp,tri} &= 6.551 \cdot 10^{-5} \frac{2.845}{0.13}(0.57 - 0.25 - 0.2) \\ &= 1.72 \cdot 10^{-4} S \end{aligned} \tag{29}$$

$$\begin{aligned} g_{dn,tri} &= 1.968 \cdot 10^{-4} \frac{0.6484}{0.13}(0.63 - 0.3 - 0.2) \\ &= 1.28 \cdot 10^{-4} S \end{aligned} \tag{30}$$

Hence, the PMOS has as on-resistance $R_{on,p} = 5.81k\Omega$ and the NMOS has as on-resistance $R_{on,n} = 7.81k\Omega$. The output impedance can be found by taking both branches in parallel and is given by

$$\begin{aligned} R_{out} &= \frac{(5.81 \cdot 10^3 + 6.5 \cdot 10^3)(7.81 \cdot 10^3 + 6.5 \cdot 10^3)}{5.81 \cdot 10^3 + 6.5 \cdot 10^3 + 7.81 \cdot 10^3 + 6.5 \cdot 10^3} \\ &= 6.6k\Omega \end{aligned} \tag{31}$$

It seems that when the on-resistance of the transistors are equal to the resistances of R_d that the output conductance is constant. In further work it can be interesting to analyze this behavior, but that is not the scope of this paper and therefore is not done in this paper.

The maximum deviation in output conductance for the Constant Resistance Inverters is given by

$$max_{dev,CRI} = \frac{150.1 \cdot 10^{-6}}{135.5 \cdot 10^{-6}} = 1.1 \tag{32}$$

The output impedance for the Constant Resistance Inverters is equal to $R_{out} = \frac{1}{0.14 \cdot 10^3} = 7.1k\Omega$. By using eq. 11 the output impedance for the SCPA is equal to $7100/34 = 208.8\Omega$. To get the desired output impedance of 5Ω is impedance scaling with a factor $\frac{208.8}{5} = 41.8$ necessary. A result of the impedance scaling is that the input capacity is increased with a factor 41.8. This is a factor 9.7 times higher than for the CMOS Inverter and Clock-overlap method. The output impedance of the SCPA is thus given by

$$R_{out,SCPA} = \frac{7100}{34 \cdot 41.8} = 5.0\Omega \tag{33}$$

D. SCPA

An 8-bit SCPA is used to analyze the effect of the linearization technique on the AM-AM and AM-PM distortions. The input is an analog tone with a frequency of 105MHz, which is converted to a digital signal. The clock speed of the sample and hold is set at 400MHz, to represent the four-phase LO that is used in figure 1. The switching time of the transistors is 10% of the clock speed, hence $T_{rf} = 0.25ns$.

The AM-AM distortion can be seen in figure 9. The AMAM curves seem to be constant at -6.5 dB, a constant AMAM response indicates an almost linear output response. For input amplitudes larger than 0 dBFS the AMAM distortion increases. This is a result of clipping and therefore an increase in AMAM distortion is expectable.

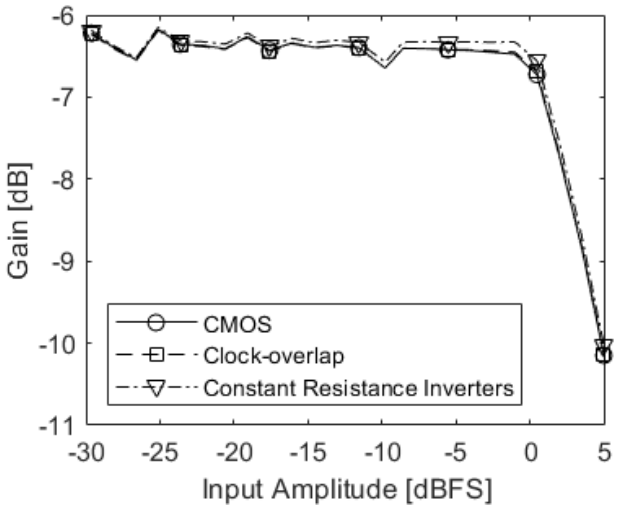


Fig. 9: AM-AM Response.

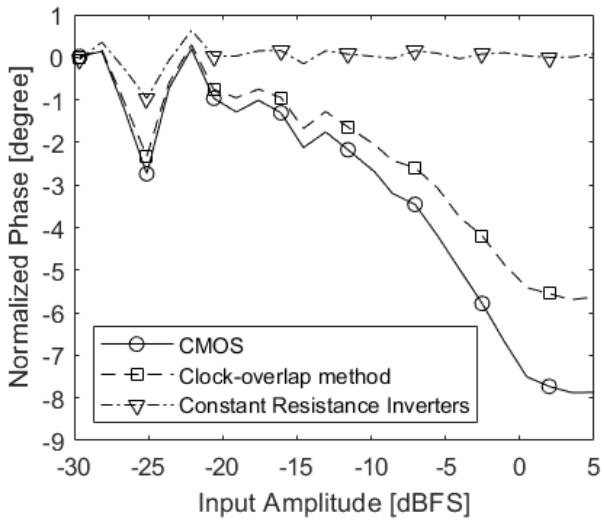


Fig. 10: AM-PM Response.

The AM-PM distortion can be seen in figure 10. The phases have been normalized to zero degrees, because it simplifies comparing the different techniques. A result of the conversion to the digital domain is the quantization noise. Due to the quantization the low input amplitudes are inaccurate and due to input clipping the high input amplitudes are inaccurate. That is why the maximum deviation in phase will be calculated for amplitudes between -20 dBFS and 0 dBFS. This deviation will be derived by subtracting the lowest phase from the highest phase.

For the CMOS Inverter, the Clock-overlap method and the Constant Resistance Inverters the deviation in phase is respectively given by

$$Phase = -1 + 7.2 = 6.2^\circ \tag{34}$$

$$Phase_{Co} = -0.8 + 5.2 = 4.4^\circ \tag{35}$$

$$Phase_{CRI} = 0.2 + 0.2 = 0.4^\circ \tag{36}$$

The Constant Resistance Inverters have the lowest deviation in phase and hence the most linear AMPM response.

VI. Conclusion

The aim of this work is to compare the Clock-overlap method and the Constant Resistance Inverters based on their effect on the linearity and the input capacity by performing transistor level simulations. An analytical model of the output conductance has been derived; it has been used to analyze the influences of the linearization technique on the output conductance. The CMOS Inverter without the use of any of the two techniques has a maximum deviation of 15.53 in the output conductance. By using the Clock-overlap method this was reduced to a maximum deviation of 4.74. The input capacity for the Clock-overlap method remains the same as for the CMOS Inverter. The Constant Resistance Inverters had a maximum deviation of 1.1, however at a cost of 9.7 times higher input capacity than the CMOS Inverter. Simulations on a 8-bit SCPA verify that the Constant Resistance Inverters are more linear than the Clock-overlap method, because it reduces the AM-PM distortion of the CMOS Inverter with 4 degrees more than the Clock-overlap method. It can be concluded that the Constant Resistance Inverters have a better linearity than the Clock-overlap method, but at a cost of a higher input capacity. The results of the Clock-overlap method are corresponding with the claim that is made in [4], that the linearity is improved by using the Clock-overlap method.

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