Efficiency comparison between Si and GaN based triple half bridge BLDC motor drivers

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***Abstract*—Many battery powered applications such as unmanned aerial vehicles and personal electric vehicles rely on brushless direct current (BLDC) motors and their complementary three-phase drivers. Efficiency is critical in these applications, as the goal is to achieve optimal performance in a small package size. The efficiency of BLDC motor drivers is continuously improving as a result of developments in semiconductor technology. In this paper, two triple half bridge BLDC motor drivers are designed, one based on Si power metal-oxide-semiconductor field-effect transistors and one based on enhancement mode GaN high electron mobility transistors. In both systems, parameters that have an effect on drive efficiency are studied. The losses in a BLDC motor driver mostly consist of conduction losses, switching losses and diode losses. For this reason, on-state resistance, turn-on time, turn-off time and diode forward voltage are the main focus.**

I. Introduction

Ever since they were invented in 1962, brushless direct current (BLDC) motors have been used in many applications due to their superior characteristics when compared to their counterparts such as induction motors and brushed direct current (DC) motors [1]. The benefits of BLDC motors include high efficiency, high reliability, high power densities and more precise torque control due to their inherently lower inertia [2]. On top of that, the commutation is performed electrically so the commutator brushes found in brushed DC motors are no longer needed. This reduces friction and wear in the system, which means the lifetime of BLDC motors is only limited by the bearings.

However, all these benefits come at the cost of a much more complex control circuitry. BLDC motor controllers generally require a microcontroller (MCU) to control the commutation sequence of the motor, where each of the three phases is driven by a half bridge [3]. The MCU generates logic signals that are used to turn on the corresponding high or low side of the half bridge. Ideally, each of these half bridges would consist of two ideal, lossless, switches that can turn on instantaneously and have a zero on-state resistance. In reality, these switches are almost always implemented using silicon power metal-oxide-semiconductor field-effect transistors (MOSFETs). These switches have a significant gate charge and a nonzero on-state resistance, which leads to power losses [4]. As BLDC motors are often used in battery powered applications such as unmanned aerial vehicles and personal electric vehicles, efficiency is very important. Semiconductor technology is continuously improving and over the years, the properties of silicon (Si) semiconductors have improved greatly. However, Moore's law shows that researchers are now close to reaching the theoretical limits of Si [5]. This means that we are forced to explore new materials in order to further advance semiconductor technology.

One of these new materials is gallium nitride (GaN): a wide bandgap, high electron mobility material. It has been shown to have many advantages over silicon, including a lower achievable on-state resistance and much lower gate capacitance which allows for faster switching [6]. There are also some downsides to the use of GaN technology, such as a slightly lower thermal conductivity and a more complicated manufacturing process [5].

The goal of this paper is to perform an efficiency comparison between a Si based and a GaN based BLDC motor driver by relating the theoretical advantages of GaN technology to practical power losses. This is done by first designing two motor drivers: one based on silicon power MOSFETs and one based on enhancement mode GaN high electron mobility transistors (HEMTs). Measurements are then performed on each driver to gain insight into the different types of power losses that occur.

This paper starts with a theoretical background on the working principle of a BLDC motor driver in Sec. II. Then, the different mechanisms that are causing power losses are explained, including a theoretical estimate of these losses based on datasheet parameters and an example load in Sec. III [7]. This is followed by a breakdown of the inherent differences between Si and GaN devices that influence their electrical characteristics in Sec. IV. Then, the design of a simple BLDC motor driver and the measurement setup will be discussed shortly in Sec. V, followed by the measurement results in Sec. VI and a conclusion in Sec. VII.

II. Motor driver theory

An Electronic Speed Controller (ESC) controls the speed and torque of a BLDC motor by supplying it with an adjustable three phase waveform. Generally speaking, ESC's consist of six transistors configured to form three separate half bridges. Each half bridge drives one of the phases by connecting it either to the positive supply rail or to ground. During a full electrical rotation, a phase follows the sequence of 120° high voltage, 60° floating, 120° low voltage, 60° floating [3]. Thus, at any given time during a commutation cycle, one phase is connected to the supply while another is connected to ground and the remaining phase is floating.

The magnetic field that is created by the neodymium magnets inside the rotor imposes a back electromotive force (back

EMF) on the floating phase. In a sensorless controller, this back EMF is used to perform position sensing for the commutation cycle. In Fig. 1, the voltage and current waveforms of each phase are shown. It can be seen that the current waveform lags the zero crossing waveform by 30°. Each time a zero crossing of the floating phase voltage occurs, the energizing sequence is advanced after a 30°delay. The 30°delay is in place to ensure that the commutation sequence is advanced at the optimal time, which results in maximum efficiency, optimal motor torque and minimum torque ripple.

The zero crossings can be detected using a comparator connected to the virtual neutral point and the floating phase as shown in Fig. 2. The virtual neutral point is created by three resistors connected to the three phases in a star configuration. This results in the zero cross signal shown in Fig. 1. A high-to-low zero crossing results in a low comparator signal and a low-to-high zero crossing gives a high signal. There are three phases and two phases are energized at any given time, which gives six possible states. During a commutation cycle, these six states are created by the MCU in a specific order based on the comparator signal.

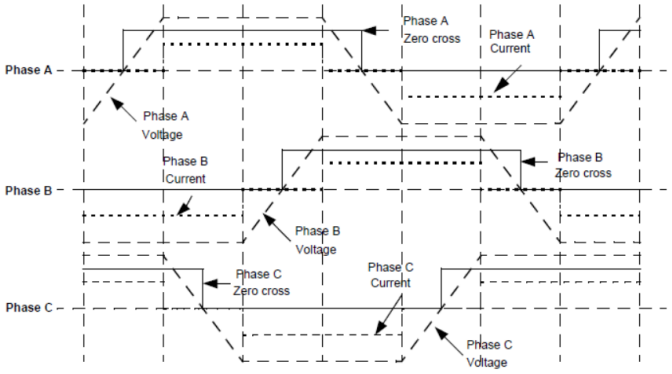


Fig. 1: Voltage and current waveforms of the three phases [8]

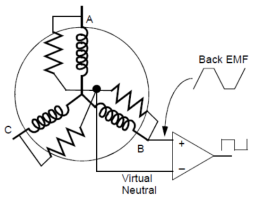


Fig. 2: Zero-crossing detection [8]

In order to control the rotational speed, the voltage applied across the two energized phases must be regulated. If both the high side and low side transistors were continuously on in the period between two zero crossings, the phase current would become very large at low rotational speeds as the back EMF is still very small.

To solve this problem, pulse width modulation (PWM) with a frequency of 30 to 60 kHz is applied to the energized high side while the corresponding low side is continuously conducting during 120° of an electrical rotation. The duty cycle is varied to change the rotational speed. A larger duty cycle results in larger phase currents at equal back EMF, and a larger maximum back EMF. This in turn results in a greater rotational speed. This type of control is called block PWM control and the resulting gate drive voltages are shown in Fig. 3. This is the simplest way to implement the BLDC commutation scheme. Other methods such as sinusoidal and space-vector commutation are capable of providing a higher efficiency and smaller torque ripple at the cost of larger computational complexity, but they are outside the scope of this paper[9].

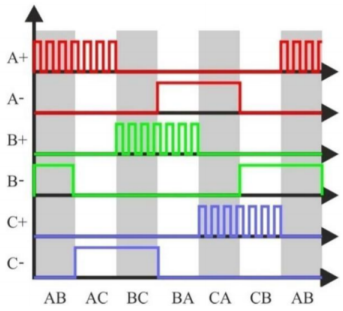


Fig. 3: Block PWM[3]

III. Theoretical power loss

Power losses in ESC's are generally dominated by the losses that occur in the switches [1]. These losses are caused by their non-ideal characteristics, such as a nonzero on-state resistance, gate capacitance and turn-on and turn-off times.

When calculating power losses in FETs in a synchronous application such as a BLDC motor driver, there are four main sources that need to be taken into account. The three largest sources are the conduction losses, switching losses and diode losses. Then there are blocking losses which are caused by leakage currents. Infineon provides an application note that contains the mathematical tools for power loss calculations in MOSFET-based converters[7]. Although these tools were originally developed to calculate losses in regular silicon MOSFETs, the same tools can be applied to GaN FETs. Using these tools, each source of power loss will be elaborated on below.

A. Conduction losses (P_c)

Conduction losses are caused by the on-state resistance of the transistor (R_{DSon}), which is typically given in the manufacturer datasheet. When current flows through the transistor in the on-state, conduction losses are given by ohms law. In Sec. VI, the real on-state resistance of the used transistors is determined experimentally.

Current flow during the time when two phases are energized depends on the phase inductance and the voltage across the phases, which is given by $V_{DD} - V_{BEMF}$. Assuming a realistic $L_p = 20\mu H$ for the phase inductance and a back EMF voltage of 0 V for the calculations below. This represents the worst-case scenario where a large mechanical load is placed on the motor and the rotational speed is very low. As rotational speed increases, back emf voltage will rise and consequentially the phase current and conduction losses will decrease.

The drain-source voltage during the on-state is given by:

$$u_{DS}(t) = R_{DSon} \cdot i_D(t) \tag{1}$$

This results in the following instantaneous power loss:

$$p_c(t) = u_{DS}(t) \cdot i_D(t) = R_{DSon} \cdot i_D^2(t) \tag{2}$$

The average continuous power loss is given by:[7]

$$P_c = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_c(t)dt = R_{DSon} \cdot I_{Drms}^2 \tag{3}$$

When the controller is loaded with a BLDC motor, the current will increase linearly during the high part of a PWM period and decrease linearly during the low part. The slope is determined by the phase inductance and the back EMF voltage generated by the rotational movement of the windings between the permanent magnets of the stator.

The current during the high part of PWM can be written down as:

$$i_D(t) = I_{sh} + \frac{1}{2 \cdot L_P} \cdot \int_0^t (V_{DD} - V_{BEMF})dt, 0 \leq t \leq \frac{D}{f_{sw}} \tag{4}$$

And the current during the low part of PWM as:

$$i_D(t) = I_{sl} - \frac{1}{2 \cdot L_P} \cdot \int_0^t (V_{DD} - V_{BEMF})dt, 0 \leq t \leq \frac{1-D}{f_{sw}} \tag{5}$$

Where i_D is the transistor drain current, I_{sh} is the phase current at the turn-on point of the PWM signal, I_{sl} is the phase current during the switch from a high to low PWM signal and L_P is the phase inductance. V_{DD} is the bus voltage and V_{BEMF} is the back EMF voltage. It can be seen that the current follows a triangle waveform during a commutation sequence, so its RMS value is easily obtained. Given that the RMS value is the RMS current in a single phase for the duration of the corresponding high-side PWM block. Due to the nature of the applied PWM, the current does not have a DC offset in our case so I_{sh} = 0 A. For a duty cycle of 50% and a back EMF voltage of 0 V, the following conduction losses are obtained:

$$I_{Drms} = \frac{2.5 \cdot 10^4 \cdot 12 \cdot 16 \cdot 10^{-4}}{\sqrt{3}} = 2.77A \tag{6}$$

$$P_c = 1.5 \cdot R_{DSon} \cdot I_{Drms}^2 = 11.52 \cdot R_{DSon} \tag{7}$$

Where P_c are the total conduction losses in the three phases and R_{DSon} is assumed equal between all six transistors. Going by the datasheet values of the Si and GaN transistors, this gives:

$$P_{c,Si} = 599mW \tag{8}$$

$$P_{c,GaN} = 576mW \tag{9}$$

Actual values are expected to be slightly lower as V_{GS} is 12 V instead of 10 V which the on-state resistance was specified for in the datasheet.

B. Switching losses (P_{sw})

Switching losses occur during switch-on and switch-off transients. Turn-on and turn-off times are influenced by many factors such as the slope of the gate voltage, output capacitance, loading condition and parasitics. An accurate theoretical value for the switching losses based on datasheet parameters cannot be given here. This is mainly due to the differences in testing conditions that were used for obtaining the datasheet rise and fall times between the Si and GaN transistors. It is expected that measurements will point out that the GaN transistor has faster rise and fall times compared to the Si transistor as this is one of the inherent benefits of GaN technology. In Fig. 4, the switching losses are visualized.

The switching losses are split up into two parts: turn-on and turn-off losses. The total switching losses are given as the sum of the turn-on and turn-off losses. There are also some additional losses as a result of the gate charging process, although these are generally small. For ease of calculation, a linear approximation of the switching process is used. This represents the worst-case calculation.

Turn-on energy:

$$E_{on} = \int_0^{tr} (u_{DS}(t) \cdot i_D(t)dt) = \frac{U_{DD}}{2} \cdot I_{Don} \cdot tr \tag{10}$$

Turn-off energy:

$$E_{off} = \int_0^{tf} (u_{DS}(t) \cdot i_D(t)dt) = \frac{U_{DD}}{2} \cdot I_{Don} \cdot tf \tag{11}$$

FET switching loss:[10]

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} = \frac{U_{DD}}{2} \cdot I_{Don} \cdot (tf + tr) \cdot f_{sw} \tag{12}$$

Gate charge loss as a function of gate capacitance:[10]

$$P_G = (Q_{g-H} + Q_{g-L}) \cdot V_{gs} \cdot f_{sw} = (C_{g-H} + C_{g-L}) \cdot V_{gs}^2 \cdot f_{sw} \tag{13}$$

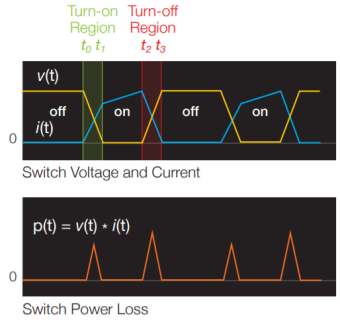


Fig. 4: Power loss in transition state[11]

C. Diode losses (P_d)

In both Si and GaN transistors, an intrinsic diode is present. During operation of the drive, this diode has two modes of operation.

During the low part of a PWM cycle, the high side transistor of the energized phase is switched off. As the load is inductive, current will continue to flow during this period. The intrinsic diode of the low side transistor of the same phase closes the

loop and allows current to keep flowing in the same direction during this time. This mode of operation is called synchronous rectification.

Each time the energized phase is switched at the end of a commutation cycle, demagnetization of this phase occurs. The energy that is stored in the phase inductance is released through the diode as the current decreases to zero. This mode of operation is called phase demagnetization.

Due to the nature of the applied PWM in the board that was designed for carrying out the measurements in this paper, current decreases to zero at the end of every low PWM pulse. This means that the phase is already demagnetized at the moment the commutation sequence is advanced, so no additional calculation for diode losses during the phase demagnetization period is required. Losses during phase demagnetization are generally smaller than those during synchronous rectification due to the smaller root mean square (RMS) current and time duration.

The losses that occur are a result of the forward voltage of the diode. In GaN FETs, this forward voltage is higher than in Si FETs[12], so diode losses are expected to be larger in GaN FETs. To maximize efficiency, it is best to keep the diode conduction time as small as possible. In a BLDC motor driver application, this can be done by turning on the transistor that is causing the diode losses. As soon as the high side turns off, there is a preprogrammed deadtime delay and then the low side turns on. Diode losses then only occur during the deadtime and can be reduced to a minimum. This approach is not followed in this paper as it increases computational complexity and timing constraints. As diode losses are generally larger in GaN than in Si devices and form a larger part of the total losses, minimizing diode conduction time is even more beneficial here.

The diode losses are estimated by using an approximation of a DC voltage source in series with a resistance. The voltage source represents the diode zero-current forward voltage and the resistance represents the on-state resistance of the diode. The parameters are read from the datasheets as shown in Fig. 5, and are then represented in Table I. The line that is used to calculate the parameters is drawn tangent to the region that is of interest, so approximately between 0 and 4.8 A. Heating of the device during operation is neglected here. It should be noted that the graph provided in the GaN datasheet does not allow for very accurate readings so the obtained parameters are only rough estimates.

For the calculations below, again a phase inductance of $L_p = 20\mu H$ and a back emf voltage of 0 V is assumed.

The diode forward voltage is given by:[7]

$$u_D(i_D) = u_{D0} + R_D \cdot i_F \tag{14}$$

Where u_{D0} is the voltage of the series voltage source, R_D is the series resistance and i_F is the diode current.

Instantaneous diode power dissipation is given by:[7]

$$P_{CD}(t) = u_D(t) \cdot i_F(t) = u_{D0} \cdot i_F(t) + R_D \cdot i_F^2(t) \tag{15}$$

This gives the following continuous power dissipation:[7]

$$P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} (p_{CD}(t)dt) = u_{D0} \cdot I_{Fav} + R_d \cdot I_{Frms}^2 \tag{16}$$

Each low-side intrinsic diode conducts for $\frac{1}{6}$ of the time. Three phases makes it equal to one diode conducting half of the time, assuming equal characteristics. Filling in the parameters shown in Table I and using the RMS current found in equation 6 gives the following values:

Si diode power dissipation:

$$P_{CD,Si} \approx \frac{1}{2}(u_{D0,Si} \cdot I_{Fav} + R_{d,Si} \cdot I_{Frms}^2) = 0.793W \tag{17}$$

GaN diode power dissipation:

$$P_{CD,GaN} \approx \frac{1}{2}(u_{D0,GaN} \cdot I_{Fav} + R_{d,GaN} \cdot I_{Frms}^2) = 1.15W \tag{18}$$

It is found that while both transistors seem to have a similar diode forward voltage during the zero-current condition, the GaN intrinsic diode has a much larger on-state resistance compared to the Si diode as shown in Table I. This will result in increasingly large diode losses in the GaN device as phase current increases, which makes it a requirement to minimize diode conduction time when used in high-current drives as explained earlier.

As the phase current is relatively low, most of the diode loss comes from the DC offset in the forward voltage. This is comparable for both transistor types. As phase current increases, the differences will become more pronounced. It can already be seen that the Si transistor is superior compared to the Si transistor when it comes to diode loss.

TABLE I: U_{D0} and R_D

	Si	GaN
$U_{D0(mV)}$	640	670
$R_D(m\Omega)$	6.4	90

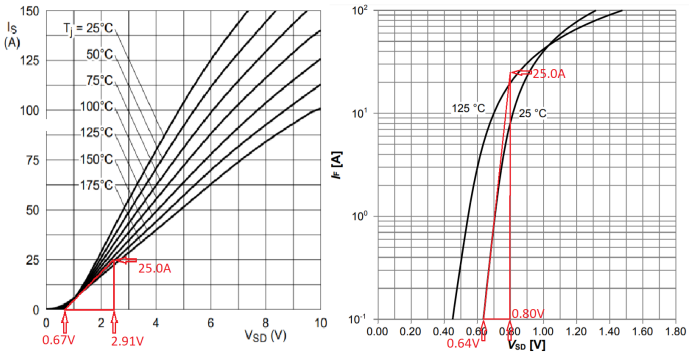


Fig. 5: GaN (left) vs Si (right) diode forward voltage

D. Blocking losses (P_b)

Blocking losses occur due to a small leakage current that is present when a voltage V_{DS} is applied in the off-state. However, these leakage currents are often so small that the

blocking losses are left out in power loss calculations. The leakage currents given in the datasheets of the Si and GaN transistors are in the nA to uA range for a drain-source voltage of 600 V. Considering the drain-source voltage is only 12 V here, leakage currents will be extremely small and are omitted.

IV. GaN vs Si

GaN technology has many performance benefits over Si technology. The main benefits are listed below, starting with an introduction to the working principle of GaN devices. This is followed by a breakdown of the benefits of GaN devices that are most beneficial in BLDC motor drivers.

A. Working principle

There are two types of GaN devices: depletion type and enhancement type devices. A depletion type device is normally on and requires a negative V_{GS} to turn off, while an enhancement type device acts like a regular MOSFET: it is normally off and requires a positive V_{GS} larger than $V_{GS,th}$ to turn on.

Depletion type devices are not very practical for use in BLDC motor drivers as they require a negative voltage to be applied before start-up to prevent a short-circuit between the supply voltage and ground. It is possible to use a depletion type device and work around this issue by placing it in cascade with a silicon MOSFET such that it practically acts as a normally off device, but this introduces additional complexity in the system [6]. Other than their complementary operating mode, depletion and enhancement type devices have similar characteristics. The better choice here is to use an enhancement type GaN device.

A GaN device consists of different elements than a Si MOSFET does. It is built on top of a silicon substrate, and a two-dimensional electron gas (2DEG) is in place between the aluminum gallium nitride (AlGaN) barrier layer and the GaN buffer layers as shown in Fig. 6. It is interrupted near the gate in the off-state, and forms a continuous conductive path when V_{GS} exceeds $V_{GS,th}$. This electron gas provides a very high charge density and electron mobility [6]. In Fig. 6, the left side represents the off-state and the right side represents the on-state of a GaN device.

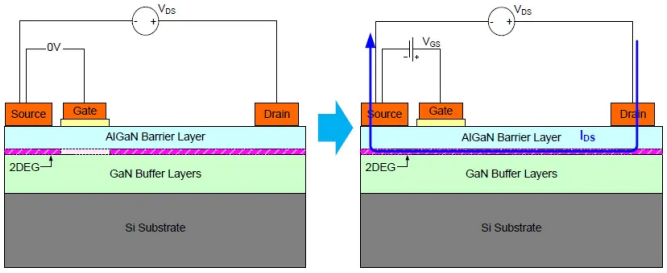


Fig. 6: GaN HEMT [6]

B. Electron Mobility

GaN devices are also called high electron mobility transistors (HEMTs). This is because GaN has an electron mobility of 2000 cm^2/Vs while Si has an electron mobility of 1500 cm^2/Vs. This means that the electrons in GaN are able to move $\frac{2000-1500}{1500} = 33\%$ faster compared to Si [5]. This contributes to the ability to use higher switching frequencies in GaN devices. While this may generally not be one of the main requirements in motor drivers, higher switching frequencies allow for larger PWM frequencies to be used. This is especially advantageous when more complex commutation schemes such as sinusoidal and space-vector commutation are used that inherently require faster switching frequencies when compared to block PWM. Higher PWM frequencies will result in smaller current ripples regardless of the commutation scheme, and this results in smoother torque and higher efficiency.

C. On-state Resistance

GaN has the potential to achieve significantly lower on-state resistances than Si, as shown in Fig. 7. This means that conduction losses will be smaller with GaN. However, as availability of GaN transistors is currently very limited and the technology is still developing, the difference in on-state resistance is not yet as significant as it will be once the technology has matured. From the datasheet parameters given in Table II, it can be seen that both the used Si and GaN transistors have a similar on-state resistance at a gate-source voltage of 10 V with GaN $R_{DS,on}$ being only slightly smaller than Si. Both transistors can be driven with a gate voltage of up to 20 V, in this case 12 V is used. This will lead to both on-state resistances being slightly smaller than the datasheet values.

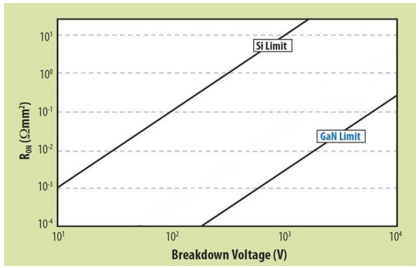


Fig. 7: Comparison of theoretical limits [13]

D. Gate Capacitance

Gate capacitance in GaN is much smaller than in Si. This has a few distinct benefits. The first is that the losses that occur as a result of charging and discharging the device are smaller. Generally, these losses only become significant at high switching frequencies and small load conditions such as in radio frequency (RF) circuits. Another advantage is that less power is required to drive the circuit, so the requirements on the gate driver are lower. This can save cost and space as a smaller, low power gate driver may be sufficient.

E. Breakdown Voltage

GaN breakdown voltage is larger than that of Si. The breakdown field of GaN is 3.3 MV/cm, while that of Si is 0.3 MV/cm. One of the reasons for this is that the bandgap of GaN is 3.2 eV, while that of Si is 1.1 eV. This significantly larger bandgap means that more energy is required

for an electron to be excited from the valence band to the conduction band. Due to this property, GaN is not as suitable for low voltage applications. However, for high voltage and high power applications, this is desirable as it results in a higher breakdown voltage and greater thermal stability at high temperatures [5]. A higher breakdown voltage allows GaN to be used in high voltage motor drivers, which reduces the current for a given power rating. This in turn results in smaller conduction losses.

F. Switching Time

Turn-on and turn-off times are smaller in GaN than in Si. As can be seen in Fig. 4, smaller time in the turn-on and turn-off region results in smaller switching losses. Switching losses are often quite large in BLDC motor drivers, so reducing the turn-on and turn-off time has the potential to increase the overall efficiency. When looking strictly at the datasheet parameters in Table II of the GaN and Si transistors that are used in this experiment, it would seem that the Si transistor has a comparable rise time as the GaN transistor while the falltime is significantly faster in Si. However, these values should be taken with a grain of salt as the testing conditions differ between the two transistors. Key parameters such as the gate-source voltage and loading condition were unequal during acquisition of these datasheet values so they cannot be compared directly.

G. Cost

The production cost of GaN devices is inherently lower than that of Si devices. For the production of GaN devices, standard manufacturing processes can be used that are already in place for the production of Si devices. If the goal is to achieve similar performance as existing Si devices, GaN devices can be made significantly smaller and more devices can be produced on a single wafer. This results in the cost of GaN devices being lower than that of their Si counterparts. Further development of GaN technology will continue to widen this gap [14].

V. Measurement Setup

The measurement setup with the BLDC motor as load is shown in Fig. 9. A second equivalent motor with an electrical load consisting of three 2Ω power resistors in star configuration is connected to the first motor to provide some form of mechanical load. This reduces the rotational speed and back-emf of the driven motor in such a way that there is a large enough difference between the bus voltage and back-emf voltage for a substantial phase current to flow when rotating at a constant speed. For the measurements where a resistive load is used, the three star-configured power resistors are connected to three phases on the printed circuit board (PCB) directly.

The 12 V power supply consists of a lithium polymer battery pack with three cells in series and a capacity of 2200 mAh. All three cells are charged to a voltage of 4.00 V using an isdt T8 balance charger. While performing the measurements, the charger is turned off for a short duration to reduce noise caused by the switching regulator in the charger. No-load output voltage after performing the measurements was found to be greater than 11.91 V in all cases, so the maximum supply voltage deviation as a result of the battery discharging is smaller than 1%. Using the isdt T8 balance charger, internal cell impedance was measured to be between 3.9 $m\Omega$ and 4.1 $m\Omega$, giving a total impedance of 12 $m\Omega$. This was confirmed using an SM8124A battery resistance tester, which uses a 1 kHz AC signal and the four-wire method to determine cell impedance. Output impedance of the supply measured at the PCB pads was found to be 13.9 $m\Omega$. For the resistive load, current is approximately 3 A and this resulted in a voltage drop of around 45 mV.

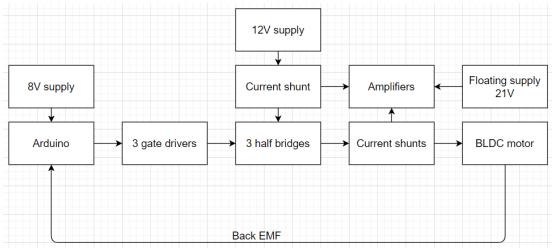


Fig. 8: Block diagram of measurement setup

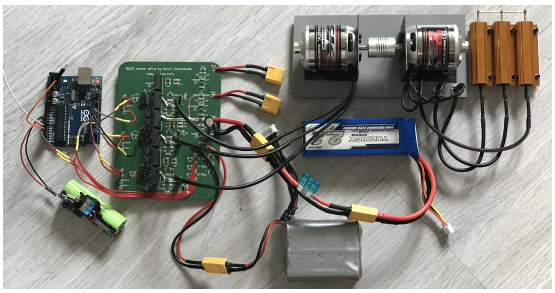


Fig. 9: Measurement setup

A. PCB

Two similar ESC's are designed for use with Si and GaN FETs. The main requirement is that the layout and components of both boards are as similar as possible to ensure comparable results, while taking into account the different properties of both types of transistors.

1) FETs: For choosing the Si and GaN FETs, some criteria are defined here to ensure that the results accurately reflect the differences as a result of the used semiconductor material rather than simply the type or quality of the transistor that is used. This proved to be a significant challenge, as there are many factors that influence power losses in transistors. Even with two silicon MOSFETs that are considered comparable based on certain parameters such as package size and on-state resistance, there would most likely be measurable differences in power loss. In Table II, key parameters are listed in the left column.

It was decided that package size, maximum drain-source voltage and continuous drain current should all be similar. Other parameters, such as gate charge, threshold voltage, turn-on and turn-off delay times and rise and fall times do not

need to be similar as these are heavily influenced by the semiconductor material.

TABLE II: Key parameters

Parameter	Si	GaN
Package	TO-247	TO-247
$V_{DS,max}$	650V	650V
$R_{DS,on} V_{GS} 10V$	52mΩ	50mΩ
$Q_{g,typ}$	68nC	15nC
$I_{D,cont}$	35A	34.5A
$I_{D,pulse}$	135A	150A
$V_{GS,th}$	3.5V	3.9V
t_r	11ns	10ns
t_f	4ns	11ns

Currently, GaN semiconductor technology is still in its infancy. This means that the availability of GaN FETs is very limited compared to their silicon counterparts.

2) Driver: The gate drivers supply current to the transistor gates based on the logic signal that is generated by the arduino uno. A gate resistor is usually placed in series with the gate driver output in order to limit the current into the transistor gate. This slows down the turn-on and turn-off of the transistor, and thereby increases switching losses. For maximum efficiency, the gate resistor should be made very small or omitted altogether in combination with the use of a powerful gate driver. However, the goal here is to capture the switching process using an oscilloscope with a sampling rate of 1 Gs/s and be able to extract accurate turn-on and turn-off times from this data. An added benefit of using a gate resistor is that it reduces ringing caused by parasitic inductances. As the layout of the PCB may or may not be optimal with respect to parasitics, this could prove very useful.

For the gate drivers, the ir2104 is chosen. This is a very common and relatively low-power half-bridge gate driver with built in deadtime. Its key parameters are shown in Table III. The same gate driver is used on both versions of the PCB.
A gate resistance of 100 Ω gives a peak gate current of approximately 120 mA which is within the specification of the driver. The slope of V_{GS} is dependent on the gate capacitance and for the transistors that were chosen earlier, V_{GS} is given by equation 19 and 20.

$$V_{GS,Si} = \frac{1}{2.85 \cdot 10^{-9}} \int I_G dt \tag{19}$$

$$V_{GS,GaN} = \frac{1}{1 \cdot 10^{-9}} \int I_G dt \tag{20}$$

A simple LTSpice simulation shows a charge time of 83 to 116 ns to reach the gate threshold voltage of 3.0V to 4.0 V for Si with a gate capacitance of 2850 pF and a gate resistance of 0.8Ω. The discharge time from 12 V back to the threshold voltage is 307 to 389 ns. The combined charge and discharge time does not necessarily need to be smaller than the driver deadtime in this case, as there is a delay of 60°in the commutation scheme between high-side turn-off and low-side turn-on and the other way around. If a different PWM scheme were used that also applies PWM to the low-side gate, deadtime should be large enough to avoid crossconduction issues that could potentially create a short between the bus line and ground. For GaN, the charge time is 34 to 48 ns with a gate capacitance of 1000 pF and a gate resistance of 2.3 Ω. Discharge time is 100 to 129 ns. Gate threshold for GaN ranges from 3.4V to 4.5 V. These times are valid assuming that $V_{GS,drive}$ behaves as an ideal square wave. Real charge times will be larger depending on the driver output rise time and its ability to maintain a steady voltage during the charging process.

TABLE III: Gate driver parameters

$I_{source}(mA)$	130
$I_{sink}(mA)$	270
$t_{on}(ns)$	680
$t_{off}(ns)$	150
$Deadtime(ns)$	520

Due to the fast-switching nature of GaN devices, they are more susceptible to resonance and instability. Although the switching is slowed down with the use of a gate resistor, GaN switching times are still expected to be fast. a DC-link snubber is added to reduce the Q factor of any resonance that might occur. Recommended values for the GaN transistor are 4 Ω in series with 20 nF.

Additionally, an RC snubber is placed on the switching node to limit the dv/dt during turn-off. This will suppress any large voltage spikes caused by rapid switching of the inductive load. Recommended values for the RC snubber are 10 Ω in series with 100 pF. Losses in the RC snubber will be larger than those in the DC-link snubber, although still extremely small due to the low capacitance value of 100 pF. While the Si device is slower, resonance and voltage spikes during turn-off could still occur. For this reason, it was decided to leave both snubbers in for the Si-based PCB.

3) Current sensing: For the current sensing, there are multiple options such as current shunts, hall sensors, current transformers, LEM current sensors and rogowski coils. The benefit of using a rogowski coil is that it is extremely fast and can sense fast transient currents in the range of a few nanoseconds. The downside is that they are quite bulky and difficult to integrate with the other electronics on the PCB, and they require an additional integrator. The two most practical options are current shunts and hall sensors. Out of these two, the current shunt in combination with a current shunt amplifier seems to be the best option as it has superior characteristics such as a lower susceptibility to noise and a larger bandwidth. In a hall sensor, the sensed wire and the sensor are coupled through a transformer that may influence the frequency response of the sensor. Shunt-based current sensing generally also has a higher accuracy as a result of the lower sensitivity to external magnetic fields, especially at low currents[15]. Driving a BLDC motor will generate significant magnetic fields, and a shunt-based solution is less likely to be affected by this. A downside of shunt-based current sensing is the additional heat dissipation in the shunts, but this can be kept to a minimum by correct scaling of the shunt resistance. Power dissipation in current shunts can be easily calculated with ohm's law.

Current shunts of 2 mΩ are placed in series with each phase. For the bus line, 2 mΩ,20 mΩ and 200 mΩ are used. The latter two were added to have the possibility of more accurate measurements at low currents in case this was found to be necessary, depending on used equipment and noise levels in measurements.
The power ratings of the used current shunts are as follows:
20 mΩ and 200 mΩ shunts are 1206 type SMD resistors rated for 500 mW
2 mΩ shunt is a 2512 type current sense resistor rated for 5 W

The continuous power dissipation as a function of phase current for the input shunts is given by:

$$P_{cont} = I_p^2 \cdot R$$

$$I_{p,max} = \sqrt{\frac{P_{cont}}{R_{shunt}}}$$

I_P represents the phase current.
Current only flows through 2 phases at a time, so the current limit imposed by the phase shunts is:

$$I_{p,max} = \sqrt{\frac{3P_{cont}}{2R_{shunt}}}$$

This is always larger than the limit of the 2 mΩ input shunt.
Maximum current for 2 mΩ, 20 mΩ and 200 mΩ respectively:

$$I_{p,max,2m} = \sqrt{\frac{5}{2 \cdot 10^{-3}}} = 50\,\text{A}$$

$$I_{p,max,20m} = \sqrt{\frac{0.5}{20 \cdot 10^{-3}}} = 5\,\text{A}$$

$$I_{p,max,200m} = \sqrt{\frac{0.5}{200 \cdot 10^{-3}}} = 1.58\,\text{A}$$

To filter out large transients that are caused by the rapid switching of the inductive load and by other effects such as parasitics and noise, a lowpass filter is placed between the shunt and the amplifier. One effect that may come into play here if no filter is used, is the parasitic inductance of the shunt itself which is approximately 3 nH.

The switching frequency of the transistors is 31.25 kHz. The cutoff frequency of the lowpass filter should be larger than this, while it should be low enough to filter out unwanted noise and transient peaks. A frequency of 97.045 kHz is achieved by using a resistance of 16.4 Ω and a capacitance of 100 nF, which yields a time constant of 1.64 μs. This is approximately 20 times faster than a single switching cycle.

The current sense amplifier should have sufficient bandwidth and gain. The ADM4073H current sense amplifier is suitable with a gain of 100 and 1.6 MHz bandwidth. This large bandwidth has the advantage that the lowpass filter has the freedom to be adjusted if the response is not satisfactory.

VI. Measurements

In this section, measurements will be performed on the PCB's. First, the measurement setup will be verified. This is followed by measurements of the conduction losses, switching losses, diode losses and total system efficiency.

A. Verification

The system is verified to test whether it works as expected, and to validate the results of other measurements. First, the proper working of the logic signals and gate voltages is verified. In Fig. 10, the two input logic signals to the gate driver can be seen in combination with the resulting high-side and low-side gate voltages. Note that these measurements were all taken with respect to PCB ground as a differential probe was not available. During the 60°of the commutation cycle before and after the high-side PWM block, the high-side measurement is referenced to the floating phase.

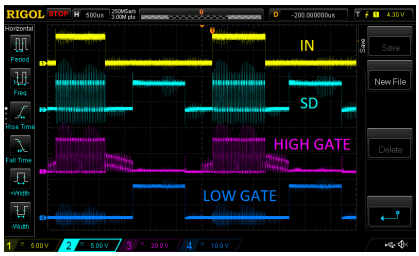


Fig. 10: Logic signals and resulting gate voltage

When measuring phase current into the motor, large spikes are observed in the output voltage of the current sense amplifier. This results in unrealistic peak values for the phase current, as the actual current could not possibly rise this quickly based on the phase inductance. These spikes do not occur when the driver is loaded with a resistive load instead, as can be seen in Fig. 11. The exact reason behind this behavior remains unclear and further research is required to get to the root of this issue. The current measurements with a resistive load seem normal and the current during a single PWM pulse can be seen in Fig. 12. For this reason, the measurements in the sections to follow are also done using the same resistive load instead of the BLDC motor. The commutation scheme is still followed, and the applied logic signals remain the same.

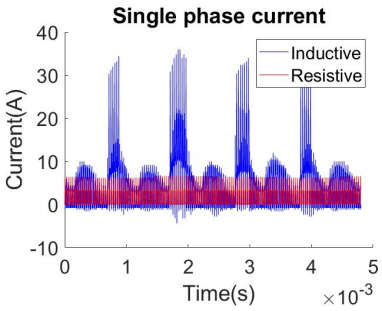


Fig. 11: Single phase output current for resistive vs inductive load

Verifying the current sensing with a resistive load is relatively straightforward as the expected value and waveform of the current are known. When measuring directly across the shunt, readings are very noisy as expected. The lowpass filter gives very clean measurements and the initial peak is also removed as shown in Fig. 12. This initial peak in the voltage across the shunt is too large to be explained by the charging

effect of parasitic capacitances, so it must be a result of the shunt inductance and does not represent an actual current flow. As the peak is very large, this will introduce some error into the current measurements even with the lowpass filter in place.

Note that measuring directly across the shunt gave too high readings of around 3.8 A steady state. This is likely due to the placement of the oscilloscope probe which introduced a small additional resistance. The resistance of the power resistors that are used as a load, is measured using an SM8124A battery resistance tester using a 1 kHz AC signal and the four-wire method similar to what was done previously in Sec. VI. The reason this meter is used is because a high accuracy LCR meter is not available, and the accuracy for resistance measurements is stated to be $\pm 3\%$ in its datasheet. The results are shown in Table IV, where A denotes the resistor that connects directly to phase A etc.

TABLE IV: Measured load resistance $\pm 3\%$

	A	B	C
$R(\Omega)$	1.93	1.93	1.89

The amplifier output is closer to the expected value in steady state with 3.2 A. The expected steady state current is $I = \frac{12}{1.93+1.89} = 3.14\,\text{A}$, although there is some margin for error as the resistance the load might deviate slightly. Additional error sources include small deviations in the supply voltage, current shunt resistance and amplifier gain.

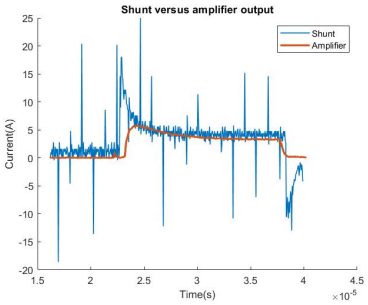


Fig. 12: Effects of current sense amplifier combined with low pass filter

B. Conduction losses

On-state resistance is measured by switching on one high-side and one low-side FET at a time using a resistive load of 2 Ω per phase. The expected current is again 3 A. Results are shown in Table V.

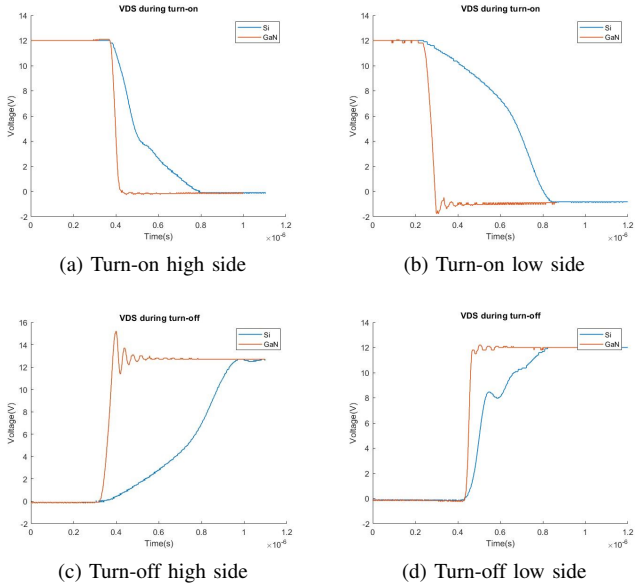
TABLE V: measured conduction loss at 12V V_{GS}

	Si						GaN					
	High side			Low side			High side			Low side		
	A	B	C	A	B	C	A	B	C	A	B	C
VDS(mV)	141.6	146.8	144.4	142.0	142.8	143.2	94.0	110.0	105.6	108.8	108.0	107.6
ID(A)	3.06	3.16	3.38	3.38	3.06	3.16	3.40	3.32	3.26	3.26	3.40	3.32
RDS(mΩ)	46.27	46.46	42.72	42.01	46.67	45.32	27.65	33.13	32.39	33.37	31.76	32.41
E(uJ)	3.47	3.71	3.90	3.84	3.49	3.62	2.56	2.93	2.75	2.83	2.94	2.86
P(mW)	72.2	77.3	81.3	80.0	72.8	75.4	53.3	60.9	57.4	59.1	61.2	59.5

Using the measured on-state resistance and current during single PWM pulse of 16 μs, conduction losses are calculated. Values in Table V are for a duty cycle of 50% and switching frequency of 31.25 kHz (switching period of 32 μs). The fourth row gives conduction loss during a single PWM pulse, the fifth row gives the average conduction loss in watts. The calculation would be similar for an inductive load, although current then increases linearly during a PWM pulse.

C. Switching losses

Main source of switching losses: turn-on and turn-off times



(a) Turn-on high side (b) Turn-on low side

(c) Turn-off high side (d) Turn-off low side

Fig. 13: V_{DS} during turn on and turn off

In Fig. 13, drain-source voltage during turn-on and turn-off of phase A high-side and low-side transistors is shown for both boards. Using matlab, 10-90% rise and fall times are extracted from the data. These values are shown in Table VI as turn-on and turn-off times.

Switching frequency for the high side transistors is 31.25 kHz, while the low side transistors have a switching frequency that is dependent on the rotational speed as this relates directly to the duration of a commutation cycle. For an electrical rotational speed of 333 Hz as used in the measurements, low-side switching frequency is 31.25 times smaller than high-side switching frequency. For a resistive load, low-side switching losses are zero as long as the driving high-side transistor is in the low part of a PWM cycle during low-side turn-on. In the case of an inductive load, phase demagnetization of the energized phase occurs as the commutation cycle advances so the current will be small during turn-on of the low-side transistor. During turn-off, switching losses will occur although this occurs less frequently than high-side switching. Thus, low-side switching losses are much smaller than high-side switching losses regardless of the load and will be omitted here.

The duration of a PWM block is 1/3 the duration of a full commutation cycle, so the switching loss in a single high-side transistor is given by:[10]

$$P_{sw-H,single} = 1/6 \cdot V_{DD} \cdot I_{p,avc} \cdot (t_r + t_f) \cdot f_{sw}[W] \quad (21)$$

Where $I_{p,avc}$ is the average phase current in the conduction period, t_r is V_{DS} rise time, t_f is the fall time and f_{sw} is the switching frequency.
The combined switching loss in three high-side transistors is given by:

$$P_{sw-H} = 1/3 \cdot E_{onoff} \cdot f_{sw} = E_{onoff} \cdot 10.42 \cdot 10^3 [W] \quad (22)$$

Where E_{onoff} is the combined turn-on and turn-off loss in joules.
A linear approximation of the switching process is used here. As can be seen from Fig. 13, V_{DS} is slightly lower during the switching process in reality as compared to a linear approximation for both turn-on and turn-off cases. A linear approximation gives the worst-case losses.

TABLE VI: High-side switching losses due to rise and fall times of V_{DS}

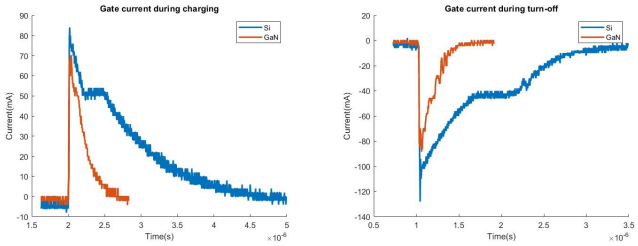
	Si			GaN		
	A	B	C	A	B	C
Turn-on(ns)	296	298	295	30.3	36.5	31.3
Turn-off(ns)	437	433	444	42.1	48.0	42.1
I_D(A)	3.06	3.16	3.38	3.40	3.32	3.26
Turn-on loss(uJ)	5.43	5.65	5.98	0.618	0.727	0.612
Turn-off loss(uJ)	8.02	8.21	9.00	0.859	0.956	0.823
Combined loss(uJ)	13.45	13.86	14.98	1.477	1.683	1.435
P(mW)	140.1	144.4	156.0	15.39	17.53	14.95

In Table VI, high-side switching losses are shown. It can be seen that the losses in GaN are approximately 9 times lower due to the significantly faster turn-on and turn-off times. Some spread between the three phases is observed in turn-on and turn-off times for GaN, which is likely due to small differences in component characteristics and small deviations in parasitics between phases on the PCB. Parasitics will play a larger role in GaN switching behavior as compared to Si due to the faster turn-on and turn-off. Spread in Si phases is found to be much smaller.

An additional source of switching losses are the driver losses as a result of the gate current. Power dissipation in high-side gate resistors is shown inTable VII. Overall power loss as a result of gate charging is relatively small. Low-side losses are omitted here as these would only make a marginal difference since no PWM is applied there. High-side losses are linearly dependent on PWM frequency. For an electrical rotational speed of 333Hz as used in the measurements, low-side losses are approximately 31 times smaller than high-side losses.

Fig. 14 shows gate current during turn-on and turn-off. A small plateau in the gate current can be observed. This is due to a plateau in the gate voltage as $V_{GS,th}$ is reached and C_{DG} is connected parallel to C_{GS}. The duration of this effect is much shorter in GaN, indicating a significantly smaller C_{DG}.

The maximum gate current is slightly lower in GaN compared to Si, which can partially be explained by the higher gate resistance of 2.3 Ω vs 0.8 Ω although this alone should not cause such as notable difference. As the duration of the peak in GaN is very small, the ability of the oscilloscope to accurately capture it using a sampling frequency of 1 Gs/s is limited.



(a) Turn-on (b) Turn-off

Fig. 14: Gate current during turn on and turn off

TABLE VII: Combined power dissipated in high-side gate resistors

	Si	GaN
$E_{on}(nJ)$	262.1	62.2
$E_{off}(nJ)$	489.5	82.2
$E_{total}(nJ)$	751.6	144.4
$P(mW)$	23.5	4.5

D. Diode losses

Diode losses do not occur when a resistive load is used, as phase current drops to zero the moment the high-side transistor of the energized phase switches off so no current flows through the intrinsic diode.

To be able to measure the diode losses that occur in the drive and see if the theoretical values that were calculated in equation 17 and 18 hold true, the BLDC motor is connected as a load. Measuring the phase current and V_{DS} on the low-side transistor during the low part of a PWM period on the same-phase high-side transistor allows the diode loss to be calculated.

Unfortunately, an issue was encountered while performing the measurements. It was found that changing the oscilloscope scale to a smaller value introduces a large DC offset of around 600 mV into the measurement. The critical step where this offset is introduced is from 1V to 500 mV per division. While the offset seems to be in the same order of magnitude every time, its exact value seems to be somewhat inconsistent which makes it very difficult to get accurate measurements for V_{DS} during the diode conduction time. This, combined with the phase current sense errors that were encountered in Fig. 11, makes that the measurement of diode losses is left out here and is left to further research.

E. Efficiency

In Table VIII, the measured conduction losses and switching losses for the resistive load are summed together to give an indication of the total power losses in both transistor types. The summed loss is found to be 1.12 W for the Si board and 0.399 W for the GaN board. The difference between total input power and total output power is found to be 2.54 W and 1.81 W for Si and GaN respectively.

While the total power losses do not match, the absolute differences between Si and GaN are very similar. From Table VIII, GaN losses are 720 mW smaller than Si losses.

Performing the same calculation on Table IX, the difference is found to be 730 mW. The remaining power loss is approximately 1.4 W for each PCB. This is a significant portion of the total loss, and the cause possibly lies within the current sensing. From Fig. 12, it is seen that the initial peak caused by the shunt parasitic inductance is attenuated by the lowpass filter although it still affects the measurement. This increases the error and may contribute to the difference in power loss that is measured. Conduction and switching losses were determined using the steady-state current so these are not influenced.

In the case of an inductive load, the gap between Si and GaN would most likely be smaller by several hundred mW due to the added diode losses as indicated by equations 17 and 18.

TABLE VIII: measured power loss

	Si						GaN					
	High side			Low side			High side			Low side		
	A	B	C	A	B	C	A	B	C	A	B	C
Conduction losses (mW)	72.2	77.3	81.3	80.0	72.8	75.4	53.3	60.9	57.4	59.1	61.2	59.5
Switching losses (mW)	140.1	144.4	156.0	-	-	-	15.4	17.5	14.9	-	-	-
P(mW)	212.3	221.7	237.3	80.0	72.8	75.4	68.7	78.4	72.3	59.1	61.2	59.5
	671.3			228.2			219.4			179.8		
	1118.9						399.2					

TABLE IX: measured efficiency

	Si	GaN
Input power	19.82W	19.46W
Output power	17.28W	17.65W
Power loss	2.54W	1.81W
Efficiency	87.15%	90.66%

VII. Conclusion

GaN technology holds several advantages over traditional Si technology that can be beneficial to the efficiency of a BLDC motor driver. The main benefits of GaN devices include a lower on-state resistance, smaller gate and output capacitances, and a higher breakdown voltage. The lower on-state resistance lowers the conduction losses, while the smaller capacitances allow for faster switching and relaxation of driver circuitry requirements. A higher breakdown voltage is beneficial in high-power drivers as a higher voltage allows the power throughput to be increased without increasing current as this would introduce additional losses into the system. It was experimentally verified that the on-state resistance and conduction losses in a GaN-based BLDC motor driver are lower than in a Si-based driver. The same was done for the turn-on and turn-off times, and the resulting switching losses.

Key to implementing GaN technology effectively in a BLDC motor driver is to keep the diode conduction time as small as possible through the use of an optimized PWM sequence, as the series resistance of the intrinsic diode is larger in comparison to Si devices. This leads to larger diode losses. A theoretical estimate is given for diode losses in a Si-based and a GaN-based driver, while real-world measurements are left to further research.

The performance advantages combined with the lower production costs as a result of their smaller size which allows more devices to be produced on a single wafer, gives GaN technology a competitive advantage over Si for use in BLDC motor drivers.

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VIII. Appendix

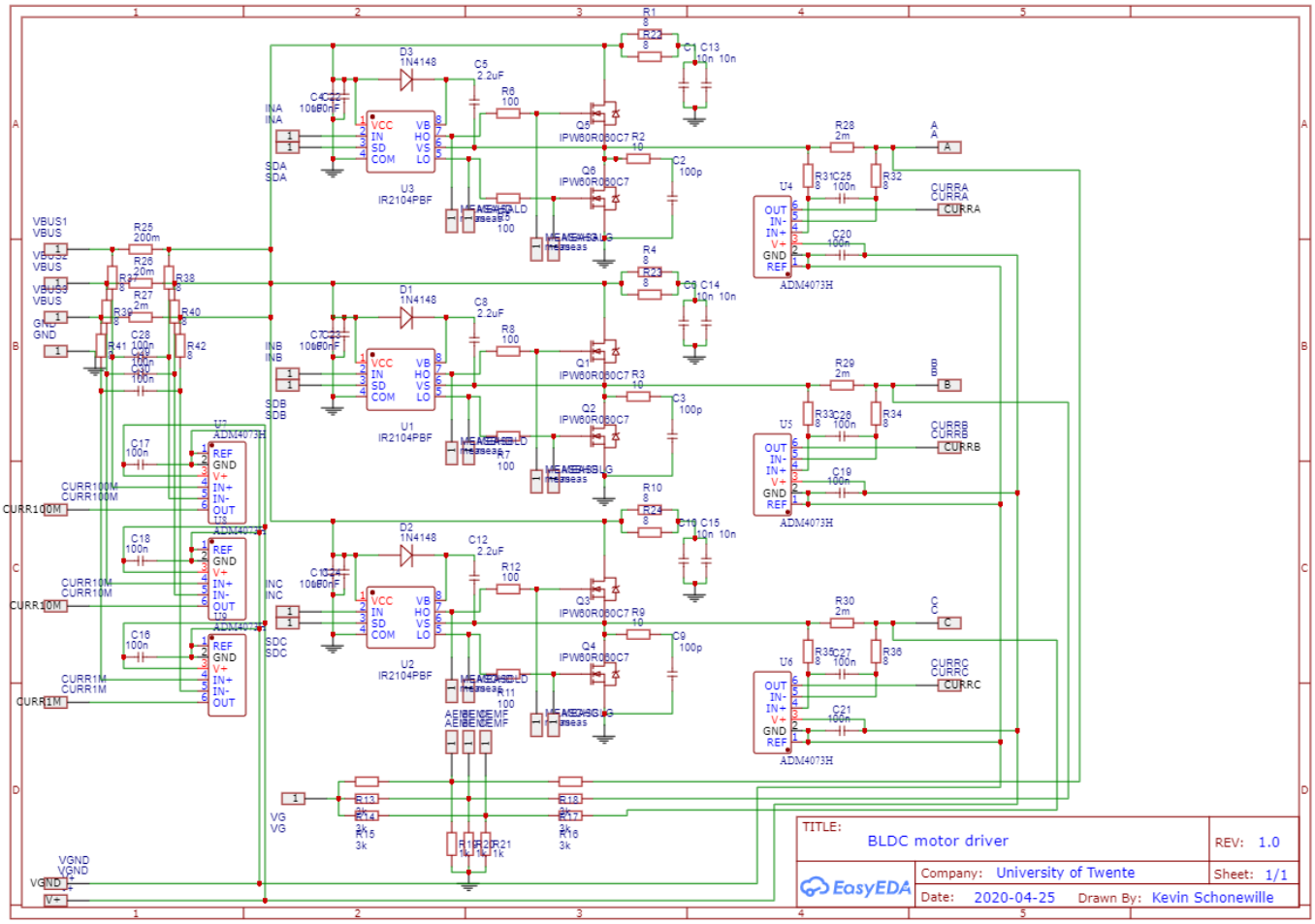

Fig. 15: Schematic diagram of the driver (Si FETs: IPW60R060C7)

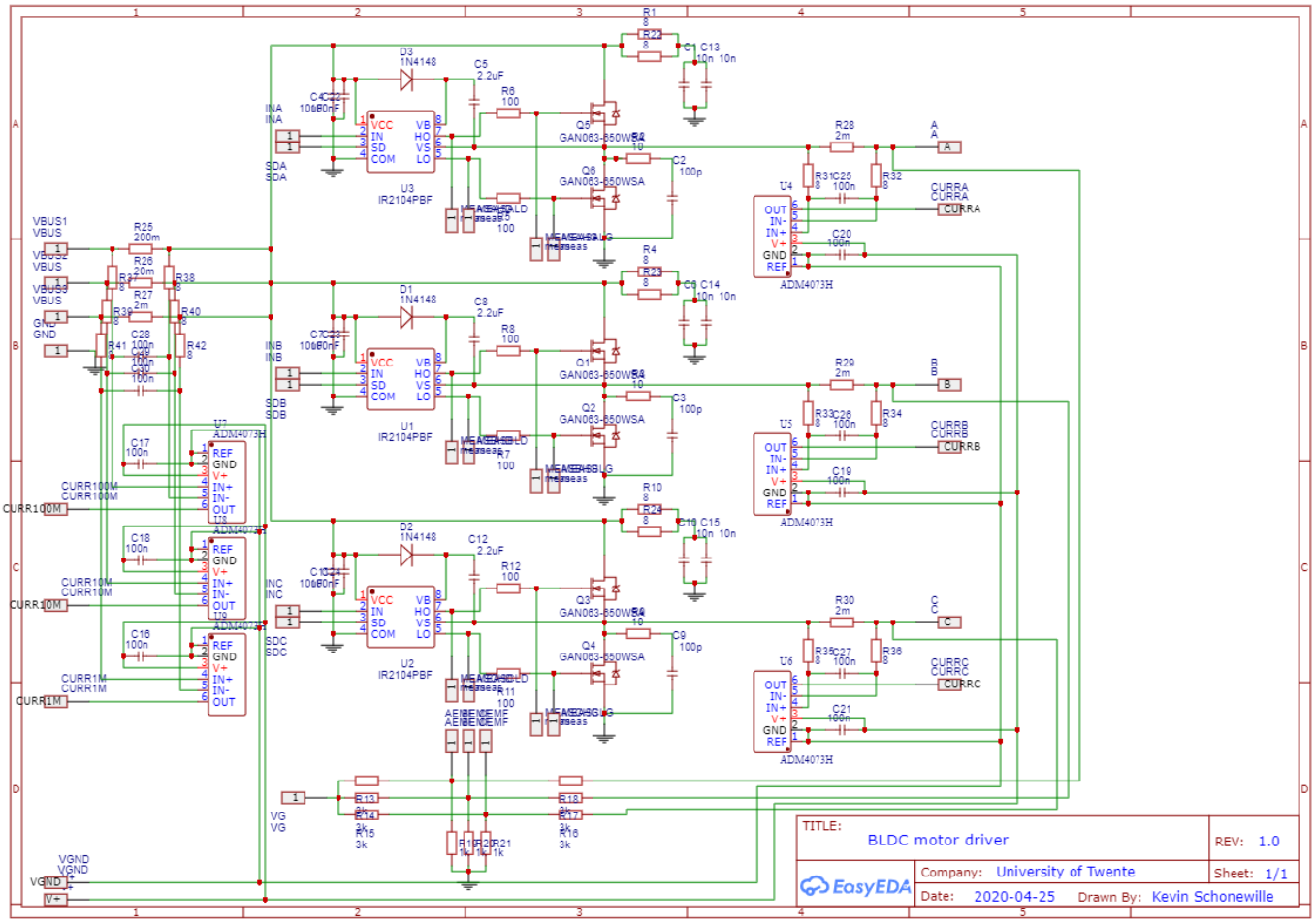

Fig. 16: Schematic diagram of the driver (GaN FETs: GAN063-650WSA)