BACHELOR THESIS REPORT

PERFORMANCE COMPARISON OF TWO DIGITAL TO TIME CONVERTER CELLS

MARIUS SLAVĖNAS

EEMCS

NOV 2020

ABSTRACT

A digital-to-time converter (DTC) is an electronic delay mechanism which can be used by the polar transmitter to encode data in Phase modulation technique or in phase lock loops to allow the division of frequency by fractional number. The DTC receives an input signal and delays the output depending on external digital code.

This report compares two popular DTC concepts: a constant slope (c. slope) and an edge-interpolated. The comparison parameters are end-point integral-non-linearity (INL), power supply rejection ratio (PSRR) and power consumption. INL provides maximum linearity deviation, which is one of the parameters when DTC is researched. PSRR provides a measure which defines the strength to reject the noise from an unstable power supply. Then, power consumes provides a power cost which tells how much power required for a device to operate correctly.

An attempt was made to distinguish the components in DTC that distort time delay by 3 dividing models in 3 supply domains assigning separate power supplies. Unfortunately, 3 supply domains affect each other, and the noisiest components can not be determined. On the other hand, simulated results showed noise dependency on the power supply. A hypothesis is that an increase in power supply voltage should reduce the time delay error, which is caused by variations in the power supply.

In this DTC comparison thesis, the c. slope and the edge-interpolated concepts were first explained. Next, LTspice simulation models were created to demonstrate the working of the concepts. Lastly, simulation results were presented, and conclusions were derived.

The simulations were done for an input signal with 33MHz frequency which is commonly used and generated by crystal oscillators. The same signal has to be applied to both concepts to deduct the noise generated by a DTC. Then, a 91ps full-scale delay is set for both designs to have identical operational range. In the initial stages of the project, time resolution was set to 100ps but after c. slope DTC simulations resulted in 91ps full-scale delay, the time resolution was changed to 91ps. The time resolution must be the same for both concepts, because resolution shows the range that a device can operate. The range is one of the factors that describe the functionality of a device.

The simulation shows that the constant slope concept had a 0.19 ps maximum INL error which is -0.01LSB, whereas the edge-interpolated concept had 8.49 ps and -0.65LSB linearity error. The linearity error of the constant slope is thus smaller than the edge-interpolated.

The constant slope DTC model rejects varying power supply noise to the time delay by at least -13.37dB, whereas the edge-interpolated has 4.37dB PSRR for a supply voltage variation by 0.1V. The PSRR shows that the edge-interpolated DTC concept is more susceptible to variations in supply voltage than the constant slope DTC concept. The edge-interpolated DTC employees MOSFETs that are susceptible to the variations of voltage in the power supply. Whereas the c. slope DTC uses a current mirror which is less susceptible to noise from the power supply and a single MOSFET. In order to improve rejection ratio, the edge-interpolated DTC current mirrors should be used to charge/discharge the time delay determining capacitor.

The power consumption of the constant slope DTC is 0.3[1] mW, whereas the edge-interpolated consumes 1.5mW. The edge-interpolator concept uses more power due to transient currents.

Comparison of parameters that were acquired from simulations shows that the constant slope DTC concept is more linear, less vulnerable to changes in supply voltage and requires less power to operate compared with the edge-interpolated DTC concept. The main problem with the c. slope DTC is that c. slope operates only on the rising edge of an input signal. Whereas, the edge-interpolated DTC can properly delay rising and falling edges of the input signal.

[1] Power comparison can not be accurate because the power consumption of DAC was not taken into account.

Contents

CHAPTER 1

INTRODUCTION

1.1 Introduction

"Time delay is often defined as the time difference between the threshold-crossing points of two clock edges. If delay is programmable by a digital code, a digital-to-time converter (DTC) results" [1]. Often used DTC concepts are variable slope, constant-slope [1] and edge-interpolate [2] circuit cells. The DTC concepts have unique, efficient applications that depend on frequency, power supply and required resolution. Also, each concept has individual advantages and disadvantages.

This research had a couple of goals. The first goal was to compare the constant slope with the edge-interpolator DTC to determine which concept will perform better in set conditions. Comparison shows which concept is more efficient in similar conditions and requirements. The second goal was to determine error sources created by a changing power supply. Known error sources can be improved in future research to reduce the influence of varying power supply.

A DTC can be used in several applications. A DTC is in a polar transmitter is used to encode the data in phase modulation. A block diagram of a polar transmitter is shown in Fig. 1. The polar transmitter requires a DTC to encode data as a variation of the instantaneous phase of a carrier signal (VCO) [3]. The phase data of a message is presented as a digital code. This code is used by the DTC to vary the instantaneous phase of a VCO signal. Thus, the message is encoded in the carrier signal via phase modulation [4].

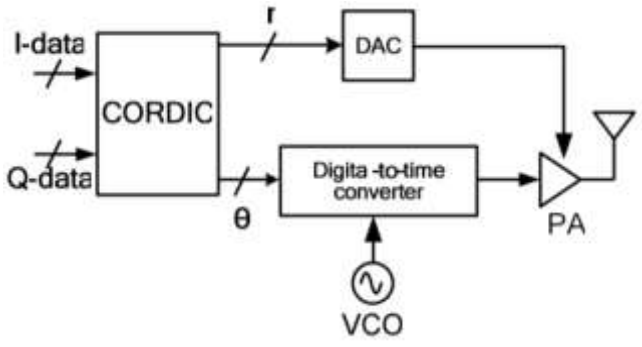


Figure 1: Block diagram of polar transmitters[3]

One more use of a DTC is in a fractional-phase locked loop (PLL) where the reference frequency can be divided by non-integer numbers. The DTC delays the Ref signal depending on the code. The DTC output produces a signal with a rising edge at the expected zero crossing of the required VCO output frequency. The block diagram of the Fractional-N PLL with a DTC

is shown in Fig. 2. In the block diagram from Fig. 2, the DTC controls a switch in the VCO feedback loop. The DTC closes the switch precisely at the expected zero-crossing of an ideal output clock of the Fractional-N PLL [4].

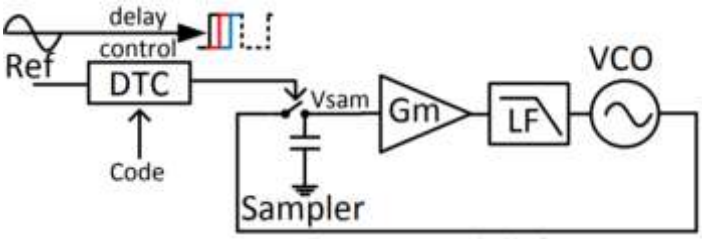


Figure 2: Block diagram of Fractional-N PLL[4]

The functionality of an electronic device can be described in 3 levels:

1. Ideal behaviour description. Provide maximum error sizes in an ideal set-up.
2. Influence of deviations. Shows the strength of additional noise generated by non-ideal input signal.
3. Cost related description. For example, required power, chip size and etc.

Therefore, the following parameters were used to compare DTC concepts: integral-non-linearity (INL), power supply rejection ratio (PSRR) and power consumption. The INL is used to acquire a linearity error of each concept. Next, the PSRR is used to measure the strength of error sources that were generated by deviating power supply. Lastly, the power consumption was calculated, to understand the power cost, which is required by DTC to operate properly.

INL: The end-point integral non-linearity of a DTC is a measure of deviation between the actual time delay provided by the DTC from the expected ideal time delay. INL error is measured when straight-line connects end-points of simulated time delay data. The INL error is a difference between the received results (blue dots) and newly drawn (red) line, as presented in Fig. 3 [6].

The INL error can be determined by taking the following steps:

1. Time delays for every code have to be obtained from measurements/simulations.
2. All obtained delays have to be presented in a graph, and a straight line has to be drawn between end-points as shown in Fig. 3.
3. The minimum time delay must be deducted from each code to neglect time delay bias which is shared trough all codes
4. Full-scale delay (τ_{fs}) ould be determined by taking the difference between end-points.

5. The INL has to be calculated via EQ 1.

$$INL(k) = \tau(k) - \frac{k}{2^N - 1}\tau_{fs} \quad (1)$$

where,

k - is the code.

N - the resolution of DTC.

τ(k) - is time delay at the code k.

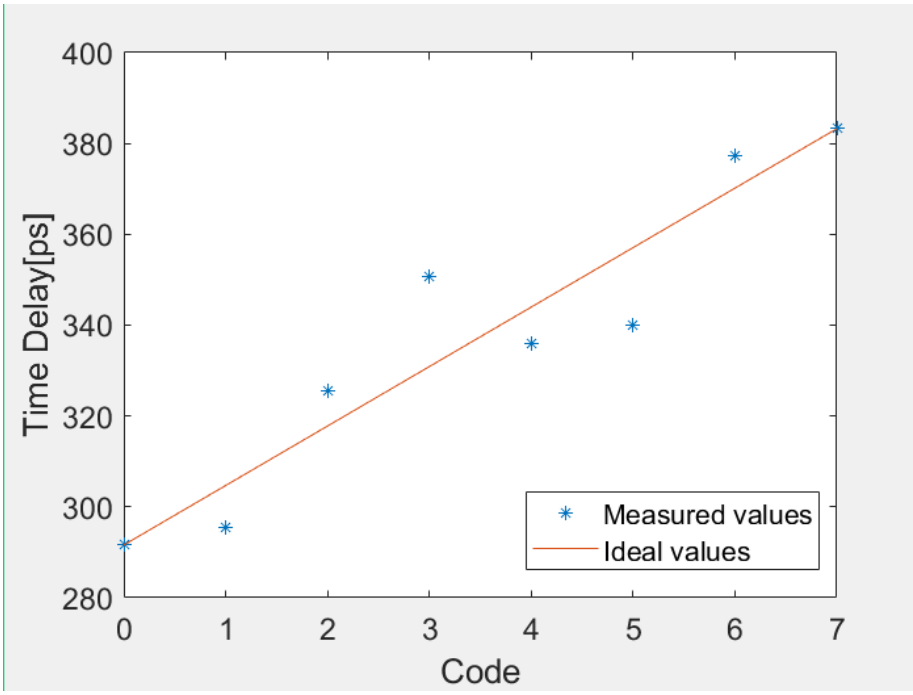


Figure 3: INL calculation graph where the INL error is time delay difference between ideal values and measured values at every code

The Power Supply Rejection Ratio (PSRR) describes the ability of a device to maintain its output while the supply voltage varies. EQ 2 presented below is the formula for PSRR [5] used in the cell comparison research.

$$PSRR = -20\log(\frac{\Delta V}{\Delta t_d}) \quad (2)$$

ΔV - is a percentage deviation in a power supply voltage. The difference between ideal and changed voltages has to be divided by ideal voltage and results presented in percent.

Δt_d - is a maximum percentage deviation between time delays when the power supply voltage of DTC is ideal and changed. Firstly, time delays for every digital code must be recorded when the power supply is ideal. Secondly, time delays for every digital code must be recorded when the power supply is changed. Then time delay errors must be calculated for each digital code.

The maximum time delay error must be divided by the time delay, which was recorded when the power supply was ideal. The calculated fraction must be presented in percent to acquire Δt_d.

Power consumption can be defined as an averaged current consumed from the supply times a supply voltage. Power will be calculated by using EQ 3.

$$P = V \bullet \bar{I} \tag{3}$$

V - DC voltage of power supply

$\bar{I}$ - average current of power supply

The structure of the report is as follows. Chapter 2 has described the constant-slope and edge-interpolated DTC concepts. Followed by this, the designs associated with both concepts are demonstrated in Chapter 3. In Chapter 4, the results of the simulated parameters are presented. Moreover, Chapter 5 presents the conclusion of thesis. Lastly, recommendations for future research has been discussed in Chapter 6.

CHAPTER 2

ANALYSIS OF DTC CONCEPTS

2.1 DTC concepts

There are many ways to implement a DTC. This report aims to check whether the constant slope or the edge-interpolated DTC consumes less power, has smaller linearity error and is less susceptible to variations in power supply. Therefore, this chapter explains concepts of interest.

2.1.1 Variable slope

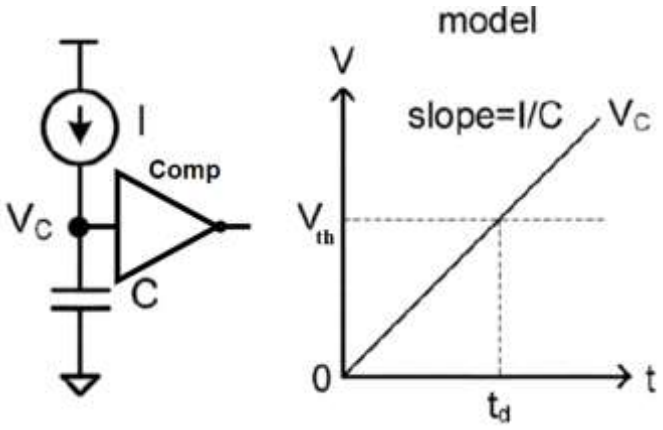


Figure 4: Ramp generation[1]

The constant slope and the edge-interpolated DTC concepts are modifications of a simple variable slope concept. The diagram of variable slope concept is shown in Fig. 4. Variable slope concept employs a current source which charges a capacitor to create a voltage ramp. Also, the variable slope utilizes a comparator (Comp) with a threshold voltage (V_{th}) which defines a delay (t_d). The delay can be calculated by using EQ 4 [1].

$$t_d = \frac{V_{th}}{S} \tag{4}$$

With S being the slope of the ramp from EQ 5

$$S = I/C \tag{5}$$

Therefore, by varying the value current I or capacitor C, it is possible to vary overall delay of this module[1].

However, the concept of variable slope is prone to linearity errors, when an inverter used as a threshold comparator [1]. All inverters have 3 different operating modes: overshoot recovery, short circuit and output discharge [6]. "During overshoot recovery, the output recovers from overshoot due to an initial input switching event; the short-circuit mode occurs when both the PMOS and NMOS conduct (but with different currents so non-zero output slope), resulting in "short circuiting" of the supply; the output-discharge mode refers to the mode with only the NMOS on." [1]. Change in the slope of inverter's input signal, vary the contribution of 3 operating modes to the transition time of output signal of an inverter. Each time the input slope changes the transition time will be different, hence INL error source in DTC concept [1].

2.1.2 Constant slope

The underlying principle associated with the constant slope is similar to the variable slope but avoids INL errors of varying slope. The constant slope concept keeps value of S constant and varies other parameters.

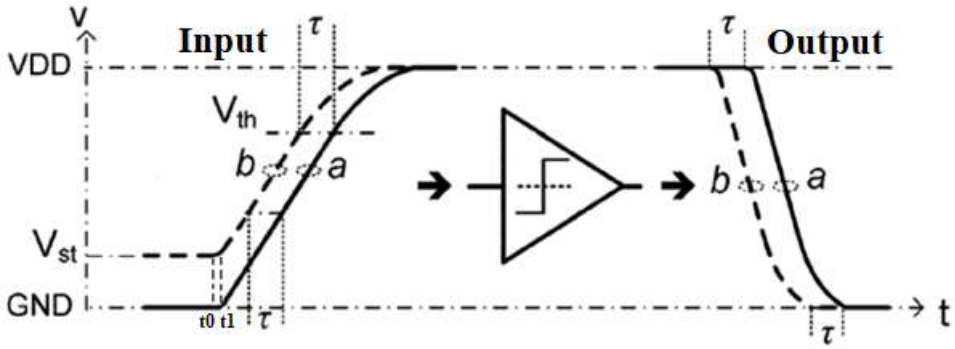


Figure 5: Delay mechanism for constant slope method with a practical input and output ramps [1]

The constant slope concept changes the starting voltage (V_{st}) across the capacitor to get different delays. The pre-charged capacitor will need less voltage range to reach V_{th}. Fig 5 shows signals with different pre-charge voltages, hence two separate delays. The time delay achieved using this concept can be calculated with EQ 6 when $V_{st} < V_{th}$ [1]

$$t_d = \frac{V_{th} - V_{st}}{S} \tag{6}$$

To generate a linearly-controlled delay, two functionality requirements must be met:

1) The input voltage ramp from Fig. 5 must have a constant-slope below maximum V_{st} [1].
2) The input voltage ramp from Fig. 5 must have a constant-shape above the maximum V_{st} [1].

Functionality requirements ensure that the trajectory of the voltage curve is shared across all the ramps, causing an addition of the same amount of delay for each ramp; thus, the linearity of DTC is not affected. Similarly, the same start-up behaviour between t0 and t1 adds an equal amount of delay for all ramps; therefore, linearity will not be affected [1].

2.1.3 Edge-interpolated

The digitally controlled edge interpolator (DCEI) generates a voltage ramp via an array of N parallel unit cells. Each cell charges the time delay determining capacitor (C_{int}) with a set amount of current ($I_{D,p}$). The implementation of cells is shown in Fig 6 a). Each cell in the parallel-connected structure is a switch which charges/discharges C_{int}. The switch is controlled by three input signals: In1, In2 and Seli. In1 and In2 are two identical input signals with a phase delay between them. The Seli is a selection signal. Seli determines whether a cell controlled by In1 (Seli = 0) or In2 (Seli = VDD). Also, Seli=0 means that the cell is *non-selected* and Seli=VDD means that the cell is *selected.*

The edge-interpolation works in two phases: Phase 1) and Phase 2).

Phase 1):

Controlled by In1 signal and operates in the time frame between the edges of In1 and In2 as shown in Fig. 6 b). In the first phase, the *non-selected* cells start charging C_{int} when In1 signal produces falling edge. Net charging current (I) is calculated by EQ 7 from Fig. 7 a) [2].

$$I = -(N - n) * I_{D,P} \tag{7}$$

Where N – is the total number of cells, n – is the number of *selected* cells.

Phase 2):

Controlled by In2 signal. The second phase starts to work when the edge of In2 is detected and continue to operate until V_{int} reaches supply voltage, as shown in Fig. 6 b). In the second phase, the selected cells will activate. Meaning the net current from selected cells will be added to the net current of non-selected cells[2]. The net current charging C_{int} will be equal to $-N*I_{D,p}$ from Fig. 7 b). Hence, the maximum possible current will charge C_{int}.

The Fig. 6 b) shows the voltage ramp slopes with a different number of selected cells.

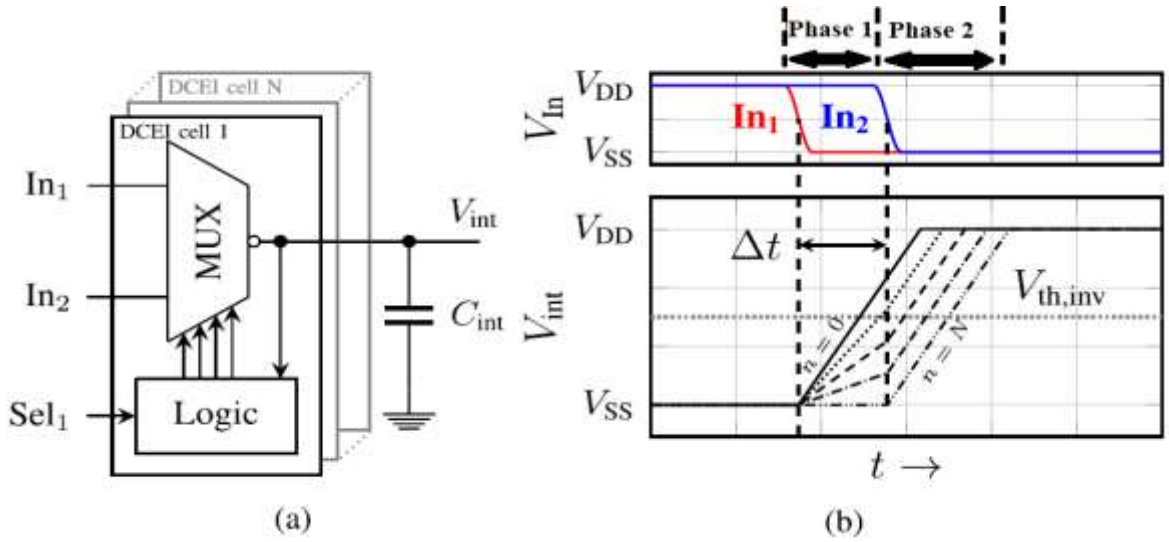


Figure 6: a) implementation of DCEI cells, and b) waveforms of interpolation process with different amount of selected cells[2]

[2] The non-selected cells are active during both phases.

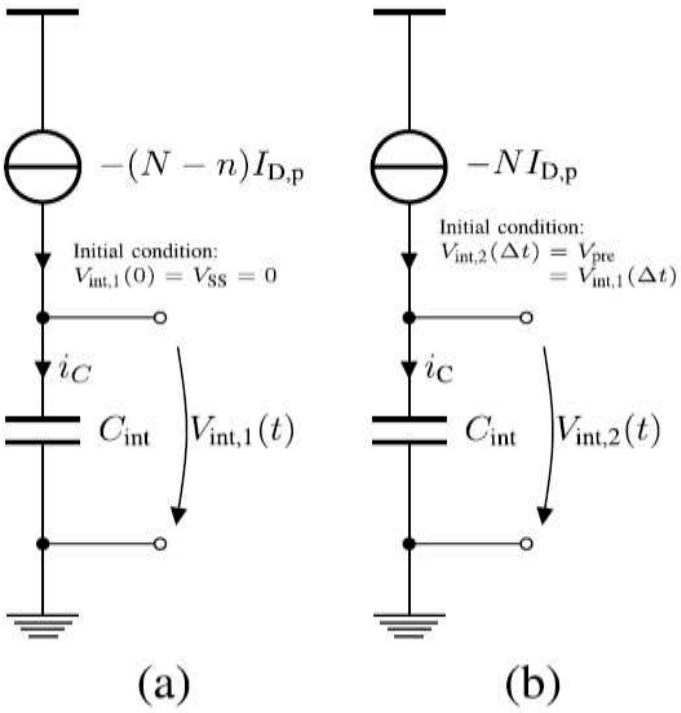


Figure 7: DCEI equivalent circuit for different regions a) $0 \leq t < \Delta t$ b) $\Delta t \leq t$. [2]

The time delay is determined using variable slope EQ 4 if V_{th} reached before Phase 2) starts, the falling edge of In2 is detected. Otherwise, EQ 6 determines the time delay and the V_{st} will be equal to the V_{int} at the time instance of the detected falling edge of In2 input signal.

Cells can supply and consume current. Therefore, the edge-interpolator DTC can interpolate on rising and falling input signals. In case the capacitor discharges the time delay can be calculated via EQ 8 and EQ 9 [2].

$$t_d = \frac{VDD - V_{th}}{S} \tag{8}$$

$$t_d = \frac{VDD - V_{th} - V_{st}}{S} \tag{9}$$

$V_{st} = V_{int}$ at the time instance of detected rising edge of In2 input signal.

2.2 Supply source variations

The central components in the DTCs are considered to be the MOSFETs. The MOSFETs can be used as switches, inverters and current/voltage sources. MOSFETs must be powered. Unfortunately, the variations of MOSFET's power supply adds noise to the signal at the Drain.

The effects of varying power supply in DTC designs is a common problem and needs to be examined.

The edge-interpolated and the constant slope DTC designs can be divided into supply domains to determine the most influential components responsible for increased time delay error. A process must be followed in order to discover the most influential. First, a power supply voltage of one domain has to be changed while keeping other supplies constant and record the time delay error. Secondly, the power supply of the initial domain has to be set back to the ideal value. Then the voltage of the next supply domain must be changed and the time delay data recorded. The process continues until all domains are tested and values are recorded.

3 supply domains with separate power supplies can be assigned to DTC designs:

1. The supply domain contains MOSFETs that are used to charge/discharge the time delay determining capacitor. The name of the power supply for this domain can be VDD1.
2. The supply of the comparator. This supply determines the trip point of an inverter in implemented designs. The name of the power supply for this domain can be VDD2.
3. The supply domain powering all secondary components: inverters and logic gates. The name of the power supply for this domain can be VDD3.

The NMOS are only susceptible to the variations at the gate voltage while in saturation as provided by quadratic MOSFET model EQ 10 because the source node of NMOS is connected to ground [7]. Hence, $t_d \propto 1/(VDD3\text{-}V_t)^2$ as can be deducted from EQ 8 and 9. When the NMOS is in the triode region, a current flow will have linear time delay proportionality $t_d \propto 1/(VDD3\text{-}V_t)$, as provided by EQ 11 [7]. Also, the current flow of NMOS will be affected by variations in VDD1 while NMOS is in the triode region. VDD1 sets the voltage magnitude at the drain node of NMOS. Therefore, $t_d \propto 1/((V_{GS} - V_t)VDD1\text{-}(VDD1)^2/2)$ can be deducted from EQ 11 if VDD3 is kept constant.

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \tag{10}$$

$$I = \mu_n C_{ox}\frac{W}{L}((V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}) \tag{11}$$

The PMOS is susceptible to voltage variations at the source and gate node, as shown by quadratic PMOS model EQ 12 [7]. As V_S node is connected with VDD1 and magnitude of V_G

node is controlled by VDD3, the PMOS is affected by supplies of first and third supply domains. When PMOS is in saturation, the $t_d \propto 1/(VDD1\text{-}V_G\text{-}|V_t|)^2$ as can be depicted from EQ 12 [7]. If the PMOS is in the triode region, a current flow is described via EQ 13, which means that $t_d \propto 1/(V_S\text{-}VDD3\text{-}|Vt|)$ and $t_d \propto 1/((VDD1 - V_G - |V_t|)VDD1\text{-}VDD1^2/2)$ [7].

$$I = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - |V_t|)^2 \tag{12}$$

$$I = \mu_p C_{ox}\frac{W}{L}((V_{SG} - |V_t|)V_{SD} - \frac{V_{SD}^2}{2}) \tag{13}$$

Moreover, supply 2 directly influences the V_{th} as shown in EQ 14 [8]

$$V_{th} = VDD/2 \tag{14}$$

Therefore, the $t_d \propto (VDD2\text{-}V_{st})$ dependency can be deducted from EQ 4 and EQ 6 for the charging time delay determining capacitor. As for the discharging time delay determining capacitor the $t_d \propto (VDD2\text{-}V_{th}\text{-}V_{st})$ relation can be deducted from EQ 8 and EQ 9.

If a current mirror structure from Fig. 8 is implemented as a current source, the varying power supply should not affect current flow. The current output of current mirror can be described via EQ 15 [9]. The output current does not depend on VDD therefore t_d does not depend on VDD too.

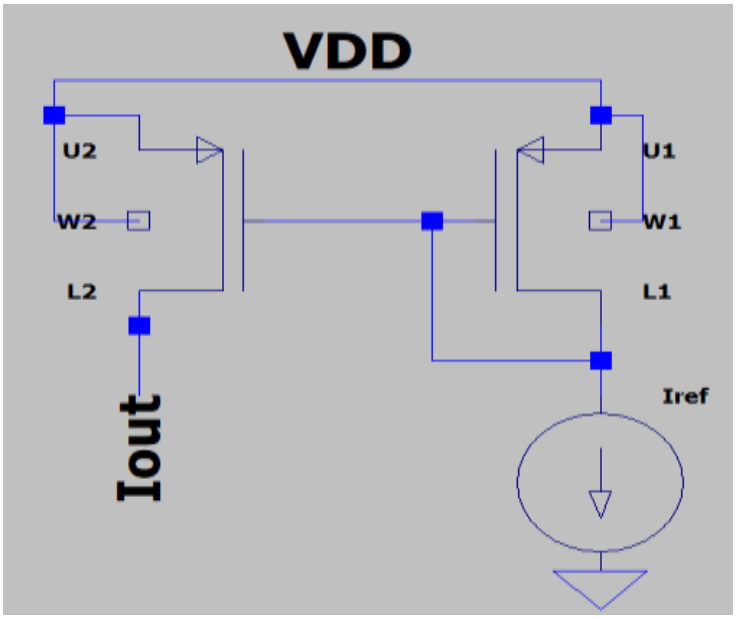


Figure 8: Current mirror structure

$$I_{out} = \frac{(W2/L2)}{(W1/L1)} Iref \quad (15)$$

2.3 Time delay error size

In real-life DTC designs, only one power source (VDD) is usually implemented. Unfortunately, varying VDD affects the current flow of every MOSFET and changes the threshold voltage of the comparator as was described in Section 2.2.

Charging of time delay determining capacitor is described via EQ 16 and the time needed to reach each voltage is described in EQ 17.

$$V_C = VDD(1 - e^{-\frac{t}{RC}}) \quad (16)$$

$$t = -RC \bullet ln(1 - \frac{V_C}{VDD}) \quad (17)$$

Where VDD is the supply voltage, C – the size of the capacitor, R – the resistance of charging MOSFET and V_C - the voltage over the capacitor at time t. The change in VDD provides different charging slopes of a capacitor. A few examples with different VDD value are plotted in Fig 9. If the threshold voltage and resistance of the charging MOSFET was kept constant, the time error would have been $t \propto \ln(1\text{-}V_C/VDD)$ proportionality. A decrease in VDD would provide a larger time error than an increase in VDD as can be seen in Fig. 9.

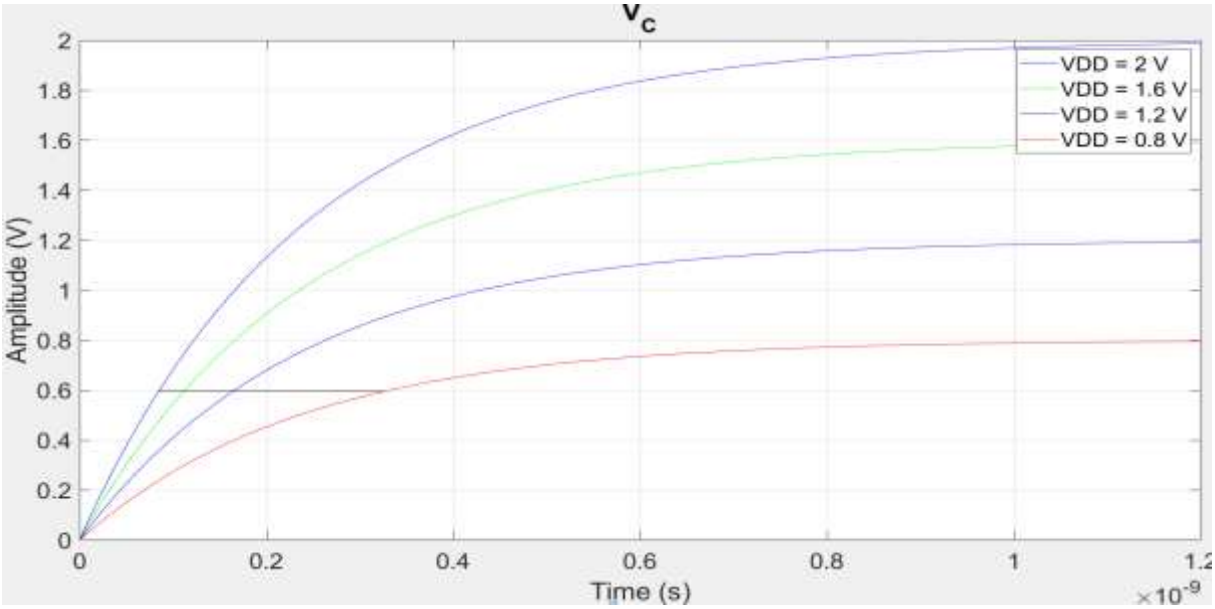


Figure 9: Voltage over charging the capacitor with varying power supply

Unfortunately, the value of V_{th} and R changes with varying VDD. EQ 17 can be simplified because the change in VDD controls V_{th} as shown in EQ 14. In order to determine the time error for different values of VDD, the $V_C = V_{th}$ time moment can be taken. As the V_{th} is half VDD, the value in logarithmic brackets will always be 0.5. Hence, EQ 17 can be simplified to EQ 18.

$$t = -RC \bullet ln\left(1 - \frac{V_C}{VDD}\right) = -RC \bullet ln\left(1 - \frac{VDD/2}{VDD}\right) = -RC \bullet ln(0.5) = 0.69RC \quad (18)$$

EQ 18 shows linear t∝R dependency because C is constant. When the VDD varies time to reach V_{th} will only depend on the resistance (R) of a MOSFET which is used to supply current. The resistance of simple PMOS is equal to EQ 19 when the V_{SD} value is small [10].

$$R = \frac{L}{\mu_p C_{ox} W(V_{SG} - |V_t|)} \quad (19)$$

The time to reach V_{th} will have t∝1/(VDD-V_G-|Vt|) proportionality. The increase and decrease in VDD should provide identical time delay errors.

CHAPTER 3

SIMULATION SET-UP

3.1 Comparison

Models of DTC concepts had to be created and simulated to extract the comparison parameters and compare the results.

A time difference between a rising edge of the input and output signals at Vth voltage for every code of 3-bit resolution (arbitrarily chosen) must be recorded to deduct time delays of a concept. After 8 time delays are recorded, an INL graph will be created by following the steps from “Introduction”. Lastly, INL is compared by taking the maximum INL value from graphs of each concept and comparing them. The INL concept with smaller INL error can be called more linear.

The PSRR calculates the influence of varying power supply. Therefore, the VDD value must be changed and the time delays for every code have to be recorded again. Next, a maximum time delay error which is caused by changing VDD must be calculated in percent. Errors are calculated by taking a deviation between the time delay value at ideal and changed VDD for every code. The biggest deviation will be the maximum error and must be converted into percent. The biggest deviation will be the denominator EQ 2. The denominator of EQ 2 should be calculated by taking the deviation between the ideal and changed VVD in percent. Finally, the rejection value in dB must be calculated via EQ 2. A concept with smaller PSRR rejects the noise created by varying power supply better than other concept of interest.

Most power efficient concept can be determined by comparing the power consumption of each concept. Power consumption is calculated by retrieving an average output current of ideal power supply over one period of an input signal and multiplying by the voltage of power supply. The DTC concept with smaller power consumption is more efficient than other DTC concept of interest.

3.2 Common parameters

The constant slope and edge-interpolated DTC concept has a few identical parameters to have a fair comparison.

The full-scale time delay 91 ps, 3-bit resolution and 1.2 V power supply was arbitrarily chosen and applied to the c. slope and edge-interpolated concept models. The full–scale delay defines

the range of possible delays. Resolution determines the number of possible delays in the full-scale range. Moreover, the input signal (XO-input, In1 and In2) for simplicity was selected to be a square wave with 33MHz frequency which is possible to obtain from crystal oscillators. The rise and fall time of the input signal was set to 1ps for both concepts because perfect square waves that that can rise/fall instantly does not exist. Therefore, to simulate real-life behaviour transitional falling and rising time is defined. Identical input signals are used for both concepts because INL determines the linearity error size that is generated by DTC device and different input signals would give different INL error in same concept. Furthermore, the size of the time delay determining capacitor was to 0.1pF to both models. The size of the capacitor is one of the main parameters that define time delay of DTC and full-scale delay for constant slope DTC[1]. Next, the provided available 130nm CMOS technology was used. Lastly, a maximum of 10 fs timestep was used to calculate accurate measurements. Even though c. slope paper provides results with accuracy of 1 fs [1], but the available processing power can only support 10fs.

3.3 Block diagrams

Block diagrams of implemented DTC designs are provided and explained in the next paragraphs.

3.3.1 Constant slope

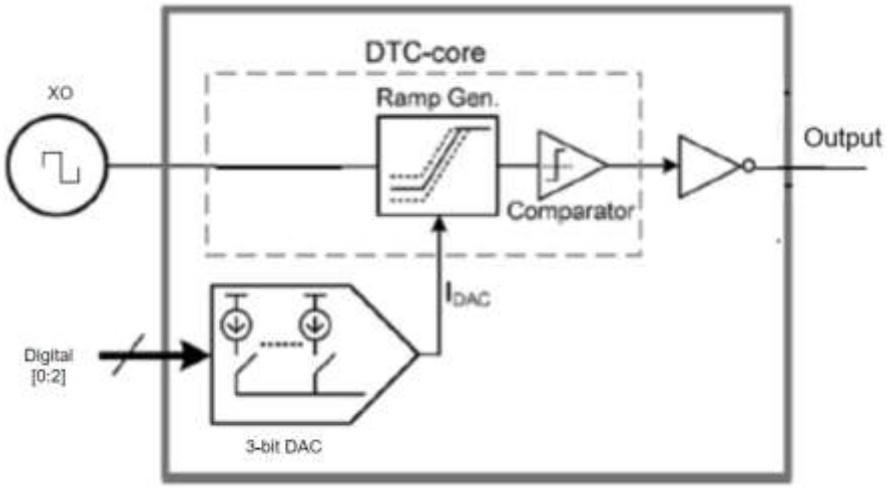


Figure 10: Block diagram of constant slope DTC [1]

The block diagram of the implemented constant slope DTC is showed in Fig. 10. The DTC requires a signal input from crystal oscillator(XO) and an external digital code. The XO signal will be used to initiate the ramp, and a digital code will control the starting voltage level of the

ramp. Lastly, the comparator will detect a threshold voltage of the ramp and output a delayed signal.

An inverter was used as a comparator which flips the signal. The second inverter was required in order to produce a signal with a linear rising edge because the constant slope DTC was designed to linearly delay and output the rising edge of XO input signal,

3.3.2 Edge-interpolated

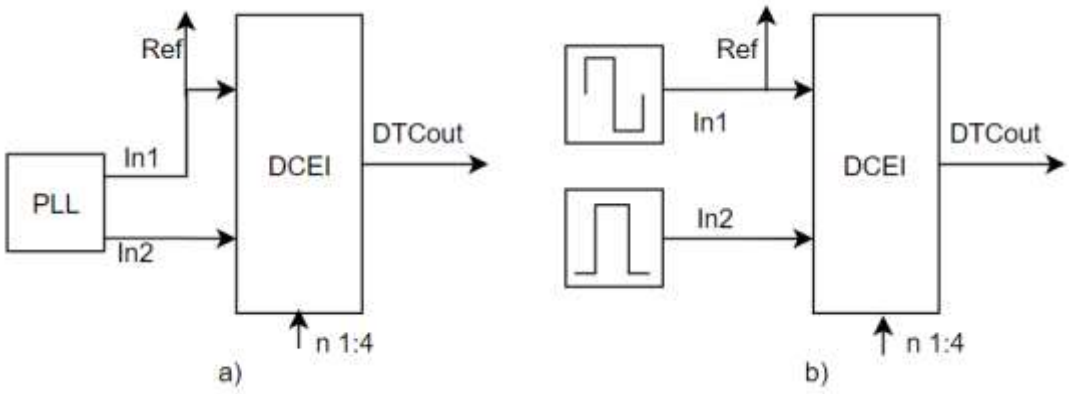


Figure 11: Block diagram of edge-interpolated DTC. a) Commonly used, and b) diagram used for the DTC comparison research

An often-used edge-interpolated DTC is presented in Fig. 11 a). The DCEI cells receive three inputs. A digital code n which determines number of selected cells (n 1:3) and specifies whether In1 (n4 = 0) or In2 (n4 = VDD) is leading. The In1 and In2 are identical signals with a phase delay between them. Also, the phase difference controls the full-scale time delay of the whole DTC. Inside the DCEI block, interpolation happens and DTCout provides a delayed signal.

The often-used edge-interpolated DTC was slightly modified and implemented in simulation model. Instead of using one complicated PLL simulation models used two wave generators to simplify the design. The In1, In2 and XO are identical signal to have fair comparison as explained in Section 3.2. Furthermore, the In2 signal is set to lag behind In1 signal by 91ps because in the edge-interpolated DTC the full-scale delay is defined by time difference between In1 and In2 signals.

3.4 DTC Architectures

The architectures of implemented concepts are presented in the following sections.

3.4.1 Constant slope

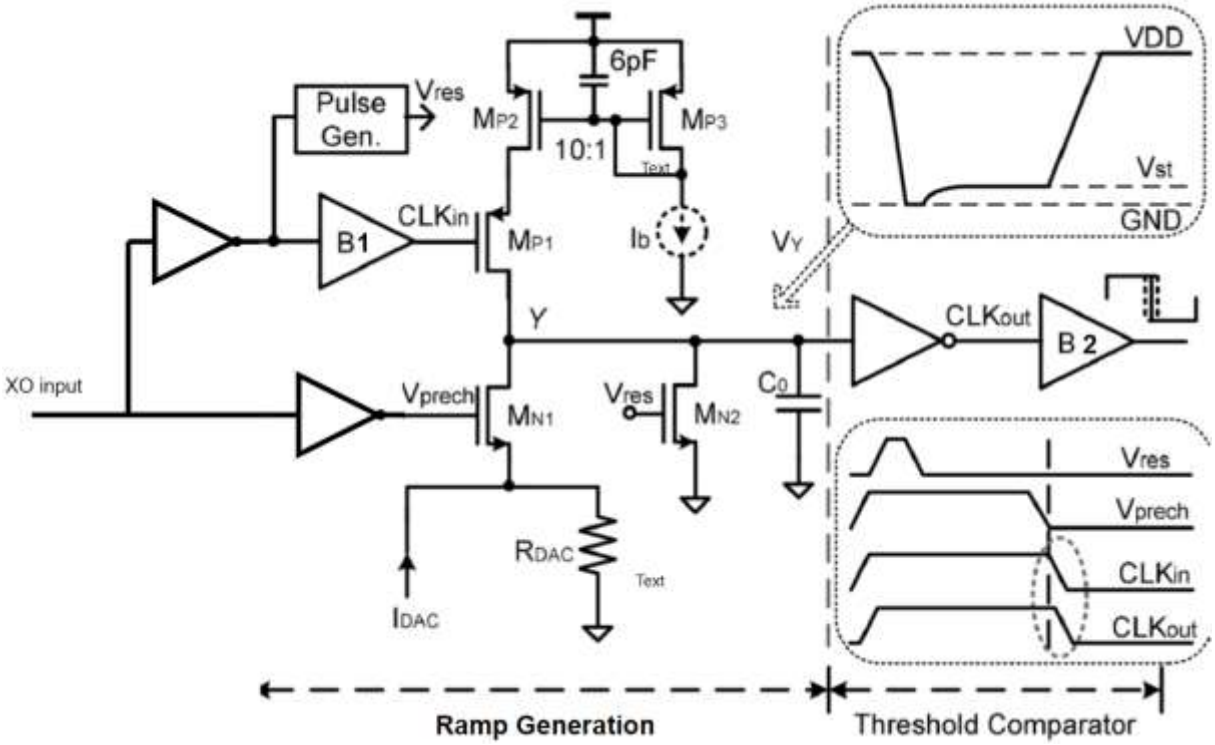


Figure 12: Circuit schematic of constant-slope DTC[1]

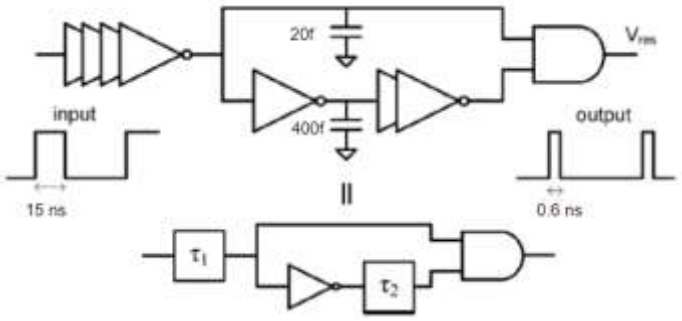


Figure 13: Pulse Generator[1]

Table I: Implemented component sizes and dimensions

Name	Size	Name	W/L
Co	0.1pF	M_{N1}	1u/0.12u
R_{DAC}	200Ω	M_{N2}	10u/0.12u
I_{DAC}	0-1mA	M_{P1}	15u/0.36u
Ib	0.026m	M_{P2}	15u/0.36u
VDD	1.2V	M_{P3}	3u/0.72u

Table II: MOSFET dimensions implemented by all inverters

Name	W/L
PMOS	1u/0.12u
NMOS	1u/0.12u

The constant slope DTC architecture is shown in Fig. 12. Dimensions if implemented components are presented in Table I and II. The "Ramp generation" operates in three stages: 1) reset – where the voltage over the time delay determining capacitor (Co) is reset to GND, 2) pre-charged – where the Co capacitor is pre-charged with the set V_{st} voltage and 3) charge – where the Co is charged.

1. In the reset stage, the capacitor Co is discharged to allow different pre-charge voltage levels. The implemented constant slope DTC provides linear rising edge of the XO signal while the falling edge is ignored. Hence, the previously mentioned operational reset stage 1 and pre-charge stage 2, work on the falling edge of XO input. Moreover, as the design employs the NMOS to discharge the Co, an inverter is required. Therefore, the XO signal travels through the inverter followed by the "Pulse generator" and activates the M_{N2} in the end.

   The "Pulse Generator" is necessary because the first two stages operate while XO input has a "low" (GND) signal; therefore, the block from Fig. 13 is used to reduce reset operating time. The "Pulse Generator" is controlled by inverters and capacitor. The top capacitor acts as a controlling agent for starting of the reset operations Whereas, the bottom capacitor controls the "width" of the output. The AND gate with two inputs determines the pulse "width" by comparing two processed inputs.
2. The pre-charge stage, which is activated by M_{N1}, is used to control the time delay by pre-charging Co. As explained in the section above, the inverted XO input signal is used to control the pre-charge. The Ohm's Law is used for setting the pre-charge voltage (V_{ST}),

   $$V_{ST} = I_{DAC} * R_{DAC} \tag{20}$$

   The I_{DAC} and R_{DAC} arbitrary chosen values that are presented in Table I.

3. The last stage is used to initiate the ramp and charge the capacitor Co with a current. The XO input signal is required to produce a rising edge to start the ramp. Then, an inversion of input is used because the PMOS switch is used to initiate the charge of a ramp. After the inverter, there is a buffer B1 (two inverters) to delay the start of the

charge. The delay is needed to initiate the charging of the capacitor after the M_{N1} switch is completely open. In a design without a buffer power would be wasted because the output of the current mirror would go to GND instead of charging the Co. The implemented B1 buffer delays activation of M_{P1} switch, which allows the current from the current mirror to only charge the Co capacitor because M_{N1} and M_{N2} are completely open. When the M_{P1} is activated, the current source will charge the capacitor. The source is made from the current mirror with the ratio 10:1. The 6pFcapacitor is used to keep the M_{P2} gate voltage stable, accordingly making the output current of the c. mirror more stable. Besides controlling the ramp, the second job of M_{P1} switch is to be a cascode transistor. The cascode improves the output resistance of M_{P2} and the linearity of the overall ramp.

The time delay created by the described architecture can be calculated by substituting EQ 5 into EQ 6.

A linear delay requires a constant current source and constant Co size. Co size was selected 0.1pF to have a 91 ps full-scale delay[3]. At VDD = 1.2 V the maximum set V_{st} = 200mV, as the M_{P1} will still be in saturation and act as a cascode for the current mirror. After voltage over Co goes beyond $V_{st,max}$, the M_{P1} switch will go to the triode region. The triode region will not affect linearity because it will have the same effect on all $V_{st,max}$ variations. Usable $V_{st,max}$ is limited by VDD because the M_{P1} MOSFET must be in saturation in the range between GND and $V_{st,max}$ to have a constant current flow.

The "Threshold comparator" employs simple inverter to sense the ramp voltage at the Y node. The threshold voltage is designed to be half-VDD (600mV), which is more than $V_{st,max}$. The last buffer (two inverters) is used to steepen the edges of the output signal.

[3] Full-scale delay in simulations gave a value of 91ps therefore it target was changed from 100ps to 91ps

3.4.2 Edge-interpolated

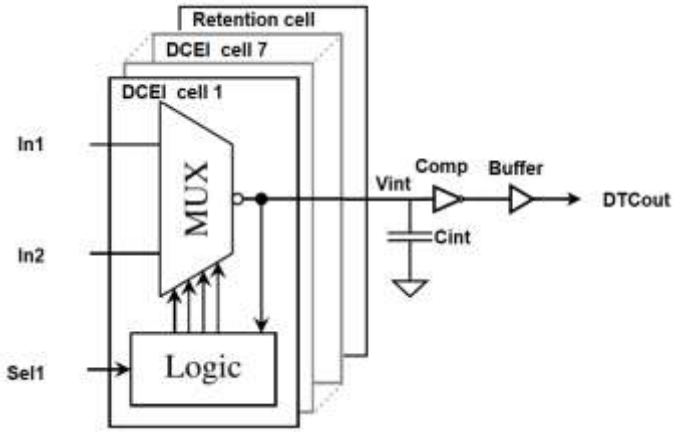


Figure 14: Architecture of DTC[2]

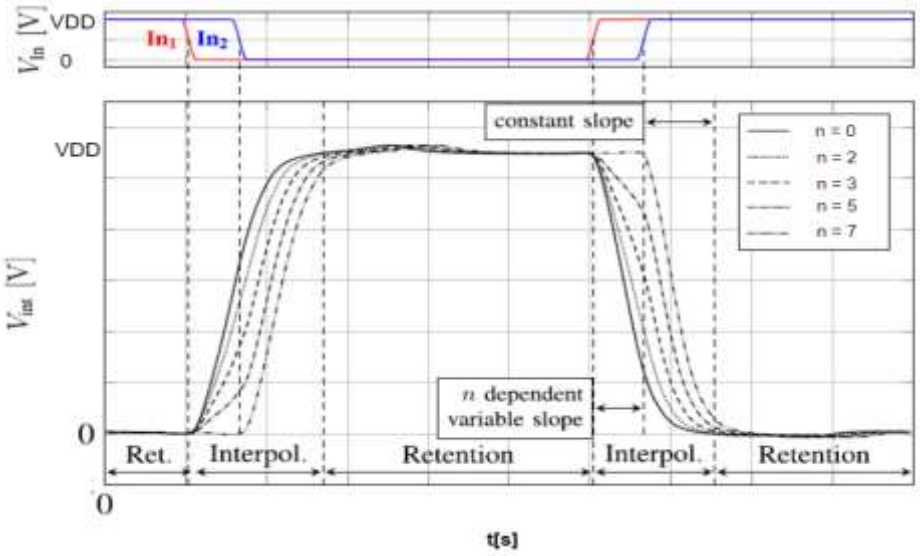


Figure 15: Waveforms of interpolation process for different n codes[2]

Table III: Implemented component sizes and dimensions

Name	Size	Name	W/L
Co	0.1p	S1/3	2.5u/0.12u
VDD	1.2V	S2/4	1.25u/0.12u
		R1/3	0.32u/0.12u
		R2/4	0.16u/0.12

The edge-interpolated DTC uses a set number of cells to charge/discharge the capacitor (Cint) and controls the time delay, as shown in Fig. 14. A larger code gives a greater time delay. The code will determine how many cells are activated by In1 and define a net current which charges the capacitor Cint before In2 edge is detected. The edge of In2 signal will activate dormant

cells. Hence, after the In2 is detected, the Cint capacitor will be charged with a maximum net current. A voltage increase over capacitor with different codes can be observed in Fig. 15.

Fig. 14 also shows a comparator (Comp) and a buffer. The comparator will detect V_{th} and output the signal where the buffer will steepen the edges of the output signal.

Table II and III describes implemented components in edge-interpolator model.

Following paragraphs will explain the working principle when only one cell is used for DCEI (N = 1).

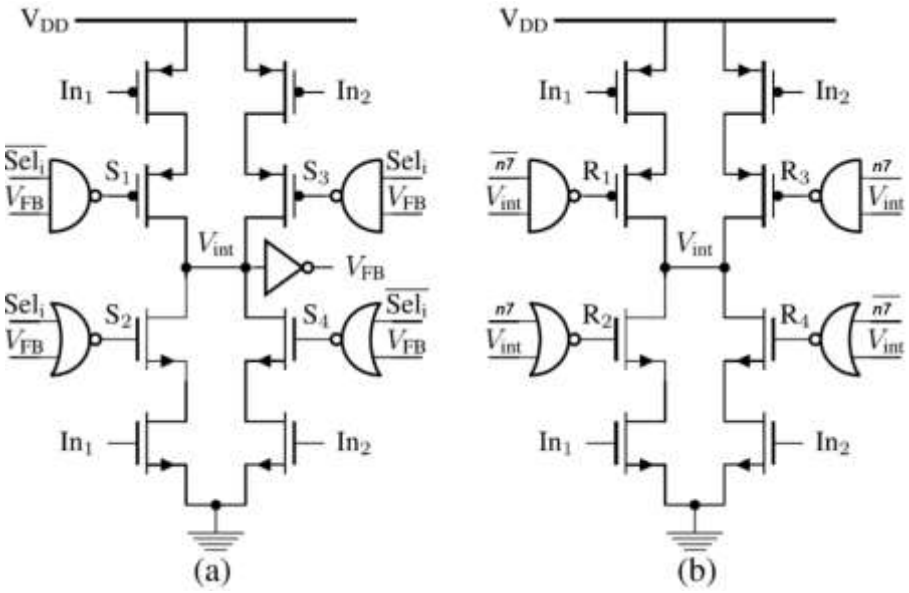


Figure 16: a) Interpolation cell, and b) retention cell[2]

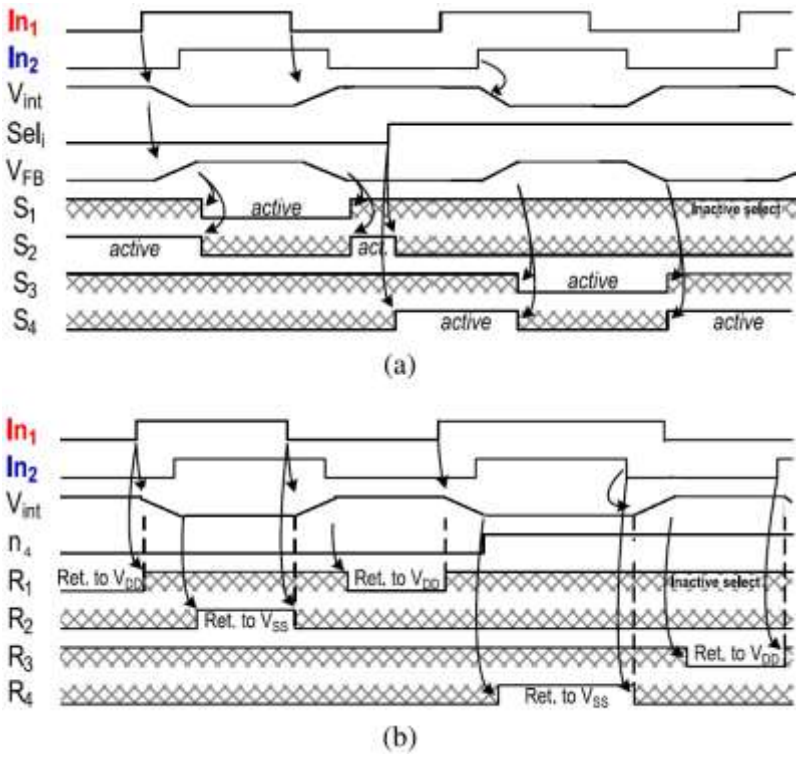


Figure 17: Logic timing diagram of a) Interpolation cell, and b) Retention cell[2]

1) Interpolation cell

The goal of the interpolation cell is to supply Cint with a current $I_{D,p}$ from EQ 21.

$$I_{D,p} = \frac{I}{N} \tag{21}$$

Where I – is the required current from EQ 6 and N is the total number of DCEI cells.

The interpolation cell has a MUX architecture design which consists of two tristate inverters and is presented in Fig. 16 a). The working principle of a single DCEI cell in DTC shown in Fig. 17 a). The Seli = GND means that the cell is ***non-selected***, and only the left side of the cell (S1 and S2) can operate. On the other hand, the Seli = VDD means that the cell is ***selected*** and only the right side of the cell (S3 and S4) can operate while S1 and S2 are always inactive.

There are two working principles of each cell:

- Working principle of ***non-selected*** cell:

  In a scenario when Vint = VDD, the S2 NMOS will be active and the S1 switch - inactive. As long as In1 is equal to GND, the node Vint will be floating. When the In1 signal start to rise, the NMOS at the very bottom left side of the interpolation cell will start to activate, and the Cint capacitor will start to

discharge. Discharge process will work until the Vint becomes GND. After the value of Vint becomes GND, the S2 switch be inactive whereas the S1 - active. The node Vint will float until the In1 start dropping to GND because of the top left PMOS being open. The top left PMOS will start to activate and the Cint will start to charge when In1 starts dropping to GND. The charging/discharging process will repeat in every cycle.

- Working principle of ***selected*** cell:

  The working principle of the selected cell is almost identical to the non-selected cell. The only difference from the non-selected cell is that S1 and S2 will always be inactive, and only the right side of the cell from Fig. 16 a) can be active. Denoting that only S3 and S4 MOSFETs can initiate closed circuit, and In2 controls the cell

2) Retention cell

The main goal of the retention cell (ret.) from Fig. 14 is to keep the Vint node at GND or VDD while the Interpolation cell is turned "OFF". Thus, avoid floating of Vint node.

As depicted in Figure 15 b) with consideration to the working principle shown in Fig. 17 b), the architectures of interpolation and retention cells are similar. The Ret cell requires In1, In2 and digital input n4, which specifies whether the In1 or the In2 is a leading signal. The n4 = GND defines In1 as a leading signal. A leading In1 signal means that only R1 and R2 switch can be activated (Left side of the cell). The Cint capacitor will be shorted to GND when the Vint=GND and the In1=VDD. Meaning, the bottom-right switches are closed ("Active"). When In1 drops to the GND, the retention cell will turn "OFF" until Vint reaches VDD. When Vint = VDD, the R2 switch will deactivate and R1 will become active. Only after the In1=GND and Vint=VDD, the current will flow through the top left PMOS to Cint and keep the Vint = VDD.

In a scenario where In2 signal is leading (n4 = VDD) similar process happens as in the previous scenario. The difference is that only the right side of ret. cell will be active, meaning the In2 signal is essential.

While Cint is getting charged, the Cint capacitor is only connected with the Interpolation cells. After the interpolation cells turn "OFF", the work of the retention cells starts. Provided edge-interpolator design allows node Vint to be connected with VDD or GND; hence the noise from floating is avoided**.**

CHAPTER 4

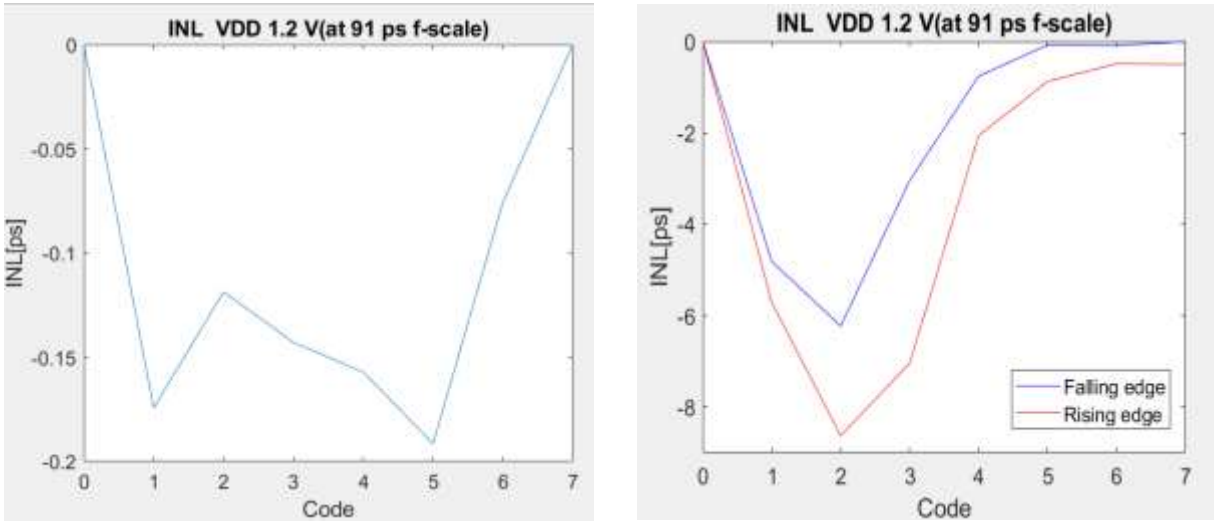
SIMULATIONS

Models of the constant slope and the edge-interpolated DTC concepts were created in LTspice simulation software in order to verify the understand of concepts and to retrieve the comparison parameters. The implemented designs are presented in Appendix A.

4.1 INL

One of the parameters used for undertaking the comparison was identified as the integral-non-linearity. Therefore, the simulations were executed, and results presented in Fig. 18. 8 codes were simulated due to 3-bit resolution and 10fs accuracy was obtained from simulations because of limited processing power.

The constant slope concept had maximum end-point INL error of 0.19ps (-0.01LSB), whereas the edge-interpolator concept had 8.49ps (-0.65LSB) error. In case, the edge-interpolated DTC has maximum INL error the increase in digital code could give decrease in delay. The constant slope DTC uses the cascode current mirror to provide a stable current supply for different delays and the voltage over capacitor increases with same slope for every different delays. The edge-interpolated DTC used multiple simple MOSFET switches to supply a current, and the current flow was distorted by the voltage effects over Cint. The edge-interpolated DTC suffers from linearity errors caused by non-constant current source which distorts charging slope of capacitor.



a) b)

Figure 18: INL diagram. a) Constant slope, and b) Edge-interpolated

4.2 PSRR

Results of simulations when power supply was varied are presented in following section. In order to save processing power, the timestep was increased to 0.2ps instead of 10fs.

4.2.1 Constant slope

Table IV shows the calculated time delay differences assuming that current mirror is always in saturation and effects of load are ignored. Firstly, the time delay created by DTC with ideal 1.2V power supply was calculated. Secondly, the time delay created by DTC with varied power supplies were calculated. Next, the difference between calculated time delay operating on ideal VDD and changed VDDs' were determined in percent and recorded in Table IV. Due to the implemented current mirror, the time delay created by the constant slope DTC model should not increase unless the power supply of comparator is varied. The modulus of delay difference is equal when VDD2 varies by the same voltage because of linear proportional $t_d \propto$ VDD2, which was described in Section 2.2.

Table IV

Calculated effects of varying power supplies to the constant slope DTC

MOSFET supply[V] (VDD3)	Comparator[V] (VDD2)	Current mirror supply[V] (VDD1)	Delay difference[4]
1.3	1.3	1.3	8.33%
1.3	1.3	1.2	8.33%
1.3	1.2	1.2	0.00%
1.3	1.2	1.3	0.00%
1.2	1.3	1.2	8.33%
1.2	1.2	1.3	0.00%
1.2	1.2	1.2	0
1.1	1.2	1.1	0.00%
1.1	1.2	1.2	0.00%
1.1	1.1	1.2	8.33%
1.1	1.1	1.1	8.33%

The recorded simulation results are presented in Table V. The simulated results do not match expectation from Table IV. Unfortunately, only one result fits the expectation. When only the

[4] Propagation time delay created by inverters and components is not included in calculations. In simulations the percentage value will be smaller.

VDD2 is increased, the time difference will increase (Bright blue marking) because even though the current supply does not change but more time is required to reach V_{th}. Most importantly, acquired results show that current mirror is susceptible to variations in its power supply; therefore, more research must be done to understand the influence of power supply to a current mirror.

Table V

Results of Constant slope concept

MOSFET supply[V] (VDD3)	Comparator[V] (VDD2)	Current mirror supply[V] (VDD1)	INL[ps]	Delay difference
1.3	1.3	1.3	0.2	-0.46%
1.3	1.3	1.2	0.1	3.30%
1.3	1.2	1.2	0.1	0.61%
1.3	1.2	1.3	0.9	-3.27%
1.2	1.3	1.2	0.2	2.63%
1.2	1.2	1.3	0.3	-3.64%
1.2	1.2	1.2	0.2	0
1.1	1.2	1.1	0.1	3.92%
1.1	1.2	1.2	0.2	-0.26%
1.1	1.1	1.2	0.3	-2.29%
1.1	1.1	1.1	0.1	1.78%

4.2.2 Edge-interpolated

Table VI shows the calculated time delay differences assuming that charging/discharging MOSFETS are always in saturation and effects of load are ignored. The flow through MOSFET was calculated for all different supply domain combinations. Next, current deviations between ideal VDD =1.2 V scenario and all other supply domain combinations were deducted in percent. Moreover, the influence of VDD2 to the V_{th} was calculated in percent. Lastly, the effects deviating current and varying V_{th} where combined to determine the influence to the delay difference.

Table VI

Calculated values for the edge-interpolator concept

MOSFET supply[V] (VDD3)	Comparator[V] (VDD2)	Delay supply[V] (VDD1)	Delay difference, falling(F)[5]	Delay difference, rising(R)
1.3	1.3	1.3	-12.49%	-27.07%
1.3	1.3	1.2	8.30%	-27.07%
1.3	1.2	1.2	0.00%	-20.47%
1.3	1.2	1.3	-19.20%	-20.47%
1.2	1.2	1.2	0.00%	0.00%
1.1	1.2	1.1	26.95%	29.53%
1.1	1.2	1.2	0.00%	29.53%
1.1	1.1	1.2	-8.30%	40.28%
1.1	1.1	1.1	16.42%	40.28%

Even though the delay difference values are very far apart but signs do match. Meaning the derived dependencies for saturated MOSFETs in Section 2.2 are correct. The big inaccuracies mainly due to neglected propagation time of inverters and ignored current flow deviation affects because of Cint influence.

The most significant time delay error was 16.33%. The error was observed when the Cint was discharging, NMOS switches were operating. The Comparator's supply was reduced; hence the V_{th} decreased. The V_{th} decrease resulted in the t_d increase as can be depicted from EQ 9 because capacitor was discharged. Also, the current flow (I_d) through NMOS decreased; therefore, the t_d increased even more. The I_d decrease was the results of the voltage decrease in the "MOSFET supply". The "MOSFET supply" regulates the output magnitude of logic gates; hence, the input gate magnitude of NMOS decreased. The reduced gate voltage of a NMOS decreased current flow because the current flow depends on V_{GS} in saturation.

[5] Propagation time delay created by inverters and components is not included in calculations. In simulations the percentage value will be smaller.

Table VII

Results of Edge-interpolator concept

MOSFET supply[V]	Comparator[V]	"Delay" supply[V]	INL[ps], falling	INL[ps], rising	Delay difference, falling(F)	Delay difference, rising(R)
1.3	1.3	1.3	8.4	9.8	-9.41%	-7.49%
1.3	1.3	1.2	4.9	11.7	1.30%	-13.15%
1.3	1.2	1.2	6.1	8.9	0.38%	-1.17%
1.3	1.2	1.3	9.3	8.9	-10.18%	-1.44%
1.2	1.2	1.2	6.2	8.5	0.00%	0.00%
1.1	1.2	1.1	2.7	8.3	13.99%	1.51%
1.1	1.2	1.2	6.3	8.6	-0.92%	1.67%
1.1	1.1	1.2	7.3	4.9	-0.99%	16.33%
1.1	1.1	1.1	3.3	7.1	13.72%	9.72%

4.2.3 Combined effects

3 supply domains were simulated to see the most influential domain on the time delay. Unfortunately, the most influential domain can not be accurately determined because delay difference depends on combined effects of all supply domains. Therefore, only experiments with a single supply are accurate.

Simulations showed that the constant slope DTC has a smaller delay difference error than the edge interpolator DTC when power supply varies. Error is bigger due to design choices. A current mirror was used in the c. slope DTC to reduce the influence of a varying power supply. Whereas, the edge-interpolator used a simple MOSFET, which is highly influenced by the variations in the power supply. The edge-interpolator can be improved by changing simple MOSFETs with a cascode current mirror as they can execute same assignments but are less susceptible to noise.

Simulated results from Table V and VII shows that a voltage decrease in a power supply is more influential to a delay difference error than an increase in voltage of a power supply. Unfortunately, the results do not match expectations. It was expected that due to the EQ 18

and 19 the $t_d \propto$ VDD. Meaning the delay difference error will be similar when VDD increases and decreases by the same voltage. The inaccuracy appeared because of the assumption that V_{SD} is a negligible value. Most likely V_{SD} value significantly influences the resistance of charging/discharging MOSFET, but further research must be conducted to verify the significance idea.

Also, the acquired delay difference results prompt the idea that time delay difference error could reduce when DTC calibrated on higher VDD voltage. Meaning, ideal VDD could be around 1.6 V or 2V instead of 1.2V to acquire better PSRR. The charging slopes will be steeper, but a delay error might be smaller when supply voltage varies.

Table VIII present calculated PSRR. The PSRR results prove that the c. slope DTC is more robust than the edge-interpolated DTC. Meaning, supply variations have lesser effects on c. slope DTC than on the edge-interpolated DTC.

Table VIII

PSRR of concepts

PSRR[dB]			
Constant slope		Edge-interpolated	
VDD = 1.3V	VDD = 1.1V	VDD = 1.3V	VDD = 1.1V
-25.13	-13.37	1.09	4.37

4.3 Power consumption

In order to determine which concept is more power-efficient, the average current of one period was measured and multiplied with VDD (1.2V). Table IX that has demonstrated the value of consumption. The constant slope only consumes 0.307mW of power. The constant slope DTC consumes almost 5 times less power than the edge-interpolated DTC. The current mirror uses most power to charge Co capacitor from Fig. 12 for the constant slope design. In the edge-interpolated design most significant power is used by “S1-4” switches from Fig.16 a). “S” switches charge and discharge the Cint capacitor.

The edge-interpolated used a lot of power to charge/discharge the capacitor. High power consumption is due to fact that a lot of inactive MOSFETs were connected with Cint. Therefore, when one MOSFET activates and start producing a current, part of supplied to current had to be used to charge parasitic capacitors of inactive MOSFETs.

Power consumption should improve by reducing the dimensions of implemented MOSFETs. Unfortunately, the reduced size would reduce the current flow. Hence, the time delay would increase too.

Table IX

Comparison of both concepts

	Constant slope	Edge Interpolated
Technology	130 nm CMOS	130 nm CMOS
Supply	1.2 V	1.2 V
Frequency	33 MHz	33 MHz
Resolution [bit]	3	3
Resolution [time]	13.09 ps	13.04 ps
INL	0.19 ps	8.49 ps
Power	0.3 mW[6]	1.5 mW

[6] Power comparison can not be accurate because the power consumption of DAC was not taken into account.

CHAPTER 5

CONCLUSION

The main goal of this was to compare the constant slope and edge-interpolator DTC concepts by INL, PSRR and power consumption. It was aimed to determine which of two provided concepts has smaller linearity error, is less susceptible to variations in supply voltage and consumes less power. Also, an unsuccessful attempt was made to distinguish error sources created by a varying power supply. Initial plan to have 3 independent supply domains with separate power supplies did not work because 3 supply domains influence each other.

The c. slope and the edge-interpolated concepts were explained, and models simulated to extract the comparison parameters. The results showed an advantage of the constant slope DTC concept against the edge–interpolated DTC concept in all interested categories.

The end-point INL error of the constant slope concept was 0.19 ps which is -0.01LSB. The edge-interpolated DTC had 8.49 ps (-0.65LSB) INL which is way bigger linearity error than the c. slope had.

The PSRR results showed that the constant slope concept rejects the influence of variations in the power supply way better than the edge-interpolated concept. The c. slope rejects noise by at least -13.37dB whereas the edge-interpolated DTC reject variation of power supply on by 4.37dB. The PSRR of the edge-interpolator could be improved by implementing A current mirror to use as a current source to charge the delay capacitor. Also, acquired simulation results prompt the possibility to reduce the effects of varying power supply by calibrating device on a higher power supply voltage.

Less power was consumed by c. slope 0.3 mW which is 5 times less power consumption then edge-interpolated concept. The edge-interpolated DTC used 1.5mW of power where significant power was lost due to transient currents that were used to charge parasitic capacitors. Size of the MOSFETs could be reduced to save power, but the time delay of a DTC would increase.

The simulation showed that the constant slope DTC concept is more reliable, robust against the supply voltage variations and power-efficient compared with the edge-interpolator DTC concept. Unfortunately, the main drawback of the c. slope concept is that the c, slope operates only on the rising edge of an input signal. Whereas, the edge-interpolated DTC can operate in applications where both edges are required.

CHAPTER 6

RECOMENDATIONS

There are a few important updates for future research. Firstly, the sizes of the MOSFETs must be appropriately set. In the current design, the inverters and logic gate MOSFETs were set to one size. Unfortunately, NMOS has more significant u_nC_{ox} value than PMOS. Therefore, to have the same response time and current, the W/L=Rt size of PMOS must be more prominent than NMOS size. The Rt_P must be 2.5 times bigger than Rt_N for an inverter.

This research worked only on DC variations in the power supply. In practise AC variations occur in real devices. Therefore, models with AC variations in power supply should be created and examined to see how real-life noise affects the devices.

Furthermore, examined concepts employed distinct sums of currents to charge the time delay determining capacitor. The maximum net current (Ic = 0.26uA) in the c. slope DTC was smaller than the maximum net current (Ie = 1.89uA. Due to 7 cells) in the edge-interpolated DTC. Hence, the time delay[7] of the constant slope was longer than the edge-interpolator. In future, the net charging current should be set identical in both presented concepts to have an unbiased comparison where time delay and full-scale delays are shared for constant slope and edge-interpolated concept.

Also, much power is wasted in the constant slope DTC. The reset stage starts before the ramp charging stage ends. Meaning that the Vreset MOSFET is active and discharges the Co while the current mirror still charges Co, hence power is wasted. The constant slope model could be improved by delaying activation of the reset stage after the charging phase is over, and the current mirror is blocked.

Next improvement should be made in the edge-interpolator DTC to block currents from the implemented wave generator. In the implemented design, the input is directly connected to the MOSFETS that charge Cint. Meaning, the power from wave generators In1 and In2 from Fig. 10 is used to activate the switches in DTC design. Therefore, power is used by the DTC but is not recorded in power consumption from Table IX.

DTC designs have to be calibrated and simulated on higher VDD voltage to check whether time delay error improves when the supply voltage varies. The deduction was made that with higher

[7] Not full-scale delay

ideal VDD voltage, the influence of varying power supply should decay. In order to prove described hypothesis further research and simulations have to be executed.

Another recommendation is to use more powerful hardware for precise results. The used computer was overheating while trying to simulate edge-interpolated DTC. Therefore, the time step size was reduced; hence accuracy suffered.

Lastly, the research was concentrated on simulation. In order to see how provided circuits operate in a real-life environment, circuits should be physically built and measurements executed.

REFERENCES

[1] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, 2015, doi: 10.1109/JSSC.2015.2414421.

[2] S. Sievert *et al.*, "A 2 GHz 244 fs-Resolution 1.2 ps-Peak-INL Edge Interpolator-Based Digital-to-Time Converter in 28 nm CMOS," vol. 1, no. 12, pp. 1–13, 2016.

[3] Y. C. Choi, S. S. Yoo, and H. J. Yoo, "A fully digital polar transmitter using a digital-to-time converter for high data rate system," *2009 IEEE Int. Symp. Radio-Frequency Integr. Technol. RFIT 2009*, pp. 56–59, 2009, doi: 10.1109/RFIT.2009.5383681.

[4] N. Markulic, K. Raczkowski, P. Wambacq, and J. Craninckx, "A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS," *Eur. Solid-State Circuits Conf.*, pp. 79–82, 2014, doi: 10.1109/ESSCIRC.2014.6942026.

[5] "How to Measure the Power Supply Rejection Ratio for the MAX38902A/MAX38902B." https://www.maximintegrated.com/en/design/technical-documents/app-notes/6/6650.html (accessed Oct. 04, 2020).

[6] J. M. Daga and D. Auvergne, "A comprehensive delay macro modeling for submicrometer CMOS logics," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 42–55, 1999, doi: 10.1109/4.736655.

[7] "MOSFET equations." https://inst.eecs.berkeley.edu/~ee105/fa05/handouts/discussions/Discussion5.pdf (accessed Nov. 09, 2020).

[8] A. Zjajo, "Circuits and Systems Group (HB 17.270) A.Zjajo@tudelft.nl Research on: Low power bio-electronic interface Power and thermal management in SoC Variability constrains in low power design Low power signal conversion," 2015. Accessed: Nov. 24, 2020. [Online]. Available: http://cas.et.tudelft.nl/~zjajo/DigiIC/slides/03_inverter.pdf.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits*. 2000.

[10] "Understanding MOSFET On-State Drain-to-Source Resistance - Technical Articles." https://www.allaboutcircuits.com/technical-articles/understanding-mosfet-on-state-drain-to-source-resistance/ (accessed Nov. 26, 2020).

APPENDIX A

For undertaking a fair comparison, the value of an input signal in the case of both the simulations was set at 33 MHz. Along with this, to obtain similar needed power consumption, the determining capacitor (Co for constant slope and Cint for the edge-interpolated concept) was set to be 0.1pf.

Both concepts had different architectures and sizes that are presented in the next paragraphs.

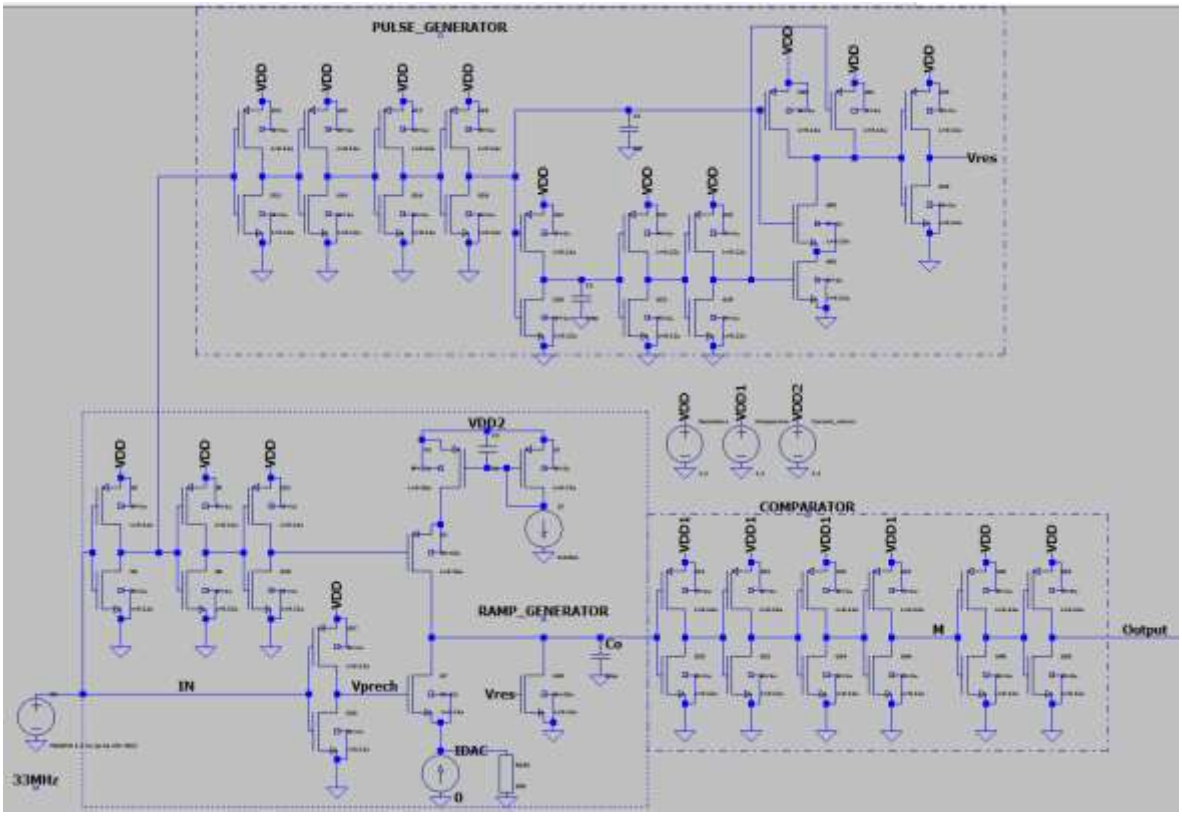


Figure A1: Full LTspice simulation model of constant slope concept

Constant slope

The full architecture of the constant slope model in LTspice is shown in Fig. A1. The in-depth model of ramp generator simulation model is shown in Fig. A2. The function of the first inverters situated in lane A and B is to invert the XO input signal. The extra two inverters in CLKin line are used as a buffer to delay arriving signal for power efficiency. The sizes of inverters are not important as long as the inverters have an operational time of less than arbitrary value of 30 ps.

The Vres NMOS is required to discharge the “Co” completely. Therefore, the size must allow enough current flow to discharge “Co” in 1/20 of XO signal period, because the discharge and pre-charge must operate while the XO input is at GND. The size of Vres was set at 10um with the help of coarse tuning. The Vprech NMOS pre-charges “Co”. The size was set to 1um width. This size allows enough current to travel through Vprech NMOS in the 9/20 of input period to charge “Co”, as only that time period is left for pre-charging.

The last component is the current mirror with ratio 10:1. The mirror must be in saturation for a proper operation. Mirror outputs 10*I_b current when all MOSFETS work in saturations. I_b value was 0.026mA, which gives a full-scale delay of 91 ps.

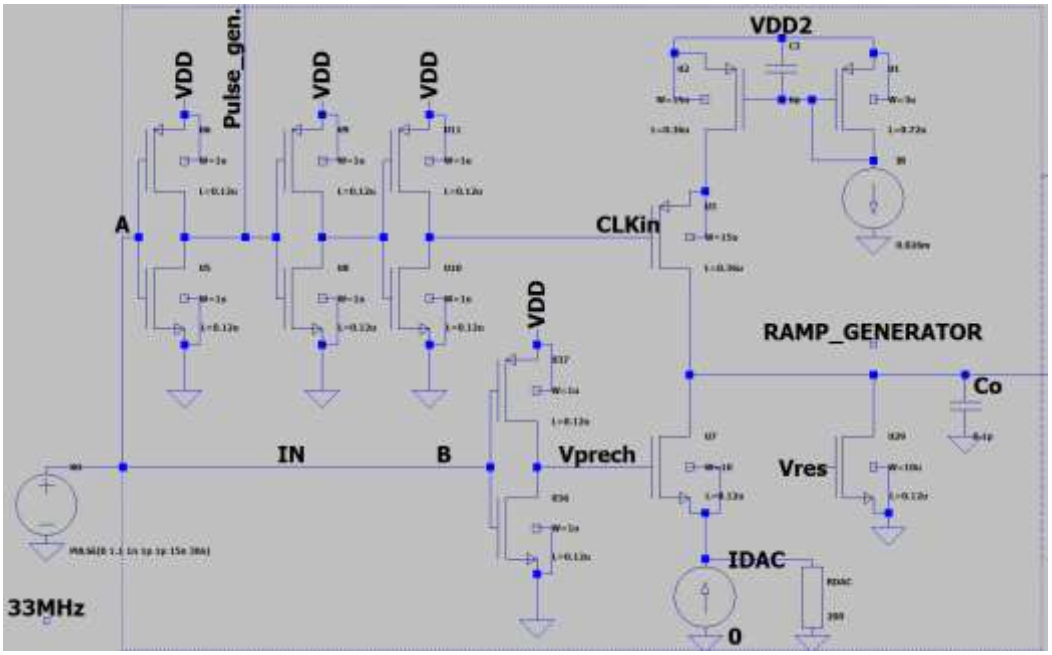


Figure A2: Ramp generator model

The "Pulse generator" in Fig. A3 is used to take the input signal and the non-GND (active) voltage of the input signal and reduce the width 10 times. The C1 and C2 capacitor sizes were tuned until the active output was shortened till expected value. C1 = 20fF and C2 = 0.4 pF sizes were selected.

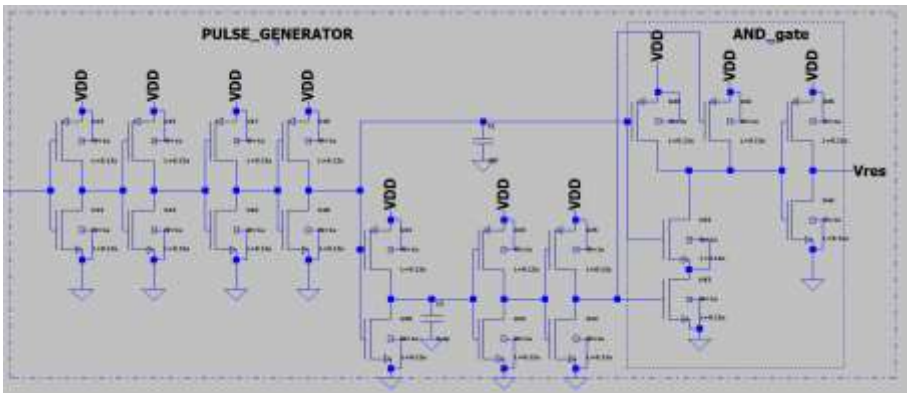


Figure A3: Pulse generator

As shown in Fig. A4, the first inverter in the Comparator block is considered to be a pure comparator for detecting a rising edge-off of XO input. The consecutive inverters act as a buffer for steepening edges associated with the signal. The next inverter is needed to bring the signal to its initial form. The M point is presented as DTC output and the measurement point. The last two inverters are used as an input for the next device. It is expected that the next device will have a buffer which will stop all currents from DTC and the last inverter simulates the digital switching which has to be activated by DTC output.

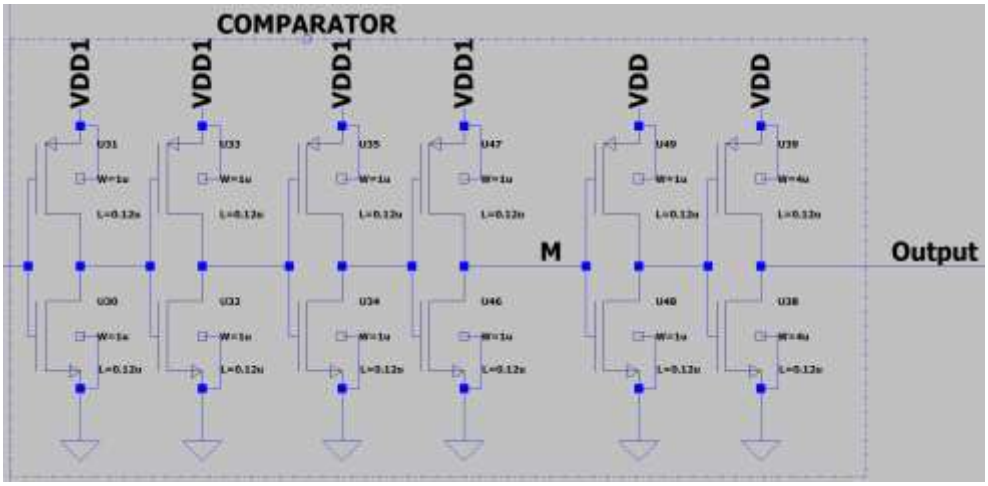


Figure A4: Comparator and output

In perfect initial conditions all VDDs' values were set to 1.2V as an ideal power supply.

Edge-interpolated

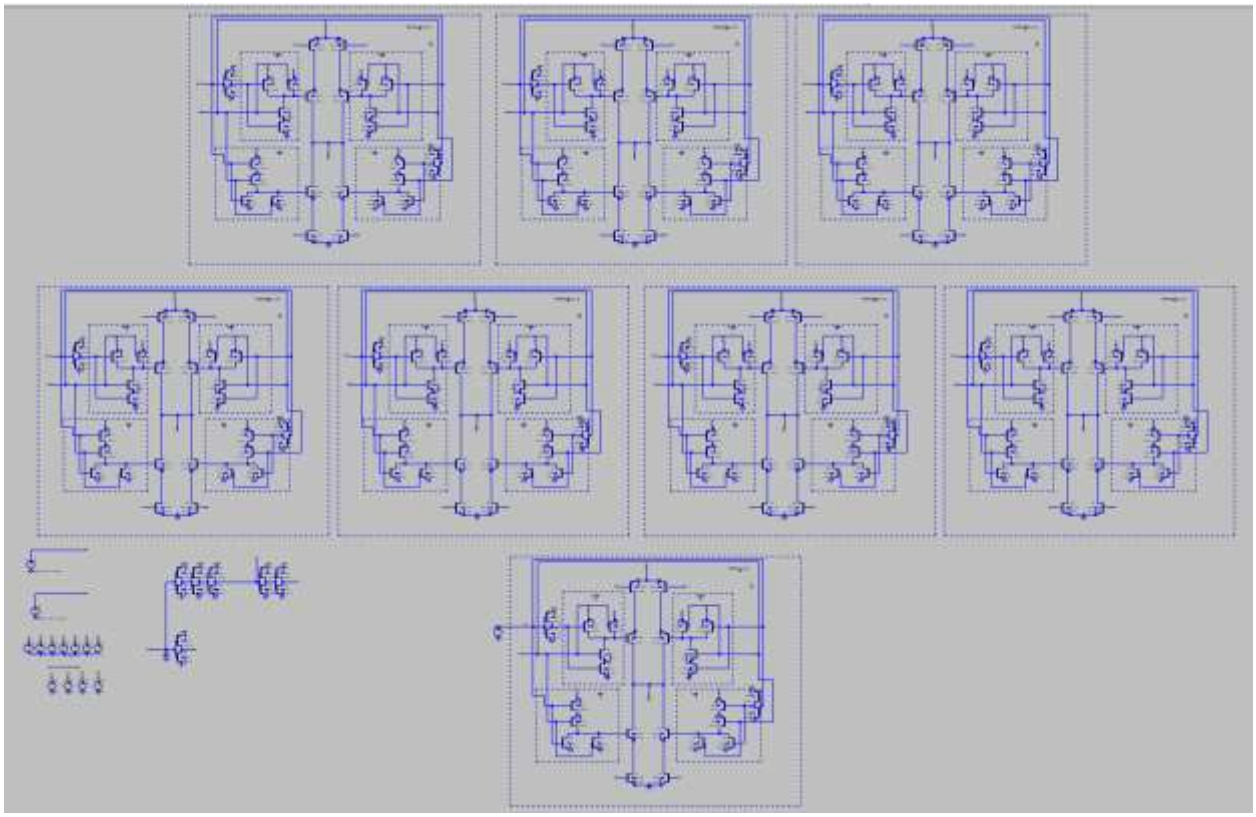


Figure A5: LTspice simulation model of edge-interpolator. 7 interpolation cells at the top and 1 retention cell at the bottom

The full model of the edge interpolator DTC is shown in Fig. A5. The number of interpolation cells was selected to be 7 because 3-bit resolution was targeted. The 92ps full-scale delay was measured in constant slope concept. Therefore, the time difference between In1 and In2 was selected to be 92ps because difference in time regulates the full scale delay.

The LTspice simulation model of a single interpolation cell is shown in Fig. A6. The arbitrary selected size for logic gate MOSFETs is 1um. In1 determines the start of "Cint" capacitor's charging if the cell is not selected (Seli = 0). The capacitor starts charging, and the tristate inverter will not change its state until the voltage over node Vint reaches V_{th}. After the threshold is reached, the comparator will detect the ramp and output the signal. As the signal was already outputted the influence of slow switching will not affect linearity or delay.

Sizes of "S" MOSFETs are vital because they charge and discharge the "Cint". The expected time delay of 0 selected cells was selected to be 50 ps. Therefore, after the validation by simulation, the size of 2.5um for S1 and S3 was selected. The NMOS allows more current to travel through hence size must be reduced. The time values of charging and discharging of the

capacitor have to be the same. Thus, after executing the simulations, the value of W =1.25um was deducted.

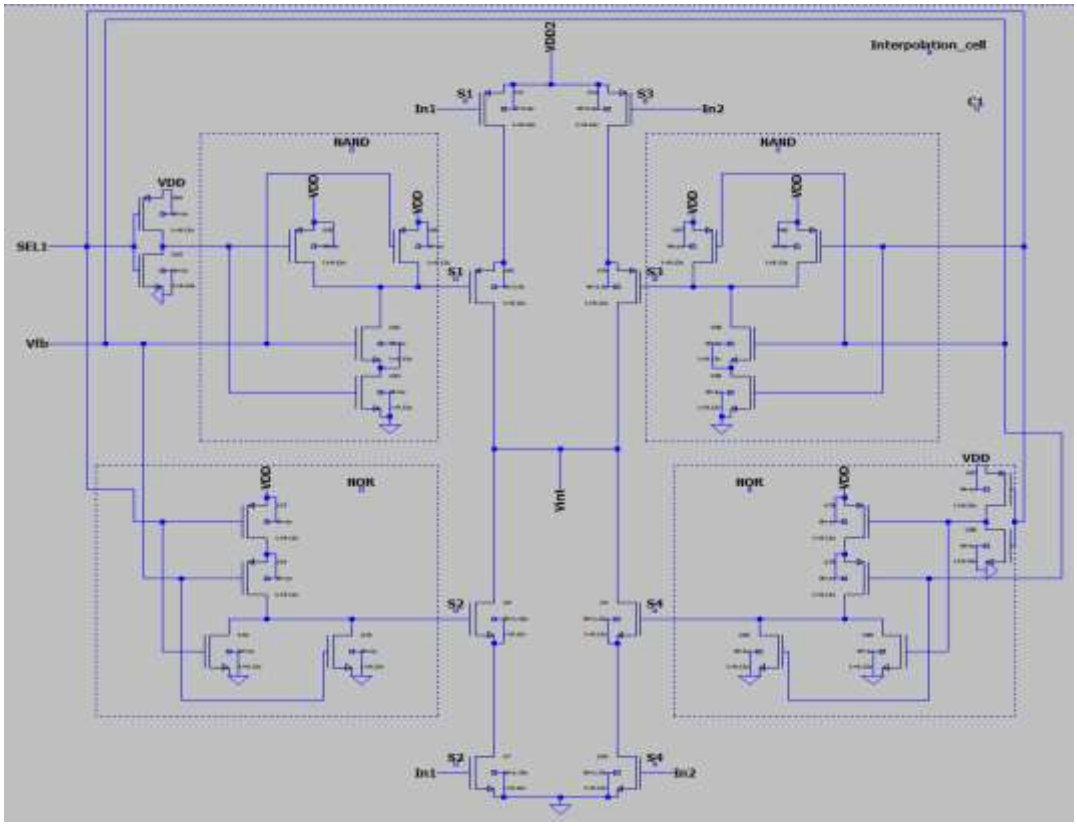


Figure A6: Interpolation cell

The sizes for NAND and NOR MOSFETs' is not essential as long as the unwanted cycles are avoided.

The in-depth simulation model of retention cell is shown in A7. The n4 source was selected to be 0 because in simulation In1 signal was always leading.

The R MOSFETs were set to be the smallest possible value because even the with W = 0.16um the Cint is completely discharged before the edge of input is detected. PMOS was set W = 0.32um to have the same expected charging and discharging current.

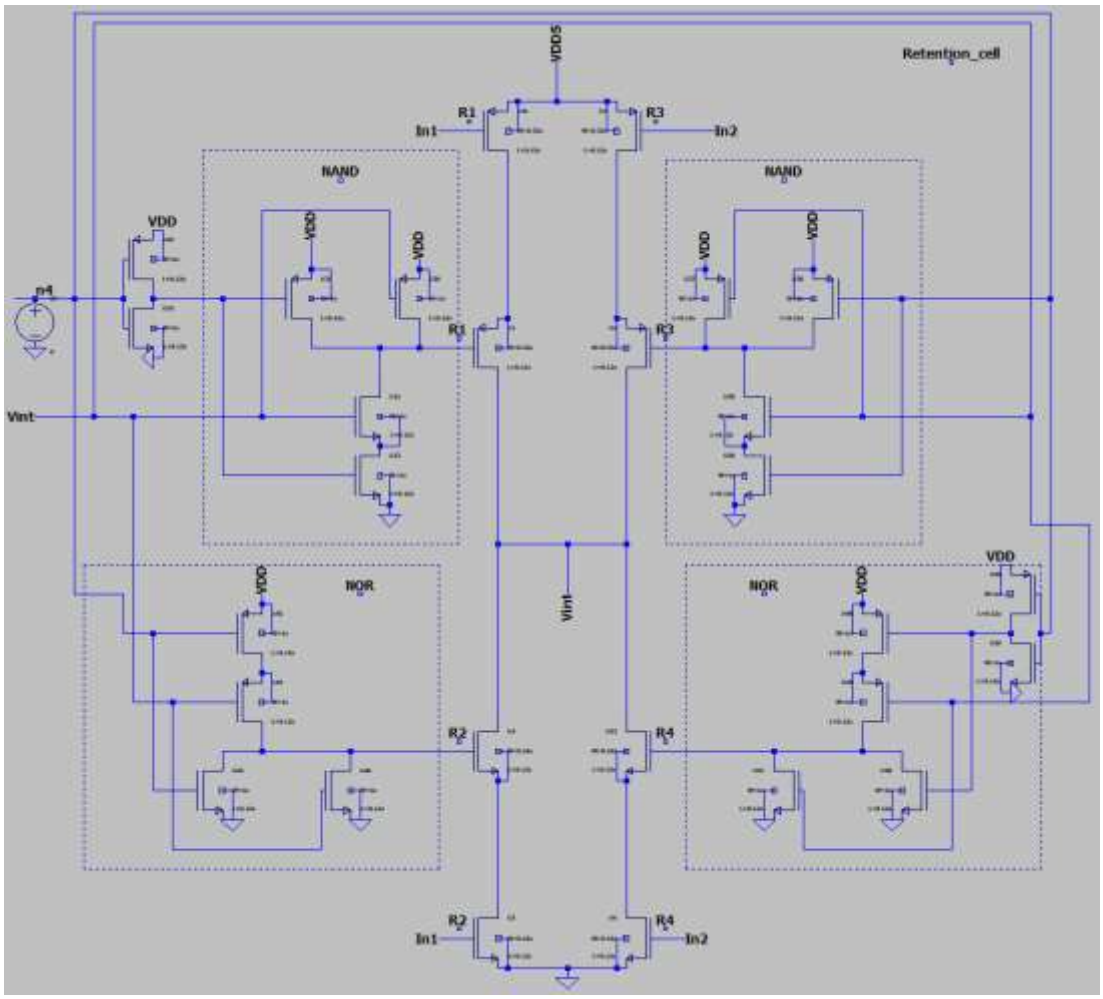


Figure A7: Retention cell

As shown in the Fig. A8, the function of the first inverter of comparator is to execute the detection while the other two inverters are responsible for working as buffer and steepening the edges. The sizes for inverters are set by maximum 30 ps for ensuring an optimum operation requirement. The last two inverters between M node and Output are used to simulate the input of the device of next device.

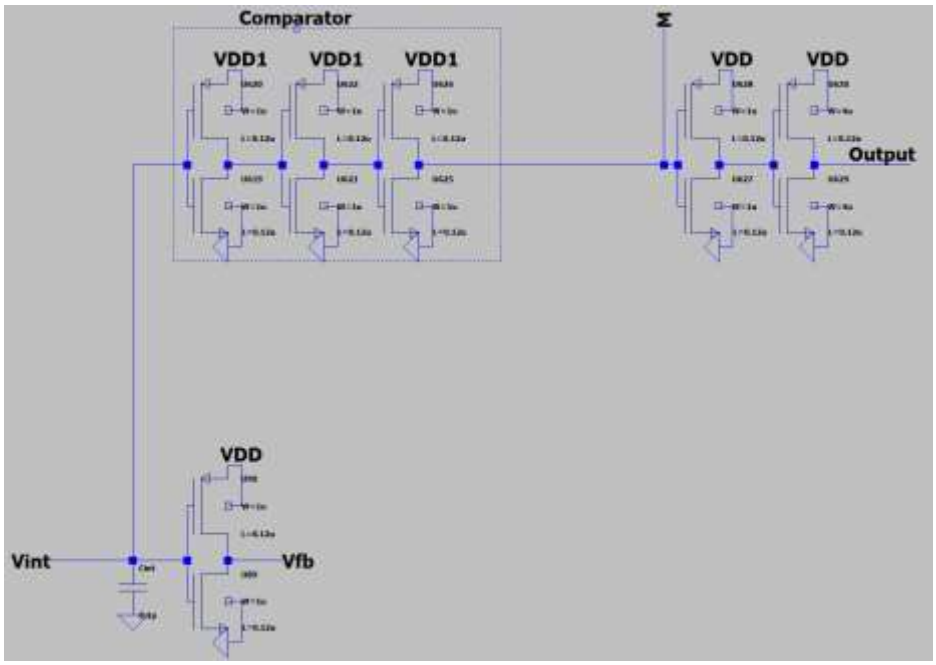


Figure A8: Cint capacitor with the comparator