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Interfaces and Correlated Electron Systems (ICE)

Investigation of Second Generation Superconductor Tapes to be used for Superconducting Electronics

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Abstract

Second Generation High Temperature Superconductor (2G-HTS) Tapes are currently fabricated by several companies around the world and used in large-scale applications such as magnets, generators and power cables. During the production of these tapes an emphasis is laid on optimizing the crystalline structure of the HTS layer, resulting in a quasi-monocrystalline layer and a tape with high critical current densities $10^6\,\mathrm{A}\cdot\mathrm{cm}^{-2}$ (77K and self-field). Due to the good crystalline qualities of these tapes it is interesting to investigate whether one can use these tapes as building blocks for superconducting electronics, which is the research objective of this thesis.
To answer this question a literature study is performed into the fabrication steps of the production of the THEVA TPL1100 and simulations are performed to get a better understanding of the Rapid Single Flux Quantum (RSFQ) branch of superconducting electronics. Furthermore, the SEM and TEM are used to investigate the surface morphology and structural properties of the tapes, to determine whether creation of microstructures is possible on the silver or GdBCO layer of the tape. Hall bars with various dimensions were then patterned and fabricated on the surface of the GdBCO layer. Photolithography was used to pattern the structures and wet chemical etching with NH_4OH/H_2O_2 (14%/14%) and H_3PO_4 (10%) to etch the silver and GdBCO respectively. An approach to do electronic measurements is outlined, but could not be performed due to several issues.
It was found that microscale structures, in the order of a hundred microns, could be created on the GdBCO layer of the tape. Wet chemical etching limited the size of the structures due to the thickness of the GdBCO layer ($\approx$ 3 micron) and underetching which would destroy small structures. However, larger structures remained intact and showed possibilities for creating electronic structures and devices on the tapes.

Contents

1.

Introduction

Since the discovery of superconductivity in 1911 by the Dutch physicist Heike Kamerlingh Onnes physicists have been intrigued by the phenomenon and have tried to further increase the critical temperature, T_c, until which superconductivity occurs in a conductor [1]. In 1986 the first high temperature superconductor (HTS), $La_{2-x}Ba_xCuO_4$, was discovered, the compound was the first of the cuprate superconductors which featured characteristic copper oxides layers and high critical temperature and critical current density. A little later the cuprate superconductor $YBa_2Cu_3O_{7-x}$ (YBCO) was discovered, which was the first superconductor to have a critical temperature above the temperature of liquid nitrogen (77 K) [2]. This greatly reduces the costs of cooling since using liquid nitrogen is much cheaper and much more accessible.

An application of these high temperature superconductors is in second generation HTS tapes, also known as coated conductors. Coated conductor technology uses a multilayered structure of which one layer is a HTS. The superconductors used in most coated conductors are REBCO superconductors, which stands for Rare-Earth Barium Copper Oxide. There are many different REBCO materials, YBCO is one of them where Yttrium is the Rare-Earth material. However, nowadays DyBCO or GdBCO superconductors are used in the tapes where Dysprosium and Gadolinium are the Rare-Earth Materials. The REBCO coated conductors are currently already being fabricated by various companies around the globe. One of them, THEVA, has supplied the tape used in this research, which is the model TPL1100.

Coated conductors are currently used in many large scale applications such as HTS power cables, generators and large magnets [3]. Due to the fact that these coated conductor tapes can be produced in batches of very long lengths (hundreds of meters) and that the superconductor layer has a quasi-monocrystalline property it is interesting to look into a potential usage of the tapes for superconducting electronics [4]. The replacement of normal conductors used for electronics with superconducting coated conductors shows much potential due to the high critical current density and superconducting properties of the coated conductors. In this research a focus will be put on the Rapid Single Flux Quantum (RSFQ) branch of superconducting electronics, which uses single flux quanta (SFQ) to represent information.
Since the world is very reliant on electronics it is interesting to investigate whether the coated conductors made using HTS materials can potentially be applied in this branch of superconducting electronics. Therefore, the research question of this bachelor thesis is:

What are the possibilities and/or current limitations for the fabrication of electronic devices using second generation high temperature superconductor tapes?

During the research I will investigate what the possibilities and/or current limitations are for fabrication of electronic devices using coated conductors. Since this is a very broad research question, several sub-questions have been formulated to divide the research into smaller sub parts. These sub-questions will be stated below and a small explanation for every question will be given:

1. What are important considerations and steps during the fabrication of 2G-HTS Tapes and how does THEVA produce the THEVA Pro-Line 1100?
2. How do RSFQ electronics work and what are interesting applications for 2G-HTS Tapes?
3. Is the surface of the tape suitable for micropatterning?
4. Is it possible to create electronic microstructures on the tapes and what are the limitations?

To answer sub-question 1 a literature study was performed regarding how the tapes are produced and what is important during fabrication, this will be discussed in chapter 2. In chapter 3 RSFQ based superconducting electronics will be discussed, in order to obtain a better understanding of this theory simulations were also performed. This was all done in order to answer sub-question 2, several interesting applications considered are transmission lines and Artificial Neural Networks. During the experimental part of the research several experimental techniques and methods have been used, these are all explained in chapter 4.
In chapter 5 the first experiments and their results will be discussed. These experiments were focused on

answering sub-question 3 and are thus mainly microscope based experiments. The SEM and TEM are used to image the surface of several layers, but also the structure of the tape. Chapter 6 focuses on the fabrication of small microscale Hall bars on the tapes, this in order to answer sub-question 4. The design, fabrication progress and electrical characterization of these structures will be discussed and analyzed to determine whether the process is reliable. Unfortunately due to several time- and technical issues, the measurements regarding electrical characterization could not be performed, but the approach which was to be done will be explained in detail.
In chapter 7 a general conclusion will be drawn regarding the research question and obtained results, also a small glimpse in the future will be given about what possibilities for further research are. Last, but not least in chapter 8 the contributions of several people who have helped during the project will be acknowledged.

2.

Second Generation High Temperature Superconductor Tapes

During this research a special kind of multilayered tape will be investigated for its suitability to be used in superconducting electronics. These tapes are called second generation (2G) High Temperature Superconductor (HTS) tapes, but are also referred to as coated conductors (CC). The superconductor used for these tapes is a so-called REBCO (Rare-Earth Barium Copper Oxide) superconductor, of which YBCO is most well known. Characteristic of REBCO superconductors is the fact that they can have very high critical current densities, in the order of $10^6\,\mathrm{A}\cdot\mathrm{cm}^{-2}$ (77K and Self-Field). However, a major challenge in producing these tapes with high critical current densities is reducing their losses due to high angle grain boundaries. To accomplish this one has to be able to produce an almost monocrystalline HTS layer, which in itself is very challenging. Since current applications require the tapes to be flexible and hundreds of meters long with an almost homogeneous high critical current density along the entire tape, the process of designing a reliable method has been ongoing for the past 20 years [5].
In this chapter these tapes will be discussed in depth since they form the basis of the research. More specifically the tapes produced by the German company THEVA[1] will be used and therefore, the focus will be on the special properties and production process of their model TPL1100.

2.1 Substrate Texture

One of the main limiting factors in the creation of long tapes with high critical current densities is the fact that cuprate superconductors, such as the REBCO type, tend to form high angle grain boundaries in the a-b plane. This results in formation of weak links at the grain boundaries of the polycrystalline layer and can significantly lower the critical current densities to $10^3 - 10^4\,\mathrm{A}\cdot\mathrm{cm}^{-2}$. To counter the formation of a high angle grain boundaries one can either biaxially texture the REBCO layer or deposit the REBCO layer on a biaxially textured substrate [6].
In figure 1 texture is schematically explained. One can claim that there is texture when the crystallographic orientation in several grains is in the same direction. Typically there are two categories of textures: one-degree (I-O) and two-degree (II-O) orientation. In I-O textures there is only alignment along one axis, for instance along the c-axis as illustrated in the top left figure. In this case the grains still have the freedom to randomly orient themselves in the a-b plane. However, in II-O textures the freedom along either the a or b axis is taken away and thus there is a crystallographic orientation along two axis, this type of texture is also known as biaxial texture. An extreme variant of biaxial texture is when the crystallographic orientation is that of a single-crystal, this means that there is no freedom around any axis and one can speak of a monocrystalline orientation [7].

2.2 Buffer Layers

It is of vital importance that several buffer layers are deposited between the metallic substrate and the HTS layer of the tape. The superconducting properties of the REBCO compounds are heavily reliant on the oxygen concentration in the copperoxide planes and chains. Too much diffusion of oxygen from the HTS layer to the substrate will result in reducing the superconducting properties, such as the critical

[1] THEVA Dünnschichttechnik GmbH Germany, info@theva.com

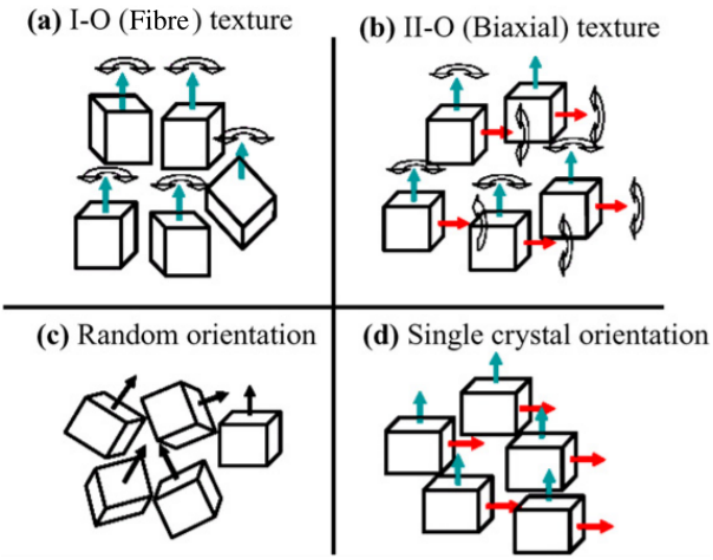


Figure 1: Different kinds of texture. a) One-degree orientation along the c-axis, b) Two-degree orientation (biaxial), c) No preferred orientation, d) Extreme variant of II-O, i.e. no freedom around any axis (Figure from [7]).

temperature, and can eventually lead to the compound not being superconducting anymore. Diffusion of oxygen to the metallic substrate occurs due to the fact that the Gibbs free energy for oxidation of many substrate materials (such as for nickel or nickel alloys) is lower then the Gibbs free energy for oxidation of copper, thus the substrate is able to drain oxygen from the HTS layer [8]. Buffers layers are deposited between the metallic substrate and HTS layer to reduce this effect, several metaloxides are good candidates for buffer layers since there oxidation energy is lower then that of nickel [9].

To prevent oxidation of the substrate surface, which is made of either a metal or alloy, a seed layer is chosen that is thermodynamically more stable than the oxidized substrate. These layers are mostly metal oxides such as CeO_2, MgO or Y_2O_3-stabilized-ZrO_2 (YSZ). To achieve epitaxial growth of the layer on the substrate it is important that the lattice parameters of the substrate and oxide buffer layer match. A barrier layer is deposited on top of the seed layer and functions as a barrier to prevent diffusion of metal from the substrate to the HTS layer. A common material used for this is YSZ, besides the fact that the texture of the material is important a high density is also favoured. A more dense layer is better at preventing metal diffusion to the HTS layer. Lastly a cap layer is deposited whose main function is the relaxation of the lattice mismatch between the barrier layer and HTS layer. This in turn results in good epitaxial growth of the HTS on the buffer stack [5].

2.3 THEVA Pro-Line 1100

Now that the importance of texture and buffer layers in producing high quality tapes with high critical current densities has been discussed, the next section will use this knowledge to explain how the tapes used in this research are produced and what their structure is. As previously said a HTS tape made by THEVA will be used, the specific tape is called the TPL1100 (Theva Pro-Line 1100 which has a 100 micron thick substrate) and a schematic figure of the tape can be seen in figure 2. As one can see in the figure the tape has a multilayered structure with various different materials. Each layer in the composite structure has a specific function to enhance either mechanical, electrical or thermal properties of the tape. Since it is important to understand what the function of each layer is and how it is produced this will be discussed in detail.

2.3.1 Hastelloy Substrate

The function of the thick metallic substrate is to provide good mechanical stability and flexibility to the tape. THEVA uses a nickel alloy called Hastelloy C-276[2] (NiMo16Cr15W), this alloy is non-magnetic and

[2]Trademark of Haynes International

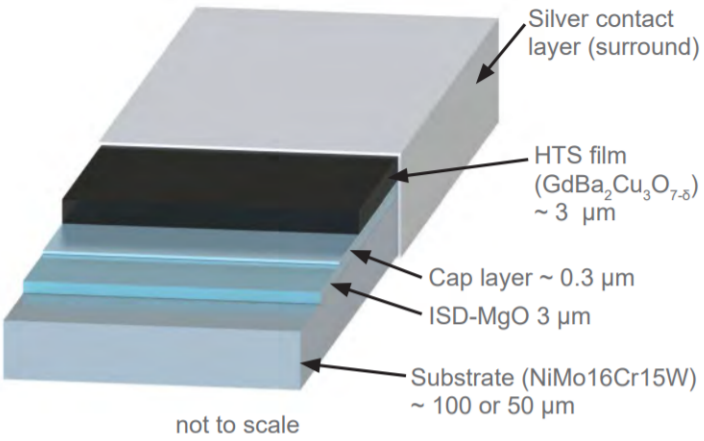


Figure 2: Schematic layout of the THEVA Pro-Line 1000 series HTS tape which is used in this research (Figure from [10]).

provides enough flexibility and mechanical stability such that the tape can also be bend. The hastelloy substrate is 12 millimeters wide and 100 micrometers thick. The hastelloy substrate is first degreased and mechanically grinded to clean and even out the surface. To further increase the condition of the surface the tape is electropolished, cleaned with de-ionized water and dried. The result of this process is that maximum surface slopes are less then $0.8\,^\circ$, which ensures that on the microscopic level the inclination angle of the ISD process is also preserved, which is the next step in the fabrication [11].

2.3.2 Inclined Substrate Deposition of MgO

What sets out THEVA from their competition is the way they deposit the first buffer layer of MgO on the hastelloy substrate. This method is called inclined substrate deposition (ISD) and the method is designed to deposit the MgO buffer layer with a biaxial texture. The hastelloy substrate is inclined with an angle of approximately $25 - 30\,^\circ$ towards the MgO evaporation source and the MgO is evaporated using an electron-beam, see figure 3. The deposition rate of the MgO deposition is high, at more than 4 nm/s. Furthermore, due to growth selection only the MgO grains with an approximate tilt (with regard to the substrate) of $20\,^\circ$ and good in-plane alignment survive the deposition process [11].

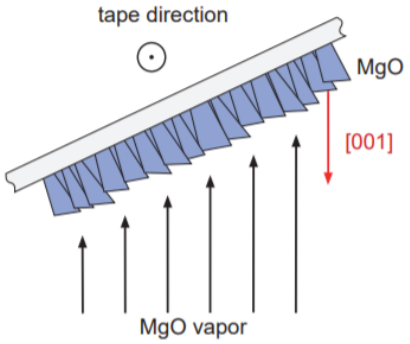


Figure 3: Schematic process of MgO deposition using the ISD technique (Figure from [10]).

The advantages of preparing a substrate using ISD come to light when comparing an ISD grown MgO substrate layer to a flat MgO layer. The HTS layer deposited on the ISD grown layer is much more capable of reducing grain size and suppressing second order phases. This difference is illustrated in figures 4 and 5. In figure 4 it is illustrated for the formation of grains. On a flat substrate, such as in figure 4 A, an a-axis grain is able to grow in a trapezoidal shape out of the layer since the growth rate in the a-b plane is faster. However, in the case of an ISD grown layer (figure 5 B) the size of grains is limited to the size of the terraces. The HTS layer takes over the terrace growth of the MgO layer and due to the terrace size and height the growth of large grains is reduced. Either due to the fact that the grains cannot grow larger then the edges of the steps (indicated with the arrow a) or that due to a higher growth rate in the a-b plane grains formed at edges can be overgrown (indicated at b) [12][13].

Furthermore, the stepped substrate surface also reduces the growth of encased impurity phases, such as areas where the chemical composition differs from the surrounding HTS layer such as copper rich segments. When such an impurity occurs in the HTS layer grown on a flat surface, it is often free to grow larger and larger since the surrounding layer will not overgrow it (due to different free surface energies and growth speeds). This means that the impurity is free to keep growing as indicated by the solid, broken and dotted lines, it can even occur that the defect grows out of the layer (see figure 5 A). When

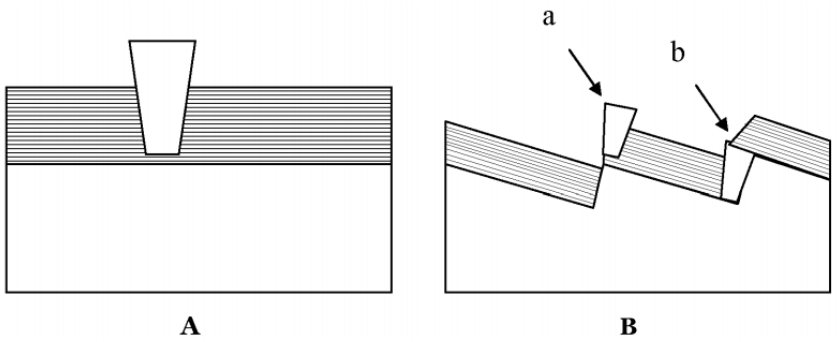


Figure 4: Trapezoidal grain, growing larger then the HTS layer, on a flat MgO substrate (A). Suppression of grains due to the stepped surface of the MgO layer, formed by ISD, which is copied by the HTS layer (B) (Figure from [12]).

one grows a HTS layer on the stepped surface made by ISD, the impurities are overgrown due to the faster growth in the a-b plane from higher steps (shown by the arrows W in figure 5 B). The impurity is pushed outward due to the growth direction and pushed towards a grain boundary (KB), which is generated by a shoulder in the stepped surface. The impurity is stopped at the grain boundary and is thus more contained then when it grows on a flat surface [13][12].

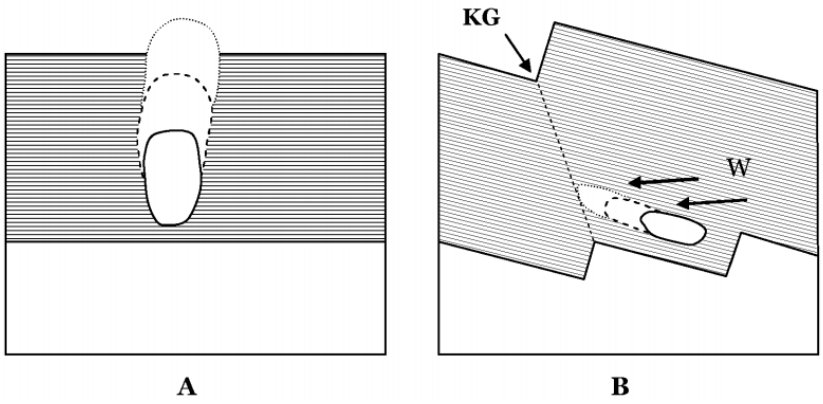


Figure 5: Growth of second order impurities on either a flat substrate layer (A) or a substrate layer deposited by ISD which has a characteristic stepped surface (B). (*KG = Korngrenze (Grain Boundary) and W = Wachstum (Growth Direction)*, figure from [12]).

The next step in the fabrication of the MgO buffer layer is to deposit a thin 200 nm film of MgO epitaxially on the thick MgO ISD layer, in this case the tape is not inclined. This layer serves as a cap layer which can close the gaps between the large columns of MgO and thus increase the surface quality for the next step which is the HTS coating [11]

2.3.3 HTS Layer

To deposit the HTS layer electron beam PVD (Physical Vapor Deposition) is used which can reach deposition rates of about 1 nm/s. The GdBCO (Gadolinium Barium Copper Oxide) compound is the HTS deposited, which has a similar unit cell as the YBCO compound but with the Yttrium atoms substituted for Gadolinium atoms [11]. The GdBCO compound is oxidized by passing it through a tube furnace with an oxygen atmosphere of 800 mbar, in order to acquire the correct oxygen stoichiometry. The Gadolinium based compound has a similar critical temperature to YBCO, about 93K, but it is mainly used since its critical current density at high magnetic field is larger then that of YBCO or DyBCO [14]. Furthermore, since the GdBCO layer is deposited on the MgO ISD layer it copies the stepped like surface of the substrate. This results in that the CuO planes are also inclined under the same angle as can be seen in figure 6. Since conduction of the superconducting Cooper pairs, which carry the superconducting current, occurs mainly in these planes there is a difference between the longitudinal and transverse critical current densities. In the figure a segment of the tape (which stretches out along the y axis) is drawn.

Due to the inclination of the CuO planes the transverse critical current density, $J_{c,T}$, is less then the longitudinal critical current density, $J_{c,L}$. The reason for this is that transverse current has to cross the CuO planes and thus a weak link is established, this is important to keep in mind when designing electronic structures on the surface [15][16]. Furthermore, THEVA specifies that the longitudinal critical current density is in the order of 10^6 A $\cdot$ cm^{-2} at 77K and self-field [10]. The inclination of the CuO planes

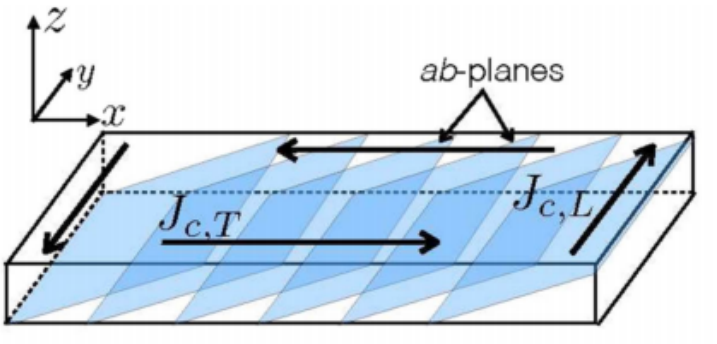


Figure 6: Critical current in the longitudinal and transverse direction of the tape. Inclination of the CuO planes result in a difference between the two critical current densities (Figure from [16]).

thus leads to an anisotropic behaviour of the critical current density, the anisotropy is also measurable when placing the tape in an external magnetic field. When the magnetic field is applied parallel to the a-b plane of the GdBCO layer a peak is observed in the critical current density [15][11].
Last, but not least a silver layer of about one micron thick is deposited around the entire tape to ensure good electrical contact with an external source. However, also to establish electrical contact between the Hastelloy substrate and HTS layer and to chemically protect the HTS layer [11].

3.

Rapid Single Flux Quantum Electronics

Since the aim of this research is to investigate whether coated conductors can be used as building blocks for superconducting electronics, a literature study and simulations were performed into a specific branch of superconducting electronics. This branch is called the Rapid Single Flux Quantum (RSFQ) Logic family and uses of Single Flux Quanta (SFQ) to represent information. This chapter focuses on discussing sub-question 2 by first establishing basic knowledge about RSFQ electronics and considering several easy circuits, such as single Josephson Junctions (JJ) and SQUIDs to simulate the Josephson effects. Furthermore, once a basis of RSFQ is established, more complex circuits such as active and passive transmission lines will be simulated. The chapter finishes with a first look into the use of RSFQ electronics in the creation of artificial neural networks (ANNs). Both transmission lines and ANNs are considered as possible applications where the use of the superconducting tapes might be considered.
Simulations were performed using the software PSCAN2[3] (Personal Superconducting Circuit ANalyzer) which specializes in simulating RSFQ circuits and was therefore preferred. Furthermore, to construct circuits with ease the student version of the schematic editor OrCad Capture CIS[4] was used.

3.1 Basics of the Rapid Single Flux Quantum Logic

Several superconducting phenomena are of fundamental importance for the operation of superconducting circuits based on the Rapid Single Flux Quantum logic. The principle of superconductivity itself enables ballistic transfer of picosecond waveforms over large distances. This is both essential for on-chip interaction and interaction between chips. When applying a magnetic field to a loop of a superconductor the flux which passes through the loop is quantized as $\Phi = \Phi_0 n$, where $\Phi_0 = 2.067 \cdot 10^{-15}$ Wb is the magnetic

[3]PSCAN2 Superconductor Circuit Simulator made by Pavel Shevchenko, `pscan2sim@gmail.com` and `http://www.pscan2sim.org/`
[4]See `https://www.orcad.com/products/orcad-capture/overview`

flux quantum. This follows from the second generalized London equation and is how information is physically represented in the RSFQ circuits. The presence or absence of a SFQ (Single Flux Quantum) in a superconducting loop represents a logical "1" or "0" respectively. Furthermore, the Josephson Junction (JJ) is used as the nonlinear element in the superconducting circuits. A JJ is a superconducting tunnel junction and due to overlapping wavefunctions on both sides of the junction a superconducting current can traverse through the barrier without any resistance. If the junction is in a superconducting loop then a transition of the junction into the resisitive state is associated with a change in the magnetic flux through the loop and thus a digital logic operation [17].
The generation of such a SFQ pulse is achieved by a Josephson phase slip of 2π which is done by momentarily exceeding the critical current of the junction. The junction is switched to its resistive state and a SFQ voltage pulse is transmitted through the junction. If one integrates the second Josephson equation over a phase difference interval of 2π one obtains the strenght of the SFQ volatge pulse generated[18]:

$$\int V(t)dt = \Phi_0 = \frac{h}{2e} \approx 2.07\,\mathrm{mV}\cdot\mathrm{ps} \tag{1}$$

Since the phase slip is of the order of several picoseconds, the RSFQ logic is able to perform operations at frequencies in the order of a 100 GHz [19].
Furthermore, RSFQ cells have very low active power dissipation. If one assumes that the critical current of a junction is of the order of $100\,\mu$A, then the energy dissipated during one switching event is [17]:

$$E_J \approx I_c\Phi_0 \approx 2\times10^{-19}\,\mathrm{J} \tag{2}$$

Typically the critical current of a junction also depends on the operation temperature of the circuit. Most circuits are cooled with liquid helium and thus operate at a temperature of 4.2 K or lower. For the circuit to operate well the critical current of its junctions should be three orders higher than the effective noise current value, which is given by [17][18]:

$$I_{noise} = \frac{2\pi}{\Phi_0}k_BT \approx 0.18\,\mu\mathrm{A} \tag{3}$$

This also limits the operation of RSFQ circuits build using high temperature superconductors and operation at temperatures near liquid nitrogen since at that temperature the noise current is about 20 times larger. At this rate the critical current of junctions should also increase significantly and the loop inductances have to be made smaller, but their size has a limit. Thus operation of RSFQ at liquid nitrogen temperatures poses several difficult problems and using HTS materials to create junctions has its own challenges and therefore it still remains questionable whether this is feasible.

3.2 Josephson Junction Dynamics and Simulations

As said earlier the Josephson Junction is the nonlinear element used in RSFQ logic. In this section the dynamics of a JJ will be discussed based on the Josephson equations and an analogy with a mechanical pendulum. Furthermore, the famous AC and DC Josephson effects will be shown using PSCAN2 simulation software in addition to the switching of the junction and subsequent generation of a SFQ Voltage pulse. Since the junctions are mostly used in pairs in a loop in RSFQ logic the Superconducting QUantum Interference Devices (SQUIDs) will also be discussed.

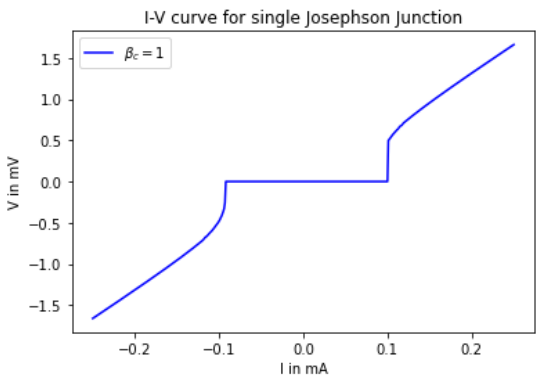
3.2.1 Josephson Junction Dynamics

The dynamics and current/voltage behaviour of a weak link such as a Josephson Junction are described by the two fundamental Josephson equations:

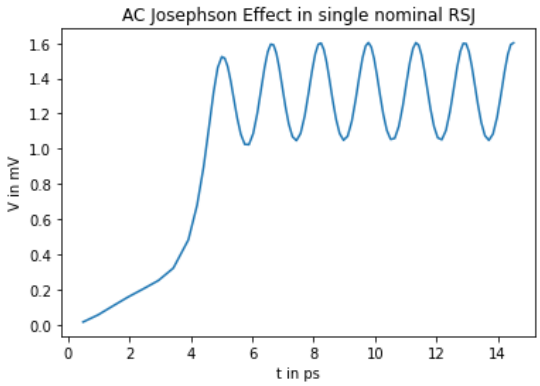
$$\begin{aligned} I_s(\phi) &= I_c\sin(\phi) \\ V(t) &= \frac{\Phi_0}{2\pi}\frac{\partial\phi}{\partial t} \end{aligned} \tag{4}$$

where $\phi = \nabla\theta$ is the superconducting order parameter difference across the junction which is also called the difference in phase across the juncton. One can relate the superconducting order parameter phase to the magnetic flux as: $\phi = 2\pi\frac{\Phi}{\Phi_0}$. Thus one indirectly relates the superconducting current through a junction to the magnetic flux through a loop and the time derivative of the flux to the voltage over the junction [20][21].

The AC and DC Josephson effect can be neatly demonstrated using PSCAN2. To show this a Josephson Junction is placed in series with a bias current source and both are grounded, the critical current of the junction is chosen as $100\,\mu$A. PSCAN2 uses a RSJ model for its junction (resistively shunted) and as a default its normal resistance is equal to one (dimensionless units), i.e. a nominally shunted JJ with McCumber-Stewart parameter: $\beta_c = 1$ [22]. The results of this simple simulation are shown in figure 7. In figure 7a the current supplied to the junction is varied from a range of $-250\,\mu$A till $250\,\mu$A and the voltage across the junction is simulated. The junction has a critical current of $100\,\mu$A and it is visible that in the range from $-I_c$ till I_c there is no voltage across the junction and it is in the superconducting state. When the current exceeds its critical value a resistance appears and the I-V curve scales according to Ohm's Law. In figure 7b a current was supplied to the junction which exceeds the critical value, thus the junction is permanently in its resistive state. The second Josephson equation predicts that the voltage has an AC component in this case and as can be seen from the figure this is exactly the case. PSCAN2 needs a few picoseconds to setup the simulation, but at around 4.5 picosecond the voltage starts to oscillate indicating AC behaviour. This verifies that also the second Josephson equation which governs the AC Josephson effect is correctly simulated by PSCAN2.



(a) Current/Voltage characteristic curve of a Josephson Junction with critical current $100\,\mu$A.



(b) Demonstration of the AC Josephson effect for a single junction.

Figure 7: Simulation of the two fundamental Josephson effects for a simple DC biased single Josephson Junction with critical current of $100\,\mu$A.

A superconductor-insulator-superconductor (SIS) junction is mostly described by a resistively and capacitively shunted junction (RCSJ) model. This model describes the junction as if it were parallel to an external shunt resistance and capacitance, in the normal conducting state the normal current would pass through this external resistance and capacitance. One can describe the currents through all these elements as a function of the phase slip, ϕ, across the junction to end up with an overarching equation describing the current dynamics of the junction [17]:

$$I/I_c = \sin\phi + \omega_c^{-1}\dot{\phi} + \beta_c\omega_c^{-2}\ddot{\phi} \tag{5}$$

where $\omega_c = \frac{2\pi}{\Phi_0} I_c R_n$ is the characteristic switching frequency of the junction with normal resistance R_n and $\beta_c = \omega_c R_n C$ is the McCumber-Stewart parameter which includes the effect of the capacitance [23]. This dynamical equation is quite similar to the equation of motion for a mechanical pendulum where capacitance is analogous to mass and resistance to damping. This analogy is illustrated in figure 8. When a junction switches to the resistive state, its phase is changed by 2π. A voltage appears over the junction, but it dies out, since the junctions return to its superconducting state. The same happens for a pendulum when one gives it a rotation of 2π and then lets it swing back to its equilibrium. Thus, a superconducting circuit can be thought of as a net of coupled pendulums [17]. Subsequent to a 2π rotation of a pendulum are oscillations around a stable equilibrium. In Josephson dynamics these oscillations are called plasma oscillations and in order for the cell to correctly work these oscillations should be vanished before the junction is switched again. To achieve this one designs the junction such that the plasma oscillation frequency is equal to the characteristic frequency and the McCumber-Stewart parameter is equal to 1 [17].

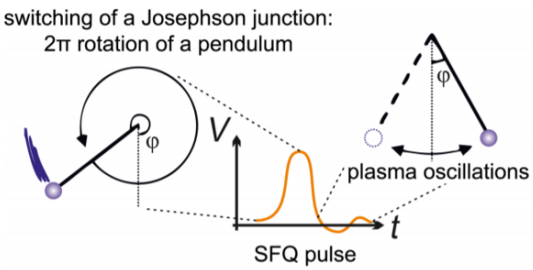


Figure 8: Analogy between the switching of a JJ and subsequent production of a voltage pulse and the rotation and subsequent oscillations of a mechanical pendulum (Figure from [17]).

3.2.2 SFQ Pulse Generation

Consider a superconducting loop with one Josephson Junction, such a device is also called an RF SQUID. According to the London equation the magnetic flux through such a loop can only take on integer multiples of the magnetic flux quantum [21]. If one where to apply a bias current to this loop which does not exceed the critical current of the junction one would end up with a circuit as shown in figure 9. Where L1 is the superconducting inductance of the loop and P1 is there to simulate a 2π phase slip of the junction i.e. a change in magnetic flux. If a magnetic field is applied perpendicular to the loop, then the magnetic flux through the loop will induce a circulating current in the loop. If the addition of the bias current and this circulating current exceeds the critical current of the junction, then the junction switches to its resistive state and a SFQ voltage pulse is generated [19].

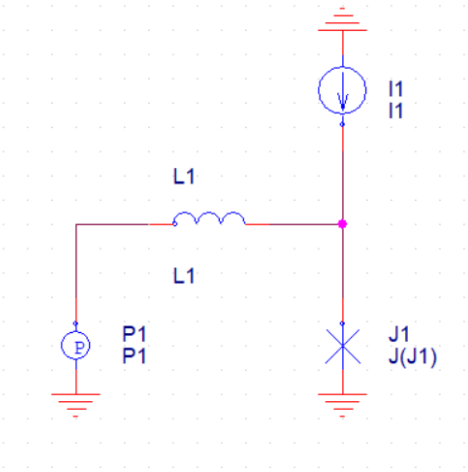


Figure 9: Schematic of a biased single junction SQUID (RF), the phase source is there to simulate the presence or absence of magnetic flux.

The critical current of the junction is chosen as $100\,\mu$A and the bias current follows from the prescript $I_b = 0.8I_c = 80\,\mu$A, also the loop inductance is chosen as $L = 3\,$pH [24]. P1 generates twice a 2π phase slip which represents the introduction of a magnetic flux quantum in the loop. The result is shown in figure 10

The change in phase of the junction by 2π and the subsequent voltage pulse generated by switching into the resisitive state are clearly visible. The pulse is only several picoseconds long and the plasma oscillations are also visible. Furthermore, the pulse is of the order of mV which was predicted by integration of the second Josephson equation, as a check the area under the curve was calculated and it was similar to the result from integrating

In this case an RF SQUID was used to show the generation of a SFQ pulse, however one can also use a DC SQUID to generate pulses. A DC SQUID is again a loop, but this time there are two junctions parallel to each other (replace the phase source in figure 9 with a second junction). This means that since the bias current splits in two at the node, one needs twice as much current to exceed the critical current of both junctions and have them be switched [21]. The use of DC SQUIDs in RSFQ is best illustrated using the so-called active Josephson Transmission Line, which is the topic of the next section.

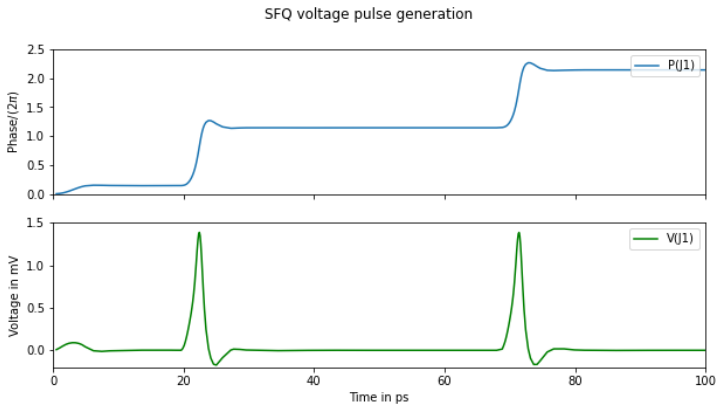


Figure 10: Two SFQ pulses are generated in the RF SQUID of figure 9. The phase of the junction is changed by 2π and hence the junction switches and a SFQ voltage pulse is generated across the junction.

3.3 Transmission Lines in RSFQ Electronics

In SFQ dynamic circuits the SFQ pulses, which last several picoseconds and have an amplitude of the order of millivolts, are passed along in the circuit and to other devices along either passive or active transmission lines. Due to the superconducting nature of the circuits the transmission along these lines is ballistic, i.e. with no resistance. Since the coated conductor tapes are produced at extremely long lengths an interesting application for them arises in the use of transmission lines. In this section both active and passive transmission lines will be discussed. The active transmission line is called the Josephson Transmission Line (JTL) and is also able to provide current or power gain to the signal. An example of a passive transmission line is for instance a microstrip which will also be discussed [24].

3.3.1 The Josephson Transmission Line

The Josephson Transmission Line (JTL) is an asynchronous RSFQ device meaning it has no internal memory and thus it generates an output SFQ pulse immediately after the arrival of an input pulse [24]. The basic principle of operation of a JTL is shown in figure 11. A JTL consists of loops of superconducting Josephson Junctions and superconducting inductances, furthermore each junction is biased. If a SFQ pulse is supplied to the left of the array then it is passed along by the JTL by the successive switching of the junctions. The switching of the junctions is based on the summation of the current flowing through the loop, this is the DC bias current, I_b, and the circulating current due to the SFQ which is trapped in the loop. If the summation of the two currents exceeds the critical current of the JJ a phase slip of 2π will occur and the junction switches to the resistive state. Switching of the junction to the resistive state will lead to the redistribution of the circulating current of the SFQ pulse to the next junction. If the next junction switches the redistribution is finished and the current junction switches back to the superconducting state. Thus whether an SFQ pulse propagates is just a matter of summing the currents and seeing whether it exceeds the critical current and switching of junctions which results in reproduction and propagation of the pulse [17].

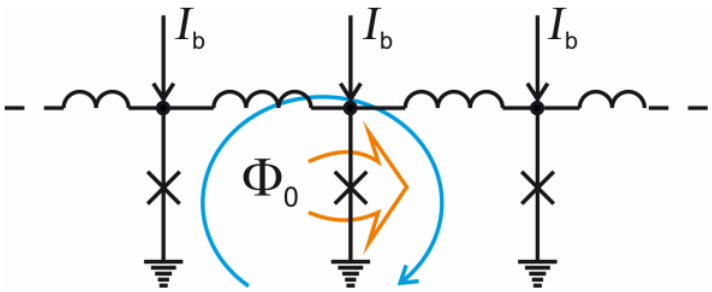


Figure 11: Principle of operation of a JTL which passes a SFQ pulse along (Figure from [17]).

To achieve correct operation of the JTL a rule of thumb is to choose the bias current using: $I_{bi} \approx 0.7 I_{ci}$

and to choose the connecting inductances as $L_i I_{ci} \approx 0.5\Phi_0$ [25]. Choosing a critical current of $100\,\mu$A, one finds bias currents of $140\,\mu$A and inductances of approximately 5 pH. The schematic of the circuit is shown in figure 12, this is a subcircuit, the overarching circuit supplies the 2π phase slip at the input and a resistance is placed at the output. The inductances L3, L4 and L5 have a value of 5 pH and L1 and L2 of 2.5 pH. The result of the simulation can be seen in figure 13.

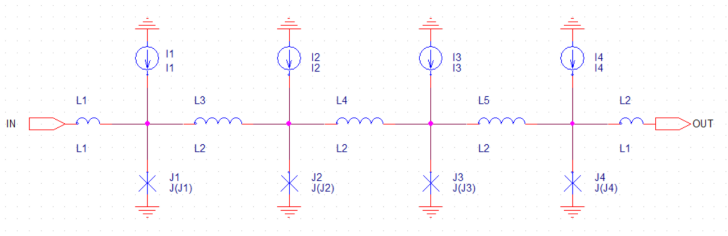


Figure 12: Schematic of a JTL with four DC biased junctions.

As one can see the SFQ is transferred through the JTL by the subsequent junctions. The spacing between successive switching of junctions is around 1.95 picoseconds which is four times the characteristic time ($\tau_0 = \frac{\Phi_0}{2\pi I_c R} \approx 0.49\,$ps) as predicted by theory [24]. Furthermore, a check was done with the areas under the voltage pulses and they all have a value of approximately $2\,\text{mV}\cdot\text{ps}$,which was predicted by the integration of the second Josephson equation.

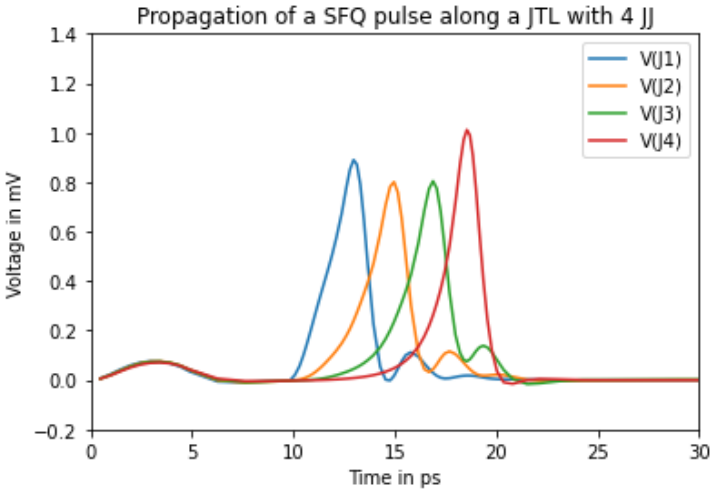


Figure 13: Propagation of a SFQ pulse through the JTL of figure 12.

One can also provide current gain by using a JTL. In order to do this one must let the critical current increase along the JTL (so also the bias currents) by a factor of $\sqrt{2}$ per junction (so also the bias current) and let the inductances decrease per loop ($L_1 > L_2$...), i.e. divide by $\sqrt{2}$ [25]. This provides a high current gain as can be seen in figure 14.

However, there are several downsides to the use of JTLs in RSFQ circuits. A major problem is regarding stationary power dissipation which is approximately 800 nW per RSFQ cell. This is due to the fact that one has to supply bias currents to the JTL. Since the bias voltage has to be an order of magnitude higher then the characteristic voltage of a junction, so $V_b \approx 10 I_c R_n$, this results in much stationary energy dissipation. However, dynamic power dissipation is much less since $P_D = I_b \Phi_0$ which is approximately 12 nW [17]. Another disadvantage of using the JTL is the fact that there is a large delay in pulse propagation. When passing through each junction the pulse is delayed by $4\tau_0$, four times the characteristic time scale. In the previous example τ_0 was about 0.5 ps, which means that the delay is 2 ps per junction. When considering a long JTL this all ads up to quite a large delay and thus the propagation speed is quite low about $10\,\mu\text{m}\cdot\text{ps}^{-1}$ [24]. Whereas the first problem, stationary power dissipation, was solved with the introduction of ERSFQ (Energy-Efficient RSFQ) and eSFQ (Energy-Efficient SFQ), where the stationary power dissipation could be reduced even to zero (See [17] for an

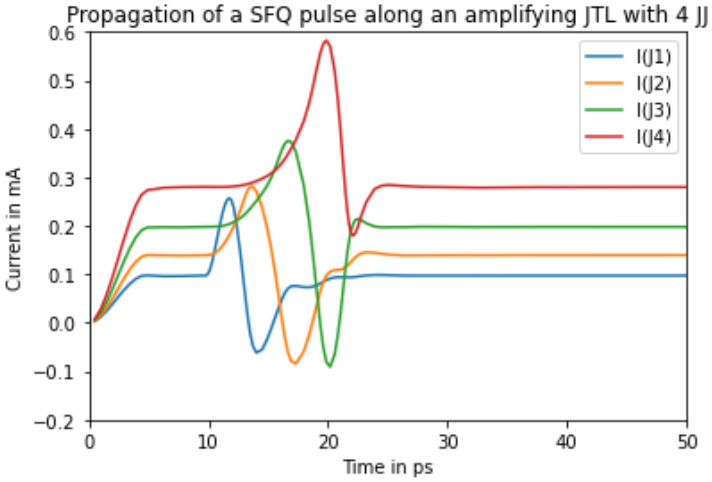


Figure 14: Amplification of the current due to increasing I_c and I_b and decreasing loop inductance.

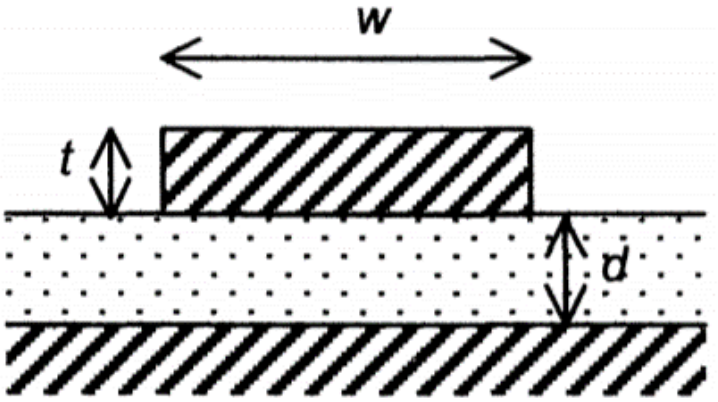


Figure 15: Schematic geometry of a microstrip transmission line. Dielectric with thickness d and superconducting strip with thickness t and width W (Figure from [24]).

explanation of both techniques). The second problem is however not as easily dealt with and is the main disadvantage of using JTLs to transmit pulses.

3.3.2 The Passive Transmission Line (Microstrip)

As said in the previous section the JTL has several disadvantages when it comes to transmitting signals, its considerable delay and low propagation speed ensure that it is not suitable for long transmission lines. An alternative to the JTL is a passive transmission line such as a microstrip. The microstrip has a very simple geometry, which can be seen in figure 15. A thick dielectric substrate on a superconducting ground plane is used. On top of the dielectric a thin and narrow strip of the same superconductor is patterned [24]. Signal propagation along these line is much faster than for the JTL and given by:

$$v \approx c\sqrt{\frac{d}{(d+2\lambda)\epsilon}} \tag{6}$$

where d and ϵ are the insulator thickness and dielectric constant respectively. Here signal propagation is about and order of magnitude higher then for the JTL, approaching almost one third of the lightspeed. Since superconductors have very low AC losses below their gap frequency on-chip and inter-chip transmission lines are able to transmit signals with very low attenuation and distortion, even for picosecond signals as in the case of RSFQ. A major downside is the fact that one has match the impedance of the transmission line to the impedance of the RSFQ circuit and thus a so-called transceiver (Transmitter-Receiver) circuit is needed which takes up considerable area on a chip [24]. Thus the use of passive

transmission lines is only suitable when a connection longer then the transceiver length, approximately 50 microns, is needed.

Unfortunately simulations could not be performed using PSCAN2 since it does not offer an element for a passive transmission line. However, Polonsky *et al.* have showed that it is indeed possible to create on-chip microstrip transmission lines with corresponding matching circuits [26]. A simulation of the propagation of a pulse is shown in figure 16 which was taken from their paper and was simulated with PSCAN (the old version of PSCAN did offer simulations with microstrips). As seen in the figure a voltage pulse is first transmitted through three junctions which are matched to the microstrip. After passing through the microstrip the pulse is transmitted through the junctions in the receiving circuit and clearly visible is that there is low attenuation to the signal.

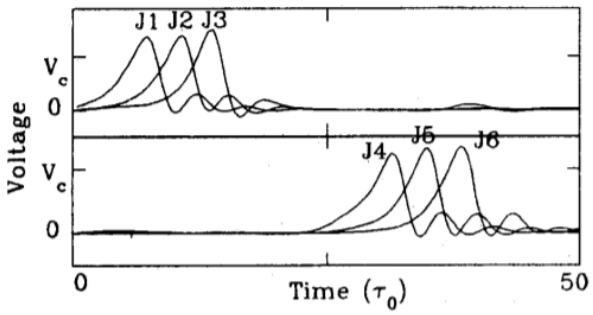


Figure 16: Simulation of the propagation of a voltage pulse along a microstrip line which was matched to two circuits (Figure from [26]).

Passive transmission lines have very simple geometries, as seen in the example of the microstrip. Since they can be used to carry a signal ballisticly over long lengths it is an interesting application for the superconducting tapes used in this research. If it is possible to create small microstructures on the tapes then it is interesting to see whether it is also possible to create long, several centimeters, passive transmission lines such as microstrips.

3.4 Artificial Neural Networks (ANN)

Artificial Neural Networks provide an interesting approach to solving difficult time consuming problems. The operation of the ANN mimics the workings of the human brain and neural network to achieve high speed, low power usage and smart solving. An approach to construct these Neural networks is with the use of RSFQ logic, since their operating frequency is in the order of a hundred GHz and power dissipation is extremely low [27].

A biological neuron consists of a soma which processes signals, dendrites which feed the soma with a signal and an axon which transmits the output signal sent from the soma. The ANN tries to mimic this behaviour, its basic principle of operation is visualized in figure 17. Input signals X_i with weights W_i are summed at the soma. The soma then checks whether the acquired value is larger then the threshold value and if this is the case it transmits an output signal, Y, through the axon [27].

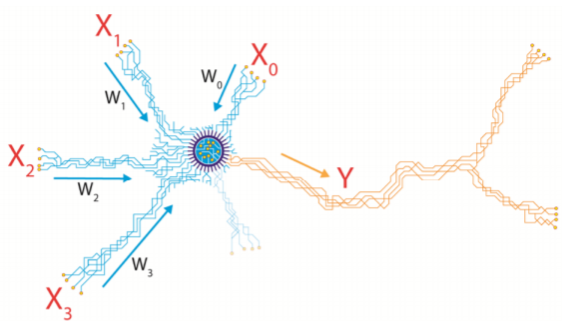


Figure 17: The mathematical model behind operation of a neuron (Figure from [27]).

In the RSFQ logic this process is mimicked using Josephson Junctions, threshold and decaying loops and JTLs. As illustrated in figure 18 the summation of incoming pulses is done by a JJ-synapse which merges incoming signals (SFQ voltage pulses) and puts the result through to the soma. The soma is a JJ-soma with threshold and decaying loops to mimic the signal decay happening in a biological soma. Furthermore, if the threshold value of the JJ-soma is triggered it sends an output SFQ pulse through a JTL [27].

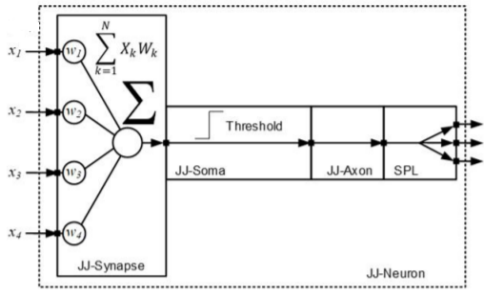


Figure 18: RSFQ variant of artificial neuron operation (Figure from [27]).

The artifical soma is the most important part of the neuron and will be discussed in detail, see figure 19 for the RSFQ circuit. Most important are the threshold and decaying loop and the mutual inductance between the two. The loops can mimic the fading of signals that are held in the threshold loop. By adjusting parameters of the loops the threshold for pulse firing can be adjusted.
The inductance IN1, IN2 and OUT are there to match the circuit to other circuits and in- or outgoing JTLs. The junction J1 and J2 determine the threshold value. RLOOP has effect on how fast current in the threshold loop is dissipated, increasing the resistance will ensure faster dissipation. Mutual inductance, K, between inductances TOP and LOOP also has effect on the decaying time of the threshold loop current. Increasing K will result in more current transferring to the decaying loop and faster dissipation of the loop current. Increasing LLOOP will result in extended decay time. RTOP1 and RTOP2 have same function as RLOOP. The DC bias current is used to adjust the quiescent point of the neuron [27].

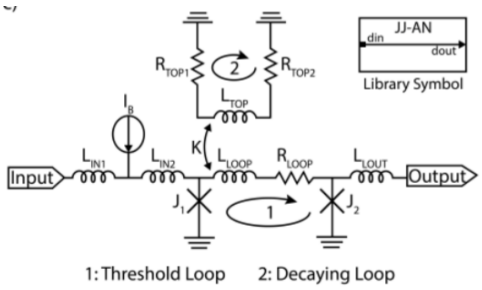


Figure 19: RSFQ circuit of an artificial JJ-soma (Figure from [27]).

A simulation was performed to see the behaviour of the JJ-Soma. The threshold value was chosen such that two pulses within approximately 30 ps would trigger the JJ-Soma to fire an output signal. Furthermore, parameters needed for the circuit were taken from Bozbey *et al.* to ensure that the circuit behaved optimal [27]. See figure 20 for the results of the simulation. Clearly visible is that when just one pulse is fired the current circulating in the threshold loop is not large enough to exceed the threshold value to switch the second junction. Thus the current is dissipated through the above explained effects. However, when one fires two subsequent pulses within an interval of 30 ps the loop current does exceed the threshold when the second pulse arrives and as such the second junction switches and a voltage pulse is transmitted. Similarly, when sending four pulses with an interval of 30 ps between each other, the JJ-Soma fires two output signals since the threshold is exceeded twice.

In a more complex system of the biological neuron, signals are delivered to the soma by a synapse and the output signal is carried away by an axon. In the RSFQ imitation the signals can be delivered and carried away by the use of JJ-Axons, which are basically Josephson Transmission Lines [27]. A simulation of such a system was carried out as well. The pulses were delivered to the JJ-Soma by the use of the

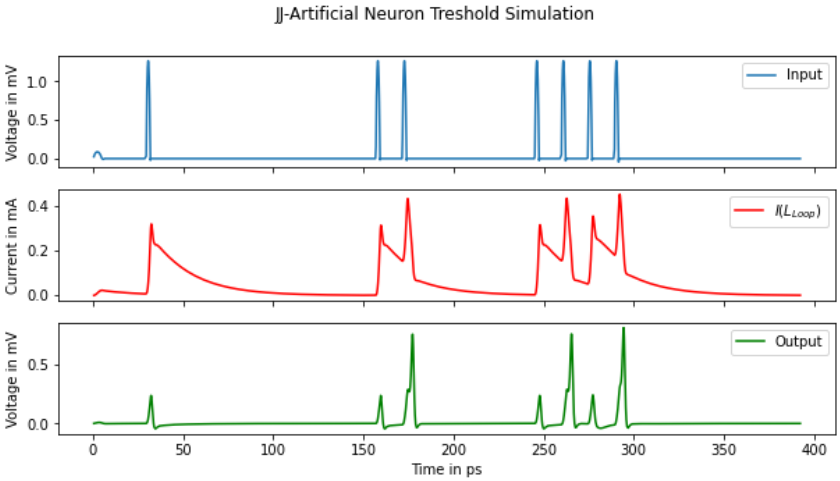
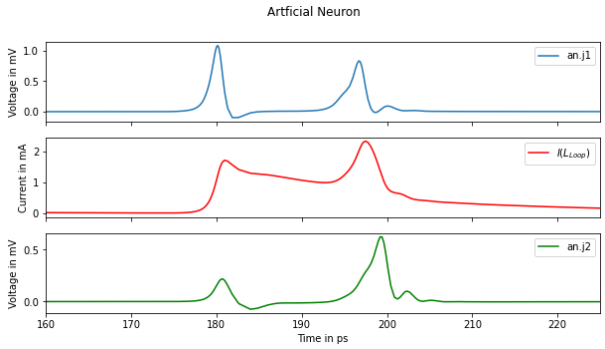
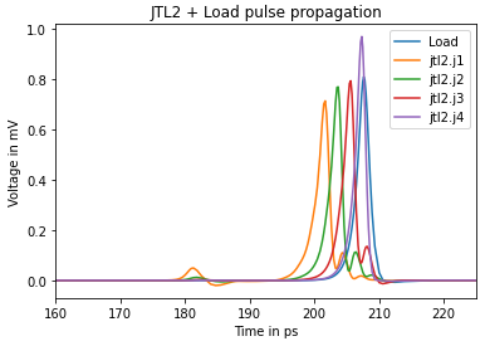


Figure 20: Threshold simulation of artificial JJ-Soma. After two pulses are fired within 30 ps of each other the JJ-Soma reaches the threshold and fires an output signal.

4-element JTL discussed in section 3.3.1, the output signal of the soma was again carried away by the same 4-element JTL. The same two-pulse threshold JJ-Soma was used as before and only adjustments were made to the inductances to match the circuits. The results of the simulation can be seen in figure 21. The voltage pulses through the input JTL are not shown since it gives no new insight. As is clearly visible in figure 21a the threshold loop current of the soma is reached when the second pulse arrives and the current is large enough to switch the second junction and produces an output signal. In figure 21b it is visible that when the threshold is exceeded the subsequent output pulse is carried away along the JTL and dumped in a load resistance.



(a) Results of the simulation of the JJ-Soma supplied with two voltage pulses. The second pulse arrives 15 ps after the first and ensures that the loop current is large enough to switch the second junction and produce an output signal.



(b) Results of the output JTL, the first pulse at 180 ps is not enough to produce an output signal. With the arrival of the second in the soma, the threshold is reached and an output pulse is transmitted along the JJ-axon.

Figure 21: Results of a more complex simulation of the JJ-Neuron with input JTL, JJ-Soma and output JTL.

Whilst this might be considered a more complex circuit it is still not near enough of an imitation of a biological neuron. However, this section has dealt with the basics of RSFQ and its potential for applications such as Artifical Neurons and Neural Networks. The introduction of clocked circuit cells, such as flip-flops, gives much more possibilities of using RSFQ in smart computation techniques such as Artificial Neural Networks. For a more in-depth read about clocked circuit cells of the RSFQ family see Bunyk *et al.* [24] or Likharev *et al.* [25]. For a good article about the potential of RSFQ electronics in the use of ANNs see Bozbey *et al.* [27]. Furthermore, as stated in section 3.3.2 it is interesting to see the potential usage for the tapes in creating transmission line structures on them. If this is possible it is also interesting to see whether the tapes (with transmission lines) can be used to function as for instance axons in the ANNs.

4.

Experimental Methods

In this chapter the experimental methods used during the experimental part of the research will be discussed. In the first section two electron microscope techniques, TEM and SEM, will be explained which were used to characterize the structure and morphology of the tapes. Furthermore, in the second section the fabrication techniques to create microsctructures on the tapes using lithography are discussed. Two approaches of etching out the patterned structures, wet chemical and ion beam, are discussed in detail. Lastly, in the last section experimental techniques concerned with measuring superconducting properties, such as the critical current, are discussed. Unfortunately these were not fully done in the end, but nevertheless the approach will be explained.

4.1 Characterization Techniques

Characterization techniques are used to investigate the surface morphology and structure of the tapes. Two forms of electron microscopy are used to achieve this. The scanning electron microscope (SEM) is a microscope used to image the surface of the sample and the tunneling electron microscope (TEM) is used to investigate the structure of the tape. The TEM was operated by dr. E.G. (Rico) Keim and sample preparation using the Focused Ion Beam (FIB) was done by H.A.G.M (Henk) van Wolferen who are both members of the Analysis group of the NanoLab Staff at the MESA+ Institute for Nanotechnology [5].

4.1.1 Scanning Electron Microscopy

The optical microscope is limited in its resolution by the light used in the microscope, therefore imaging of micro- and nanostructures with small features using a normal microscope is difficult. The SEM however uses a beam of electrons instead of a beam of light. Since the wavelength of electrons is inversely proportional to the square root of the energy of the electrons, the wavelength can be reduced drastically by giving the electrons more energy.
In a typical SEM a small filament of tungsten is used to thermoelectrically emit electrons. The resultant electrons are repelled by a cathode and drawn to an anode and are thus accelerated. Several lenses are used to focus the electron beam on a small spot on the surface. When the electrons are incident on the surface the so-called primary electrons (primary since they originate from the filament source of the SEM) transfer their energy to the electrons of the sample and to the lattice of the sample. In this research the Secondary Electron Image (SEI) technique was used. This technique is dependent on the fact that since the primary electrons give of their energy to the electrons of the sample and lattice, it is possible for an electron to be emitted from the surface and be detected. These electrons are called secondary electrons (since they originate from the surface of the sample) and are low in energy which means that they come from the top most part of the surface, about several Å deep [8].
The specific SEM used during this project can be seen in figure 22, the specific model is the JEOL JSM-5610 and it is located in the Thin Film Lab of ICE in the NanoLab.

4.1.2 Tunneling Electron Microscopy

The principle of TEM is very similar to that of SEM. However, in the case of the TEM the electrons are transmitted through the material and scattering due to interaction with the sample results in an intensity pattern which gives an image of the specimen. Again because of the fact that electron are accelerated in the TEM to high energies (order of 100 keV) their wavelengths are extremely small and thus even individual atoms in a lattice can be imaged since the resolution is so good.
The TEM offers various operational modes to obtain information about various different aspects of the specimen. Since samples have to be extremely thin for enough electrons to transmit through it, the sample has to be prepared using the Focused Ion Beam (FIB). The FIB is used to prepare samples for TEM cross-section imaging, the FIB is able to take a lamella out of a larger sample and thin it using gallium ions such that it becomes thin enough to be analyzed in the TEM. In this research the TEM was used to obtain cross-sectional images of the tapes. The FIB was used to cut out a lamella and to thin out the cross-section lamella, due to different etching speeds for different elements it is quite difficult to

[5] For personal information see `https://www.utwente.nl/en/mesaplus/infrastructure/nanolab/people/`

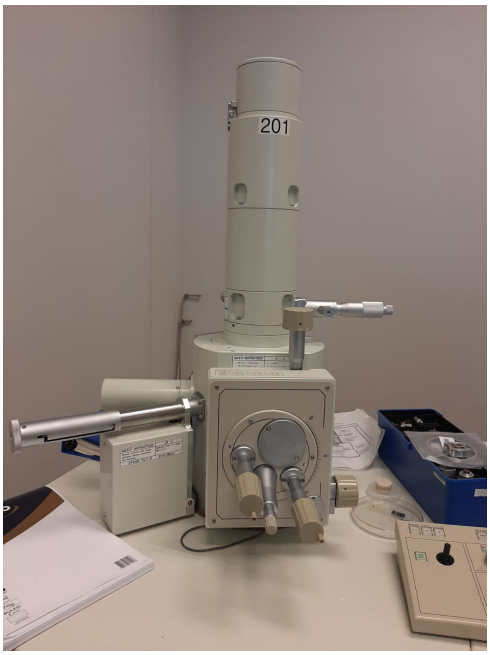
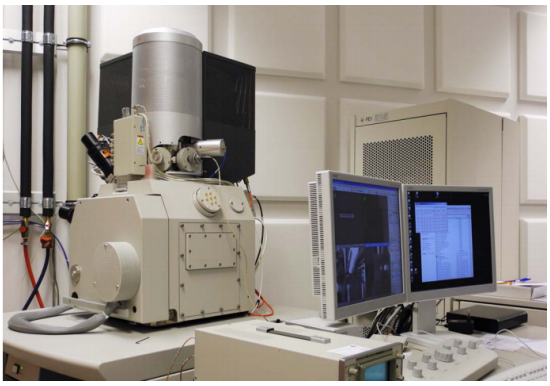


Figure 22: The JEOL JSM-5610 SEM used in this project.

thin out a multilayered structure [8].
The FIB used in this research is a Nova 600 Dualbeam SEM/FIB (figure 23a) which also has a SEM installed, gallium ions are used as the ions in the etching beam. This SEM/FIB is located in MESA+ Analysis Lab and is operated by H.A.G.M van Wolferen. The TEM used is a Philips CM300ST-FEG TEM 300kV (figure 23b) with a GATAN camera. It is also located in the MESA+ Analysis lab and is operated by dr. E.G. Keim.



(a) Nova 600 Dualbeam SEM/FIB located in the MESA+ analysis lab.

(b) Philips CM300ST-FEG TEM 300kV with GATAN Camera.

Figure 23: Images of the TEM and FIB used, both are located in the MESA+ Analysis Lab (Images were taken from MESA+ website[6]).

4.2 Microstructure Fabrication Techniques

The goal of the research is to determine whether the tapes can be used in superconducting electronics. Since all current day electrons are fabricated using small micro/nanostructures it is of interest to see whether one is able to fabricate such structures on the tapes as well. To pattern structures on the tapes photolithography will be used, which will be discussed in the first section. In order to process the

[6]See `https://www.utwente.nl/en/mesaplus/infrastructure/nanolab/analysis/facilities/`

patterned structure chemical etching techniques will be discussed, one which relies on energetic ions and the other which uses wet chemicals.

4.2.1 Photolithography

Photolithography is one of the most widely used lithography techniques used to pattern microscale structures on substrates. The technique focuses on transferring the pattern of a mask onto a layer of light sensitive photoresist with the use of a light source. The main limit in the resolution of the photolithography process is the wavelength of the light used. In most photolithography processes the light used is UV, for a smaller resolution one for instance has to use electron beam lithography.
The process of photolithography can be seen in figure 24, but there are several steps prior to light exposure which are also of importance. Of course the surface onto which the resist has to be placed has to be cleaned in order to remove any grease and moisture. Then the photoresist can be applied on the sample. This is done by adding several droplets on the surface and then using a spinner which rotates at a very high frequency to even out the resist over the entire sample, this process is also referred to as spincoating. There are several variants of resist with varying thicknesses, a thicker resist ensures that the sample is more protected since it takes longer to etch through the resist, but resolution of the structures is smaller. For a thinner resist smaller structures can be created, but at a risk of the etchant etching too fast through the resist. In order to increase the quality of the resist coating, the sample is baked at approximately 100 degrees Celsius on a hotplate [28].
Now the resist coating is ready to be exposed to the light source, this process is nicely illustrated in figure 24. A mask is placed in the lithography station which contains the 2D geometry of the structure one wants to build. This means that the mask blocks the light from irradiating certain positions. Where the resist is exposed to the UV light source a chemical change occurs in the resist. Depending on whether positive or negative resist is used there are two results. For positive resist the irradiated region of photoresist changes such that when the sample is put in the developer the exposed area of resist becomes soluble in the developer. With negative resist the process is reversed and an exposed area now becomes stronger and unexposed areas dissolve in the developer. Now the structure which one wants to build is protected by the resist and the next step in the process is to etch away the material which is not protected using either wet or dry chemical etching. After etching the photoresist has to be removed, this is simply done by putting the sample in an acetone bath and afterwards spraying ethanol over the sample [28].

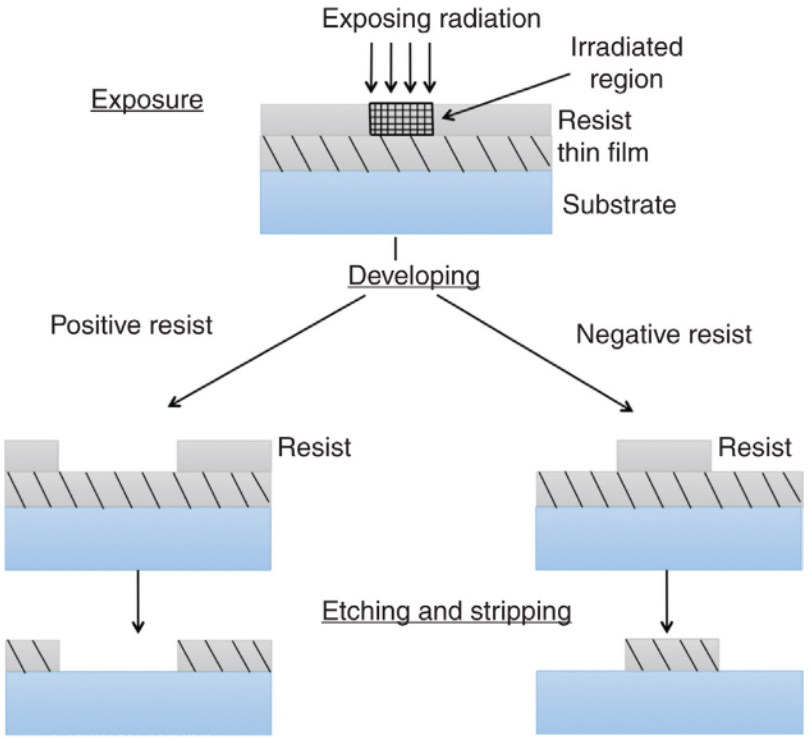


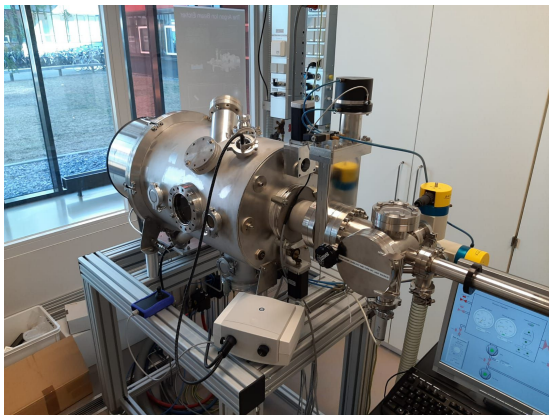
Figure 24: The process of light exposure and subsequent development and etching of a sample which is patterned using the photolithography process (Figure from [28]).

Unfortunately due to the regulations of the University of Twente regarding the Covid-19 measures, it was not possible for new (Bachelor or Master) students to work in the cleanroom of the NanoLab of the University. Therefore, I could not perform the steps in the lithography regarding the light exposure and resist development myself. The technician, F.J.G. Roesthuis, from the ICE group was however so kind to do this for me.

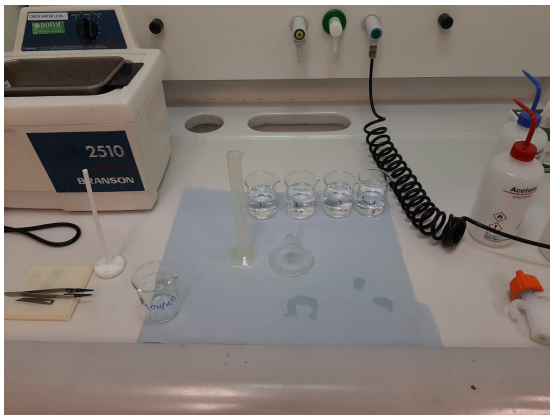
4.2.2 Ion Beam Etching

There are several approaches which can be used to process a patterned sample. The first which will be discussed is the use of an ion beam to etch away material. This technique is a dry etching technique since no liquid etchant is used, in fact a plasma of noble gas ions is used to etch away unprotected material from the sample.
A current is passed through a cathodic filament which results in thermoelectric electrons which are accelerated towards an anode. The noble gas argon is injected into the same chamber (discharge chamber) and due to collisions with the high energetic electrons a plasma is formed which contains among other things also argon ions. An accelerator grid is used to accelerate the argon ions in a beam towards the sample in the process chamber. In the process chamber a neutralizer feeds electrons to the beam to make the beam neutral and reduce surface interaction. The incident argon beam slams into the surface and expells material from the surface. The entire system is operated at Ultra High Vacuum to reduce interactions of the beam prior to reaching the surface of the sample [8].

The Argon Ion Beam etcher used to etch samples can be seen in figure 25a, the specific model used is the Veeco Ion Tech Inc. MPS-5001 which is located in the Thin Film Lab of ICE.



(a) Veeco Ion Tech Inc. MPS-5001, which is located in the Thin Film lab of ICE.



(b) Set-up used for chemical etching of samples and subsequent cleaning in water.

Figure 25: Two types of chemical etching methods used. (a) Dry chemical etching using an Argon Ion Beam. (b) Wet chemical etching using various acid/base solutions.

4.2.3 Wet Chemical Etching

The second approach which can be used to etch away material after patterning is with the use of liquid etchants, therefore called wet chemical etching.
The principle of wet chemical etching is to use solutions of acids or bases in water to enable chemical reactions to etch away the material. In most cases wet chemical etching is isotropic which means that the etching speed is the same in all directions. This can result in a phenomenon known as underetching, where the etchant solution etches under the resist and etches away part of the structure. It is therefore important to immediately clean the sample with water once it is out of the solution, to stop the etching process.
In this research several solutions were used: phosphoric acid (10%, H3PO4), ammonia hydrogen peroxide (14%/14%, NH4OH/H2O2) and a commercial chromium etcher from the cleanroom (Ceric(IV) Ammoniumnitrate). The set-up used for chemical etching can be seen in figure 25b, samples are placed on the white sample holder and stirred up and down in the beaker containing the etchant. After a period of time they are cleaned in several beakers and dried to remove any chemicals from the surface.

4.3 Transport Properties

In order to develop functioning electronic devices it is important to understand the electrical transport properties of the device such as the current/voltage behaviour. However, in order to do this one has to couple the small microstructure to macroscopic measuring equipment such as voltmeters. Furthermore, to measure superconducting properties such as the critical current one also has to cool the system to low temperatures. Thus, in order to measure the current/voltage characteristics of a device and hence obtain the critical current one has to make a connection between the microscopic voltage and current contact pads present on the sample with the macroscopic input of the measuring apparatus and cool the entire sample down to 77K.

This is done using a Printed Circuit Board (PCB), the sample containing the device is connected to the PCB using a wire bonder. A thin, 25 micron diameter, aluminium wire is pressed onto the microscopic contact pad, the bonder fires a thermosonic pulse which presses the wire onto the contact and hence smears out the wire to create contact and a bond. The bonder is then displaced to the macroscopic contact pad on the PCB where again the wire is pressed to the surface and the second bond is formed. A bond is now formed between the (micro) contacts on the sample and the (macro) contacts on the PCB. The wire bonder used in this research is a MECH-EL Industries MEI 907 which forms the aluminium wire bonds, each wire can carry approximately 1 A before it breaks. In order to supply large currents to the sample, many bonds need to be made in order to ensure that the bonds do not break. In order to connect the PCB to macroscopic equipment such as nanovoltmeters and a power supply copper wires are soldered to the PCB in order to carry enough current to the sample. The PCB (with sample attached) and part of the copper wires is placed in a liquid nitrogen bath (77K) to make sure that the GdBCO is superconducting ($T_c \approx 93K$).

To do accurate measurements of the current/voltage relation it is helpfull to employ the four-point probe method. In this approach four contacts leads are attached to the contacts pads of the sample. Two of them (the outer ones) function as current leads and the other two function as voltage leads (inner ones), which is schematically drawn in figure 26. Typically when measuring electrical resistance of a sample the resistance of the contacts and leads is not that large. However, when working at low temperatures and measuring small resistances the contact and lead resistance can be quite large, this is the case for superconductors. The four-point probe method is able to fix this problem and eliminate the influence of the lead and contact resistance during the measurement. Hence one can accurately measure the resistance of a sample between the two voltage probes and thus measure the transition to the superconducting state [29].

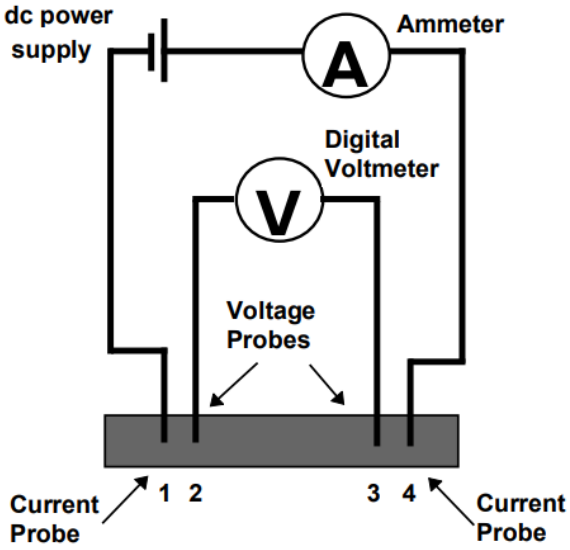


Figure 26: Schematic of the four-point probe method. Two outer probes are used as a current feed and a drain, the inner probes function as voltage probes and hence measure the resistance between the two voltage probes (Figure from [29]).

5.

Structural and Surface Characterization of 2G-HTS Tapes

In this chapter the first experimental results regarding characterization of the tapes will be shown and discussed. In line with the third sub-question it is important to know the structure of the tapes and the morphology of the top layers in order to come to a good conclusion whether they are suitable for fabrication of electronics, the SEM and TEM will be used to investigate these properties. The techniques were already explained in the last chapter, therefore this chapter focuses on the experimental details and the results obtained from using these microscopes. First the cross-sectional imaging done with the TEM will be discussed and afterwards the SEM images obtained from both the silver coating and HTS layer will be shown. Finally, the chapter concludes with an answer regarding research sub-question 3 in order to see which layer is more suitable for micropatterning.

5.1 TEM Cross-Section Imaging

The sample was prepared by the FIB such that it was thin enough to be used in the TEM. The goal of analysis using the TEM was to obtain high-resolution images of the cross-section (CS) of the tape. Such that one can identify the different layers, their thickness and look for defects deeper in the material. The accelerator potential difference of the TEM was 300 kV, meaning that electrons would be accelerated towards energies of 300 keV. When operating at 300 kV the TEM has a point resolution of 0.2 nm and line resolution of 0.14 nm, meaning that extremely small features can be resolved from each other [30]. The results from this cross-sectional imaging will be shown and discussed in this section.

Using the TEM a CS image was made of the top part of the tape, the substrate is only barely visible see figure 27. Immediately visible is the distinction in both intensity and structure of the different layers. The Platina layer on the left (indicated with Pt) was glued (light gray layer) to the silver layer during the preparation with the FIB, in order to give stability and protection to the sample during the thinning process. Indicated with *Thin* is a section of the sample which is brighter than the rest. This is also due to the FIB preparation, here the sample has been accidentally thinned out more. A thin edge on the right was also thinned out more with the FIB, but this was done intentionally. Furthermore, due to the fact that the FIB cuts out a small lamella from a larger sample curtaining occurs on the bottom which can be seen in the MgO(2) layer, where grooves/curtains are clearly visible.

The various layers of the sample can be easily seen and their thickness can be roughly estimated. The silver coating has an approximate thickness of about one micrometer. The GdBCO layer has an approximate thickness of 3 micrometers. It is difficult to see where the second MgO cap layer begins. However, curtaining starts to occur more in the MgO(2) and therefore the thickness of the MgO(1) layer can be estimated to be approximately 0.5 micrometers. The first MgO layer which is deposited using ISD is approximately 3 micrometers thick. The hastelloy substrate could unfortunately not be imaged, since it is much larger then the rest. When comparing these estimated thicknesses with the schematic of the TPL1100 tape discussed in chapter 2.3 (figure 2), one sees that they are very similar apart from the MgO(2) layer which was of course difficult to estimate.

Furthermore, there are several interesting qualitative things to see in the CS image. First of all, one can clearly see that at the interface between MgO(1) (Caplayer) and GdBCO layers there is a kind of sawtooth structure which is of course a result of the fact that the layer below (MgO(2)) is deposited using ISD which generates such a pattern. The sawtooth structure is taken over by the GdBCO layer as well, but at the interface between the silver and GdBCO layer it is only slightly visible. Also pointed to in the figure are holes in the cross-section. It is not quite clear how these holes have appeared, since it could not have been a result of the FIB thinning due to the fact that the Platina should protect the sample. However, they could also be more amorphous parts in the GdBCO layer where the composition and structure of the spot differs from the surrounding material.

The lattice parameter and growth direction of the GdBCO c-axis can be checked by using lattice fringes of a high-resolution lattice image with FFT analysis. The lattice parameters of the $GdBa_2Cu_3O_{7-x}$ unit cell are given by: $a = 3.837\,\text{Å}$, $b = 3.677\,\text{Å}$ and $c = 11.786\,\text{Å}$ [31]. From the lattice fringes and FFT of

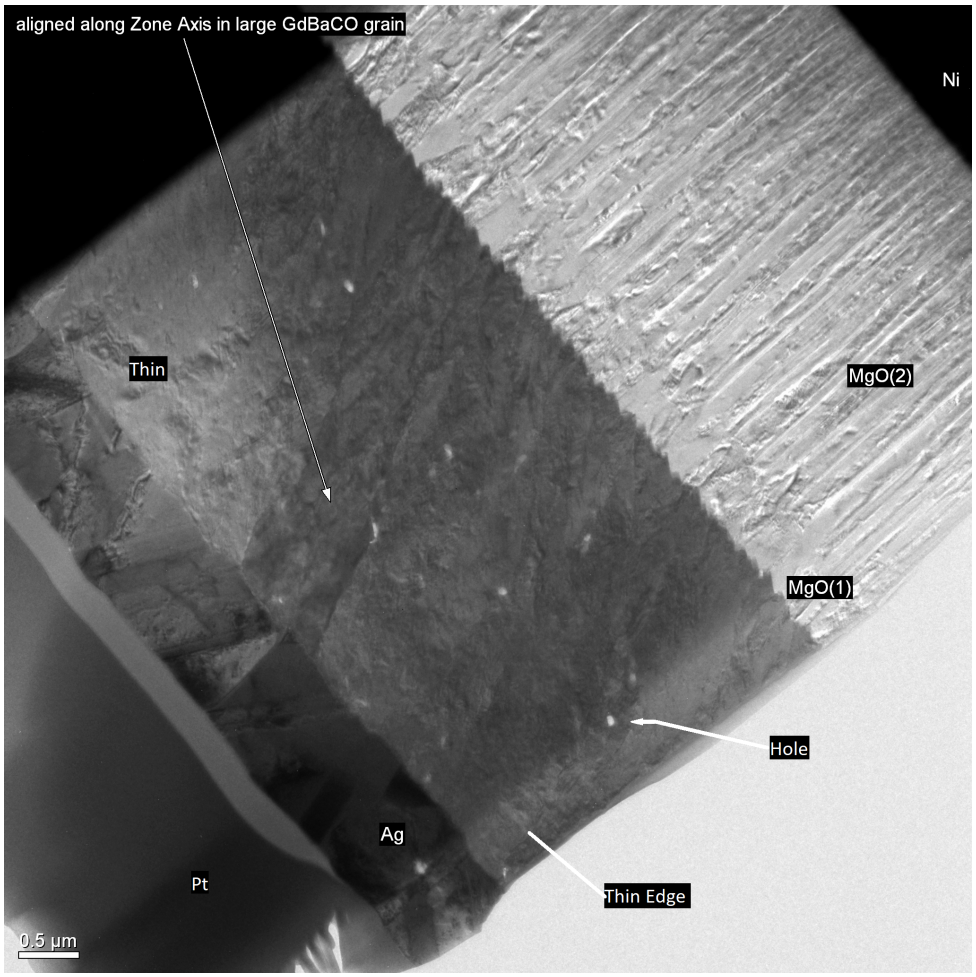


Figure 27: TEM CS image of the top part (exc. substrate) of the tape. Several interesting features are indicated. The image was aligned along the zone axis of a HTS grain.

these fringes in figure 28 the c-axis lattice parameter of the GdBCO unit cell can be determined. The spacing to the first spot in the FFT is 1.182 nm which is very close to the earlier mentioned value of 1.178 nm. However, the spacing to the second spot is 1.218 nm, this means that there are amorphous aspects in the layer since the two should of course be equal. This was also confirmed by several other lattice fringe images where the d-spacing also varied between the 1.14 and 1.174 nm showing more evidence of amorphous aspects. Furthermore, the growth direction of the c-axis of the HTS layer can also be obtained from the FFT as the amount of degrees to the x-axis. Several lattice fringe images were made and from these it was found that the angle varied between the 36 and 44 degrees (where 36 degrees is from figure 28). From the specifications as told in chapter 2 this angle should be around 30 degrees. Thus, the obtained results deviate quite a lot from that. There are several reasons for why this could occur, it could for instance be that there are certain regions in the tape where the growth angle is larger due to amorphous defects or stacking defects. Nevertheless it does definitely show that the GdBCO layer is inclined with respect to the substrate normal which is a result of taking over the angle from the ISD of the MgO(2) layer.

5.2 SEM Surface Characterization

To image the surface of the different top layers (Silver and GdBCO) and look at the roughness and morphology the SEM was used. Small rectangular samples of 6x6 mm were cut out using a laser cutter in order to reduce bending of the edges by mechanical cutting. Only the Secondary Electron Image (SEI) mode was used which was discussed in the last chapter. Furthermore, the SEM was operated with an accelerating voltage of 30kV and in many cases samples were inclined at 45 degrees to increase the electron yield and create better images. Also the spot size of the electron beam was varied between 18 and 30 depending on what was to be imaged, smaller features required a smaller spot size. To image the

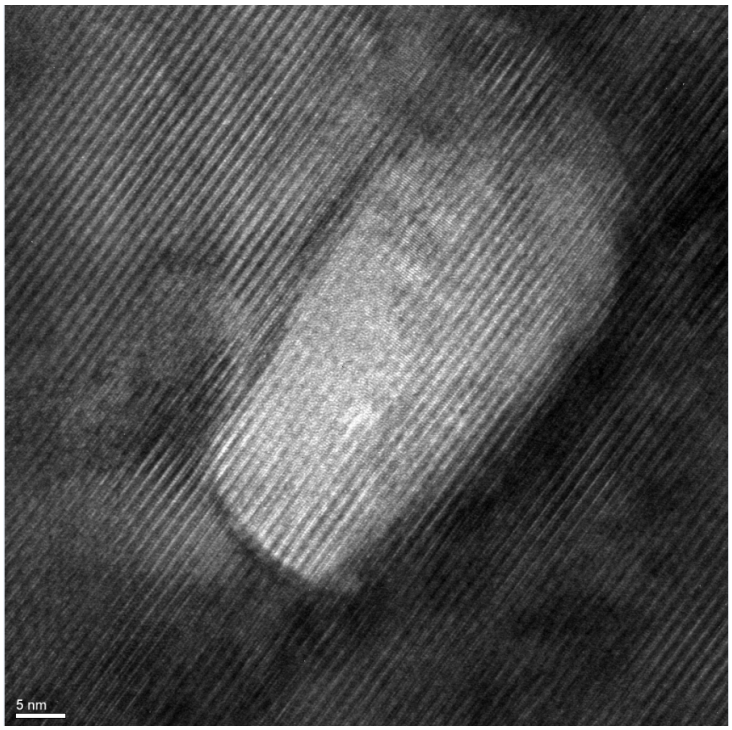


Figure 28: Lattice Fringes of the c-axis of the GdBCO layer, an amorphous region is chosen.

HTS layer the silver layer had to be etched away, the different approaches and results will be discussed later in section 5.2.2.

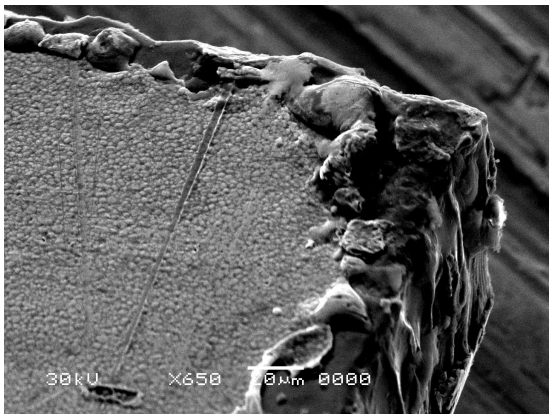
5.2.1 Silver Coating

The first goal when using the SEM was to image the surface of the silver coating to see whether its morphology would be suitable for microstructures. However, first the edges of the sample where inspected to see what the effect of the laser cutter was on the edges, this result can be seen in figure 29. In figure 29a the edge of the substrate side of the tape can be seen. In figure 29b the edge of the top side of the tape can be seen. Clearly visible from both images is that due to the laser cutting the edge of the sample is damaged. The laser of course heats up the sample near the edges and thus the structure is deformed there. In figure 29b one can also see deformations where the laser has made holes in the sample. Also several spots or droplets can be seen about 100 micrometer near the edges. Scratches are visible in both figures but they are not a result of the laser cutter. Further inward (more then a hundred microns), there is no effect visible of the laser cutting.

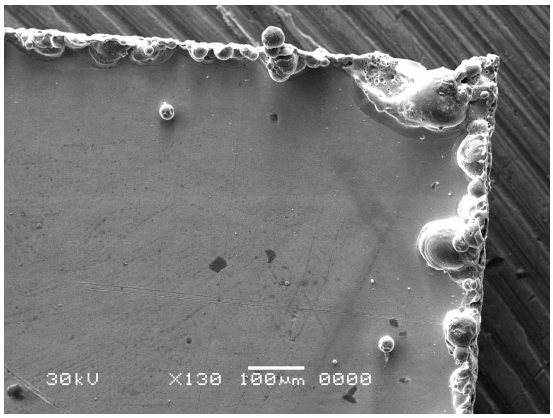
Furthermore, the surface of the silver coating was also imaged more inward such that there were no effects of the sample cutting influencing the surface. The results of these images can be seen in figure 30, one can immediately see in both figures that there are small, several microns large, clusters of silver. Furthermore, in figure 30a many small scratches are distinguishable and in figure 30b even a very wide scratch. Also in both figures larger deformations such as the large spot in figure 30b are abundant on the surface. Other images were also taken of the silver surface and these confirmed that large droplets, scratches and spots are abundant over the entire surface.

5.2.2 GdBCO Layer

To image the HTS layer which is made of the Gadolinium Barium Copper Oxide (GdBCO) compound, the SEM is used as well. However, first the silver coating has to be removed to image the surface of the HTS layer. In chapter 4.2 several methods for chemical etching were explained and these were used to etch away the silver coating prior to SEM imaging. Since, the method used to etch away can have effect on the structural integrity and surface of the HTS layer, each method with their results will be discussed. In order to differentiate between different layers a simple handheld Multimeter was used. Measuring the resistance of the silver layer would return a very low value, about $2 - 4\,\Omega$, the MgO layer is a strong insulator and measuring its resistance would give an overload (order of MΩ) for the multimeter. The



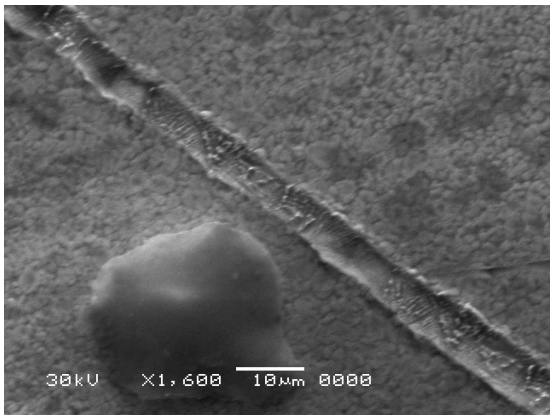
(a) Side view of edge of the sample cut out by a laser (Silver subtrate side).



(b) Top view of edge of the sample cut out by laser (Silver top side).

Figure 29: SEM images taken of the edge of the tapes cut with a laser cutter, to image the damage done during cutting.

(a) Image of the silver coating with many thin scratches and small clusters of silver.



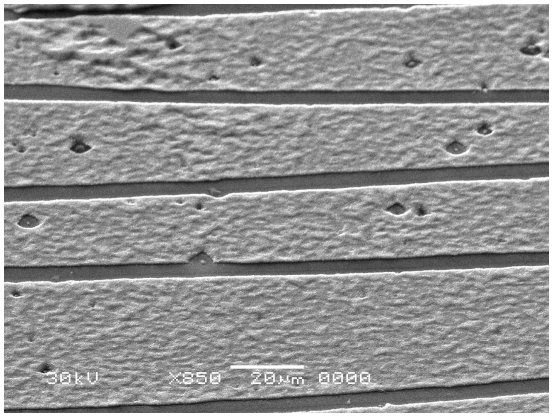
(b) Image of large spot and scratch on the silver surface.

Figure 30: SEM images of the silver coating which shows clusters of silver atoms, but also many scratches and other deformations.

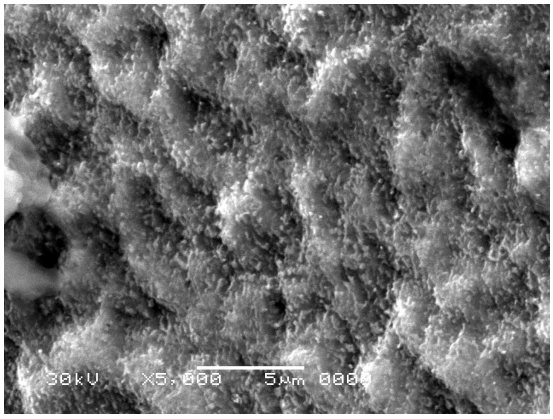
GdBCO layer is also an insulator but not as good as MgO therefore it would give a high but measurable resistance, in the order of kΩ.
First the use of the commercial Chromium etchant which also etches silver will be discussed. Then the Argon Ion Beam etcher will be used to see whether dry chemical etching gives better results. Lastly, a diluted solution of ammonia and hydrogen peroxide will be used.

5.2.2.1 Commercial Chromium Etchant First a commercial chromium etchant used in the fabrication of masks for lithography was used since next to chromium it can also etch silver and copper. The solution used is Ceric(IV)Ammoniumnittrate perchloric acid. To prevent it from etching away the copper in GdBCO the setup of figure 25b was used to clean the sample as quick as possible. The tape was put into the solution on a sample holder and after approximately 30 seconds of moving the holder up and down, the black GdBCO layer was visible. The sample quickly had to be cleaned using the three water beakers to make sure the etchant could not etch further into the GdBCO layer. The surface of the resultant HTS layer can be seen in the figure 31. In figure 31a trenches are visible which occur in the HTS layer after etching, also there are small holes where the etchant has also etched through the HTS layer. The trenches originate during the chemical etching process and start at the edges of the sample. This happens very quickly already and is probably due to the exposed side of the HTS layer where the etchant is able to etch into the CuO planes of the layer. In figure 31b a SEM image is taken of the surface of the HTS layer, visible is the sawtooth structure which results from the ISD process. Since the etchant etches the CuO faster then the rest of the compound it probably etches the GdBCO in a saw tooth manner,

which can be seen in figure 31b. Furthermore, very small speckles of HTS material are visible.



(a) Image of trenches which appear during the wet chemical etching process.



(b) Image of the surface of the HTS layer, visible is the saw tooth structure of the layer and speckles of small clusters of HTS.

Figure 31: SEM images of the HTS layer after wet chemical etching with the Commercial Chromium etchant.

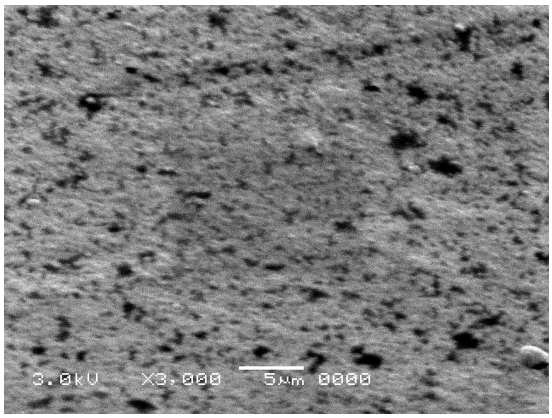
5.2.2.2 Argon Ion Beam Etcher The second approach to etch the silver layer away is a dry chemical etching method using argon ions in a beam. This technique was discussed in chapter 4.2.2 and the settings used are quickly summarized. In order to ensure good thermal contact between the sample and substrate holder, the sample was 'glued' to the holder with silver paste to ensure that the sample would not heat up. The process was done at ultra high vacuum (before argon gas inlet), the sample holder was inclined to 45 degrees to yield a higher etching rate and it was also rotated at 4 rounds per minute to correctly expose the entire sample to the beam. The argon gas flow was set at 5 mL per minute such that the operating pressure was $2.9 \cdot 10^{-4}$ mbar. Further settings regarding the beam, accelerator and discharge voltage and current are summarized in table 1.

Table 1: Settings used during the Argon Ion Beam etching process to etch an approximately one micron thick silver layer.

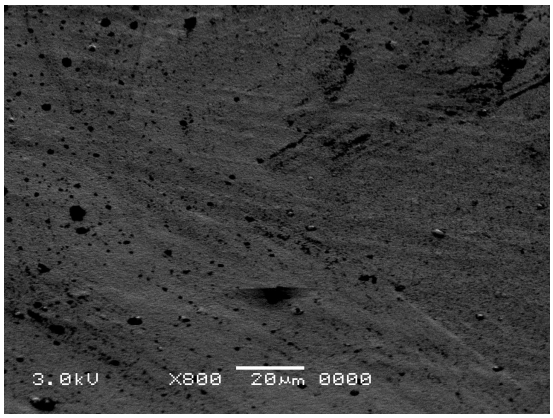
Setting	**Value (Unit)**	**Setting**	**Value (Unit)**
Beam Voltage	500 (V)	Filament Current	7.62 (A)
Beam Current	100 (mA)	Keeper Voltage	23.6 (V)
Accelerator Voltage	100 (V)	Neutralizer Current	125 (mA)
Accelerator Current	5 (mA)	Filament Current Limit	7.5 (A)
Discharge Voltage	50 (V)	Neutralizer Current Limit	5 (A)
Discharge Current	1.02 (A)		

The sample was irradiated for 35 to 40 minutes with these settings up untill the entire sample was black, meaning the HTS layer was exposed and the silver etched away. The resultant etching speed was estimated to be approximately 35 nm/min. After etching the sample was inspected using the SEM to see what the effect of argon ion etching is on the surface of the HTS layer. The results of this can be found in figure 32.
In figure 32a a close up of the surface is made. The image is not great due to the fact that the surface is extremely chaotic. However, this was expected since the high energetic argon ions bombard the surface and expell material wherever they land which is random. Therefore there are also many black spots, where more material is etched away then in the surrounding area. Furthermore, in figure 32b a more zoomed out surface image can be seen. Due to the fact that GdBCO is an insulator the image is very dark due to charge (electrons from the SEM) piling up in the sample. However, it is still visible that the surface is not very smooth, several large holes and islands can be seen which are a result of the random etching of the argon ions.
Also since during the argon etching it occurred that at certain spots the silver was already etched away, but not at other places. Since the silver has to be completely removed this meant that these spots (where

the silver was already removed) were now exposed to the argon ions and thus the ions start to etch GdBCO away as well. Luckily the etching speed for a material such as GdBCO is much lower, the etch rate for YBCO was around the 4 nm/min. So this is not terrible, but it is probably why there are so many holes visible on the SEM images.



(a) Close up of the HTS surface, many holes are visible which are a result of random argon etching.



(b) Larger image where holes and islands in and on the GdBCO layer are visible.

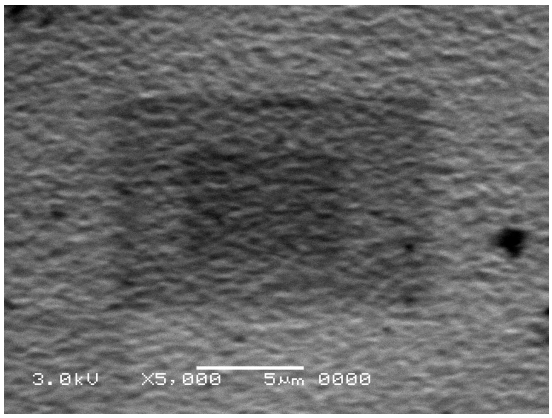
Figure 32: Two SEM images of the HTS surface after the argon ion beam etching process.

5.2.2.3 Ammonia Hydrogen Peroxide Etchant The third approach used to remove the silver layer is also a wet chemical etching approach, but this time with a solution of ammonia and hydrogen peroxide to etch away the silver. The ammonia peroxide solution is highly selective since it only etches the silver and does not effect the cuprate HTS layer. The ammonia peroxide solution was diluted to a 14%/14% (NH_4OH/H_2O_2), which meant that 15 mL ammonia was needed (bottle NH_4OH 28%), 13.5 mL hydrogen peroxide (bottle H_2O_2 31%) and only 1.5 mL of distilled water to make a solution of 30 mL in which the samples can be etched. Again the sample need to be cleaned and dried such that there are no chemicals left on the sample.
The surface of the sample was investigated with the SEM to see whether the ammonia peroxide solution was truly selective in only affecting the silver layer and not the HTS layer. The results of this SEM imaging can be seen in figure 33. Again in both figures there are rectangles which are darker on the images, this is due to the fact that GdBCO is an insulator. Due to it being an insulator it gets charged up by the electrons from the SEM beam and the excess charge cannot be drained due to the insulating behaviour. In figure 33a a larger image of the surface is shown, where the black squares are visible, and in figure 33b a more magnified image can be seen. In both cases it is clearly visible that the surface has some kind of hilly morphology which could still be a result from the ISD process, but can also just be because of the deposition of the GdBCO. Furthermore, these small hills are much smaller then the ones observed in figure 31, these features are in the order of hundred nanometers instead of microns.

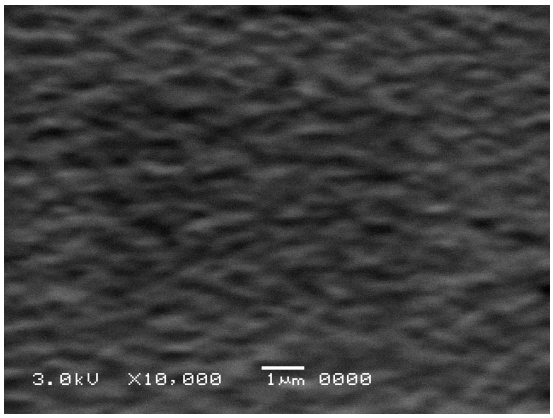
5.3 Conclusion

In the introduction of this chapter I stated that the goal of the chapter and more specifically the investigation of the surface and structure of the tapes was to determine which layer, the silver or GdBCO, was more suitable for micro structuring.

From the results of the TEM cross-section images the thickness of the silver layer can be estimated to be approximately one micron and it could be seen that it was polycrystalline. Furthermore, the thickness and cross-sectional structure of the other layers could also be seen and they agree with the specifications as given by the tape producer THEVA for this specific model. Also from the lattice fringes and FFT it could be concluded that the GdBCO was correctly deposited along the c-axis with roughly the corresponding lattice parameter however the angle of the growth direction was much larger then the prerequisites given by THEVA.
From the SEM surface characterization measurements a conclusion can be drawn regarding the morphology and suitability of the silver and GdBCO layer for micro structuring and regarding the preferred



(a) Larger images of the surface morphology of the GdBCO layer. A hilly morphology is visible.



(b) Close up of the surface where the hilly structure is more visible.

Figure 33: SEM images of the HTS layer after wet chemical etching using a NH_4OH/H_2O_2 solution.

etching method for removal of the silver from the tape. Firstly, it was quite clear from the results of figure 30 that the surface of the silver coating was extremely rough and contained many defects such as scratches and tens of micron large droplets of silver. In the case of the GdBCO layer the surface as obtained after Argon ion etching (figure 32) and after NH_4OH/H_2O_2 etching (figure 33) is much more smooth and has less defects. Therefore it can be concluded that the silver should be etched away and that patterning should occur in or on the HTS layer. Furthermore, the use of the commercial chromium etchant was not wanted since it gave rise to trenches and deformed the surface. The etching method preferred is the wet chemical etching using NH_4OH/H_2O_2 since it is more selective then the Argon ion etching and does not etch away parts of the GdBCO layer.

6.

Hall Bar Fabrication and Electronic Characterization

The goal of this research was to determine whether the 2G HTS tapes produced by THEVA could be used in the fabrication of superconducting electronics. Therefore in this chapter the techniques for microstructure fabrication as explained in chapter 4 will be used to pattern and etch out small structures in the HTS layer. The initial aim was to build transmission line structures on the tapes which would be several centimeters long. Unfortunately suitable masks for these structures were not present in the cleanroom and since cleanroom usage was already limited it was chosen that the fabrication of a new mask would cost too much time. However masks with Hall bar structures could be used and these were already made. Hall bars are six-terminal structures, where two terminals serve as current terminals and four as voltage terminals. This meant that due to the longitudinal placement of voltage terminals, longitudinal resistance measurements could be performed and hence transport properties could be measured.
In this chapter the fabrication of three Hall Bars with different dimensions will be discussed using photolithography and wet chemical etching. Also to see whether these structures would still possess the same superconducting properties as the tapes transport measurements regarding the critical current should also be performed, unfortunately this was not possible and several reasons why will be explained.

6.1 Design, Fabrication and Characterization

Due to the fact that there were already several masks for Hall bars in the cleanroom it was chosen to create several Hall bars with different dimensions to see how they would survive the fabrication process. A schematic image of the geometry of a Hall bar can be seen in figure 34. Hall bars are normally used to measure the quantum Hall effect, to measure this a magnetic field has to be applied perpendicular to the geometry i.e. coming out of the page. When applying such a high magnetic field edge states, which carry current from left to right are present on one side of the bar (for instance on the side of contacts 3 and 4) and states carrying current from right to left are on the other side. Due to there being almost no overlap

between these states back scattering is not possible even though impurities are present [32]. However, in the case of this research no magnetic field will be applied and the Hall bar will be used to measure the longitudinal resistance of the GdBCO Hall bar to determine the critical current of the sample, therefore the Hall bar is basically just a strip with contacts and leads. A current will be supplied to the bar at contact 1 and contact 2 will serve as a drain (ground), the other contacts are voltage contacts and they will be used to measure the resistance of the sample at varying current.

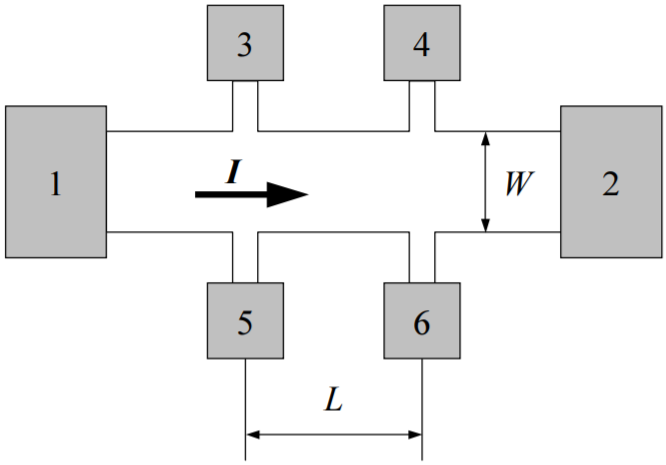


Figure 34: Schematic figure of Hall bar geometry indicating the width (W) and length (L) of the bar. Contacts 1 and 2 are current pads and Contacts 3, 4, 5 and 6 are voltage pads (Figure from [33]).

In this section first the different Hall bar geometries which were designed will be discussed. Afterwards the process of fabricating these structures using lithography and wet chemical etching with NH_4OH/H_2O_2 and H_3PO_4 will be explained. Last but not least the procedure for experiments regarding the measuring of the transport properties of the 100 micron wide Hall bar will be discussed.

6.1.1 Hall Bar Design Geometries

Since it is interesting to see what sizes of structures one can pattern and successfully etch using wet chemicals three different bars would be patterned into the GdBCO layer. The bars would vary in both the width of the bar itself and the length between the longitudinal voltage contacts. In table 2 the three geometries are numbered and their respective width and length of the Hall Bar are given, where the width and length correspond to W and L respectively in figure 34. Normally for the contact pads one would deposit them using a thin layer of gold. However, it was chosen to protect the silver layer of the tape on top of the contacts during the lithography and thus to use those as the contact pads. Of course for the larger bars the contacts were also larger, since they would have to supply more current.

Table 2: Geometry sizes of the three different Hall bars designed.

Hall Bar	**Width** (μm)	**Length** (μm)
#1	400	800
#2	100	400
#3	10	400

6.1.2 Patterning and Etching

The three Hall bar geometries were all on the same mask and therefore they could all be patterned at the same time during the lithography. The patterning and etching of the geometry will first be discussed and afterwards the patterning and etching of the contacts.

6.1.2.1 Hall Bar Fabrication Droplets of photoresist Olin 906-12 were placed on the sample and spincoating of the resist for 45 seconds at 4000 RPM ensured that the resist would be evenly spread

across the sample. Olin 906-12 is a positive resist and thus becomes weaker when exposed to light, also the thickness after spincoating was approximately 1.7 micron to be able to pattern finer structures. The sample with resist was baked at 90 degrees Celsius for one minute on the hotplate prior to light exposure. Using the mask the sample was exposed to light for 6 to 7 seconds in a $10\,\mathrm{mV \cdot cm^{-2}}$ UV iLine lithography device, which has a Hg lamp with wavelength 365 nm. After light exposure the sample, with now weakened spots, was developed in OPD 4262 for one minute.

Now the geometry is protected by the approximately 1.7 micron thick resist, but the rest is unprotected and can be etched away. The solution of NH_4OH/H_2O_2 (14%/14%) was used to etch away the unprotected silver layer, again the set up of figure 25b is used. The sample was dipped in the solution for approximately 3 to 5 seconds and subsequently quickly washed with distilled water and dried with nitrogen gas. Now the remaining unprotected GdBCO had to be etched away such that the underlying MgO layer would be visible. To etch away the GdBCO a solution of phosphoric acid (10% H_3PO_4) would be used in the same set up as used earlier. The sample on the white holder was dipped up and down the solution for approximately 75 seconds until the MgO layer, which has an oily shine was visible. The sample was then quickly washed in several washing beakers with distilled water and also dried to make sure there were no chemicals on the sample anymore. In order to remove the left over photoresist from the surface the sample was put in an acetone bath and stirred by an ultrasonic cleaner (Branson 2510) until the resist was dissolved. After coming out of the bath the sample was cleaned with ethanol and dried with nitrogen gas.

6.1.2.2 Contact Fabrication For the fabrication of the contacts a different approach had to be used. A mask which is normally used for lift off had to be used meaning that thus a negative resist had to be used during lithography, i.e. one that strengthens by exposure to light. The resist used is nLof 2035 which is a negative resist and has a thickness of 3.5 microns. Several droplets of nLof 2035 were spincoated at 4000 RPM for 45 seconds such that the resist was spread out and reached a fairly uniform thickness of about 3 microns. It was then baked at 110 degrees Celsius for one minute on the hotplate. The resist was then exposed to the same $10\,\mathrm{mW \cdot cm^{-2}}$ iLine Hg lamp (365 nm) for 15 seconds. A post bake was performed also at 110 degrees Celsius for one minute on the hot plate, this is done to strengthen the protecting resist. The sample was then developed in OPD 4262 for two minutes to remove resist from places where it was not needed.

The contact pads (voltage and current) of the Hall bars are now protected and the excess silver could be etched away with the NH_4OH/H_2O_2 (14%/14%) solution. The sample was placed on the holder and dipped in the solution for about 3-5 seconds and then quickly washed in distilled water and dried with nitrogen gas. To remove the resist from the sample the sample was placed in an acetone bath which was placed in an ultrasonic cleaner (Branson 2510) for 30 seconds to completely remove the resist from the surface. The sample was then cleaned with ethanol and dried with nitrogen gas.

6.1.3 Electronic Characterization

It was chosen to only do electronic measurements for the 100 micron wide Hall bar. This was because if the critical current density is of the order of $10^6\,\mathrm{A \cdot cm^{-2}} = 0.01\,\mathrm{A \cdot \mu m^{-2}}$ then for a 100 by 3 micron bar the critical current would be approximately between 3 and 4 A. In the case of the 400 micron wide bar this would reach 12 to 16 A which would be too much current for the copper wiring and wire bonds. Unfortunately due to a limit in time and several technical problems it was not possible to do the electronic characterization of the 100 micron Hall bar. The approach as discussed in chapter 4 was partially done and the results and difficulties will be discussed.
The copper wires with surrounding insulation, about 2 millimeter in diameter, were soldered to the PCB and the sample was placed on the PCB. However, wire bonding from the silver contact pads to the copper strips on the PCB did unfortunately not work. This was because the bonds would either not stick on the silver or when they would stick they would break due to high tension, since the bonds were quite long. However, if this would have worked then the copper wires would have been made longer by soldering them to longer wires which would be connect using bolts to the nanovoltmeters and a power supply capable of delivering 5A. The PCB with sample and connecting copper wires would be lowered into a liquid nitrogen bath at 77K and the voltage as measured by two longitudinal voltage probes would be measured whilst varying the current in a range of 2 to 5 A to give the current voltage characteristics and hence determine the critical current which would be in between 3 and 4 A.

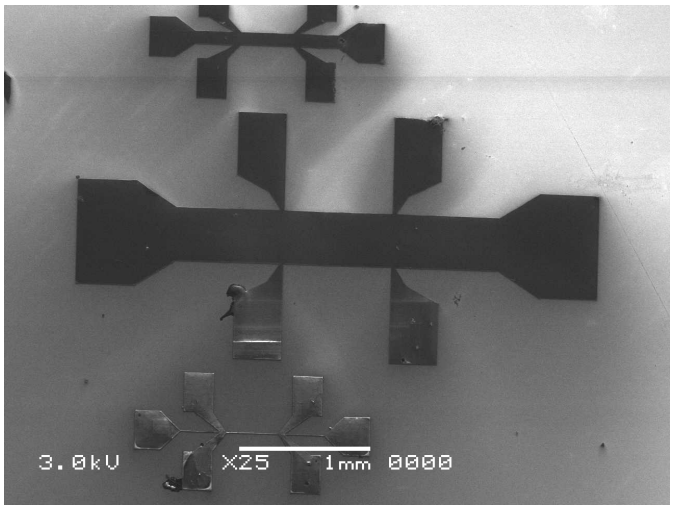
6.2 Results and Discussion

In the first section the results of the imaging with the SEM of the fabricated Hall bars will be shown to see them 'evolve' during the fabrication process and to see if anything strange happens during the fabrication which could lead to damage. Furthermore, results will also be shown regarding the effect of underetching due to the wet chemical etching on the width of the 100 micron bar. Unfortunately no measurements could be done regarding the critical current. However, several problems occurred which will be discussed.

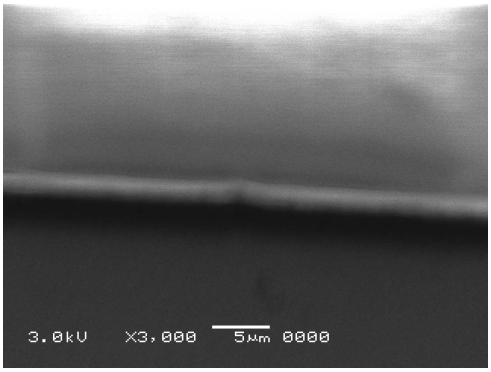
6.2.1 Microscopy Analysis of Hall Bars

The SEM was used to image the Hall bars during and after the fabrication process, to investigate whether the fabrication process worked sufficiently. The three most important steps and the results from the SEM will be discussed in this section. First the SEM will be used to investigate the bars after the top silver layer was removed and the Hall bars were protected with resist. Then they will be imaged after the HTS layer is etched away with phosphoric acid and lastly after the contacts are correctly etched onto the bars.

6.2.1.1 Silver Layer Removal In figure 35 two images are shown which nicely summarize the results of looking at the bars after the silver removal. In figure 35a the three Hall bars are imaged together in one figure where one can easily see the difference in size. Also the geometries look sharp and little to no impurities can be seen on the surface. In figure 35b a SEM image was taken at 45 degrees inclination to "look" under the resist and silver layer and to see whether the ammonia hydrogen peroxide also underetches. There is a small shadow visible and the edge of the layer is brighter which are both indications of that there is underetching happening. However, it looks like it is not that extreme and as expected the ammonia hydrogen peroxide solution under etches only slightly.



(a) Image of the three Hall Bar geometries.



(b) Image of underetching happening in the Ag layer under the photoresist layer.

Figure 35: SEM images of the geometries and surface of the sample after the unprotected silver layer was etched away with the NH_4OH/H_2O_2 solution.

However, upon closer inspection of the 100 micron wide Hall bar several impurities could be seen through the resist layer, see figure 36 for the results. Several 'scars' are clearly visible on the silver layer and there is what appears to be a large 50 micron wide hole at the beginning of one of the current pads. It is difficult to say how these scars and other defects have occurred, but it is probably due to the ammonia solution which is apparently able to etch away material on some places beneath the resist, since the scars all originate at the edges of the bars. The large hole could have been already present prior to spincoating. Or there could have been a dirty spot on the silver ensuring that the resist could not correctly protect the layer.

6.2.1.2 GdBCO Layer Removal Since the GdBCO layer removal takes much longer it was expected that this process would have much more influence on the quality of the surface and of the geometries. In figure 37 two images are again shown of the bars after etching. In figure 37a all three bars are

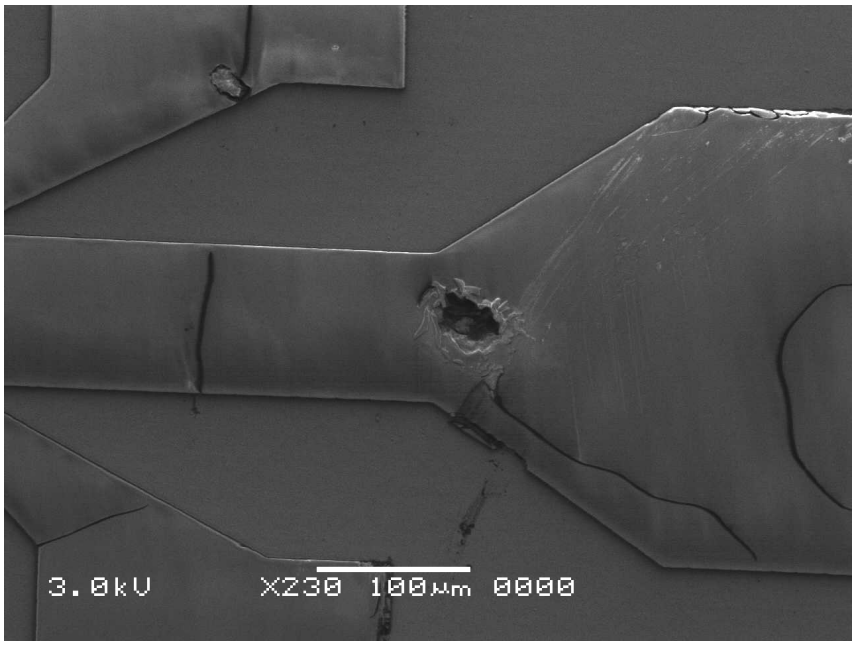
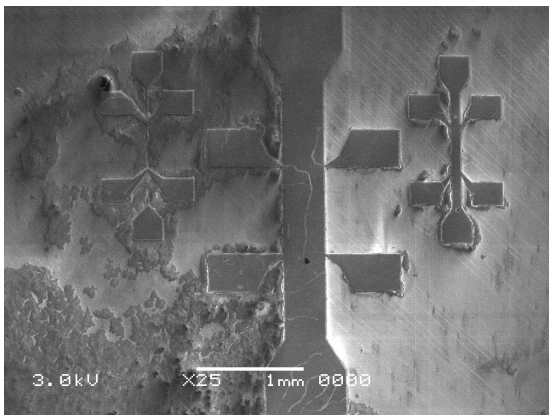
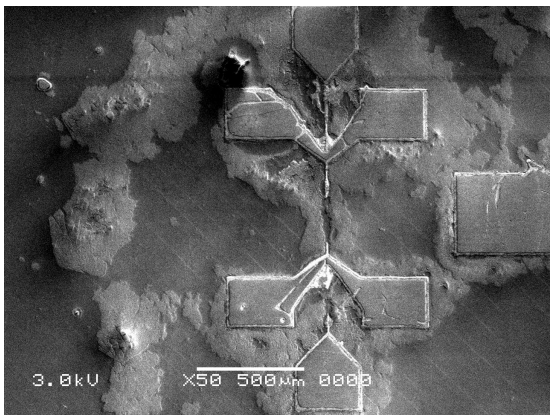


Figure 36: Impurities on the surface of the 100 micron wide Hall bar. Several scars are visible which originate at the edges and are probably a result of the chemical etching. Also a large hole is present at a current pad.

visible, in this figure it is also much clearer that the scars which appeared during silver etching are still there, probably since the phosphoric acid can also flow into those scars and etch further into the bar. Furthermore, etching of the GdBCO layer takes much longer and since after 70 seconds the sample had to be taken out, to reduce the amount of underetching, there are still stains of GdBCO visible (in the bottom left). Unfortunately the 10 micron wide Hall bar did not survive the etching process with phosphoric acid, in figure 37b the remnants of the bar are still visible. The reason why this smaller bar did not survive is because underetching by the phosphoric acid is quite large and thus the bar is thinned and thinned until it breaks. Surrounding the broken bar the stains of GdBCO are also still visible.
SEM images were also taken of the edges of the bars after etching using again an inclined approach to look into the underetching. These images confirmed that just like figure 35b that under etching occurred only it was much more extreme this time.



(a) Hall Bar geometries after phosphoric acid etching. Stains of leftover GdBCO are visible and the scars on the bars as well.

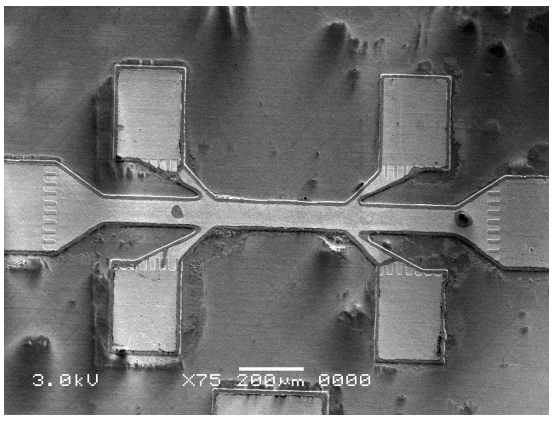


(b) Hall bar with width 10 micron is completely broken during the etching process due to under etching of the acid.

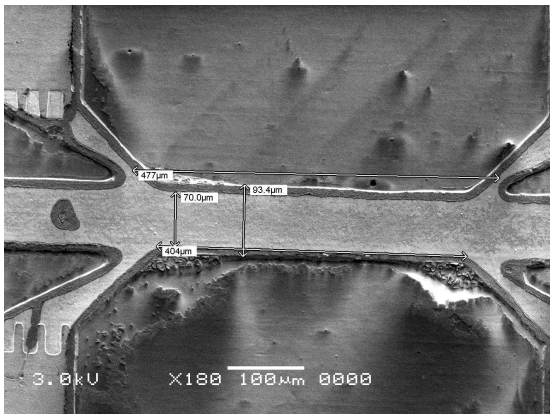
Figure 37: SEM images of the Hall bars after phosphoric acid etching, which has a significant impact on the Hall bars.

6.2.1.3 Contact Etching The etching out of the contacts was again done with the ammonia hydrogen peroxide solution. From the earlier use of this solution we know that it under etches slightly and therefore it is again important to do the etching as quickly as possible. In figure 38a a SEM image of the completely fabricated 100 micron wide Hall bar can be seen. The contacts are clearly visible, since they are slightly darker and have a tooth like interface with the bar. Two spots/holes are visible on the bar and near all contacts apart from the top right one there are scars. These could pose problems with measuring the longitudinal voltage, since there could arise resistance because of the impurities.
In figure 38b a more close-up image of the 100 micron Hall bar can be seen, in which also several dimension of the width and length have been measured. From these measurements it is instantly clear that under etching by the phosphoric acid and also by the ammonia hydrogen peroxide solution has a huge effect on the width of the bar. We already now that the 10 micron bar did not survive the chemical etching process. Looking at the measured width of the light gray area of the bar one finds that the width in 70 microns after the fabrication process. This would mean that due to under etching the bar has been effectively reduced by 30 microns during the etching, which is by all means not a small amount. Furthermore, the length of the bar is still roughly what it was on the mask, approximately 400 microns. The 400 micron bar is not shown here, but after measuring the width of that bar it was also clear that it had been reduced from a width of 400 to about 375 microns. However, since this bar is much larger the effect is much less of a problem then for the 100 micron. However, the 400 micron bar showed much more scars across the bar and on the contacts and was thus not deemed suitable for transport measurements.

Furthermore, surrounding the bar, contacts and leads a dark gray/black edge is visible. When looking with an inclination at this edge it looked like the light gray area was on top of the black area. So it is not quite clear how this could occur, it does however happen during the phosphoric acid etching. It could be that this part is heavily effected by the etching and is therefore not superconducting anymore thus the bar is effectively thinned, by about 30 microns.



(a) Geometry of the 100 micron wide Hall bar. Silver contacts are clearly visible, on the voltage and current pads. Furthermore, several scars and spots on the bar are visible.



(b) Close up of the bar itself. The width was measured and it is clear that the width is drastically reduced by the etching process.

Figure 38: SEM images of the 100 micron wide Hall bar after the contacts had been correctly etched.

6.2.2 Critical Current Measurements

As said earlier the eventual measurement of the current/voltage behaviour of the Hall bar could not be done due to time- and several technical issues. The wire bonder which was supposed to connect the silver voltage and current pads to the copper strips on the PCB, but it could not form the bonds and in the cases were a bond would stick it would only last for a short time and would eventually snap due to tension. I am not quite sure why the bonds would not stick however I think that it could perhaps be that the power and time of the thermosonic pulse have to be optimized. Furthermore, the bonds had to be quite long, about 8 millimeters, and for an inexperienced user (as me) that was quite a challenge. However, when looking at figure 38a it would have been interesting to see whether measurements would actually work. As you can see there are many scars and spots visible near the voltage and current pads which could have resulted in a lot of resistance and could have made the results unusable.

6.3 Conclusion

Even though it was not possible to eventually measure the electrical behaviour of the Hall bars fabricated I believe that an interesting approach has been made to fabricate structures on the tapes.
Patterning using photolithography on the silver showed that high resolution structures could be created. The use of wet chemical etching with NH_4OH/H_2O_2 (14%/14%) to etch away the silver seems like a very reliable and safe approach and achieved in removing the unprotected silver without affecting the structure to much. However, whether using silver as the contact layer is reliable remains questionable due to the appearance of scars and holes in the silver layer which in turn results in the same defects in the GdBCO layer. On the SEM images it was already visible that the silver is very scratched and has many small defects. Therefore, it would perhaps be better to remove the entire silver layer with NH_4OH/H_2O_2 and directly do lithography and patterning on the GdBCO layer and use a sputtering machine to create for instance gold contacts on the surface. The etching of the GdBCO with H_3PO_4 (10%) is effective to say the least, it etches rapidly through the layer but also under etches quite significantly and hence the width of the bar is reduced by 30 microns. However due to the thickness of the GdBCO layer (3 micron) it is not possible to use dry chemical etching since it would take to long. Perhaps a more diluted solution of H_3PO_4, about 5%, will give more control of the etching process and eventually results in finer structures. The use of the H_3PO_4 (10%) etchant also gave a certain minimum size one could structure, since the 10 micron bar did not survive the process. Due to the fact that both widths of the 400 and 100 micron bars were reduced with 30 microns, structures should be in the order of 100 microns if they wish to effectively survive.
In conclusion, Hall bars with widths of 100 and 400 micrometers have been fabricated using an easy and quick process. It is thus possible to create small microstructures on the tapes which function as electronic structures. However, there are limitations regarding the size due to under etching effects from chemical etching.

7.

Conclusion

The goal of this bachelor thesis research was to investigate what the possibilities and limitations are concerning the use of 2G-HTS tapes in the fabrication of superconducting electronic devices. To try to answer this research question several sub-questions were formulated and the research was performed according to these questions. The most important results of the research performed according to these sub-questions is stated below.

During the literature study concerning the steps and considerations in the fabrication process of the 2G-HTS tapes made by THEVA it was found that the ISD process is used to create a MgO substrate buffer layer with a biaxial texture onto which the GdBCO layer is deposited. This is done to create a HTS layer with a biaxial texture which is imported since it reduces the losses to the critical current density due to high-angle grain boundaries. Furthermore, this ensures that the HTS layer in the tapes has a quasi-monocrystalline crystallographic direction which means that high critical current densities in the order of $10^6\,\mathrm{A}\cdot\mathrm{cm}^{-2}$ (77K and Self-Field) can be achieved. Also, since the GdBCO layer takes over the inclined c-axis (with respect to the substrate normal) growth direction from the ISD-MgO layer, the CuO are inclined with respect to the substrate. This means that there is an anisotropic behaviour of the critical current density, i.e. the longitudinal critical current density is higher then the transverse critical current density. This is an important consideration when designing 2D electronic structures on the tapes, since this anisotropy is thus also present in the electronic structures.

When investigating superconducting electronics of the RSFQ family it became clear that this was an interesting and promising branch of superconducting electronics. However, since there are still some technical difficulties with implementing HTS materials in RSFQ electronics due to higher noise current at 77K and difficulties in producing reliable structures with HTS materials it remains questionable when it could be investigated if the tapes are suitable candidates. Nevertheless creating transmission line structures, like the passive microstrip, on the tapes is an interesting application. Since they are produced at very long lengths it could be possible to create long transmission lines which can transfer signals over large distances without dissipating energy. Furthermore, the use of transmission lines in Artificial Neural

Networks is important to mimic behaviour of the axon. If it is possible to create reliable and long transmission lines on the tapes then one can look into the possibility of integrating these into ANNs.

During the experimental characterization of the tapes several interesting results were discovered. First of all the TEM analysis showed that in the cross-section image (figure 27) of the tape it was clearly visible that the thicknesses of the layers corresponded to what THEVA stated. Furthermore, it was also confirmed using lattice fringes (figure 28) that the c-axis of the GdBCO layer was inclined with respect to the substrate normal as was expected. However, the inclination angle was much larger (37-44 degrees) then the approximate 30 degrees that THEVA specified. This could be a result of amorphous aspects in the layer or growing defects. Furthermore, inspection using the SEM of the surface morphology showed that the silver layer was not suitable for micropatterning (figure 30). There were many scratches and large droplets of silver visible on the surface. Several etching methods were proposed to remove the silver layer and of those the use of the chemical NH_4OH/H_2O_2 (14%/14%) proved to be the most reliable, since using argon ions made the GdBCO surface to chaotic (figure 32) and the chromium etchant created trenches in the GdBCO layer (figure 31). The resultant GdBCO layer after etching with ammonia hydrogen peroxide showed a hilly morphology. However, variations were only in the order of several hundreds of nanometers (figure 33), which when creating structures in the range of ten of microns is not terrible.

Hall bars were patterned and etched into the GdBCO layer using photolithography and etching with wet chemicals NH_4OH/H_2O_2 (14%/14%) and H_3PO_4 (10%). Three bars were patterned and etched out with varying widths as 10, 100 and 400 microns. The silver coating surrounding the tapes was used on the top to function as contacts and was thus protected with resist, the other silver was etched away with the ammonia hydrogen peroxide solution. After etching it could be seen that the solution underetches slightly (figure 35b), but there appear scars in the silver layer which are a result of the solution etching faster at certain places (figure 36). The unprotected GdBCO was etched away with a H_3PO_4 (10%) solution, the phosphoric acid etches isotropically and hence underetching was a large effect. Due to this the 10 micron wide bar did not survive the fabrication process and both the 400 and 100 micron bars were thinned by approximately 30 microns (Figures 37b and 38b). It is thus advised to use a more dilute solution of phosphoric acid or another chemical such that there is more control over the etching process. Contacts were then again etched out with the ammonia hydrogen peroxide solution and the resultant 100 micron wide bar can be seen in figure 38a. Unfortunately electronic characterization measurements could not be performed, but an approach to do these measurements is outlined in C4.3 and C6.2.2. However, two 400 and 100 micron wide Hall bars were successfully created and hence creation of small microscale electronic structures is definitely possible on the tapes. Difficulties lie in etching away the thick layer of GdBCO due to underetching phenomena when using wet chemicals and it is advised to remove the entire silver layer prior to creating structures and sputter the contacts later on the structure to remove the effect of the scars.

To conclude, there are definitely possibilities to use the 2G-HTS tapes to create electronic structures and hence use them in the creation of superconducting electronics, the creation of several microscale Hall bars in this project is proof of that. However, there are several limitations of which the thickness of the GdBCO layer is probably the most important one. Since this layer is 3 micron thick etching has to be done using wet chemicals and hence there is enough time for the etchant to underetch. This results in that the size of structures which one can create is limited by the amount the chemical underetches, which is quite a lot. However, more research into this problem could result in a better and more reliable etching procedure which in turn will give better structures. Nevertheless I believe that there are definitely possibilities and a follow-up to this project should be able to delve deeper into solving problems which arose during this thesis. I still believe that the use of the tapes in the creation of transmission line networks either in ANNs or in other applications of superconducting electronics is an interesting follow-up topic for further research.

8.

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Bibliography

[1] D. van Delft en P. Kes. The Discovery of Superconductivity. *Europhysics News*, 63(1):21 – 25, 2011. doi: 10.1051/epn/2011104.

[2] R. Bhattacharya and M. P. Paranthaman. *High Temperature Superconductors*. Wiley, 2010. ISBN 978-3-527-40827-6.

[3] M. Eistere, S. H. Moon, and H. C. Freyhardt. Current developments in HTSC coated conducters for applications. *Superconductivity Science and Technology*, 29(6), 2016. doi: 10.1088/0953-2048/29/6/060301.

[4] Y. M. Lu, C. B. Cai, Z. Y. Liu, Y. Q. Guo, H. B. Jiang, Y. J. Zhang, M. J. Li, F. Fan, C. Y. Bai, Q. Lu, W. Z. Dou, and W. Yang. Advance in Long-Length REBCO Coated Conductors Prepared by Reel-to-Reel Metalorganic Solution and Ion-Beam-Assisted Deposition. *IEEE Transactions on Applied Superconductivity*, 29(5):1–5, 2019. doi: 10.1109/TASC.2019.2910021.

[5] A. Goyal. *Second-Generation HTS Conductors*. Kluwer Academic Publishers, 2005. ISBN 978-0-387-25839-3. doi: doi.org/10.1007/b106635.

[6] Y. Iijima, N. Tanabe, O. Kohno, and Y. Ikeno. In-plane aligned YBaCuO thin films deposited on polycrystalline metallic substrates. *Applied Physics Letters*, 60(6):769–771, 1991. doi: 10.1063/1.106514.

[7] F. Tang, T. Parker, G. C. Wang, and T. M. Lu. Surface texture evolution of polycrystalline and nanostructured films: RHEED surface pole figure analysis. *Journal of Physics D: Applied Physics*, 40:427 – 439, 2007. doi: 10.1063/1.2403916.

[8] M. Ohring. *Materials Science of Thin Films: Deposition and Structure*. Academic Press, 2nd edition, 2002. ISBN 978-0-12-524975-1.

[9] G. Sipos, B. Utz, W. Schmidt, H.W. Neumueller, and P. Mueller. Investigation of buffer layers for ybco coated conductors. *Physica C: Superconductivity*, 341-348, Part 3:1457 – 1458, 2000. ISSN 0921-4534. doi: 10.1016/S0921-4534(00)01031-5.

[10] THEVA Pro-Line HTS Wire: General Properties. THEVA Dünnschichttechnnik GmbH ,`https://www.theva.de/wp-content/uploads/2018/05/171218_THEVA_Broschuere_Pro-Line_generalproperties.pdf`, December 2017.

[11] W. Prusseit, C. Hoffmann, R. Nemetschek, G. Sigl, J. Handke, A. Lümkemann, and H. Kinder. Reel to Reel Coated Conductor Fabrication by Evaporation. *IEEE Transactions on Applied Superconductivity*, 16(2):996–998, 2006. doi: 10.1109/TASC.2006.873263.

[12] R. Semerad and W. Prusseit. High Temperature Superconducting Tape Conductor Having High Critical Ampacity *(German)*. WIPO (PCT), February 2012. WO 2012/013415 A1.

[13] W. Prusseit, M. Bauer, V. Grosse, R. Semerad, G. Sigl, M. Dürrschnabel, Z. Aabdin, and O. Eibl. Working Around HTS Thickness Limitations – towards 1000+A/cm – Class Coated Conductors. *Physcis Procedia*, 36:1417–1422, 2012. doi: 10.1016/j.phpro.2012.06.146.

[14] S. Choi, J. Lee, G. Shin, J. Lee, G. Hong, S. Moon, and S. Yoo. Characteristics of High-J_c GdBCO Coated Conductors Fabricated by the RCE-DR Process. *IEEE Transactions on Applied Superconductivity*, 23(3), 2013. doi: 10.1109/TASC.2012.2234814.

[15] M Lao, J Bernardi, M Bauer, and M Eisterer. Critical current anisotropy of GdBCO tapes grown on ISD–MgO buffered substrate. *Superconductor Science and Technology*, 28(12), 2015. doi: 10.1088/0953-2048/28/12/124002.

[16] M. Lao, J. Hecher, M. Sieger, P. Pahlke, M. Bauer, R. Hühne, and M. Eisterer. Planar current anisotropy and field dependence of j_c in coated conductors assesed by scanning Hall probe microscopy. *Superconductor Science and Technology*, 30(2), 2016. doi: 10.1088/1361-6668/30/2/024004.

[17] I. I. Soloviev, N. V. Klenov, S.V. Bakurskiy, M. Y. Kupriyanov, A. L. Gudkov, and A. S. Sidorenko. Beyond Moore's technologies: operation principles of a superconductor alternative. *Beilstein Journal of Nanotechnology*, 8:2689–2710, 2017. doi: 10.3762/bjnano.8.269.

[18] K.K. Liharev. Superconductor Digital Electronics. *Physica C: Superconductivity and its Applications*, 482:6–18, 2012. doi: 10.1016/j.physc.2012.05.016.

[19] V. Michal, E. Baggetta, M. Aurino, S. Bouat, and J. Villegier. Superconducting RSFQ logic: Towards 100GHz digital electronics. In *Proceedings of 21st International Conference Radioelektronika 2011*, pages 1–8, 2011. doi: 10.1109/RADIOELEK.2011.5936486.

[20] B.D. Josephson. Possible new effects in superconductive tunnelling. *Physics Letters*, 1:251–253, 1962. doi: 10.1016/0031-9163(62)91369-0.

[21] V.V. Schmidt. *The Physics of Superconductors: Introduction to Fundamentals and Applications*. Springer-Verlag Berlin Heidelberg, 1st edition, 1997. ISBN 978-3-662-03501-6. doi: 10.1007/978-3-662-03501-6.

[22] P. Shevchenko. PSCAN2 Superconductor Circuit Simulator: Manual, version 1.3. `http://www.pscan2sim.org/documentation.html`, May 2019.

[23] W.C. Stewart. Current-voltage characteristics of superconducting tunnel junctions. *Journal of Applied Physics*, 45:452, 1974.

[24] Paul B., K.K. Likharev, and D. Zinoviev. RSFQ technology: Physics and devices. *International Journal of High Speed Electronics and Systems*, 11(1):257–305, 2001. doi: 10.1142/S012915640100085X.

[25] K. K. Likharev and V.K. Semenov. RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Tetrahertz-Clock-Frquency Digital System. *IEEE Transactions on Applied Superconductivity*, 1(1):3–28, 1991. doi: 10.1109/77.80745.

[26] S.V. Polonsky, V.K. Semenov, and D.F. Schneider. Transmission of Single-Flux-Quantum Pulses Along Superconducting Microstrip Lines. *IEEE Transaction on Applied Superconductivity*, 3(1): 2598–2600, 1993. doi: 10.1109/77.233525.

[27] A. Bozbey, M.A. Karamuftuoglu, S. Razmkhah, and M. Ozbayoglu. Single Flux Quantum Based Ultrahigh Speed Spiking Neuromorphic Processor Architecture. arXiv:1812.10354, 2018.

[28] J. P. Singh, R. Bhardwaj, A. Sharma, B. Kaur, S. O. Won, S. Gautam, and K.H. Chae. Chapter 2 - Fabrication of Magnetic Tunnel Junctions. In *Advanced Applications in Manufacturing Engineering*, pages 53 – 77. Woodhead Publishing, 2019. ISBN 978-0-08-102414-0. doi: 10.1016/B978-0-08-102414-0.00002-1.

[29] Colorado Supercondcutor Inc. Experiment Guide for Superconductor Demonstrations. From `https://www8.physics.utoronto.ca/~phy326/htc/Colorado_Superconductors_Guide.pdf`, May 2007.

[30] E.G. Keim. EF-TEM Properties. MESA+ Institute for Nanotechnology: Analysis Group, `https://www.utwente.nl/en/mesaplus/infrastructure/nanolab/analysis/facilities/tem/`.

[31] V. Vinila, R. Jacob, A. Mony, H. Nair, S. Issac, S. Rajan, A. Nair, D. Satheesh, and J. Isac. Ceramic Nanocrystalline Superconductor Gadolinium Barium Copper Oxide (GdBaCuO) at Different Treating Temperatures. *Journal of Crystallization Process and Technology*, 04:168–176, 2014. doi: 10.4236/jcpt.2014.43021.

[32] S. Datta. *Electronic Transport in Mesoscopic Systems (Cambridge Studies in Semiconductor Physics and Microelectronic Engineering)*. Cambridge University Press, 1995. ISBN 9780511805776. doi: 10.1017/CBO9780511805776.

[33] L.A. Ponomarenko, D.T.N. de Lang, A. de Visser, V.A. Kulbachinskii, G.B. Galiev, H. Künzel, and A.M.M. Pruisken. The effect of carrier density gradients on magnetotransport data measured in hall bar geometry. *Solid State Communications*, 130(10):705 – 710, 2004. doi: 10.1016/j.ssc.2004.02.021.