University of Twente

Bachelor Thesis

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Room temperature characterization of Dopant Network Processing Units

And optimization of the measuring process

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And know I would like to end my acknowledgements with some words in my local dialect on request of Mohamadreza and Dilu:
Dis'n goan wie op verzoek van de beglieders es ewm onmeunig hard in t Twents skriem. Ik hoop daj t un beetje leazen könt.
Ik woll gearn alle leu daank'n die mie hebt met hölp'n um dit verslag te skriem'n. Oh ja, ik soll em'n will'n ofsloeten deur te zegg'n: bloas nig zo hoog van'n toant en dow't heanig an he keals.
Good goan!
P.S. google translate probably doesn't work, so good luck translating ;)

2 Terminology

GA = Genetic Algorithm
DNN = Deep Neural Network
A.I. = Artificial Intelligence
DNPU = Dopant Network Processing Unit
NDR = Negative Differential Resistance
ANN = Artificial Neural Network
ADC = Analog to Digital Converter
DAC = Digital to Analog Converter
LN2 = Liquid Nitrogen
WB = Wire Bonding
ICO = Input, Control and Output
K = Kelvin

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3 Abstract

The latest research trend in the field of Artificial Intelligence (A.I.) is to improve the computing efficiency for Deep Neural Networks (DNN). A Dopant Network Processing Unit (DNPU) allows for parallelism and more efficiency in a Neural Network. DNPUs can show tunable non-linear behavior at 77 Kelvin (K), due to a special kind of conduction, which is called hopping conduction. The thesis will provide an experimental answer to the following research question: "What characteristics of DNPU's at room temperature indicate working devices at 77 Kelvin?", meanwhile tyring to improve and speed up the measuring process. Measurements will be performed using a probe station to check the IV characteristics of the DNPU, which represents the resistance range. The resistance depends on the doping concentration and the reactive ion etching depth applied in fabrication. Hopping conduction, which is needed for tunable non-linearity, is dependent on the doping concentration and is thus coupled with resistance. The results showed that the resistance of the connections of the device at room temperature could indicate non-linearity at 77 K. Another outcome is the step by step guide to characterize the DNPU devices, because after experimentation, extra safety features like grounding while wire bonding had to be incorporated. Conclusively, DNPUs can be characterized at room temperature with IV curves and can indicate non-linearity at 77 K. The results showed devices with more non-linear connections at a resistance value around 2 MΩ. Future experimenting is required to collect more data points to back up this claim and provide more data on tunable non-linearity

4 Introduction

Deep Neural Network (DNN) models have been used as a solution for the growing industry of Artificial Intelligence in the past decade. DNNs are brain inspired networks with multiple hidden layers. In a general sense, the more hidden layers or the deeper the network, the more expensive they are to train and the easier they are to use in the inference phase [19]. One of the latest research trends is to improve the computing efficiency, which enables a deep neural network to make faster computations. Potentially, cutting the cost of training down in terms of price and time and decreasing energy consumption within your system.

Recently, the BRAINS team of the NanoElectronics group in the University of Twente has developed a new type of device specifically designed for the neuromorphic computing field, which is called a Dopant Network Processing Unit(DNPU). DNPUs allow for parallelism and more efficiency in a Neural Network [2]. A DNPU is a lightly doped silicon device, which can show non-linear behavior at 77 K. Using a back gate voltage, it can also show non-linear behavior at room temperature. This non-linearity can be utilized to perform complex operations. Due to this extra added complexity, the DNPU can select a higher number of different functions as possible solution than a traditional perceptron ANN, which means it has more capacity.

The assignment in this thesis is to explore and characterize DNPU devices at room temperature and take out the promising devices to test for computational capacity/efficiency and tunable non-linearity at 77 K. The main research question this thesis will be answering is:

- What characteristics of DNPU's at room temperature indicate working devices at 77 Kelvin?

The side research question that will be answered is:

- How can we optimize the measuring process, while eliminating bottle necks?

The paper layout contributes to finding an answer to the main research question. In Section 5 (Theory), relevant details that go in depth on the physics of the device and on the working principles behind the measurements will be discussed.

In Section 6 (Methods), the measurement setups, process flow, and details behind the fabrication process are highlighted. Measuring could have great impact on the results, just like the fabrication process. They both could provide possible explanations if something isn't working properly in a certain batch/chip. In Section 7 (Results), the obtained measurement results that couple back to the research question are displayed. In Section 8 (Conclusion), a conclusion based on these results and the provided theory of Section 5 (Theory) is drawn. Moreover, several encountered issues, that could improve future experiments for example, are discussed and a set of beneficial experiments for future research will be regarded. Section 9.1 (Appendix A) contains a step by step guide for reproducing the experiments.

5 Theory

5.1 The 8 electrode Dopant Network Processing Unit

A Dopant Network Processing Unit (DNPU) consists of an active region of 26 by 60 µm, containing a doped semiconductor material (n- or p-type). The place where the endpoints of the 8 electrodes come together, on the doped region, forms a circle with a cross section of about 300 nm, which is shown in the top half of Figure 1. Each electrode of the device can be configured either as an input, output or as a control electrode. A typical configuration, for example, is that 2 electrodes function as input, 5 electrodes function as a control, and 1 electrode functions as the output. The bottom half of Figure 1 represents a cross sectional schematic of a fabricated DNPU [15].

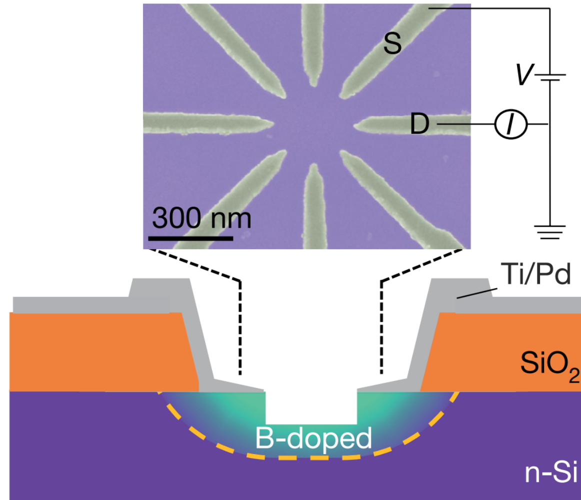


Figure 1: Top picture: Top view on the active region, where the 8 electrodes come together on a circled radius of 300 nm in a DNPU. Bottom picture: A cross sectional schematic of a DNPU device [2].

5.1.1 The electrodes

All eight electrodes are made out of a Titanium bedding with a Palladium top layer. Titanium functions as a good middle layer, because it has good adhesive properties with oxides. As a lot of metals/semiconductors (including silicon) oxidize, it makes a good choice for a middle layer between the SiO2 and Palladium. In Figure 2 we can see a picture on how the substrates are stacked on top of each other. Part of the DNPU device does not make straight contact with the doped silicon layer. This part is stacked bottom up: a lightly n-type doped silicon wafer, a silicon oxide layer, a titanium bedding and a palladium top layer. This is however not applied in the active region where the electrodes contacts the active region (see Figure 1), because there wouldn't be good contact between the doped region and the metal. This has to do with the work function, an interesting property of the palladium top layer is that it has a comparable work function to boron doped silicon. Palladium's work function is between 5.22 and 5.60 eV, while boron doped silicon's is around 5.00 eV [11]. This is important as the Fermi levels are about equal in height when the work functions are comparable and thus the charge transfer loss between the materials is small. More information on Fermi levels can be found in the IV curve section related to non-Ohmic contacts.

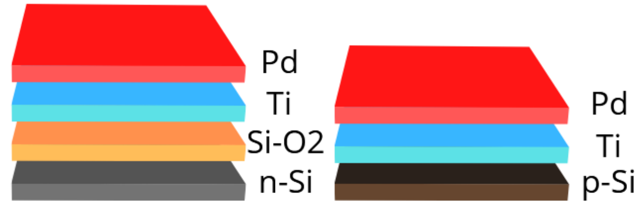


Figure 2: The sequence of material layering in two different parts on the chip. The first picture shows the layering of non-connected electrodes and the second picture shows how the connected electrodes are layered (Figure 1 shows where in the device/chip these layers are). Left picture from the bottom up: lightly n-doped silicon wafer, a silicon-Oxide layer, a titanium adhesive layer and palladium as a top layer. The right picture from bottom up: a p-doped silicon active region, an adhesive titanium middle layer and a palladium top layer.

The applied voltage to a material influences the Fermi level. The relation between the electrostatic potential, the applied voltage, and the work function of a material is given in Equation (1):

$$\phi = V - \frac{W}{e} \tag{1}$$

$$\begin{cases} \phi & \text{Electrostatic potential} \\ V & \text{Applied voltage to the material} \\ W & \text{The work function of a material} \\ e & \text{The electron charge} = 1.6021 \times 10^{-19} \text{ Coulomb} \end{cases}$$

5.1.2 Hopping regime

The DNPU has a p-type doped area (active area), which introduces impure n- or p-type atoms into the silicon [8, 2]. Impurity atoms cause an imbalance in the charge carrier concentration of the material. A charge carrier is an electrically charged particle that is free to move, so either holes or electrons. The imbalance means that the concentration of holes and electrons are not equal under thermal equilibrium. The formula in Equation (2) describes the imbalance in equilibrium in doped silicon [9].

$$N_0 * P_0 = N_I^2 \tag{2}$$

Cited from: [9]

$$\begin{cases} N_0 & \text{Concentration conducting electrons} \\ P_0 & \text{Concentration conducting holes} \\ N_I^2 & \text{Materials intrinsic charge carrier concentration} \end{cases}$$

The hopping regime -in simple terms- is a lightly doped semiconductor at low temperatures, which is needed to achieve tunable non-linear conductivity in a DNPU. The conductivity is determined by a materials ability to let charge carriers cross the band gap, whereas the band gap is determined by the energy levels within the system. Intrinsic silicon contains a conduction and a valence band. Introducing donor atoms (n-type), like arsenic creates a new energy level close to the conduction band. Introducing acceptor atoms (p-type) such as boron, on the other hand, creates new energy levels close to the valence band.
Figure 3 demonstrates the introduction of new energy levels of n-type and p-type semiconductors.

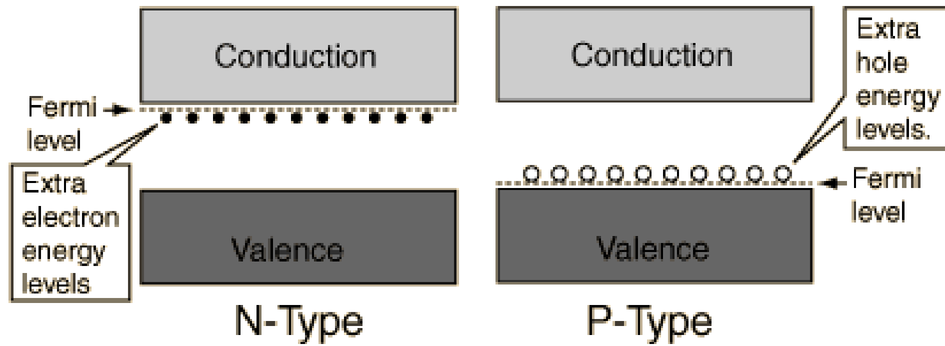


Figure 3: New energy levels introduced for a p-type and an n-type semiconductor [13].

The energy level between the conduction and valence band is called the ionization energy. At room temperature (293.15 K) charge carriers can move freely, because the thermal energy is greater than the ionization energy. At lower temperatures, however, the thermal energy is not greater than the ionization energy. Therefore, the charge carriers can not move freely anymore between the valence and conduction band. Thus, as long as no energy is added to the system, there is no conduction taking place between these bands. Instead, electrons conduct between the impurity atoms, which is called the hopping regime.

5.1.3 Hopping transport and resistance

The introduction of impurity atoms gives extra energy levels in the material, which are known as impurity states. An electron can hop from impurity state to another free impurity state, i.e., a hole. This is known as hopping transport and the phenomena can in physics be described as wave function overlap, which is also known as the Bohr radius. This means that the wave function overlap of multiple impurity states determines the energy transfer between these energy levels. Therefore, the conduction at lower temperatures is determined by the spread of the impurity states (acceptor or donor atoms). An increase in the concentration of impurity states (higher doping concentrations) gives rise to more wave function overlap and thus more conduction takes place. In other words, the material behaves more like metal. A decrease in impurity concentration does the opposite and can make the hopping occur less frequent, lowering conduction and thus behaving more like an insulator. The Mott concentration is the concentration of impurity, where the behaviour changes from insulator to a metal conduction between the impurity atoms. A concentration lower than the Mott concentration means that the dopant layer would behave as an insulator and a higher concentration means the layer behaves similar to a conductor. In semiconductors with doping concentrations below the Mott concentration, hopping of electrons from impurity to impurity is thus the pre-dominant conduction type [8].

In Figure 4, conduction in different types of doping concentration are represented. In situation **a**, the system acts like an insulator with a cold temperature and a doping concentration below the Mott concentration. Situation **b** sketches the system when it's above the Mott concentration, where the system acts more like a metal. Situation **c** represents an insulator type with increased temperature. Although the dopant spread still looks like an insulator, the increase in temperature causes the wave function to overlap more. Situation **c** is what hopping looks like, a low doping concentration and relatively low temperature, that causes hopping conduction.

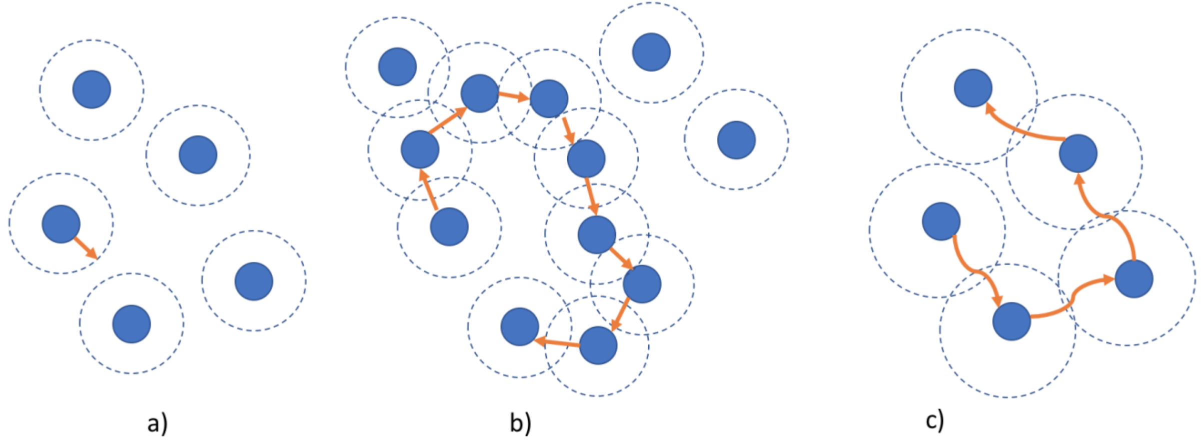


Figure 4: The blue dots represent the dopants with the circles representing their bohr radius (overlap in wave functions). ***a*** *shows an insulator like conduction,* ***b*** *a metal like conduction and* ***c*** *a hopping conduction [8].*

Each impurity state can be considered to have a center, the impurity center. Hopping from impurity center to impurity center takes energy, so every impurity center that has a wave function overlap with another impurity center has a resistance between them. This resistance is inversely proportional to the probability of an electron transitioning from center to center. The resistance between two impurity centers can be described with equation Equation (3).
Cited from: [8].

$$R_{ij} = R_0 e^{U_{ij}} \tag{3}$$

$$\begin{cases} R_{ij} & \text{Resistance between impurity center i and j} \\ R_0 & \text{Constant depending on the material of the impurity center} \\ U_{ij} & \text{Transition probability} \end{cases}$$

Here U_{ij} can be described by:

$$U_{ij} = \frac{2r_{ij}}{a_B} + \frac{\epsilon_{ij}}{T} \tag{4}$$

$$\begin{cases} r_{ij} & \text{Distance between impurity center i and j} \\ a_B & \text{Effective Bohr radius of an isolated impurity approximated as hydrogen} \\ \epsilon_{ij} & \text{Energy difference between impurity centers i and j} \\ T & \text{Temperature (Kelvin)} \end{cases}$$

The resistance between impurity atoms can be modelled as charge islands interconnected by resistances, as exemplified in Figure 5 [8, 12]. For a DNPU, the resistance is smallest on the surface, because the spread of the dopant material is lower deeper into the substrate. This means that deeper into the substrate there is less overlap in wave functions, increasing resistance. This suggests that surface conduction dominates (2D variable range hopping) [2].

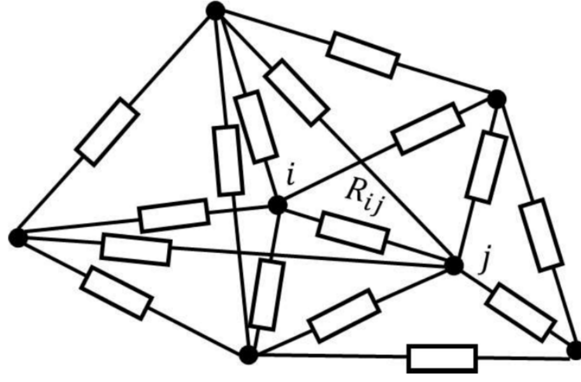


Figure 5: An interconnected resistance network of charge islands described by Abrahams and Miller [12].

5.2 Hopping, band conduction and back gate

The chance of finding a working device rises when there is strictly hopping taking place and no band conduction [2]. In Figure 6, it is shown that above 160 K, where both hopping and band conduction occur, the abundance to find a working device is below 5% for the two different applied fitness function thresholds. The abundance is defined as the overall chance of finding Boolean logic.
Therefore, by suppressing the band conduction regime at higher temperatures, the chances of finding a working device at these higher temperatures increases.

Suppressing band conduction can be done by applying a back gate voltage. A back gate voltage introduces a charged layer below the doped layer, depleting the present p-n junction. Effectively you are backwards biasing your p-n junction, hence increasing the width of your depletion region. Dopants near the p-n junction are more likely to ionize at room temperature, but the increase in width of the p-n junction increases the energy needed for ionization at room temperature, which results in suppression of the conduction band [2].

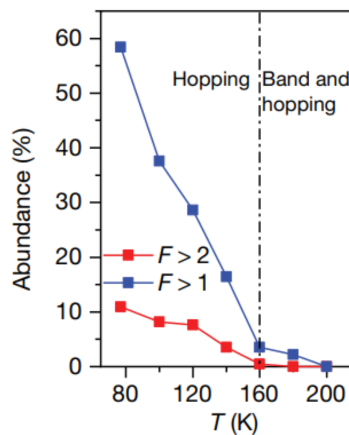


Figure 6: Abundance of logic gates as a function of temperature for two different fitness function threshold values (F(blue)>1 and F(red)>2) [2].

5.3 Thermal breakdown

Rapid changes in temperature of a material can cause thermal stress, which is caused by strain due to the rapid expansion and/or contraction of the material. If the strain exceeds the tensile strength of the material, the device could break or crack. Tensile strength is the maximum stress a material can take while stretched or pulled, which is a material dependent property. It's called thermal breakdown when

this thermal stress exceeds the tensile strength and breaks or cracks the device. Gradually cooling or heating can thus prevent thermal breakdown [18, 7, 17].

5.4 IV curves

IV curves map the resistance of a device by inputting a voltage and measuring the output current. The current is usually displayed on the y-axis and the voltage on the x-axis.

5.4.1 Room temperature, Ohmic contact

At room temperature, a DNPU device isn't in the hopping regime and should conduct freely. This free conduction means IV curves should be linear, obeying Ohm's law. An electrode at room temperature is an Ohmic contact, which means it behaves linear. If no energy is added to the system, the linear line should cross zero current at zero volt.

If, however, one were to add energy to the system, like for example light, the IV curve would shift up. The light excites the semiconductor electrons, therefore making the linear graph not cross zero current at zero volts. See Figure 7 for a sketch of an Ohmic IV curve at room temperature with and without light source.

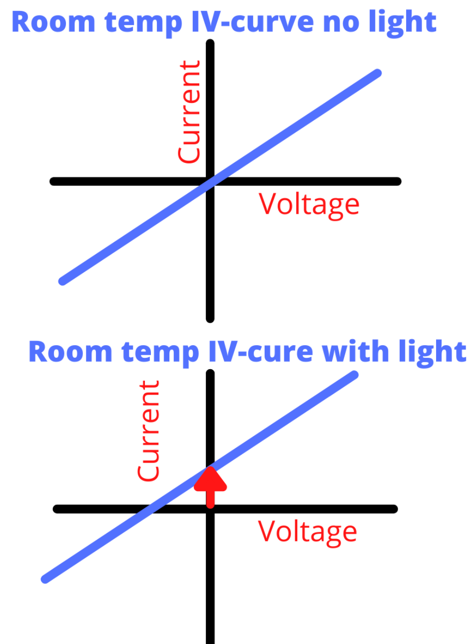


Figure 7: Top picture: sketch of an IV curve at room temperature without light source. Bottom picture: sketch of an IV curve at room temperature with a light source, here the graph gets shifted up due to the added energy.

5.4.2 Room temperature non-Ohmic contact

Non-Ohmic contacts show non-linear behavior at room temperature. A non-Ohmic contact contains a junction of two different (semi-)conducting materials, which means the junction has two different Fermi levels. The position of these Fermi levels determines the built-in potential of the junction (the electric field strength) [9].

5.4.2.1 Diodes

Some DNPU devices use a boron doping (p-type) on a slightly n-doped wafer, which creates a small p-n junction within your device. A diode is also a p-n junction, that consists of a p-type doped semiconductor combined with an n-type doped semiconductor. At the p-n junction, a depletion layer is formed, this layer contains a built-in electric field.
When forward biasing a diode, we increase the minority carriers on both side of the depletion region.

A linear increase in voltage increases, the current exponentially. This non-linear function is shown in Equation (5). The non-linear behavior is sparked due to Boltzmann relations [9].

$$I = I_0(e^{\frac{e_{electron}V}{kT}} - 1) \tag{5}$$

cited from: [4].

$$\begin{cases} I & \text{Current} \\ I_0 & \text{Maximum reverse current} \\ e_{electron} & \text{The electron charge} = 1.60217 \times 10^{-19} \text{ (Coulomb)} \\ V & \text{Applied voltage} \\ k & \text{Boltzmann constant} = 1.3806 \text{ x } 10^{23} (JK^{-1}) \\ T & \text{Temperature (Kelvin)} \end{cases}$$

Diodes can also be connected in reverse, this shows a leakage current up till the breakdown voltage, where the current moves exponentially downward. In Figure 8 the current behavior is plotted against a voltage range for a p-n junction. The back gate, which is effectively a p-n junction, also has to be connected in reverse bias. This is to deplete the junction, but avoiding introducing a lot of extra current in your system. Using the reverse biasing for the back gate would, however, mean that you cannot exceed the breakdown voltage, where you introduce a lot of current.

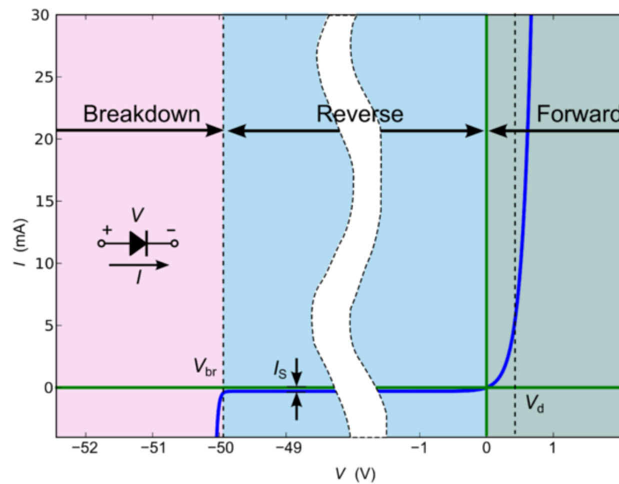


Figure 8: Current in a diode (p-n junction) over a voltage range [3]

5.4.2.2 Schottky barriers

A Schottky barrier is a comparable kind of junction to the p-n junction, this junction however, consists of a doped semiconductor material with a metallic material. The main difference between the p-n junction, is that for a Schottky barrier the depletion layer doesn't extend into the metal. In the metal, there is only a small accumulation of charge against the junction sidewall. The barrier height depends on the aggregated materials that form the Schottky barrier. The barrier height, as seen for the electrons, can be changed by applying a voltage. This is somehow similar to the p-n junctions of diodes that contain a built-in voltage. When the barrier is too small to show non-linearity, the Schottky barrier behaves like an Ohmic contact. Schottky barriers can also behave like diodes and show rectification. The main differences between a Schotky barrier and p-n junction are:

1. The built-in voltage when forward biasing is much lower for a Schottky barrier
2. The Schottky barrier has a relatively high series resistance compared to a p-n junction
3. When reverse biasing, the leakage current of a Schottky barrier is relatively high

Figure 9 sketches the difference between a Schottky barrier and a p-n junction.
The Schottky barrier it is relatively harder to create than a p-n junction. Silicon and other semiconductors react with oxygen and form an oxide layer, due to this layer it's hard to directly create a Schottky barrier onto this metal. As a solution, silicon material that reacts with a metal (silicides) are used. Although they aren't actual metals, they do behave like metals [9].

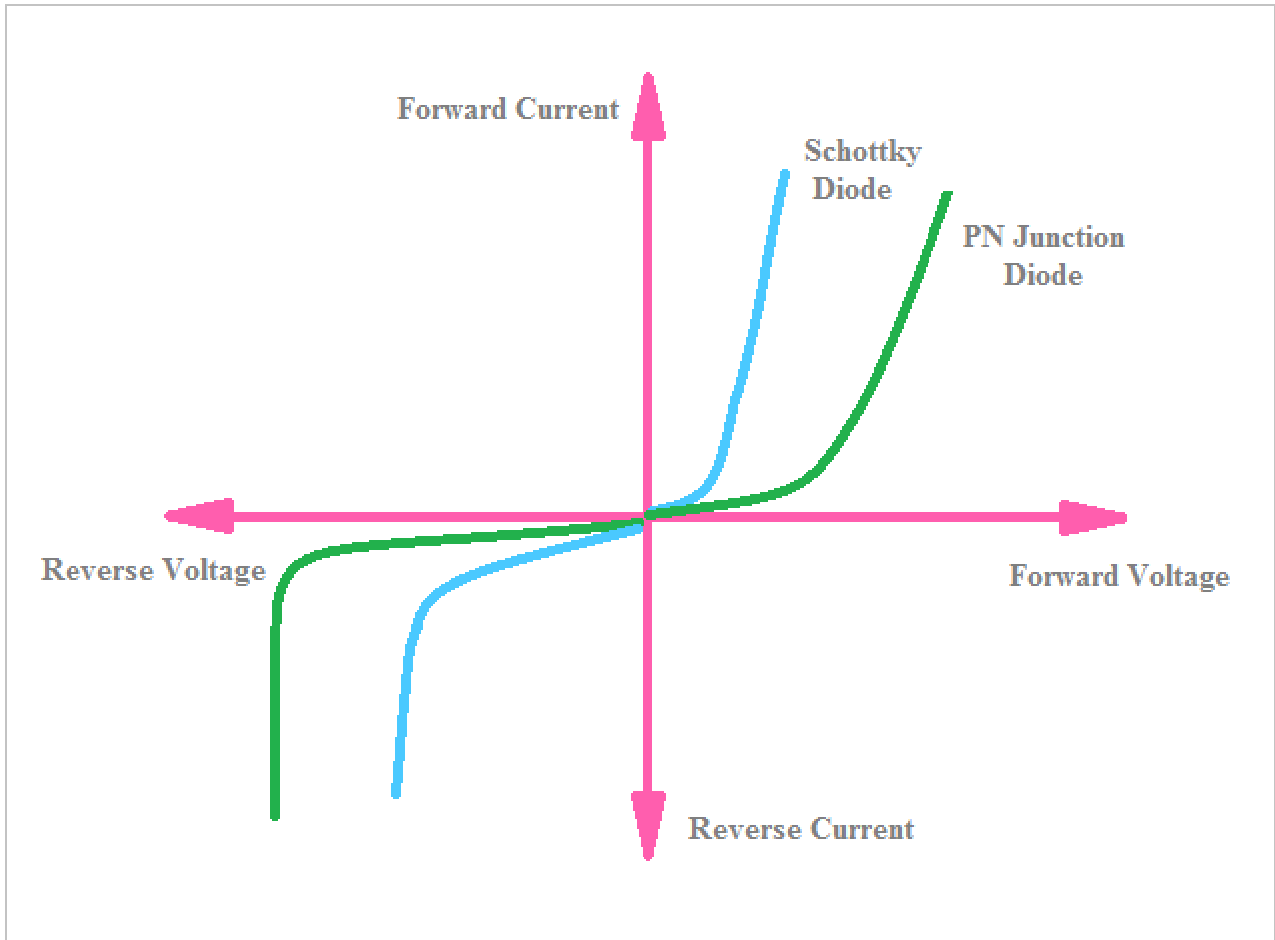


Figure 9: Sketch of a current in a diode (p-n junction) compared to the current in a Schottky barrier [16].

5.4.2.3 Tunnel junction

A tunneling junction is in a general description a Schotkty barrier with a low barrier height. This barrier height depends on the materials that are combined, which are in this case palladium/titanium and doped silicon. The depletion layer width is determined by the doping concentration. Counter-intuitively, the higher the doping, the smaller the depletion layer according to Equation (6). The width of this depletion layer determines the chances of tunneling. The smaller the width of the depletion layer, the higher the changes of tunneling, thus the more Ohmic your contact is. So small doping concentrations could create non-Ohmic contacts [9].

Equation cited from: [9].

$$x_{dn} = \sqrt{\frac{2\epsilon_S V_{bi}}{qN}} \tag{6}$$

$$\begin{cases} x_{dn} & \text{Width of the depletion layer} \\ \epsilon_S & \text{Di-electric constant silicon} = 10^{-12}(Fcm^{-1}) \\ V_{bi} & \text{Built-in voltage} \\ q & \text{The electron charge} = 1.6021 \times 10^{-19} \text{ (Coulomb)} \\ N & \text{Doping concentration} \end{cases}$$

5.4.3 77 Kelvin

Liquid nitrogen will provide an environment of 77 K for the DNPU. At this temperature the non-linear hopping conduction can take place. The non-linear behavior of a DNPU device changes with temperature, Figure 10 shows how the non-linear behavior is changed over temperature [2].

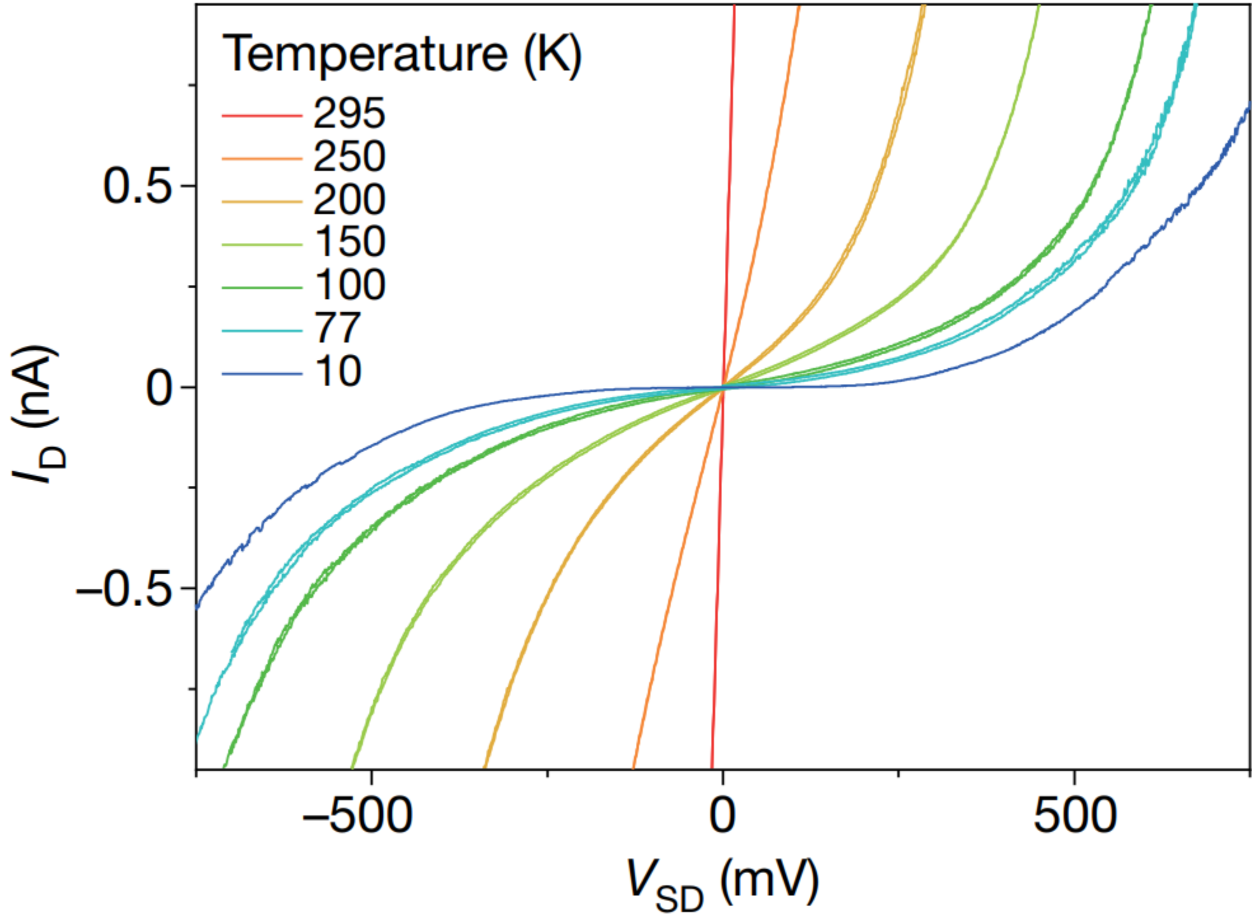


Figure 10: Non-linear behavior of a DNPU plotted at different temperatures [2].

5.4.3.1 Negative Differential Resistance(NDR)

When applying a signal into the DNPU, the control electrodes influence the flow of this signal to the output, because the control voltages attached to these electrodes can change the potential landscape of the DNPU device. Therefore, they can cause less hopping (which means less current flow) between a certain voltage range. A descending current with a rising voltage is called a Negative Differential Resistance (NDR), because the slope of the IV curve is negative. The negative slope indicates a negative resistance. It has been proven that DNPUs can show this NDR behavior by applying a control voltage. Figure 11 shows an example of Negative Differential Resistance for different control voltages in a DNPU dipped at 77 K. For this figure the author made use of a three phased measurement [6].

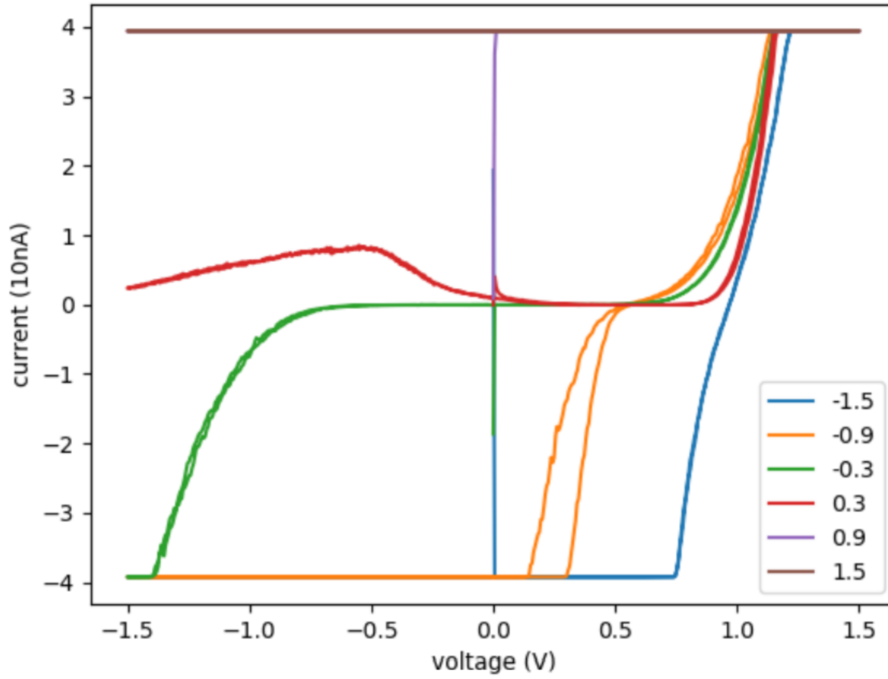


Figure 11: Different control voltages applied to the DNPU with a three phased measurement at 77 Kelvin, to obtain tunable non-linearity. Here NDR is seen in the red line between -0.5 V and 0 V [6].

5.4.3.2 Three phased measurement

A three phased measurement can be used at 77 K. It consists of an input, control, and an output signal. The three phased measurement is a quick way to test for NDR. If the control voltage is set to zero, one would measure a normal IV curve (input to output). NDR is beneficial for providing non-linear responses that facilitate finding non-linear Boolean logic gates such as XOR, since XOR is not directly linearly separable.

5.5 Genetic Algorithm

The Genetic Algorithm (GA) can be used for on-chip or off-chip training. On-chip means training by directly inputting the input and reading out the output from the chip. Training off-chip means trying to train the chip with a surrogate model, by making use of a DNN for example [15].
The GA tries to 'evolve' a set of control voltages in order to mimic a certain output function for a pre-set input. In order to do this, the output function will be compared to the target after each iteration (One iteration is also called a generation). The outcome of this comparison determines the fitness of the set of parameters that is used. The set of parameters is in this case the set of control voltages applied to the DNPU. The fitness, in basic terms, is a number that represents how well a generation has mimicked the target. On basis of the fitness of a set of parameters in a generation, the GA determines which parameters of the set need to reproduce, mutate or be substituted. After this evaluation another generation is produced and so on, until a set number of generations has ran or whenever an optimal solution has been found [8, 1].

5.5.1 Fitness

The fitness uses the Corrsig fit function. This function works by first measuring the correlation between two signals using Pearson's correlation. Pearson's correlation can take a value from -1 up to 1. Here 0 indicates no correlation, + means there is a positive correlation and - means a negative correlation. The second step is passing this correlation through a pre-defined separation threshold of 2.5 nA. Lastly the output of the threshold is passed through a sigmoid function, which is a non-linear function that maps the fitness between 0 and 1.
The higher or lower the correlation in the first step, the higher the fitness in the mapping of the last

step. An intuitive example on how Pearson's correlation works is given in Figure 12. In this picture r represents Pearson's correlation coefficient, which can be seen to be higher, when dots are more grouped along the line.

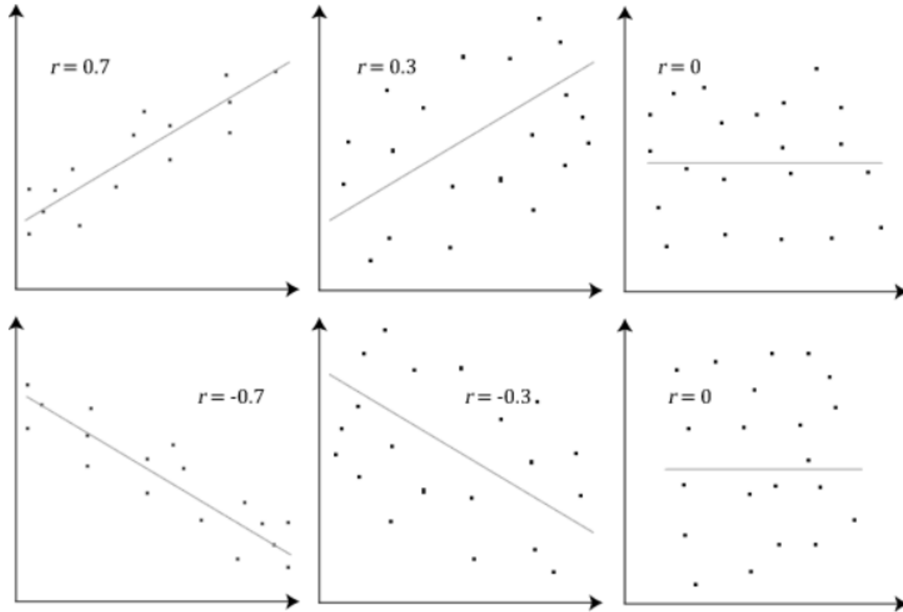


Figure 12: Pearson's correlation coefficient seen for different graph scenario's [14].

5.6 Linear separability in Boolean logic gates

There are 6 major logic gates in CMOS technology: OR, NOR, AND, NAND, XOR and XNOR gates. The X(N)OR gate is not directly linearly separable, this is also shown in figure Figure 13 for an XOR gate. In this figure, two lines are needed to separate the two different categories of data points. A normal ANN would need one hidden layer with two neurons to resolve the X(N)OR gates [2]. A functioning DNPU could simply emulate this ANN network, which suggests it could be the basic building block of an universal function generator.

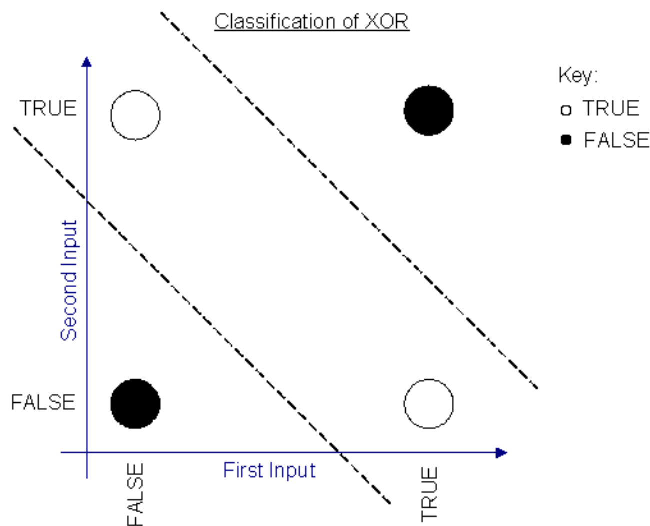


Figure 13: XOR data points represented with a linear solution [10].

6 Methods

The method section is focused on the measurements, the measurement setup and on the fabrication of the device.

6.1 Steps

6.1.1 Room temperature

The first step is IV measurements at room temperature to characterize the device. On basis of these measurements, good criteria can be deduced to find possible working devices. To measure at room temperature an Everbeing dark box including probes, microscope and a plateau in combination with a HP Elitebook 8560w laptop containing IV measurement software and a Keithley 2400 Source Meter will be used. A summarizing picture of this setup can be found in Figure 14. The IV measurement makes use of a saw tooth wave function that goes from 0 V to +90 mV to -90 mV back again to 0 Volt (see Figure 15 for a sketch of this). The reason for sweeping at such low voltages and doing a voltage sweep that starts and ends at zero is to prevent possible damage to the chip.

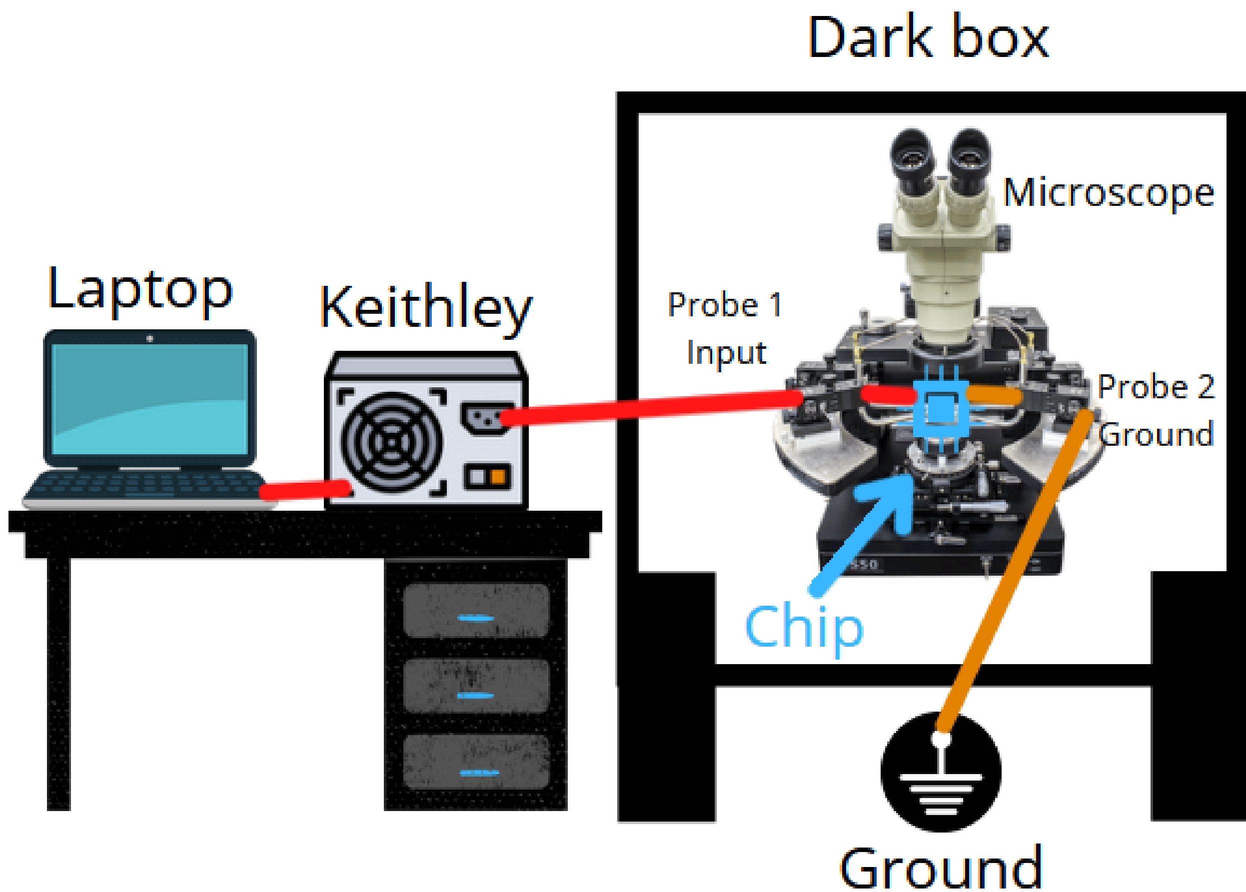


Figure 14: Probe station setup used for measurements at room temperature, with the red wires as input connections and the orange/brown wires as ground connection.

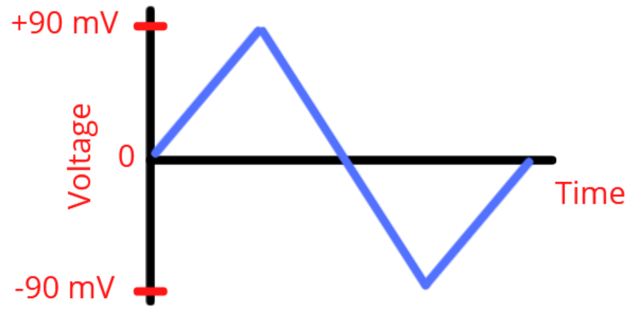


Figure 15: Input signal used for IV measurements.

To simplify the process flow and measurements, the chips will be divided into production batches, the devices on each chip will be numbered with row and column number and the electrodes will be numbered in a clock wise direction. The numbering of the devices and electrodes is visualized in Figure 16. There is a total of 6 batches, a batch consist out of chips that were fabricated together. The number of chips in every batch is summarized in Table 1. One chip contains 16 devices. The bottom row of the chip is labeled device 1-1 up to device 1-4 (from left to right). The second row seen from the bottom is labeled as device 2-1 up to 2-4 (from left to right) and so on up to device 4-4. On some chips the devices on row 2 and device 1-1 are not connected as a DNPU configuration, but these are used for other purposes. So effectively the chip contains 11 working devices. The number of working devices per chip has also been highlighted in Table 1. Every device has 14 electrodes, only 8 of these electrodes are connected to the active region of the device. The electrodes are numbered 1 up to 8 starting from the left corner of the device in clockwise direction. For the IV measurements an input and an output are required. This means two electrodes are connected together, which is called a connection. The connections are labeled the same way as the electrodes, so a connection between electrode 1 and 2 is called connection 1. This goes on up to connection 8.

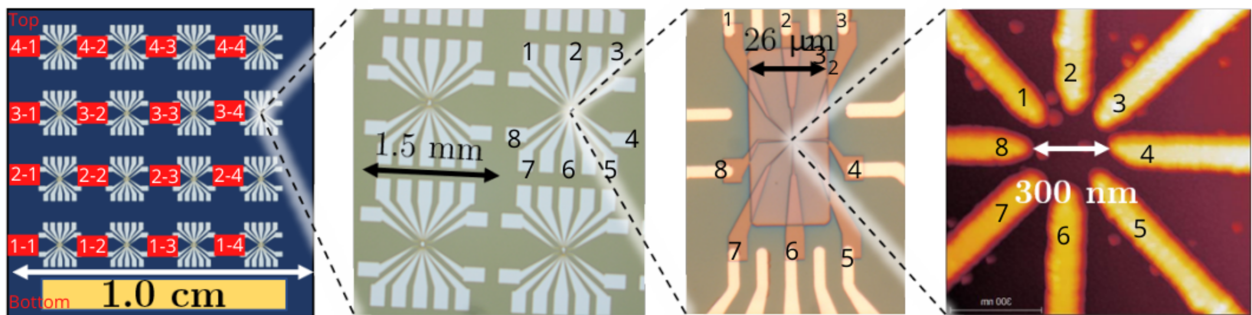


Figure 16: Chip design on different length scales included with labeling of the device numbers and electrode numbers. The complete chip (left, schematic) shows the devices and the device each number represents compared to the top and bottom. Picture 2 shows the zoomed in device and the numbering of the electrodes on this device. The third picture is the dopant region with a visualization which electrodes are connected to the doped region. The last picture (4th right), shows the 8 electrodes on the active region with the electrode numbering. This picture was adapted from [20].

Table 1: The number of chips each batch number contains and the number of working devices per chip.

Batch	Number of chips	Number of working devices per chip
1	5	11
2	2	11
3	1	11
4	5	11
5	1	16
6	2	Chip 1: 4, Chip 2: 8

6.1.2 77 Kelvin

The second step is dipping the device in liquid nitrogen in order to search for tunable non-linear behavior. Before this can happen, the device will need to be wire bonded onto the PCB, which can connect to the dipstick in the measurement setup. The measurement setup uses a dipstick, a Norhof LN2(Liquid Nitrogen) vessel, A HP 8560W laptop with the BSPY software, a matrix module 24 x 1 TU-DELFT-QT(151204), a M0 Dual ISO-Out module, a M1b I measure module, the National Instruments NI-USB-6216 ADC and the National Instruments cDaq 9171 DAC. The measurement setup is shown in figure Figure 17.

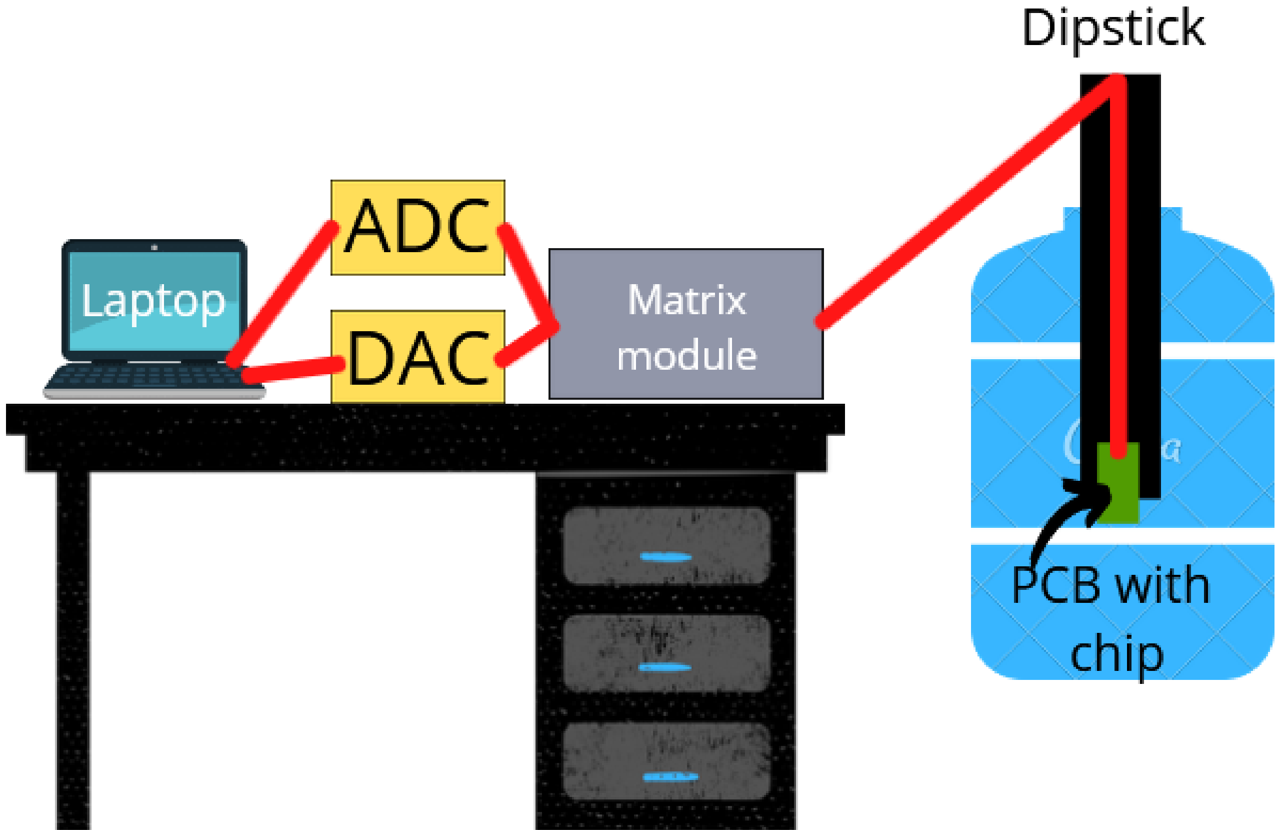


Figure 17: Dipping setup used to measure at 77 K. The laptop contains the brainspy software used for the measurements.

6.1.2.1 Wire bonding and PCB connection to dipstick

The initial steps before wire bonding are cleaning the PCB and chip and placing the chip on the PCB pad with double sided tape.

When attaching the chip to the PCB, take note in the orientation of the chip, as this makes it easier later on in the process. The best orientation of the device has been shown in Figure 18. In this orientation connect electrode 1 to pad 2 of the PCB, electrode 2 to pad 3, electrode 3 to pad 4, electrode 4 to pad 5, electrode 5 to pad 7, electrode 6 to pad 8, electrode 7 to pad 9 and electrode 8 to pad 10. In Figure 18 it also shows how the PCB pads are connected with the connector that can connect with the dipstick. The dipstick outputs wires that can be connected with the matrix module. These wires are labeled A0 up to A12. These are connected to the PCB in the following way:
2 PCB = A0 Dipstick
3 PCB = A1 Dipstick
4 PCB = A2 Dipstick
5 PCB = A3 Dipstick
7 PCB = A4 Dipstick
8 PCB = A5 Dipstick
9 PCB = A6 Dipstick
10 PCB = A7 Dipstick
11 PCB = A10 Dipstick

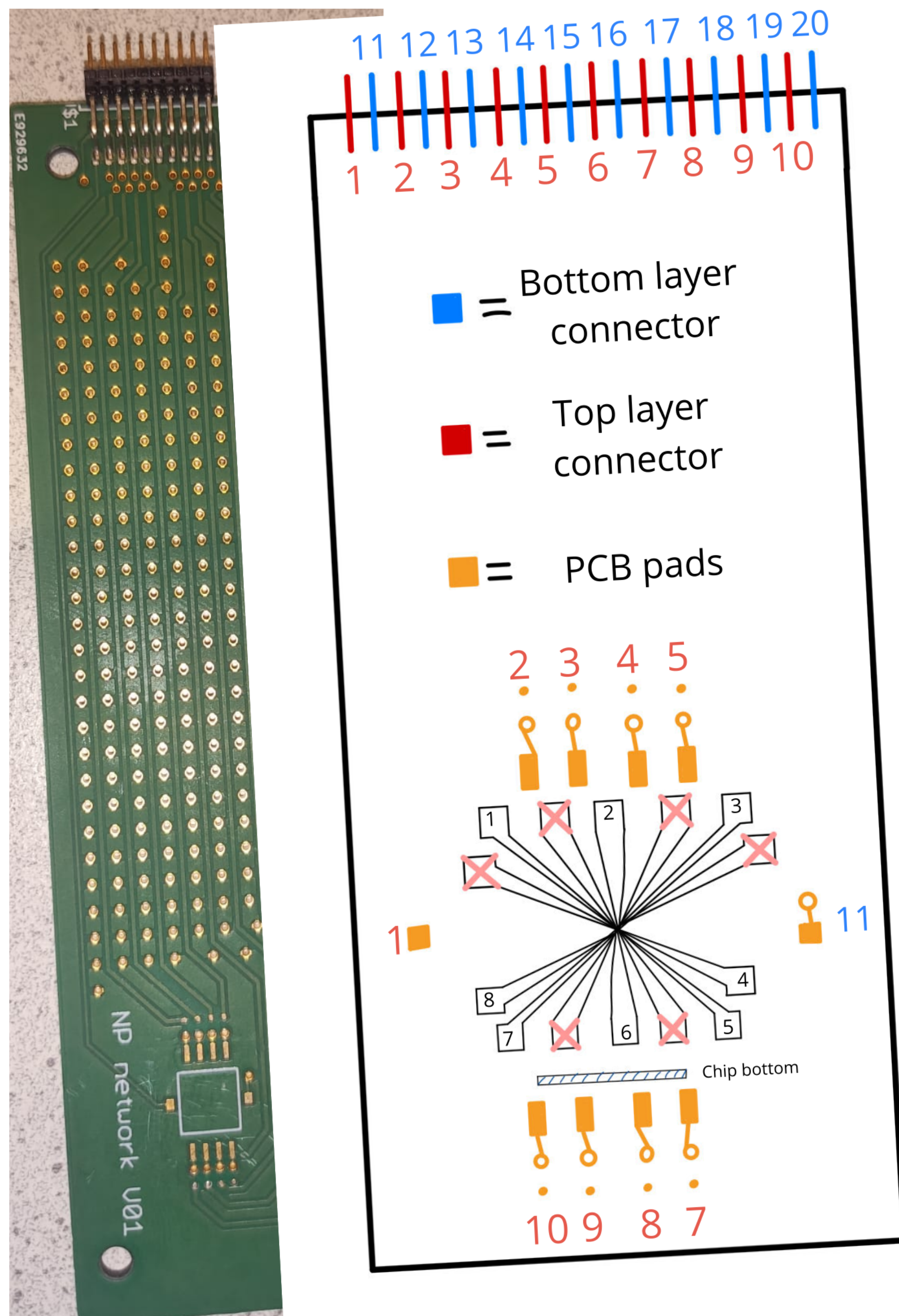


Figure 18: Left: The designed PCB by thesis predecessors in the Nano Electronics group of the University of Twente. Right: The PCB connectors in connection with the pads on the PCB and the orientation of the device on the PCB.

6.1.2.2 Three phased measurement

A three phased measurement is performed at 77 K to check for non-linearity and tunability. It has 3 connections to the chip, one input, a control and an output signal. These connections are labeled in clock wise direction from the top left corner again. So electrodes 1, 2 and 3 are labeled as connection 1 and so on up to connection 8. The control voltage that is applied has to ramp up before the input signal is applied, for protective purposes. This input signal is just like in the IV measurements, a saw tooth wave. In Figure 19 the saw tooth wave and the ramping up of the control voltage have been sketched out below each other. The IV measurements at 77 K can handle higher voltages as input signal, due to the lower temperature. The control voltage can be varied in voltage from -1.2 up to 1.2 Volt. A higher control voltage can influence the potential landscape more and show tunable non-linearity in the form of NDR.

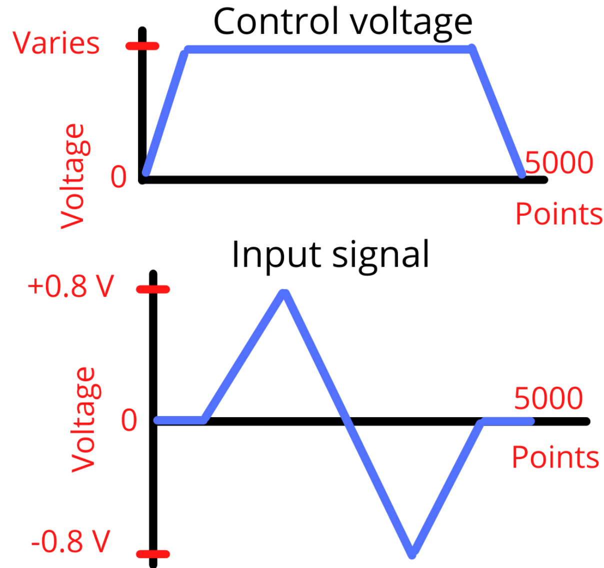


Figure 19: Top picture is the control voltage signal used in the three measurements and the bottom picture is the voltage sweep applied on the input pin of a three phased measurement. The saw tooth wave only starts when the control voltage is ramped up to it's steady value. The software makes use of 5000 data points, this determines the x-axis.

6.1.2.3 Classifier

A classifier tests if the DNPU device shows tunable non-linear behavior at room temperature, by mimicking a Boolean logic gate that has data points that are not directly linearly separable, as shown in the theory. The classifier makes use of two inputs (this is required for Boolean logic), one output and 5 control signals. The classifier makes use of a GA, after every run the fitness is updated. An increase in the fitness is a good sign. A higher fitness means an increase in synthesized and target overlap.

6.2 Fabrication

All 6 batches were produced at the University of Twente by Tao Chen and Bram van de Ven. The way these devices were fabricated could matter when characterizing them, because some processes have a non uniform nature [8]. Hence it is not possible to create two identical devices with the same characteristics. More information on the fabrication is useful to identify mistakes during the production process. This section will highlight the most important points that could influence the characterization of the device. The complete fabrication process of the DNPU device is visualized in Figure 20.

6.3 Preparing the wafer

Initially, before creating any structures on the wafer, the oxide layer is grown on top of a lightly doped n or p type silicon wafer. Lightly doped silicon is used, because this can create a barrier that is needed for back gating and it's relatively cheaper. The oxidized layer functions as a protective layer for the silicon.

6.3.1 Doping

The second step is to dope the wafers with impurity atoms. Two different kind of dopants have been used, arsenicum, a n-type dopant and boron, a n-type dopant. To implent this dopant, ion implantation is used, here ions are accelerated at the desired location of the active area, during which they penetrate into the bulk [2]. The impurity gets halted by collisions, so deeper into the active area there is less dopant material. Another possible method would be thermal diffusion of the dopant material into the active area, there are however two main advantages over this in the ion implementation method. The first advantage is that the extension into the dopant is more straight, where diffusion would cause an

equal amount of dopant in every direction. The second advantage is that with ion implantation, the peak dopant concentration is better controllable [8]. This doping concentration is important for the hopping regime, on which the non-linearity in the device depends.

6.3.2 Photo-lithography

The larger pad structures (micro scale) with a titanium bedding and a palladium top layer are created with photo-lithography. Photo-lithography makes use of a photo resist layer that forms a protective area for the parts that shouldn't contain any pad structures. The Photo-lithography can only be used up to micro scale, so for the nano structured electrodes, ending in the 300 nm circled radius, E-beam lithography is used. Before proceeding however, lift off needs to happen [8].

6.3.3 Lift off

After the pad structures are created, the protective layer of photo-resist will need to be dissolved. This also causes the metal on top of this resist to 'lift-off', leaving only the pad structures [8]. A danger of lift off is that it can cause spherical formation of metal droplets, leftover droplets could for example create a short between the metal pads. Lift off can also cause electrodes to break.

6.3.4 E-beam lithography

To create the nano scale structures required for the metal electrodes on the 300 nm circle, a more precise technique is required. In E-beam lithography, an initial layer of photo-resist is bombarded with precision high energy electrons to remove a nano-scale accurate pattern from the photo resist [8]. After this the electrode material can be deposited and lift off can be implemented again to remove the protective photo-resist layer.

6.3.5 Reactive Ion Etching

The electrodes must not form a Schottky barrier with the semiconductor material, hence the doping underneath the contact point of the electrode should be high. A higher concentration means a metallic like behavior, as discussed in theory. The structure in between the pads however, needs to have a low enough doping concentration for hopping to occur at the surface. To achieve this, the doped silicon is etched away until the doping is small enough for the hopping regime to occur (doping gets lower deeper into the surface). To prevent isotropic etching, which happens with wet etching. Reactive ion etching accelerates plasma particles directly on to the doped surface, creating a more an-isotropic hole.

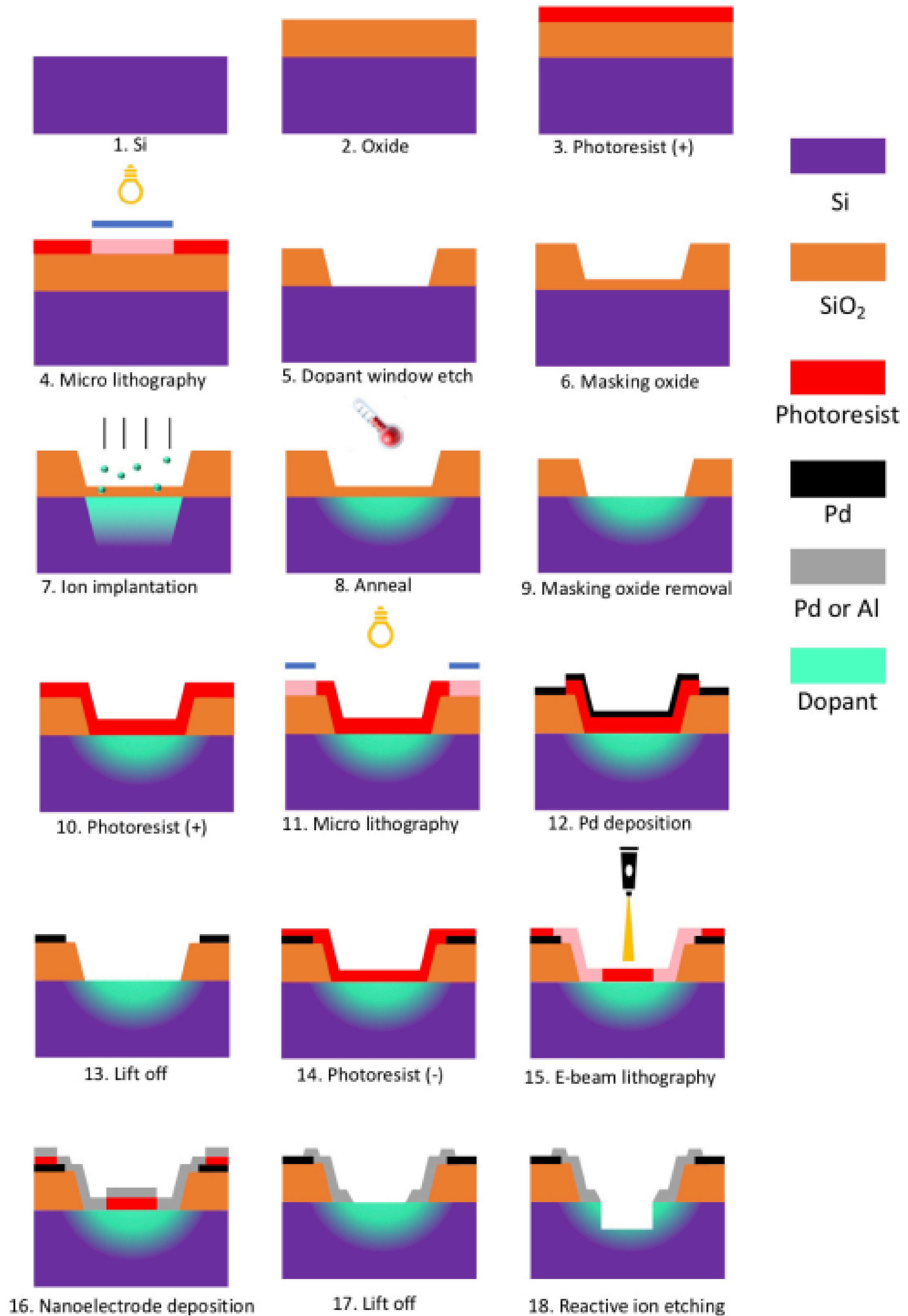


Figure 20: The fabrication process visually summarized in 18 steps, in step 12 the addition of a sub layer titanium is missing [8]

7 Results

Part of this section represents the result and discusses them, because some of the results were used in order to optimize/change the measuring process. One of the outcomes is a comprehensive manual, including pictures and time spent. The manual is a a step by step guide towards reproducing the experiments. The manual can be found in the appendix, see Section 9.1. Some of the findings in the results are the potential devices that were found at room temperature, the characterization of some dipped devices that had potential and the characterization of a working DNPU device that is used as a comparison.

7.1 Room temperature measurements

7.1.1 Normal resistance

To have a guideline of the resistance range on the results of room temperature measurements on A DNPU, an output of the Digital-to-Analog Converter (DAC) and an input to the Analog-to-Digital Converter (ADC) were connected to a several predefined resistance values at the dipping setup. This gave the results displayed in Figure 21 and Figure 22. We see that at 1 GΩ the graph shows a lot of noise, this is because the current range is close to the noise level of the DAC module. The noise is seen properly, when looking at the open circuit graph. It is in the range of -0.05 up to 0.125 nA. Another thing that is noticeable is the clipping at about 350 nA. The clipping value scales with the feedback resistance and op-amps used in the ADC. The clipping in this setup is not fully fixed and also depends on the battery level. The probe station setup, showed clipping at 1000 nA, an example of clipping in this probe station can be seen in Figure 24.

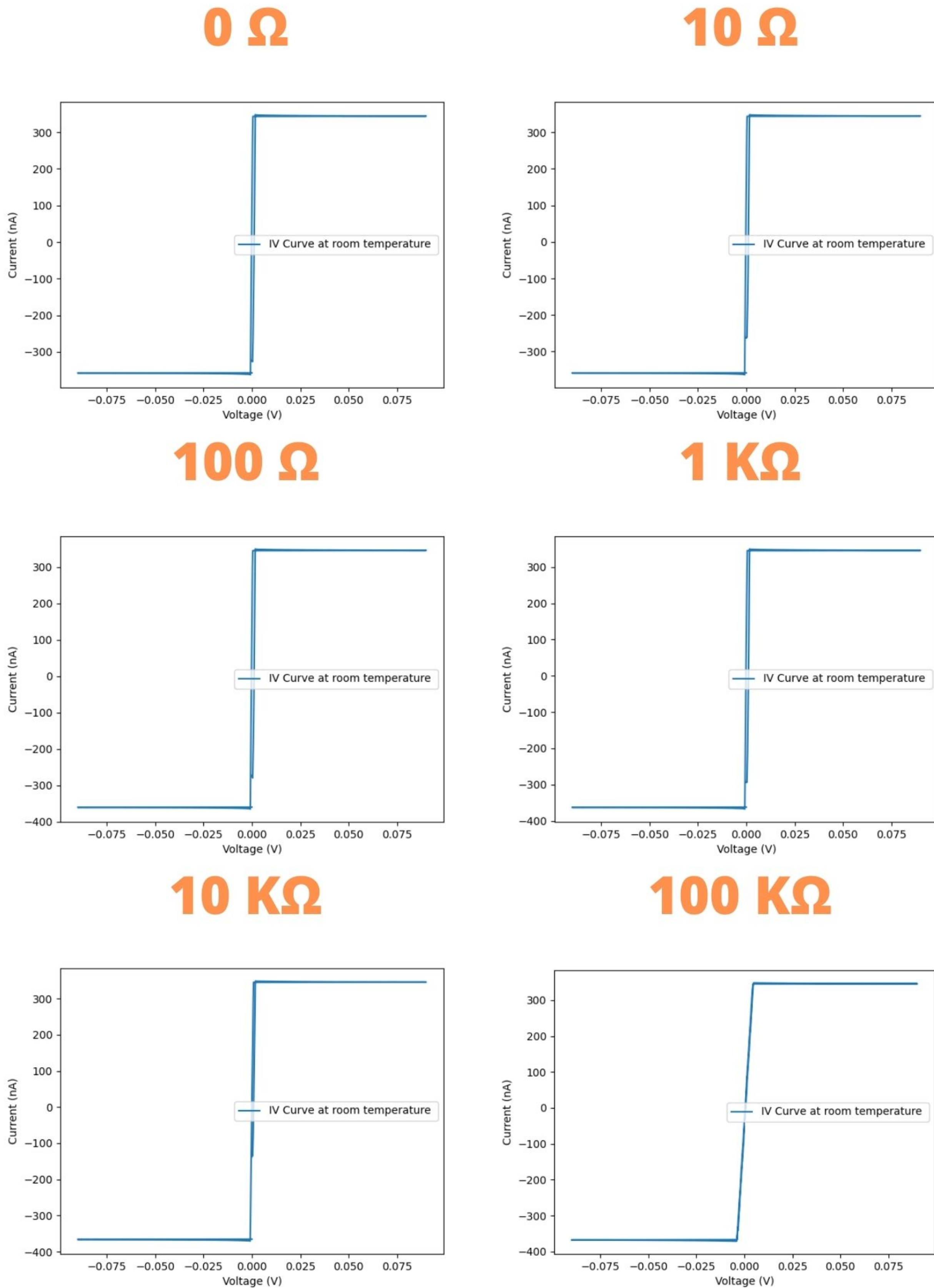
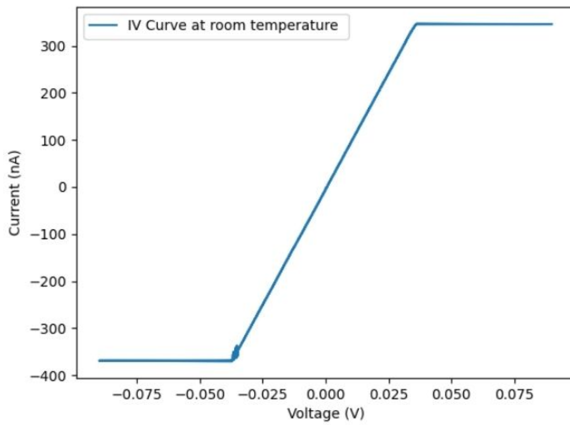
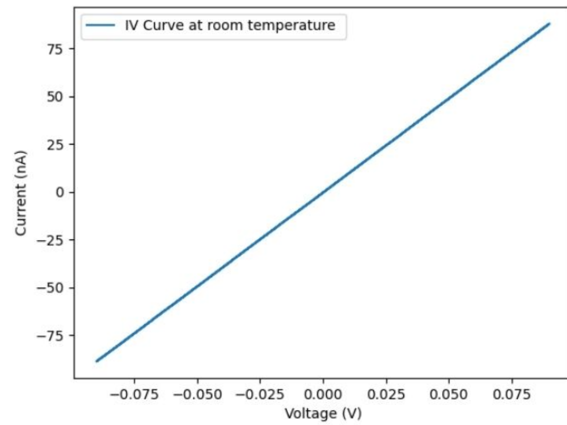


Figure 21: IV curves of 0 Ω up to 100 KΩ, using the same measurement setup as that used to measure the DNPUs at room temperature before dipping.

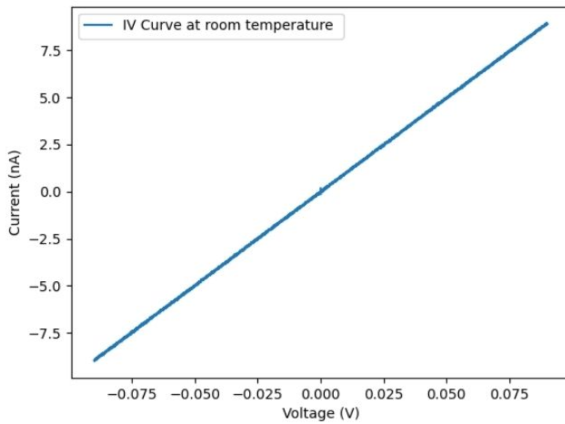
1 MΩ



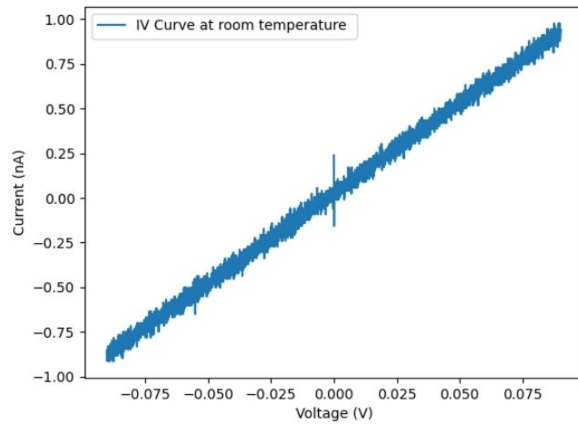
10 MΩ



100 MΩ



1 GΩ



∞ Ω (open circuit)

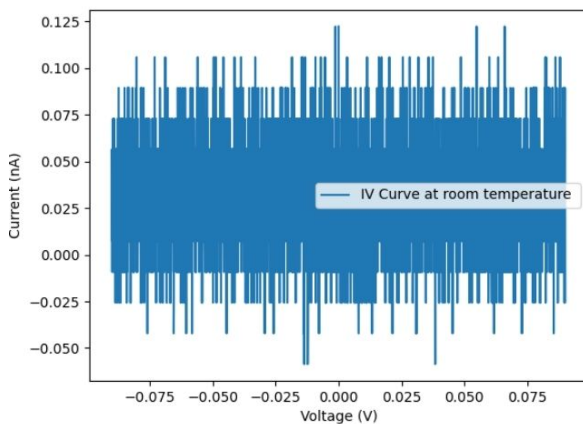


Figure 22: IV curves of 1 MΩ up to ∞ Ω (open circuit), using the same measurement setup as that used to measure the DNPUs at room temperature before dipping.

7.1.2 Broken electrodes, scrambled curves

When connecting the probes and measuring the IV curve, some connections show a scrambled signal, this connection type is defined as broken. Looking at Figure 23, an example of such a scrambled signal can be noticed. Moreover, noticeable is the low currents in the range of pA compared to the normal resistances, which strongly indicates that the picked up signal is noise related.

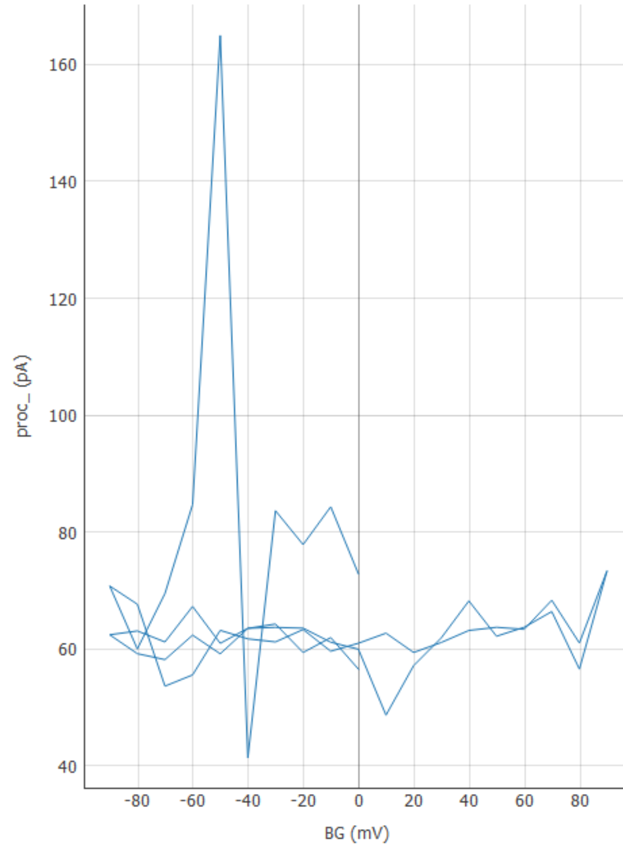


Figure 23: Scrambled signal of a broken connection between electrode 2 and 3 of device 3-1 chip 1 batch 5.

7.1.3 Shorts and very low resistances

A short or very low resistance, means there is clipping taking place at the readout voltage, which is considered 90 mV. An example of a device with a low resistance can be seen in Figure 24. The graph seems to reach 1 nA at +-10 mV, which means the resistance value is around 10 KΩ. This is peculiar low, considering that a lot of resistance values found on the DNPU are in the range of MΩ (where they don't clip in this setup). These shorts and very low currents were labeled as undesirable. The number of shorts and/or low resistances, when compared against the rest of the connections, were found to be relatively rare and out of the average resistance range of the other measurements.

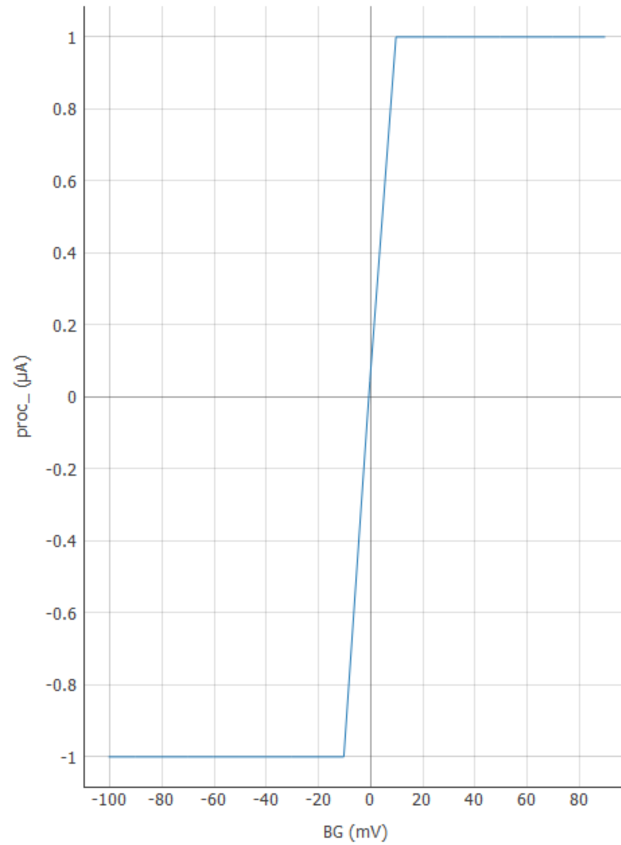


Figure 24: Very low resistance in a DNPU connection, clipping occurring at around 10 mV at a value of 1000 nA.

7.1.4 Non-linear curves room temperature

Room temperature measurements also showed graphs with non-linear behavior, which is not consistent with Ohm's law. This non-Ohmic behavior, could for example be caused by some non-Ohmic structures discussed in the theory. The DNPU device contains a Schottky barrier (in principle all metal to semiconductor contacts on chips), which behaves non-linear at room temperature. These non-linear curves were not considered broken or completely out of the ordinary, as about 2 to 3 (sometimes less, sometimes more) connections in a device showed this non-linearity. So there is still potential to show non-linear behavior at 77 K. It should however not be able to show tunable non-linear behavior as it behaves as a Schottky barrier. Unfortunately this tunability at 77 K was not tested during experimenting.

Two kinds of non-linear curves could be found. The first kind seems to have a vertical asymptote in the positive voltage plane and a horizontal one in the negative voltage plane, as shown in Figure 25. The other kind has it the other way around, so a vertical asymptote in the negative voltage plane and a horizontal asymptote in the positive voltage plane, as shown in Figure 26.

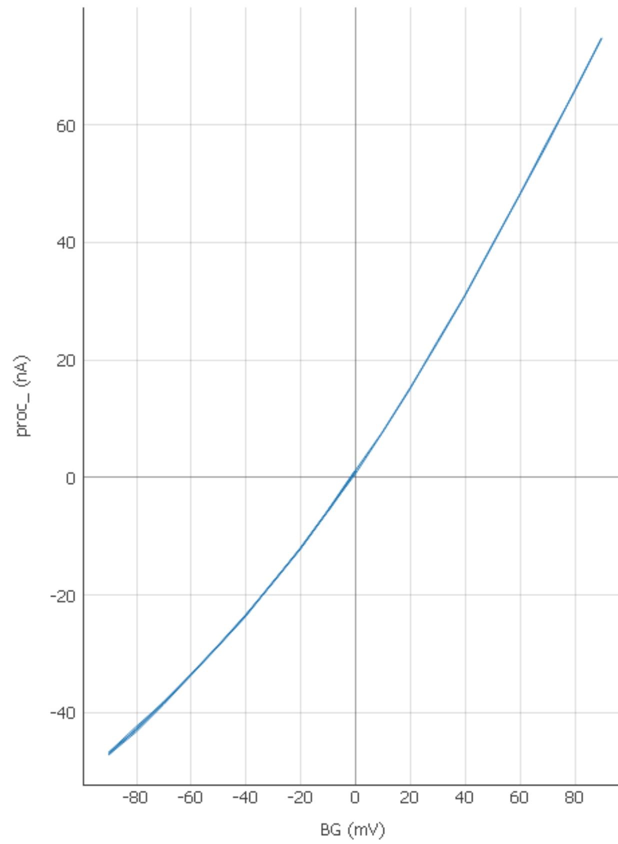


Figure 25: Batch 5 Chip 1 Device 4-4 Connection 6 IV curve at room temperature.

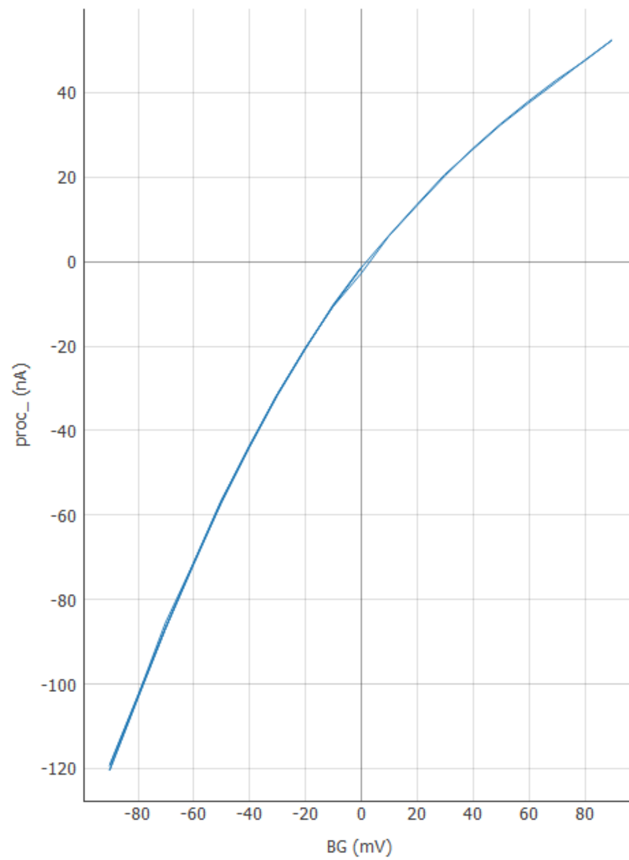


Figure 26: Batch 5 Chip 1 Device 4-4 Connection 7 IV curve at room temperature.

7.2 Criteria to select potential chips

Based on some of the findings described above, a set of criteria was used in order to classify devices that have the potential to work properly (show tunable non-linear behavior). The following criteria are used:

1. The device cannot contain any broken connections. With broken is meant that the IV curve of the connection gives a scrambled signal.
2. The device cannot contain any connections that is shorted or has such a low resistance that it's clipping at the readout voltage (90 mV).
3. At least 6 out of the 8 connections need to have a current around the same value +- 20 nA difference.

7.3 First room temperature measurement

Below here, an overview is represented of the batches and chips that have been measured at room temperature before wire bonding. The data in the table represents the amount of devices on a chip that show potential to work according to the criteria specified in Section 7.2. After a small calculation, the estimated chances of finding a potential device come down to 33,8%. This means that about 1/3 of the devices show good potential according to the specified criteria.

Table 2: Summary of the room temperature measurements with the probe station on all the batches and chips available at that moment.

Batch number	**Chip number**	**Number of devices on chip**	**Number of connected devices**	**Measured devices**	**Potential devices, according to criteria**
1	**1**	16	11	3	1
	2	16	11	11	4
	3	16	11	11	4
	4	16	11	11	1
	5	16	11	0	0
2	**1**	16	11	4	2
	2	16	11	0	0
3	**1**	16	11	3	0
4	**1**	16	11	0	0
	2	16	11	0	0
	3	16	11	0	0
	4	16	11	0	0
	5	16	11	0	0
5	**1**	16	16	16	10
6	**1**	4	4	4	0
	2	8	8	8	2

7.4 Room temperature measurements after wire bonding

In the initial measurement phases, no extra room temperature measurements were performed after wire bonding. To see the influence of wire bonding on the device characteristic, some devices were measured after the wire bond session before they were dipped.
In Figure 27 we see several connections of batch 4 device 1-2. Unfortunately, it was later found out

that this chip was measured upside down at room temperature, so only connections 1, 2, 5 and 6 are included for this data(these are still valid upside down). It can be seen that the current ranges don't differ more than a few to 5 nA from each other. This means that the resistance range stayed the same and all of the electrodes survived the wire bonding.

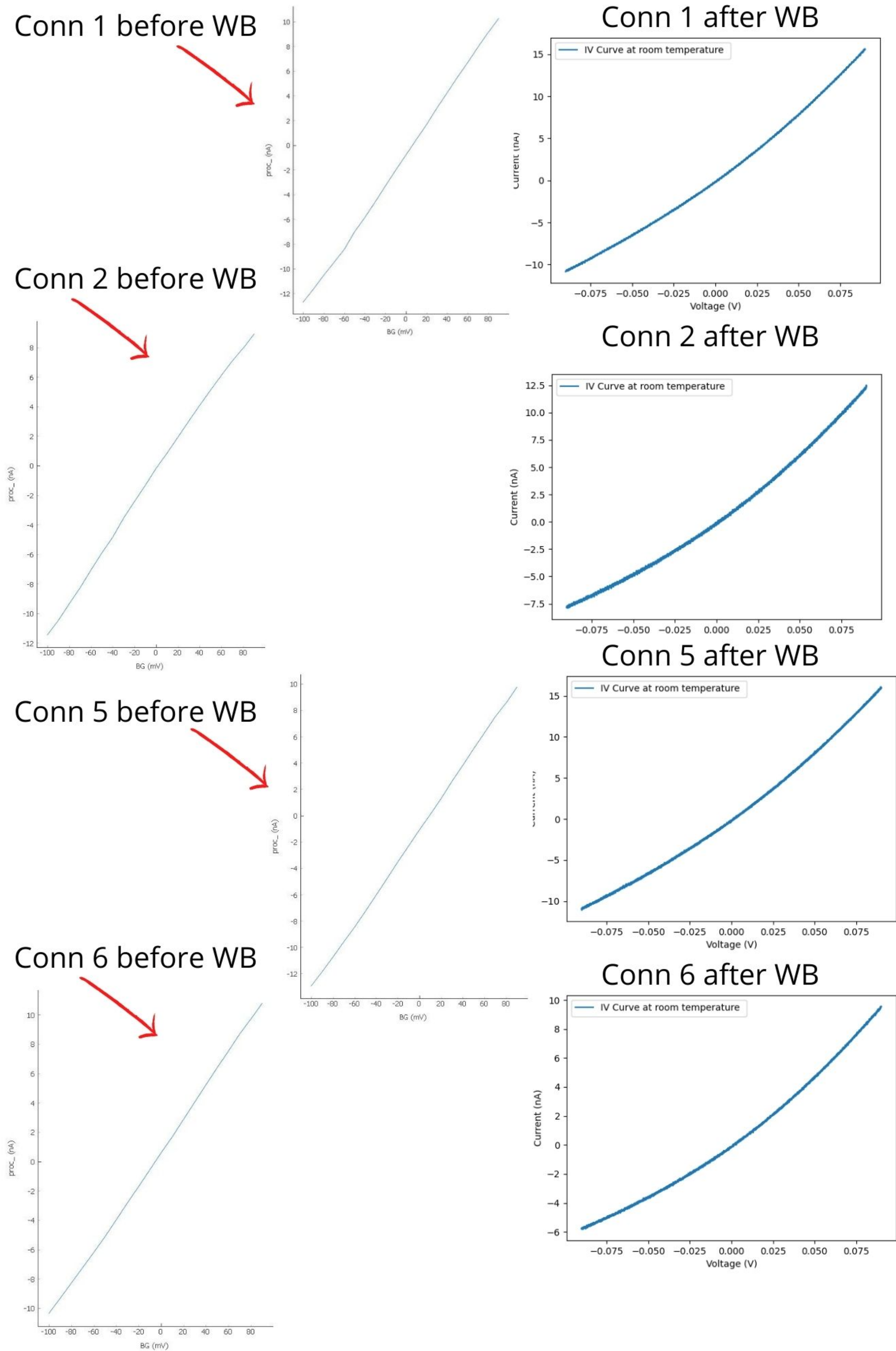


Figure 27: Batch 4 chip 1 device 1-2, before and after wire bonding. The graphs are different, as different setups were used to measure at room temperature (dipstick and probe station).

Another test on Batch 5 chip 1 device, showed that the device does get destroyed after wire bonding, while taking precautions into consideration. These figures have been compared in Figure 28 and Figure 29.

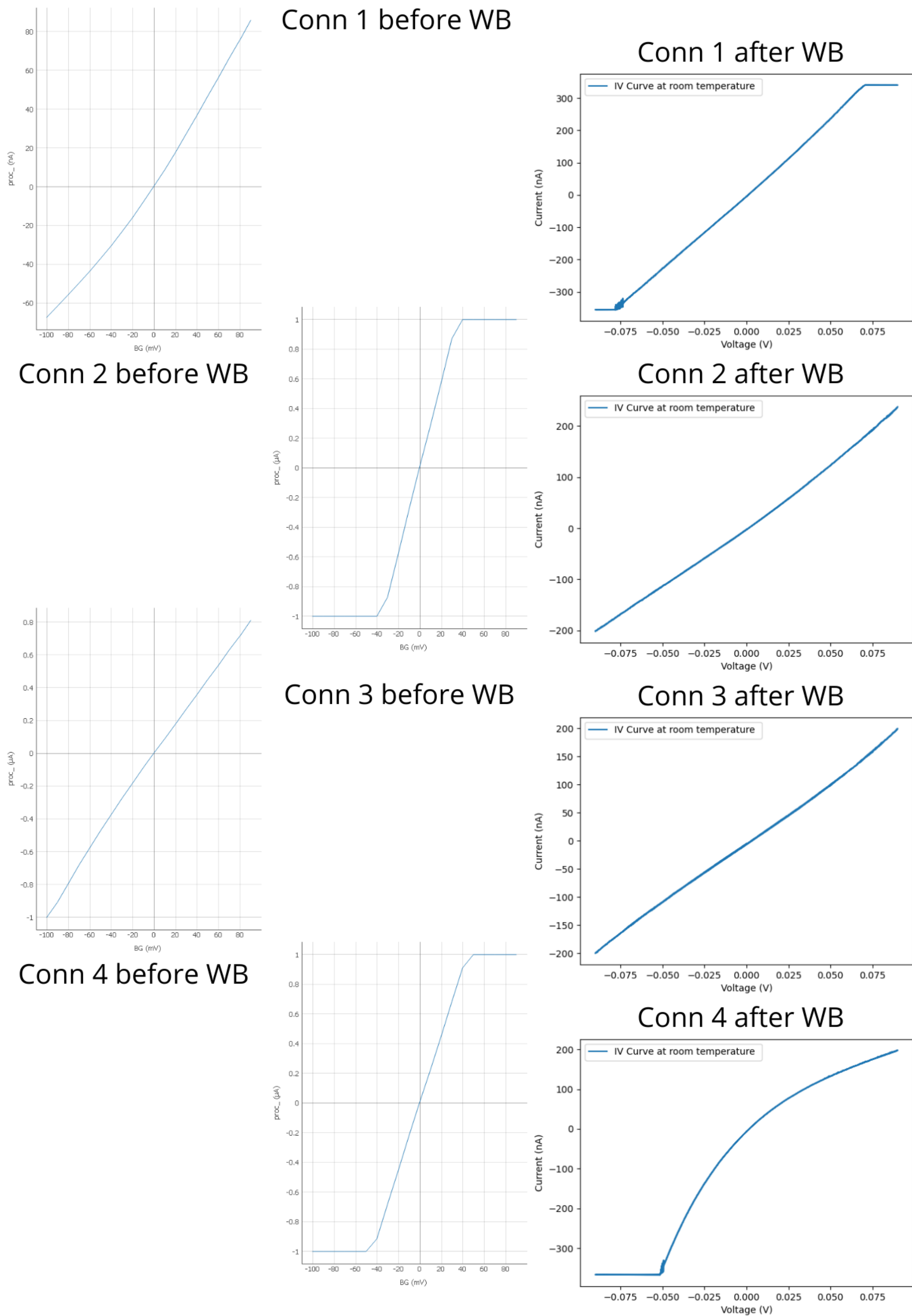


Figure 28: Batch 5 chip 1 device 4-2 connections 1 until 4 before and after wire bonding. The graphs are different, as different setups were used to measure at room temperature (dipstick and probe station).

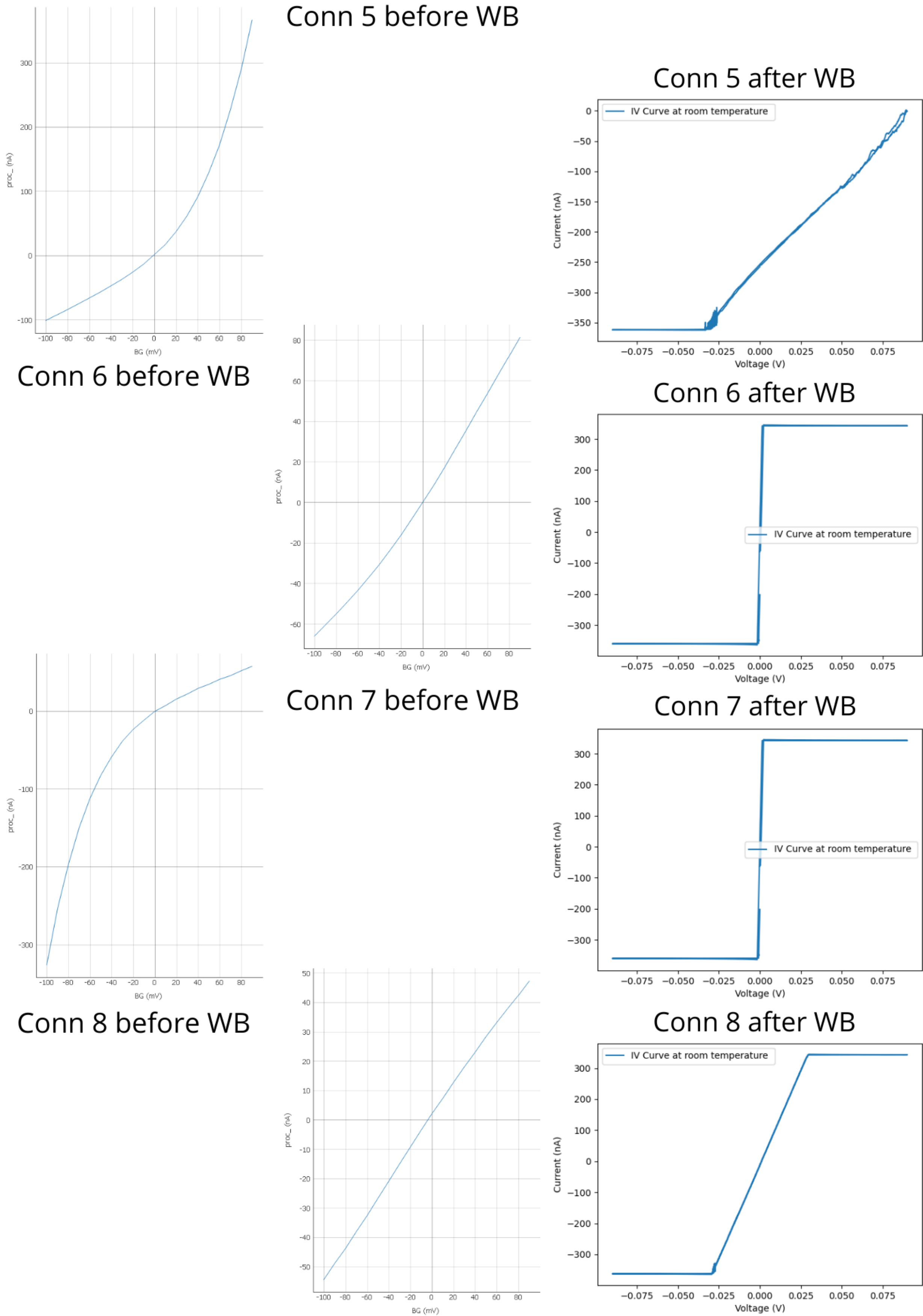


Figure 29: Batch 5 chip 1 device 4-2 connections 5 until 8 before and after wire bonding. The graphs are different, as different setups were used to measure at room temperature (dipstick and probe station).

7.5 77 Kelvin

After performing measurements at room temperature and preparing the chips for dipping, they need to be dipped into liquid nitrogen to test for tunable non-linearity.

7.6 Different Input, Control and Outputs(ICO) configurations three phased measurements

To test out the influence of the placement of the input, output and control, a test with several different ICO configurations was performed.
Looking at the data of this three phased measurement in Figure 30 up to Figure 35, it can be seen that the placement of the control electrode of 0 V does not influence the IV curve. In Figure 30, for example the input was placed on electrode 1 and the output was placed on electrode 3. This graph shows a non-linear curve with current ranging between -4 and +4 nA. In Figure 34 the input and output are the other way around; thus, input on electrode 3 and output on electrode 1. In this graph the curve is also non-linear and the resistance range is comparable (-7 up to 10 nA). The same is shown in the other combinations of input and output. For this reason ICO configuration 1 was used in the three phased measurements.

Note that the graphs headers can be a little confusing, which is due to the code that outputted the graphs. The output, input ,and control electrode were not changed in the code, these were changed physically in the matrix module. This was done, because the output wires had to be changed physically in this setup. So pay attention to the description of the Figure for the correct input, control and output electrodes.

Table 3: Different ICO configurations on batch 4 chip 1 device 4-3, while keeping control voltage zero.

Configuration	**1**	**2**	**3**	**4**	**5**	**6**
Input	1	1	2	2	3	3
Control	2	3	1	3	2	1
Output	3	2	3	1	1	2
Results	See Figure 30	See Figure 31	See Figure 32	See Figure 33	See Figure 34	See Figure 35

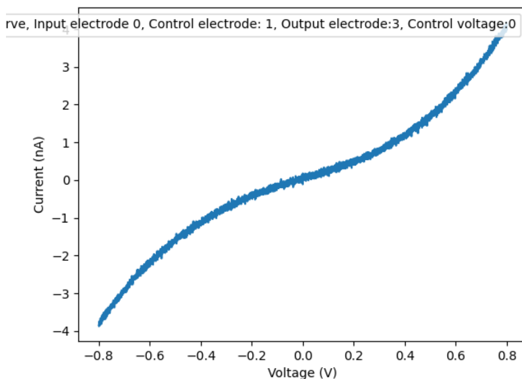


Figure 30: IV curve three phased measurement, Input = 1, Control = 2 & Output = 3, Control voltage = 0 V.

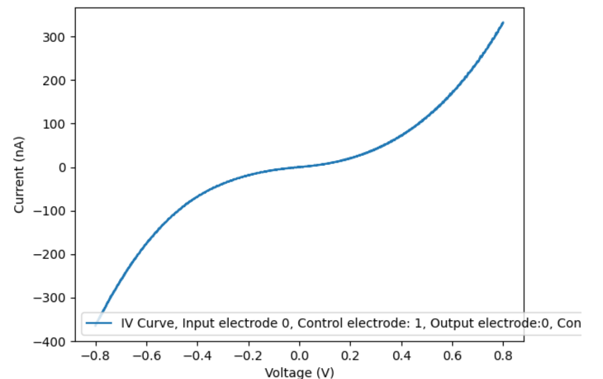


Figure 31: IV curve three phased measurement, Input = 1, Control = 3 & Output = 2, Control voltage = 0 V.

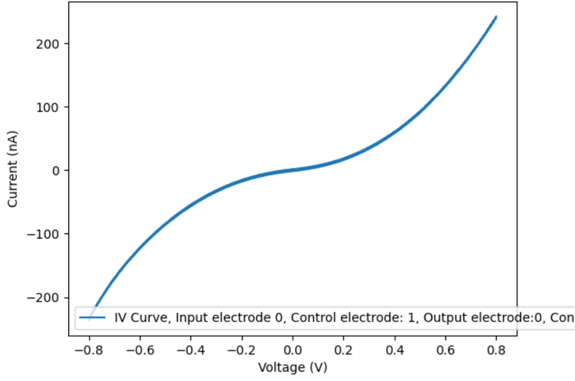


Figure 32: IV curve three phased measurement, Input = 2, Control = 1 & Output = 3, Control voltage = 0 V.

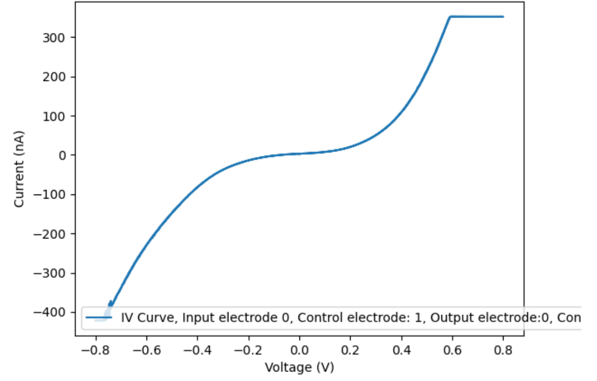


Figure 33: IV curve three phased measurement, Input = 2, Control = 3 & Output = 1, Control voltage = 0 V.

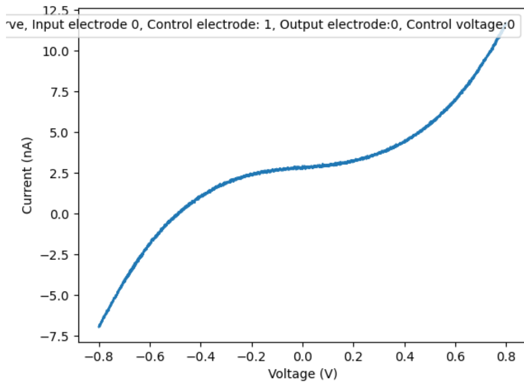


Figure 34: IV curve three phased measurement, Input = 3, Control = 2 & Output = 1, Control voltage = 0V.

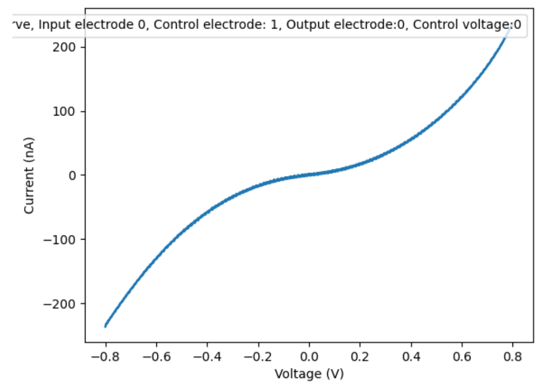


Figure 35: IV curve three phased measurement, Input = 3, Control = 1 & Output = 2, Control voltage = 0V.

7.6.1 Arsenic chip, graphs at 77 Kelvin of a working device

A working Arsenic doped (n-doping) device has been tested to see how it behaves at 77 K. In Figure 36 we see the IV curves at 77 K of all device connections. It can be seen that some of them have a small clipping, so these connections are a little bit out of bounds, but overall the connections show very good non-linearity. The main difference with the non-Ohmic contacts that were discussed in the theory section is that these connections don't rectify (no reverse breakdown voltage) and have almost no to none leakage current (the line is completely flat). There can be seen some hysteresis, which can be caused by some capacitive cross talk within the wires of the setup.

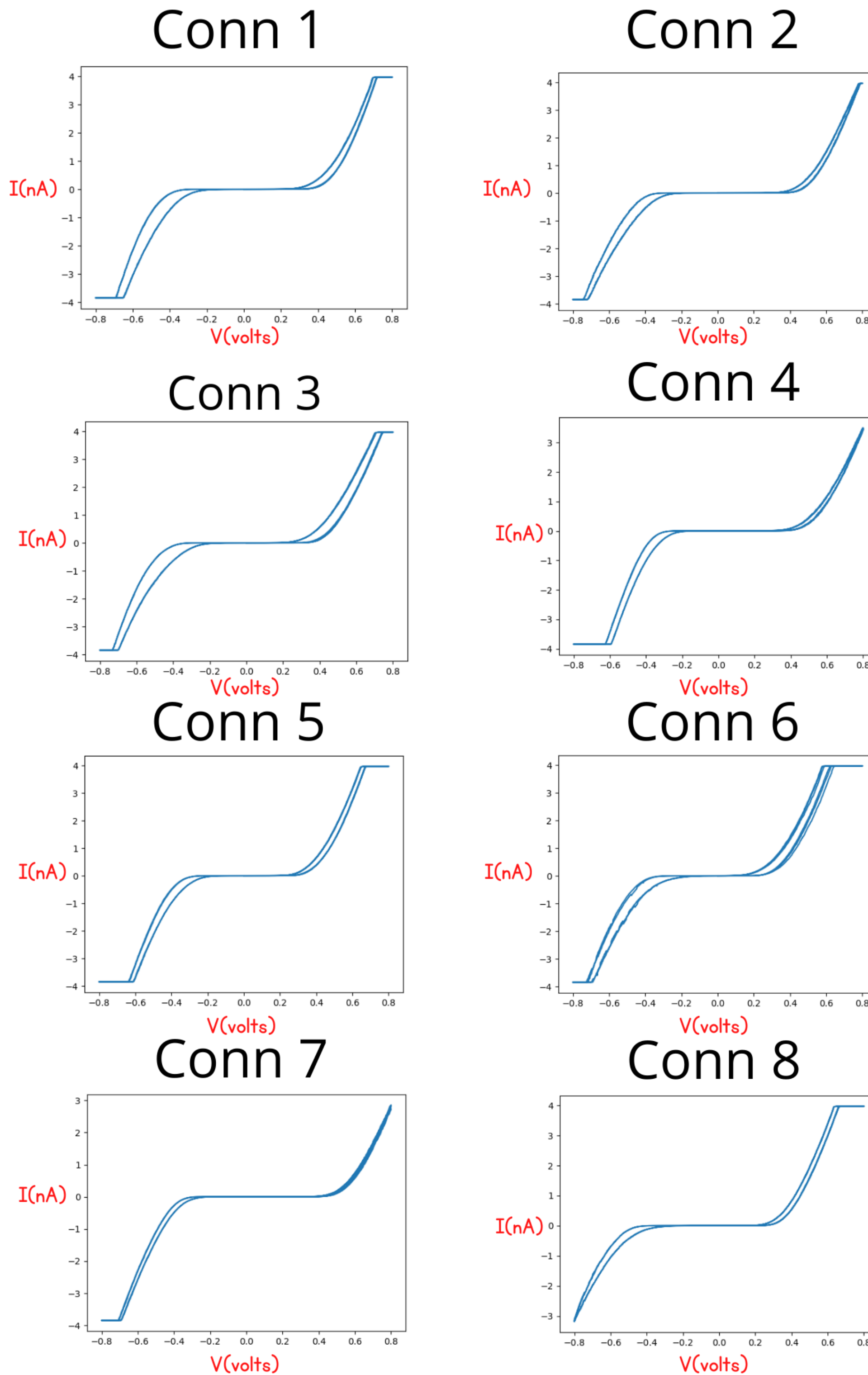


Figure 36: The IV curves of the connections on one of the working Arsenic doped devices, dipped in liquid Nitrogen in the Switch setup.

To check for tunability, connection 4 and 7 were subjected to a three phased measurement. The result of this three phase measurement test is plotted in Figure 37 and Figure 38. In these figures NDR shows when negative voltages are applied to the control electrode. That means tunability can be achieved using these connections.

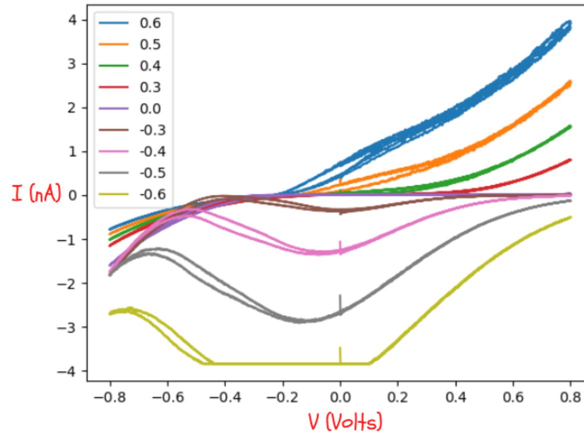


Figure 37: A three phased measurement in ICO configuration, with different applied control voltages on connection 4 of the working Arsenic doped device.

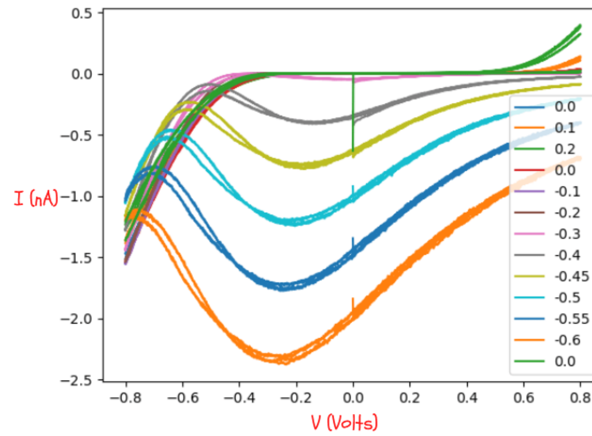


Figure 38: A three phased measurement in ICO configuration, with different applied control voltages on connection 7 of the working Arsenic doped device.

To test the device for it's ability to reproduce rest of the connections an XOR classifier test has been performed. The resulted fitness of this classifier is shown in Figure 39. The result shows an increase in the fitness over the span of several generations. This is a positive result, as it means the training improves the ability to mimic this XOR logic gate, and therefore it can resolve non-linear tasks. In the second graph it's shown that at the maximum achieved fitness of 1.39, the algorithm actually mimics this XOR gate (See Figure 41). XOR is defined as 1 for 01 and 10, the input signal in Figure 40 overlaps with the data at the right moment for XOR to occur.

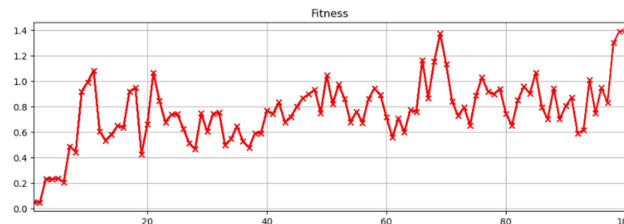


Figure 39: Fitness results over several generations.

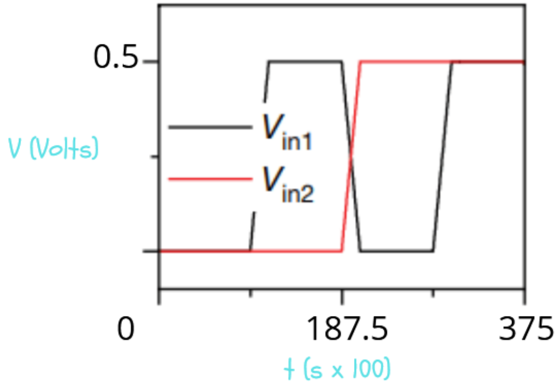


Figure 40: Input signal into the two inputs of the DNPU. Adapted from [2]

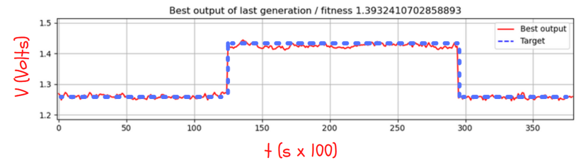


Figure 41: The Boolean logic compared to the target at the best achieved fitness of 1.39. This target has been drawn in by hand, as the real target was shifted down a lot.

Unfortunately the dipped Arsenic chips couldn't be measured at room temperature, but other Arsenic devices have been measured at room temperature. The difference between these Arsenic devices is the reactive ion etching depth applied. This influences the resistance range. Chip 2 had a different etch depth, so has a slightly different resistance than the dipped chip. Combining the resistances of all the devices, we get to an average resistance of about 0.173 MΩ.

Table 4: Batch 6 chip 2. The average resistances of the working connections of all measured devices on the arsenic chip.

Device	**4-1**	**3-1**	**3-2**	**2-1**	**1-1**	**1-2**
Average resistance (Ω)	0.11 MΩ	0.189 MΩ	0.187 MΩ	0.213 MΩ	0.145 MΩ	0.175 MΩ

7.6.2 Criteria 77 Kelvin

When looking at the IV curves at 77 K of the working arsenic chip in Figure 36 it can be seen that they all have a relatively flat curve between -0.4 and +0.4 V and that their non-linear currents within -0.8 V to +0.8 V are within the range of -4 up to + 4 nA. As different etching depths were used for the Arsenic chip, which influences the current, the 4 nA range cannot be used as a general argument. So an IV curve measurement on an Arsenic doped chip needs to have the following criteria to be classified as working:

1. Show non-linearity
2. A flat curve between -0.4 V and +0.4 V
3. The current range on both sides has to be about equal

Since no measurements with working boron doped devices have been performed. It's not sure if these criteria also holds for the boron doped devices. Thus, as a guideline for the boron doped devices, the picture from Tao Chen et al.[2] will be used. This picture is also plotted in Figure 10. At 77 K the non-linear line seems to run flat between -0.1 V and +0.1 V and the current range of the connection is within -0.9 and +0.9 nA at a voltage range of -0.75 V to +0.75 V. The criteria for the boron doped devices is thus:

1. Show non-linearity
2. A flat curve between -0.1 V and +0.1 V
3. The current range on both sides has to be about equal

7.6.3 IV measurements at 77 Kelvin

On several promising devices three phased measurements with a control voltage of 0 volt have been tested to test for their non-linear behavior.

Table 5: The number of working electrodes at 77 K of several different chips from different batches according to the specified criteria. These were then compared to the average resistance of the device itself.

Batch and device	Percentage number of connections adhering to criteria compared to the measured amount of connections (input reference)	Average resistance range of all working connections on the device at room temperature
Ba_1_ch_2_dev_1_2 (Boron doped)	37.5 % (3/8)	4.85 MΩ
Ba_1_ch_3_dev_4_2 (Boron doped)	25 % (2/8)	0.757 MΩ
Ba_1_ch_4_dev_3_3 (Boron doped)	57.14 % (4/7)	1.33 MΩ
Ba_2_ch_1_dev_4_4 (Boron doped)	0 % (0/8)	10.4 MΩ
Ba_4_ch_1_dev_1_2 (Boron doped)	0 % (0/4)	9.11 MΩ
Ba_5_ch_1_dev_2_4 (Boron doped)	62.5 % (5/8)	2.94 MΩ

The data from Table 5 has also been plotted in Figure 42, according to this data the resistance of the connections on the boron doped device seems to have an optimum at about 2MΩ. These connections were not tested on tunability however, so non-linearity could have been formed by Schottky barriers or other non-Ohmic structures. To what extent this plot is accurate is thus unclear, a lot more data points would need to be collected to clarify and backup these results.

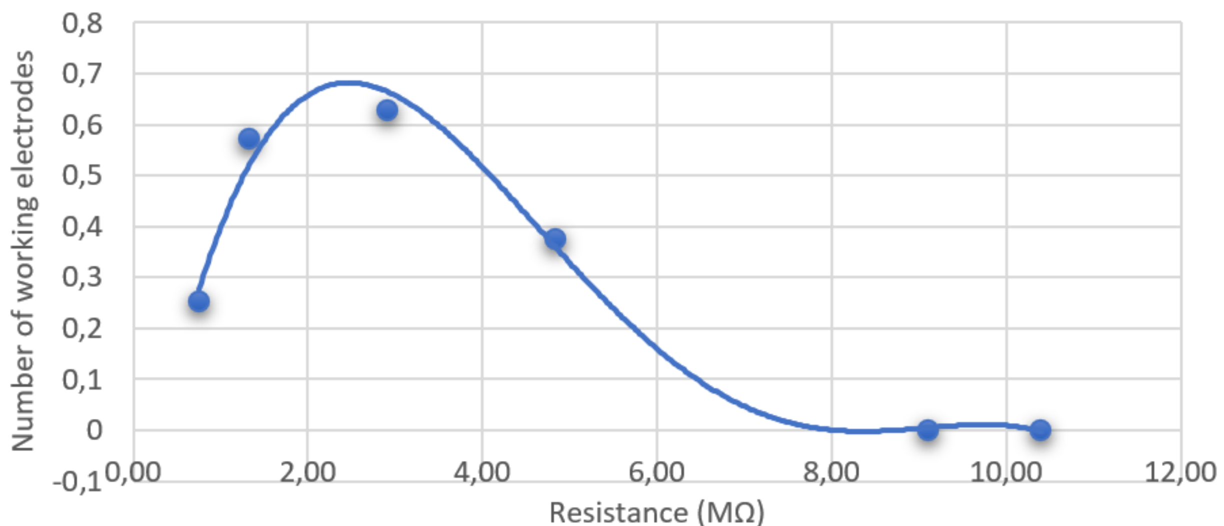


Figure 42: The resistance of the working connections on the chip at room temperature compared the amount of electrodes classified as working at 77 K.

7.7 XOR classifier test result

The classifier tries to change the potential landscape over the course of several evolution, such that it can mimic the Boolean XOR gate. All batches that were dipped and classified can be seen in Table 6.

Table 6: XOR classification results containing the best fitness achieved in the Genetic Algorithm, the training accuracy(so how good can it mimic the XOR gate) and the judgement if it works or not is in the last column (so does the training data actually mimic XOR logic).

Batch, chip and device	Best fitness	Training accuracy	Does the graph mimic XOR Boolean logic?
Ba_1_Ch_2_dev_1_2	0.4	50 %	No
Ba_1_Ch_3_dev_4_3	0.356	67.5 %	No
Ba_1_Ch_4_dev_3_3	0.35	50 %	No
Ba_2_Ch_1_dev_4_4	0.4251	37.5 %	No
Ba_5_Ch_1_dev_2_4	0.38	68 %	No

7.8 Classifier with changed IO configuration

In Figure 43 the training accuracy of the first classification of batch 5 chip 1 device 4-2 has been plotted.The configuration used in the first classification:
Inputs: Electrode 1 and 2
Output: Electrode 8
Control: Electrode 3, 4, 5, 6 and 7

This configuration was however sub-optimal, due to the fact that some of the electrodes on these graphs didn't show promising IV curves. By changing this configuration, so that the input and output were connected to good functioning electrodes, an improvement from 58.5% to 68% accuracy was achieved when classifying. This second configurations was configured as follows:
Inputs: Electrode 2 and 7
Output: Electrode 5
Control: Electrode 1, 3, 4, 6 and 8

It seems that this configuration had more influence on the potential landscape, which caused the the classifier to mimic the Boolean logic gate better. This is also deducted from the maximum fitness that was achieved. For the first configuration, the max fitness was approximately 0.34 and for the second configuration the max fitness was 0.38. The higher fitness makes sense when looking at the figures. The pearson correlation in fig. 44 is higher, because the points are more grouped together along the line. The signal is still however random due to the linearity in the output waveform. It is stacking the inputs on each other to form the output.

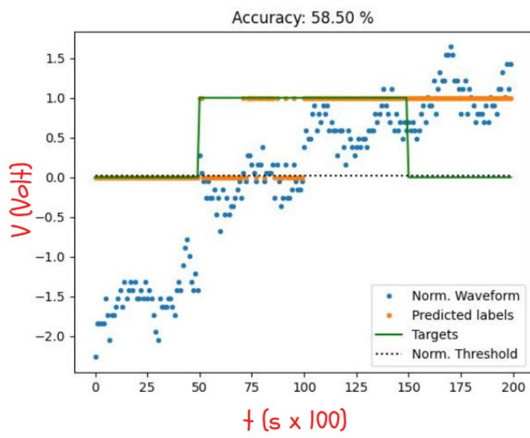


Figure 43: Batch 5 chip 1 device 4-2 training accuracy after classification in the first configuration.

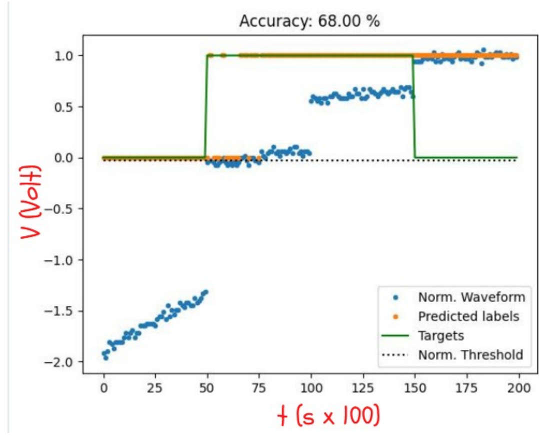


Figure 44: Batch 5 chip 1 device 4-2 training accuracy after classification in the second configuration.

8 Conclusion

The main question research question of this thesis was as follows:
What characteristics of DNPU's at room temperature indicate working devices at 77 Kelvin? In order to answer this question, a set of criteria to find potential devices at room temperature were derived (see Section 7.2). These criteria formed the basis of selecting potential devices suitable for measuring at sub-zero temperatures. From the total of 24 potential devices, 6 were wire bonded and dipped. The overall resistance characteristics of these dipped devices was compared to the percentage of connections adhering to the criteria for a good non-linear graph at 77 K. These criteria were based upon the measured working arsenic device that was available in the lab and on the boron doped device presented in the paper of Tao Chen et al. [2]. The trend line in Figure 42 shows that resistance could be a potential characteristic choice for finding working electrodes, and consequently, potential working devices. The resistance contains a sweet spot at around 2 MΩ. The theory discussed the hopping regime, which is related to the doping concentration and the temperature. The doping concentration influences the conductivity, and subsequently, the resistance of the material. Therefore, there is strong reason to suspect that there should be an optimum resistance in the device. However, the amount of data collected on these dipped devices is relatively low and the connections were not tested for tunable non-linear behavior, which could mean the non-linear graph is a Schottky barrier or other non-Ohmic contact. In order to draw a better conclusion on what resistances at room temperature are indeed strongly connected to non-linear characteristics at 77 K, more data is needed. Conclusively, DNPUs can be characterized at room temperature with IV curves. Scrambled IV curve represent broken electrodes and can indicate devices with less potential to work at 77 K. The resistance of the IV curve is another indicator for possible working devices at 77 K, because resistance is strongly coupled with the hopping regime, which is required for tunable non-linearity. Tunable non-linearity was however not achieved in the classifier tests (see table 6).

The side question this thesis tried to answer was:
How can we optimize the measuring process, while eliminating bottle necks?
This side research question was intended, to improve and accelerate the measurement process for future measurements. Improvements were found in, for example, the wire bonding, which had influence on the characteristics of the device as the IV plots of the device changed (see Section 7.4). Another founding was that changing the input, control, and output in a classification could improve the fitness of a Boolean XOR classification. Therefore, based on some of these outcomes while experimenting, a manual has been created that shows the best approach to find working devices, with the current measurement tools. Safety features, like extra grounding, have also been included. This manual with the best measuring process flow is put in the appendix, see Section 9.1. Some conditions that could still be improved time and process wise in the measurement process are:

1. The PCB used for the experiments presented in this thesis could only contain one chip per time. Having a PCB that can contain more chips, would potentially speed up the process flow.
2. The wire broke of a lot when wire bonding, due to the fact that the chip was to big for the PCB. The chip overlapped some of the electrical pads. This made it necessary to wire bond not the rectangular pads, but the circular pads that were connected to the rectangular pads. This made it hard for the wire to stick to the surface and cause it to break. Effort into designing a PCB that the chip could fit on correctly, would be effort well spent.
3. Wire bonding and dipping, were the main bottle necks in the speed of the measuring process, as they both could take up to half a day each. Especially, when the wire bonder broke down, which took a lot off time to fix. A good improvement is to introduce an automatic wire bonder or flip chip bonding instead of manual wire bonding. Flip chip bonding attaches the chip to the PCB by flipping the chip upside down on the PCB. The chip hereby contains metalized particles on it's connection pads. By aligning the chip and PCB properly, they can thus be simply connected by pressing them together [5].
4. To omit the bottle neck of dipping a good suggestion is to spend some time doing research on room temperature measurements with a back gate to suppress the conduction band. If working

properly, this could indicate working devices at room temperature, which saves the hassle of dipping. Another even better suggestion is to combine wire bonding and back gate measurements. By bonding the device first, including connecting the back gate, room temperature measurements can be done with software. Using software means you can start up the measurement and automatically run several tests, which saves up time. Another advantage is that the chances of killing a device due to electrostatic discharges when wire bonding decreases, as you have already bonded the device. Thus, this could potentially save an extra room temperature measurement. If a device shows working features, it can then be dipped immediately.

8.1 Further experimenting

Further research is needed to find the optimal boron doping concentration for working devices.
Also research is needed into applying a back gate at room temperature to check for working devices in order to improve the measuring process.
And lastly extra research is required in finding out what exactly the behavior of non-linear graphs at room temperature is at 77 K, because tunability of these non-linear graphs has not yet been tested with a three phased measurement.

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9 Appendix

9.1 A

This part below here is the entire manual that can be referenced for future students, due to time constraints some parts of the manual might not be entirely finished yet:

9.1.1 sequence of steps to take in general

To fully characterize a device the following general steps were taken. These steps are outlined in detail in the method section to follow in the same order as below here.

1. We start off by taking the chips out of the vacuum pump.
2. Then we measure all devices on one chip at room temperature with the probe station in the dark box.
3. Now we place the chip onto the PCB and wire bond a device on the chip with the PCB pads.
4. We connect the PCB onto the dipstick and perform a room temperature measurement, while the chip and PCB are still connected to the dipstick. This is done in order to verify that wire bonding did not do any damage to the device on the chip.
5. Now we slowly dip the device in liquid nitrogen and let it cool down, after this we use three phased measurements to check for non-linear behavior at 77 K.
6. We can then run an extra classifier measurement still at 77 K to test whether or not the device can mimic an XOR gate.
7. If the chip works don't undip it. If the classifier was unsuccessfully undip the dipstick and let it cool down to room temperature.
8. Do an IV measurement at room temperature again while the device is still on the dipstick to test if the device still works.
9. Put the chip back in vacuum or wire bond a new device on the chip and dip it again.

Some general outlines when handling the DNPU chips:

1. Always handle the chips with gloves
2. Don't touch the devices on the chip
3. Pick up and handle the chip with tweezers that has rubber on the endpoints. Try to avoid metal tweezers, as these might give an electrostatic discharge if you accidentally touch one of the devices.
4. Always put the chips back into vacuum when you are not using them for a long time
5. When moving the chip around from lab to lab for example, keep it in the protective enclosure

9.1.2 Vacuum pump

- A vacuum pump is used to store chips in so that they don't get into contact with particles. These particles could be electrostatically loaded.
- Opening and closing of the vacuum pump should not take more than **2 to 3 minutes**

9.1.2.1 Equipment used

- Adixen Diaphragm vacuum pump AMD 1
- Bel-Art vacuum container
- Tubing
- Bruker and Gel-pak chip boxes(these contain an adhesive layer were the chips can stick on)
- Waterproof marker

9.1.2.2 Work flow

Step 1 few seconds

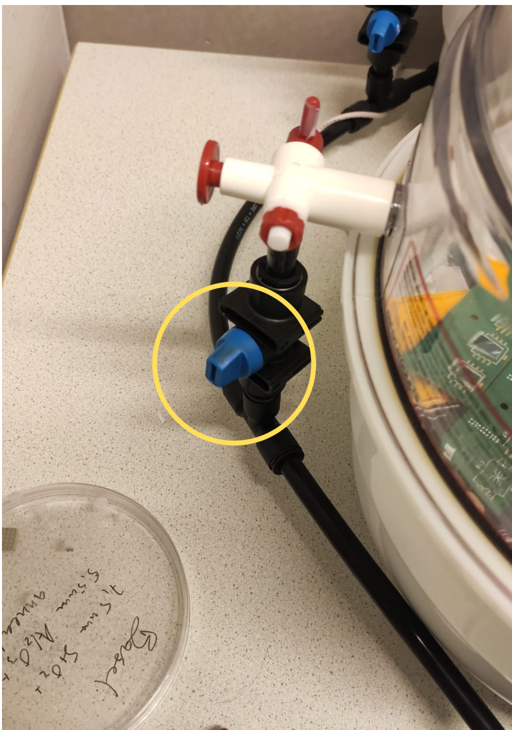

Figure 45: The blue button that regulates the air outlet to the vacuum pump

- To remove the glass top hat, first twist the blue button 90 degrees in the opposite direction of where it's stuck (it can only move one way). The blue button can be seen by the yellow encirclement in Figure 45.
- The blue button cuts off the suction

Step 2 few seconds

- Pull out the red little plug on the side of the the top
- This red plug let's the air into the top hat

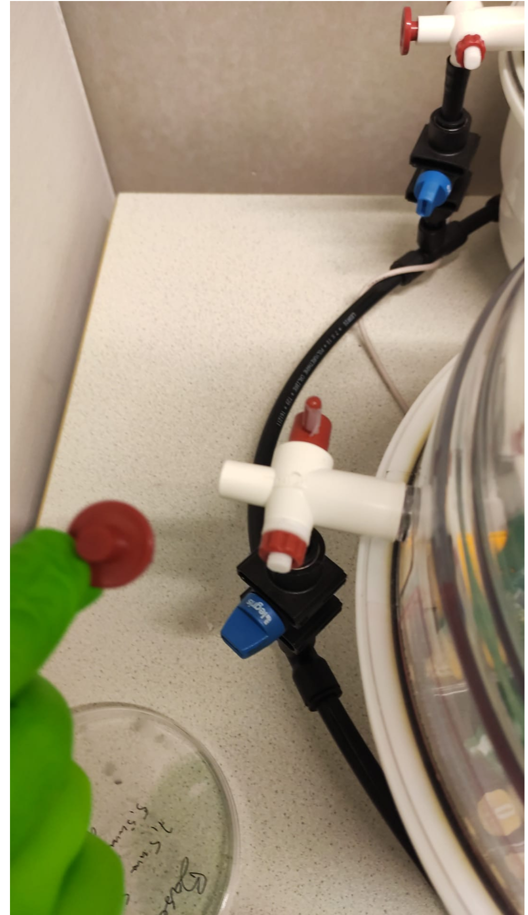

Figure 46: Pulling out the red knob on the side of the vacuum pump

Step 3 few seconds

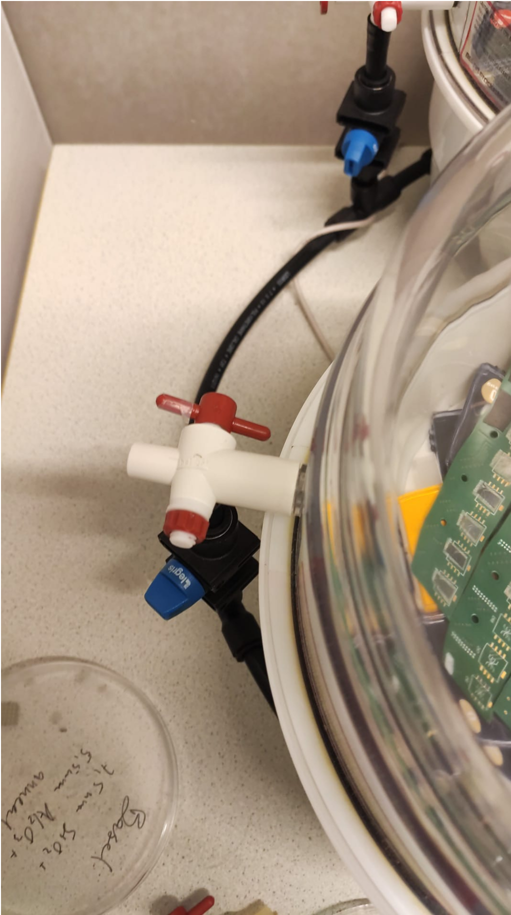

Figure 47: Twisting the red knob containing

- Twist the red knob with the plastic around to the opposite side of the transparent top hat. Figure 47
- This knob let's the air into the vacuum box

Step 4 1 minute

- Wait until all the air is out of the the vacuum box and lift off the top hat. Figure 48
- Repeat the steps in a backwards order to put a chip back into the vacuum box.

Figure 48: Lifting the top hat of the box

9.1.2.3 Extra need to knows vacuum pump

- Don't twist the red knob back with the adhesive tape to the bottom, doing this can cause the red button to suck itself stuck. So the next time you open it, you have to put a lot of force on the red knob. This can cause a violent burst of air to enter your vacuum pump blowing a lot of the chips away

- Make sure your chips are always protected within a special chip container were chips stick to the bottom of the container, letting in air could go wrong and blow the containers away. If the chips are loose in the container, they could get damaged. See figure Figure 49 for the containers I used.

Figure 49: Special chip boxes/containers that contain an adhesive layer to stick the chips in

9.1.3 IV measurements room temperature

- IV measurements at room temperature are done to characterize the devices, so we can see if any connections have shorts or if connections are broken(no connection at all)

9.1.3.1 Equipment used

- Everbeing dark box, including probes, microscope and plateau
- Schott lamp
- HP Elitebook 8560w with IV measurement software
- Keithley 2400 Source Meter
- Pincet with rubber ends

9.1.3.2 Work flow

Place chip in dark box 1 minute

Figure 50: Everbeing dark box

- Get the chip out of vacuum - Place chip in dark box and turn off the light, close the doors to prevent any light from entering.

Setting up 1 minute

- Start up the software under C:/qtNE in the file explorer
- Open up your measurement script
- Set the filename correctly for the right connection at the sample name in your measurement script. The following structure was used in our experiments: Batch$_C$hip$_D$evice$_C$onnection.$SofirstprovidetheBatc$ … $SeeFigure\ 51wereu$
$- Savethefile(ctrl + s)$

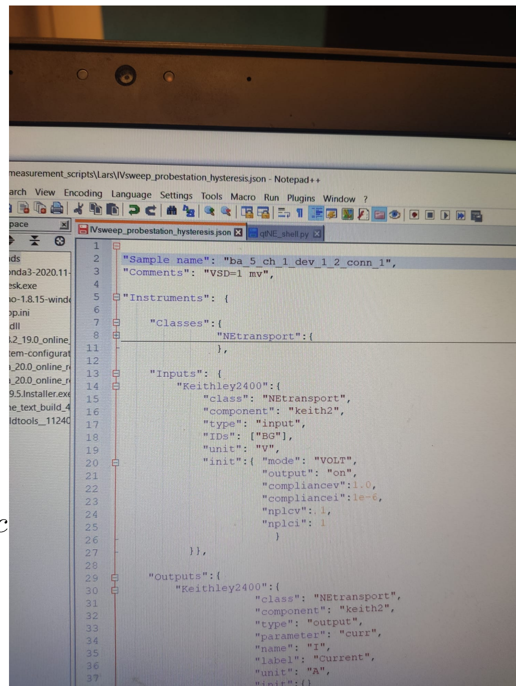

Figure 51: The measurement file that will be ran

Move the probe needles correctly 2 minutes

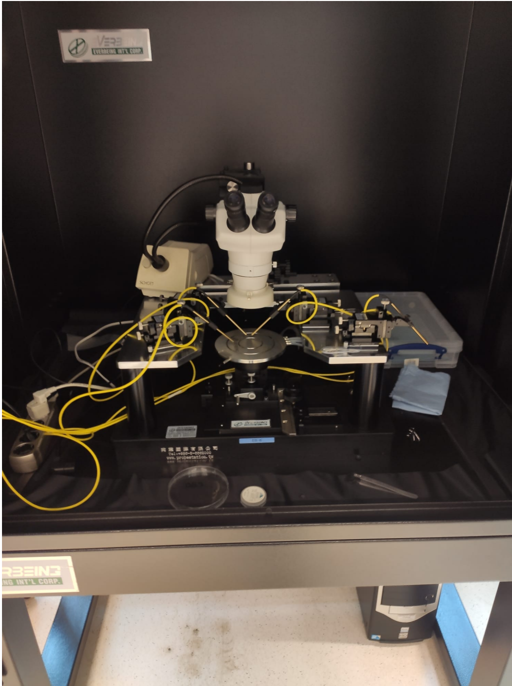

Figure 52: Probe station, including lamp, microscope and probes

- Turn on the light in the dark box
- Look into the microscope and move the needles onto the right Electrodes of the device
- See **??** 9.1.3.3 on how to move the needles
- Make sure you move the needle connected to ground first, to prevent any electrostatic discharge
- Watch until the needle slides over the electrode pad, then you know it makes contact.

Start up IV measurement 1 minute

- Open the measurement queuer
- Click on 'add file' and add your measurement file
- Start up IV-measurement. To minimize any damage, make sure the sweep starts and ends at zero volt(You can see this on the Keithley Figure 53
- The sweep voltage range for the hysteresis iv measurement is between -90 mV and + 90 mV to prevent damage at room temperature.

Figure 53: Check the Keithley in order to see the sweep voltages

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Re-configuring the needles 2 minutes

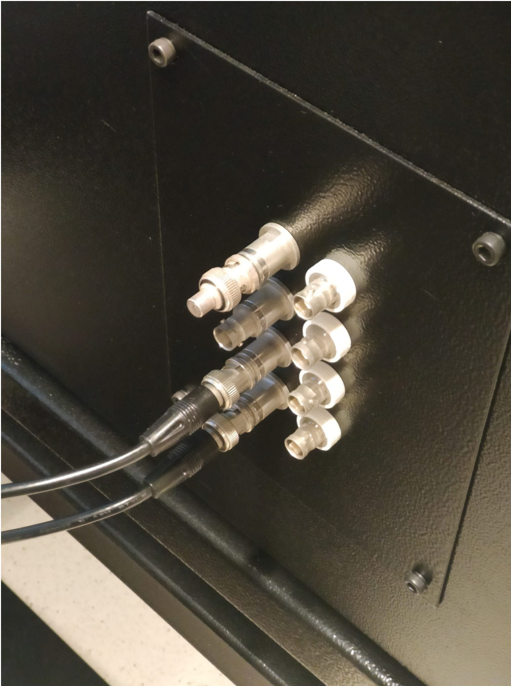

Figure 54: Ground connected to the dark box

- Move the the needles up again, make sure you move the input up first and then the ground. - Repeat the measurement steps done before here again for the entire device - Measure all the connections of the device. - Move up to the next device on the chip or start analyzing the data of one device or analyze the data immediately after one device.

Collecting bulk data and analyze data 5 minutes per device

As time and resources are limited, a way to analyze and find the devices with the most potential has to be implemented. For this purpose a set of criteria is used:

1. The device cannot contain any broken connections. With broken is meant that the iv-curve of the connection gives a scrambled signal
2. The device cannot contain any connections that is shorted or has such a low resistance that it's clipping at the readout voltage (90 mV)
3. At least 6 out of the 8 connections need to have a current around the same value +- 20 nA difference.

- My advise would be to collect the data in excel or a similar program, as data manipulation is a lot easier in here.
- In this excel label the batch number, device number and the connections. Specify for each connection if it works and/or if something is wrong (broken or short/low resistance for example). Also collect the current at a certain readout voltage, to have a good idea of the voltage range
- An example of how the data was collected for these IV measurements at room temperature can be seen in Figure 55

Batch X

Chip		Device	Potential option for dipping	
x	Connection	X - X	Current at readout voltage (nA)	Resistance range
	1	Short	1000	9,00E+04
	2	Broken	-	#VALUE!
	3	Works	25	3,60E+06
	4	Works, HC, SNLD	30	3,00E+06
	5	Works, GL	20	4,50E+06
	6	Works, WK	21	4,29E+06
	7	Works	24	3,75E+06
	8	Works	19	4,74E+06

Figure 55: An example of how the data was collected

9.1.3.3 Extra need to knows room temperature IV measurements

- Check your first graph after measuring.
- By changing the step size in the measuring software, you can create smoother curves. Be aware that increasing the step size, increases your measuring time.
- Moving the needles:
  - When standing in front of the dark box, you can move the needles horizontally by using the knob named 'center'. See Figure 56
  - You can move the needles vertically by using the knob named 'back'. See Figure 56
  - You can move the needles up and down with the 'up' knob that is on top of the probe. See Figure 57

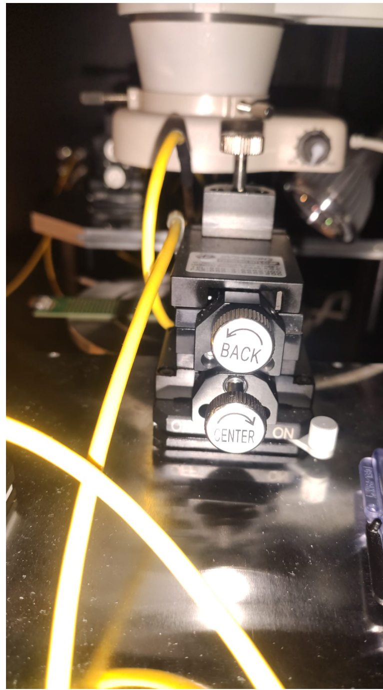

Figure 56: Back and center knob on the probes. Center is for horizontal movement, Back is for vertical movement

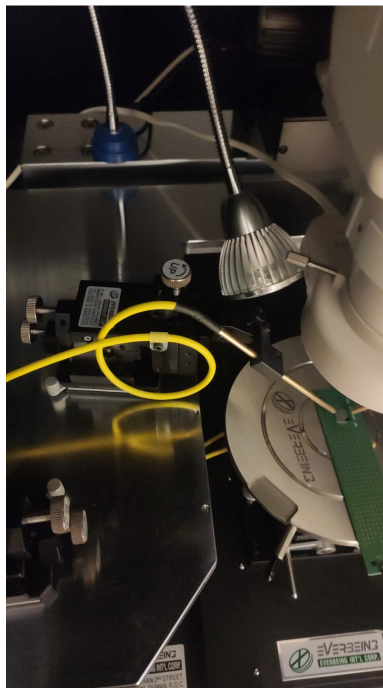

Figure 57: Up knob on the probes. Center is for horizontal movement, Back is for vertical movement

9.1.4 Wire bonding

9.1.4.1 Equipment used

- Wirebonder
- PCB designed by Utwente
- PCB holder

- Double sided tape
- Scissors
- Pincet
- Aceton
- Protection glasses
- High pressure blow dryer

9.1.4.2 Work flow

- In general, wear gloves through this entire process and handle the chip with care.
- Don't take the chip out of it's protective casing until the moment you need it.

Clean PCB 5 minutes

Figure 58: Aceton, Isopropanol 2 and the dry blower used to clean the PCB

- Put on your protection glasses and wear gloves. - Clean PCB with Acetone and Isopropanol-2(wear gloves and eye protection gear). Rinse liquids off with air blower.
- This is done in order to remove any excessive dirt and remove any layers of fat on the pads, so that the wire bond will stick better.

Add double sided tape on the PCB 3 minutes

- Attach small strip of double sided tape on the PCB in the middle of the pads.
- Make sure the double sided tape is cut to the correct size, so that it doesn't cover the metallic pads
- See figure Figure 59

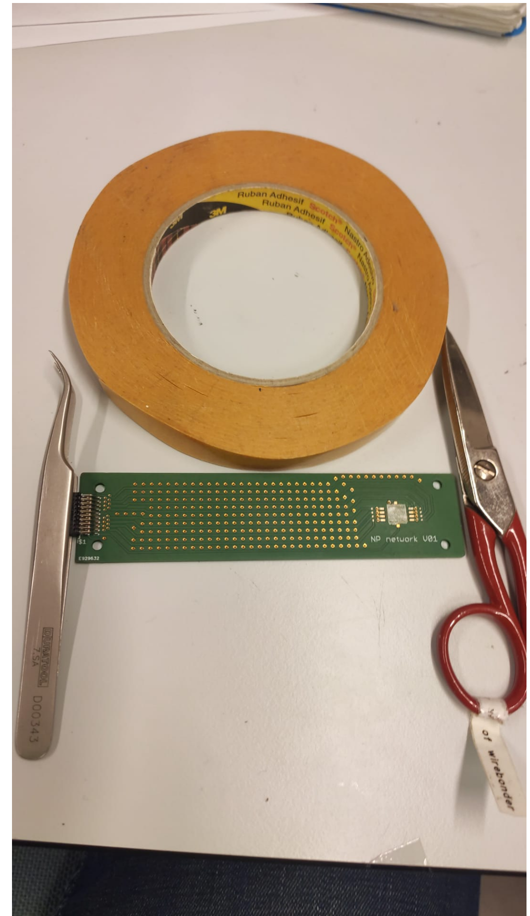

Figure 59: A piece of double sided tape attached onto the PCB pad

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place chip onto PCB 1 minute

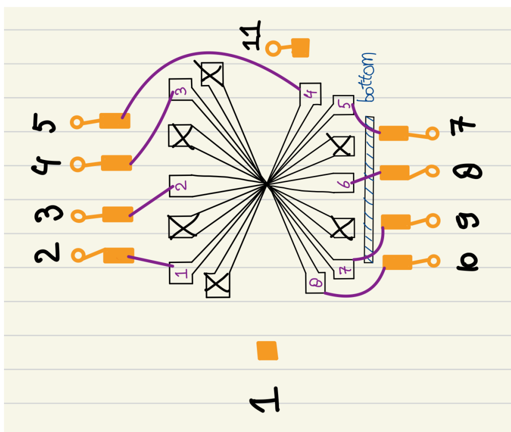

Figure 60: Left: The designed PCB. Right: The PCB connectors connection to the pads

- Attach chip(watch orientation! This saves up a lot of time later) and press firmly with tweezers on two edges at the same time
- The chip can be best oriented like shown in Figure 60, this has to do with the connection to the dipstick. This connection can be seen in Figure 63.
- Clean the chip now with Acetone and Isopropanol-2(wear gloves and eye protection gear). Rinse liquids off with air blower.

Grounding PCB 2 minutes

- Ground the PCB with the wire bonder by bonding a wire around the input pins and attaching this wire on the ground connection.

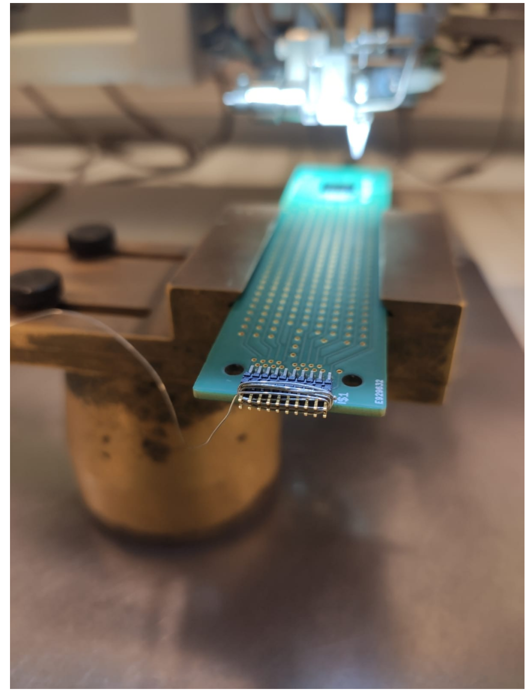

Figure 61: Wire wrapped around the connector pins of the PCB in order to ground it

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Grounding yourself 10 seconds

Figure 62: Wearing the grounding bracelet connected with the wire bonder

- Ground yourself with the device by using the bracelet

Placing PCB in metallic holder 10 seconds

- Place the PCB in the slid of the metalic holder
- Screw the black knobs in order to tighten the grip
- This place holder is needed for the correct height and to make sure the PCB can't move around
- There is a knob on the wire bonders plateau to put it even higher
- Move PCB around under the microscope until you see the chip
- Set the microscope with the correct zoom, so that you can see the entire chip and select the right amount of zoom
- Make sure the wire bonder is not out of reach of where you have to place your connections. Test this by keeping the wire bonder up while moving along the lines you want to place your wire bonds.

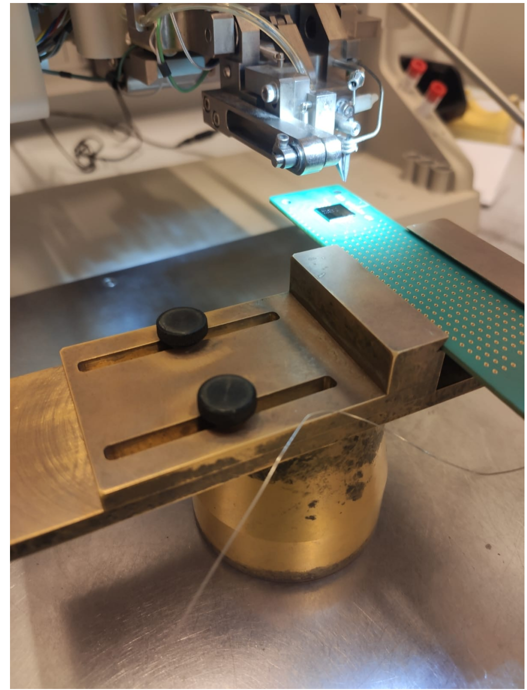

Figure 63: Metallic place holder containing PCB

Attaching wire bonds 30 up to 60 minutes

Figure 64: Wire bonder interface with buffer 30 selected

- Turn on the wire bonder and select buffer 30 with the buffer knob.
- Buffer 30 is defined as:
Power = 300
Time = 30 ms
Feed = 45 degrees
- To make a wire bond, place the needle down onto the substrate and wait until you hear a click. This click means the clamp is opened and the wire can feed through.
- Make sure to wire bond in a straight line as much as possible, going sideways may cause the wire to break off.
- Don't pull to hard on the wire bonder.

9.1.4.3 Extra need to knows when wire bonding

When wire bonding several issues can occur. The following issues are most common and can be best solved like so:

1. **Wire out of the feeding hole**
   Opening up the clamp and trying to deposit your wire onto the substrate can sometimes cause the wire to break off or snap out of the feeding hole. To solve this pull the wire far out of the tube and make sure the twist/kink of the wire is pointing upward right.
   Cut off the end piece of the wire, to make sure it isn't twisted/folded.
   Pick up the wire with a pincet and twist the wire such that it points downward towards the clamp of the wire bonder machine.
   Open up the clamp of the machine with the switch on the far left of it
   Now carefully push the wire against the lowest point of the tip, and move up and down a little,

don't push to hard. It's important you don't bent the wire
When you feel the wire is slightly in the hole, don't push it in, instead move it upward between the clamp and close the clamp
It should now be feeded through the hole of the pin
Open up the clamp again and pull the wire through
Cut off the residue wire

2. **Wire out of the tube**
   Good advise would be to use the pincets that have rubber end points
   use two pincets, place one behind the top hole of the tube to guide the wire slightly
   Use the other one to grab soft hold on the wire (with emphasis on soft! Grabbing on to hard may bent the wire, which makes it really hard to get it through the tube).
   slowly pull the wire through the tube

3. **Pin not aligned properly**
   Grab hold of a small mirror with a pincet
   hold the mirror below/behind the pin to check if the pin needs to move up or down in order to align it.
   Use the small hex key and twist the bolt slightly, so that the pin is loose
   pick up two pincets, hold the pin with one and move it up/down with the other.
   When aligned properly, screw bolt tight again and check with the mirror, while feeding the wire

4. **Pin clogged** Sometimes you can't get the wire through the hole, because a piece of wire or garbage is blocking the hole, this is why there are usually two pins in the lab
   Take a pincet and place a mirror below/behind the pin to check whether it is clogged or not (You can sometimes see a little blockade or a piece of wire hanging out of the hole).
   If it is clogged or if you're unsure, take out the pin by unscrewing the bolt(not all the way)
   Put the pin in a tube with Isopropanol(it needs to be completely dipped under)
   Place this tube in the ultra sonicator bath and put the timer at his max.
   Now take the other pin and follow the allignment procedure in Item 3

9.1.5 Dipping

9.1.5.1 Equipment used

- Dipstick
- Liquid nitrogen(around 60L)
- Norhof LN2(Liquid Nitrogen) vessel
- Cyro-gloves tempshield
- Structure with wheels to move the liquid nitrogen vessel around.
- Cork

9.1.5.2 Work flow

Inserting plug into matrix module 1 minute

- By inputting a small plug in the back we can connect the top row and the bottom row of the matrix module with each other.
- in other setups this plug is missing and we can directly connect the dipstick with the matrix module

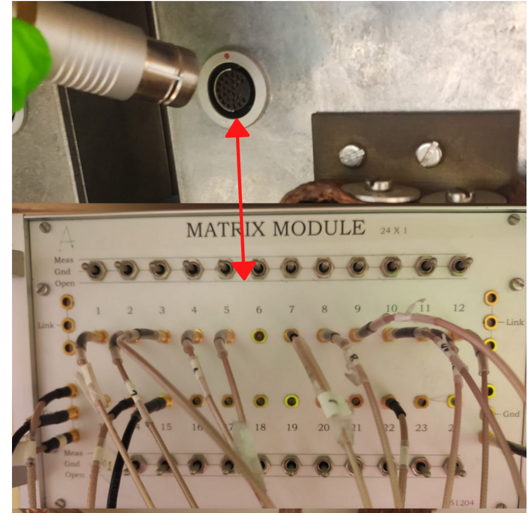

Figure 65: Top picture shows the plug you need to insert into the back of matrix module. The bottom picture shows the matrix module, which will have the top and bottom row connected due to the plug.

Grounding the device 1 minute

Figure 66: Connecting the ground with the matrix ground

- Ground the dipping device properly before connecting PCB

Attach PCB to dipstick 1 minute

- Connect PCB and attach screw with nut in one corner

Figure 67: PCB attached to the dipstick and screwed in place with a nut

Slide protective shield over 3 minutes

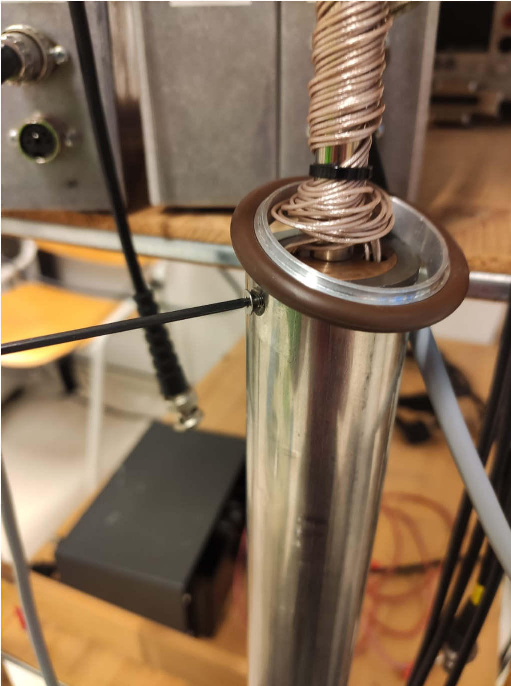

Figure 68: Protective shield over the dipstick, with screws in place

- Slide protective shield over and place screws in

IV-measurement room temperature dipstick 10 minutes

- Do an extra IV measurement at room temperature in order to verify you haven't destroyed the device after wire bonding.
- Follow the first few steps in Section 9.1.6 to setup the connection to the bspy software.
- Open up the bspy-smg folder in your code environment
- Select the voltage range for all 7 input pins in the settings file of the software (One input pin is used for the spike voltage). The voltage range should not exceed +-90 mV to prevent damage for this room temperature measurement
- Select the input pin in the software
- Physically change the input pins on the matrix module and test all 8 connections (so first place the input on the matrix channel which is connected to electrode 1). And the output on the second channel. Make sure you put the channels you measure to measure in the matrix module.
- Select the IV-curve measurement in the Simple.py file in bspy-smg folder and run it.
- Store the iv-curve and compare the resistance range with the room temperature measurement before wire bonding.

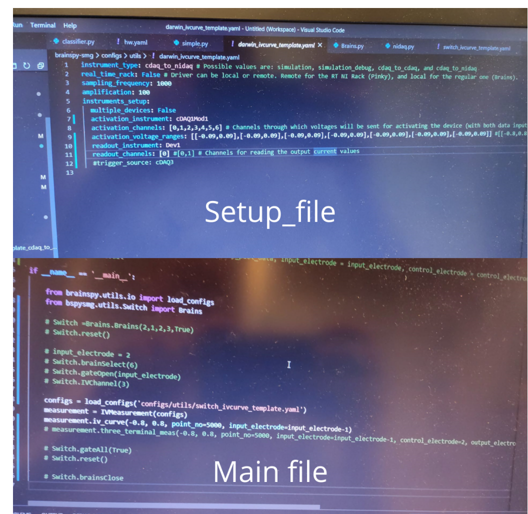

Figure 69: Settings file and the simple.py file in the bspy folder

Fill up the liquid nitrogen tank 15 minutes

Figure 70: Filling up the liquid nitrogen tank

- Put the liquid nitrogen tank onto the structure with wheels
- Take it to the filling point and fill the tank up until the dipstick can at least be fully submerged, the more you fill it, the longer it will last.
- After filling, close off the top exit with a cork for minimal loss.

Dip the device in 10 minutes

- Dip device in, wait when you see some smoke appearing(this means the tip is touching the liquid nitrogen). Slowly lower the dipstick over the course of 5 to 10 minutes into the barrel. This is to prevent thermal breakdown
- Wear protective gloves for the cold if you have to lower the dipstick in with your hands

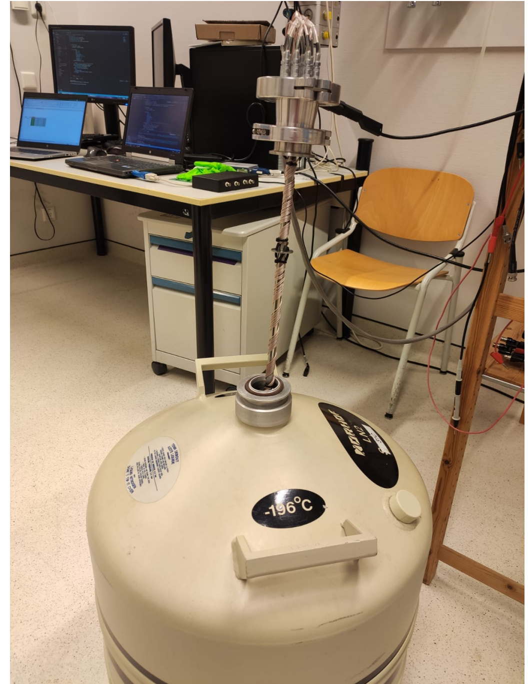

Figure 71: Dipstick in the vat with liquid nitrogen

9.1.5.3 Extra need to knows for dipping

- A vat of 60L liquid nitrogen lasts about two weeks, after that you should refill it.

9.1.6 Three phased measurements 77 Kelvin

9.1.6.1 Equipment used

- A HP 8560W laptop with the BSPY software
- Matrix module 24 x 1 TU-DELFT-QT, 151204
- M0 Dual ISO-Out module
- M1b I measure module
- National Instruments, NI-USB-6216 ADC
- National Instruments, cDaq 9171 DAC
- Coax cables
- Link module

9.1.6.2 Work flow

Setting up the ADC and the DAC 5 minutes

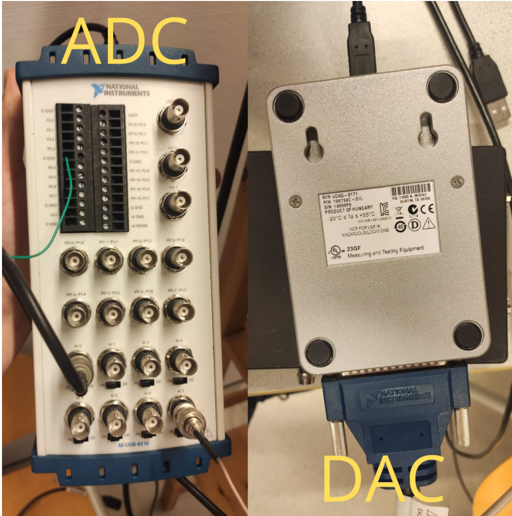

Figure 72: The DAC and ADC used in this setup

- Plug the USB cable of the ADC and DAC into the laptop.
- Plug the ground(s) of the DAC cable into the matrix module.
- Check the setting file: 'darwin_ivcurve_template.yaml' in the bspy-smg folder and set the min and max voltage ranges in 'activation_voltage_ranges' of all the channels, make sure you don't exceed +- 1.2 Volt.
- Fill in the readout channel at 'readout_channels'(can be number zero to 7), connect the M0 Dual ISO-Out module via a cable to the filled in readout channel.

Connect the spike channel 3 minutes

- In the bspy-smg folder select the 'tasks.py' file, go to the 'add_synchronization' function and at fill in the number you want the spike to exit and input at 'activation_channel_no' and at 'readout_channel_no'. (Initially these are both set to 7, so A07 outputs the spike on the DAC and A07 is the input channel on the ADC).
- Physically connect these channels together, you can do this most easiest by connecting a link module.

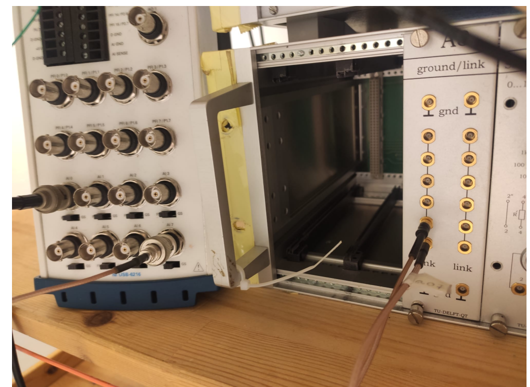

Figure 73: Spike channels A07 of the ADC and DAC connected with the link module

Connect the dipstick 1 minute

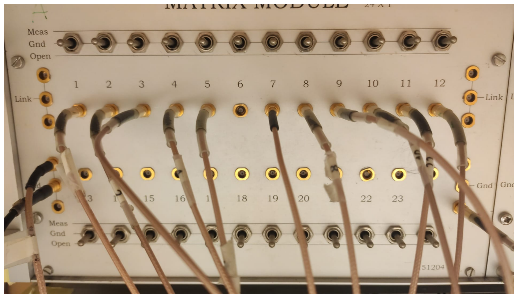

Figure 74: Dipstick connection 1 on 1, notice that channel 6 is broken.

- Put all the inputs of the matrix module to ground before connecting anything from the dipstick to prevent electrostatic discharge
- Connect the dipstick in a logical way, so input 1 of the device connects with input 1 of the matrix module, if you followed the orientation in the wire bonding section, this should be the case.

Configure channels 3 minutes

- In the bspy-smg folder select the 'simple.py' file and at 'measurement.iv_curve(' fill in the input_electrode and control_electrode
- The number you input directly represents the channel this signal will be outputted on, so a 1 would mean channel A01 is selected, a 2 would mean A02 is selected.
- Configure the right inputs into the code and physically change the output and inputs to the correct three channels on the matrix module.
successfully measured all electrodes ones.
- Use an ICO configuration, so first channel: Input signal, second channel: Control voltage and the third channel: Output signal.
- Set the correct control voltage, first start off with a control voltage of 0 Volt, which is just a normal iv-curve
- Put the channels you use to measure by flipping the switch of these channels up on the matrix module. So put them to 'Meas'.
- Start up the measurement by pressing f5 while in the 'simple.py' file.
- Now measure all 8 ICO configurations with 0 control voltage.
- After that test the channels that showed good non-linear iv-curves on their NDR by applying a non-zero control voltage

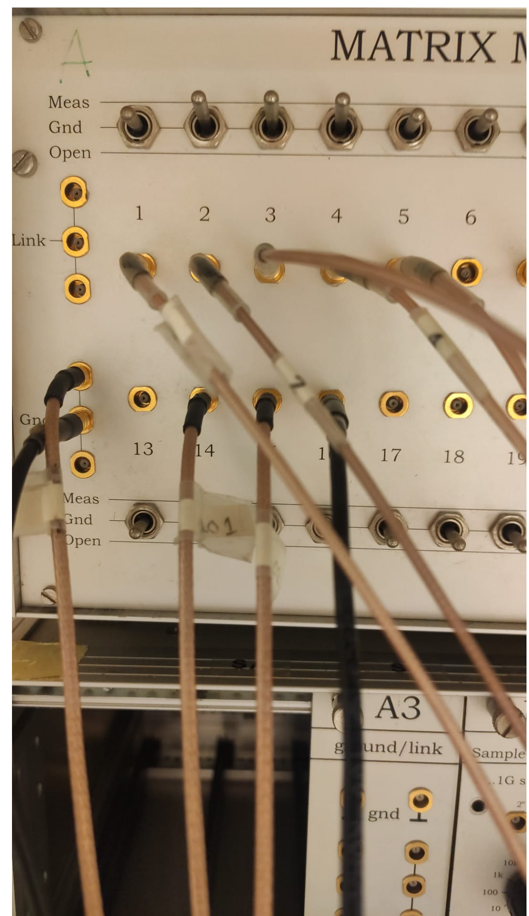

Figure 75: ICO configurations of matrix module with A1 as the input signal, A2 as control input and the black cable as the output

9.1.6.3 Extra need to knows three phased measurements at 77 Kelvin

- When not flipping a switch you can get a noisy graph. Be aware of this when measuring, so that

you don't mistake a measurement as bad, when it's actually a measuring mistake.

9.1.7 XOR classification of DNPU

With this classification, you can test if the DNPU can mimic an XOR gate. If it can, it means it can achieve NDR and can thus achieve the non-linearity needed for an efficient ANN.

9.1.7.1 Equipment used

- Same equipment as in Section 9.1.6

9.1.7.2 Work flow

Setting up (5 minutes) and running (60 -120 minutes)

- After your three phased measurement, you know the channels that showed good non-linearity.
- Based on this information, you can decide how to place the inputs and outputs best before running a classification. If all channels showed promising non-linearity, the placement can be best such that the input channels are farthest apart from the output, but both by the same amount of distance from the output.
- Connect all inputs of the DAC to the right inputs of the matrix module, according to the just above mentioned points.
- Make sure the matrix modules are switched to measure - Start up your classification and let it run for about two hours, sometimes it does 2 measurements.
- It will output a few files after the measurements, the most important take aways are the fitness and the training accuracy.
- In Figure 76, we see an example of an output file, the dotted points are the output from running and the green shape represents the target shape. The dotted line here is the decision threshold. The accuracy determines your separability of 0 and 1 and the fitness determines how well your output overlaps your target shape.
- In Figure 76 it can be seen that the target shape is not mimicked properly, so the fitness is bad and the device does not have the computational capability to mimick XOR.

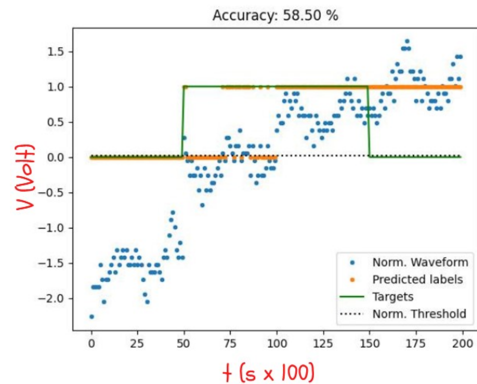

Figure 76: Batch 5 chip 1, training accuracy output

9.1.8 Taking out the dipstick

9.1.8.1 Equipment used

- Protective gloves

9.1.8.2 Work flow

Take out the dipstick very slowly 10 minutes

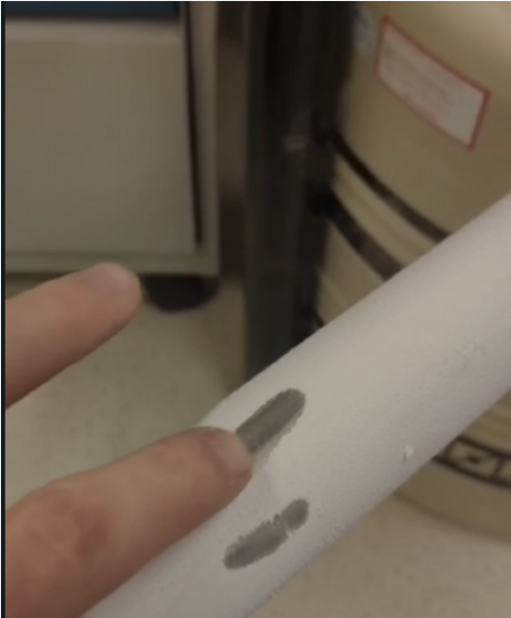

Figure 77: The dipstick taken out of the liquid nitrogen vessel

- Put on your protective gloves before taking it out
- When taking out the dipstick, make sure you do it slowly. So take about 5 to 10 minutes again to take it out, to prevent possible thermal breakdown
- Let the dipstick cool off for about an hour, we can see an example of how cold the dipstick becomes in Figure 77 after it's been just taken out of the liquid nitrogen vessel.

IV measurements room temperature 10 minutes

- After it has been cooled down, perform another IV measurement at room temperature with the dipstick