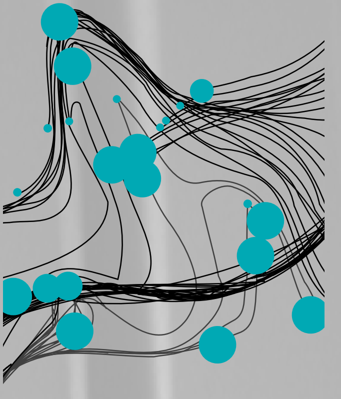
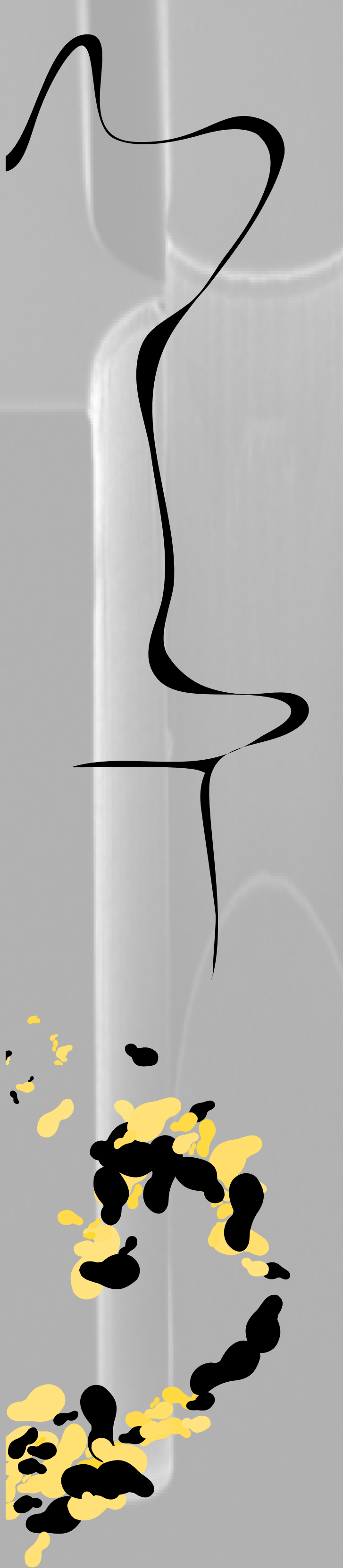
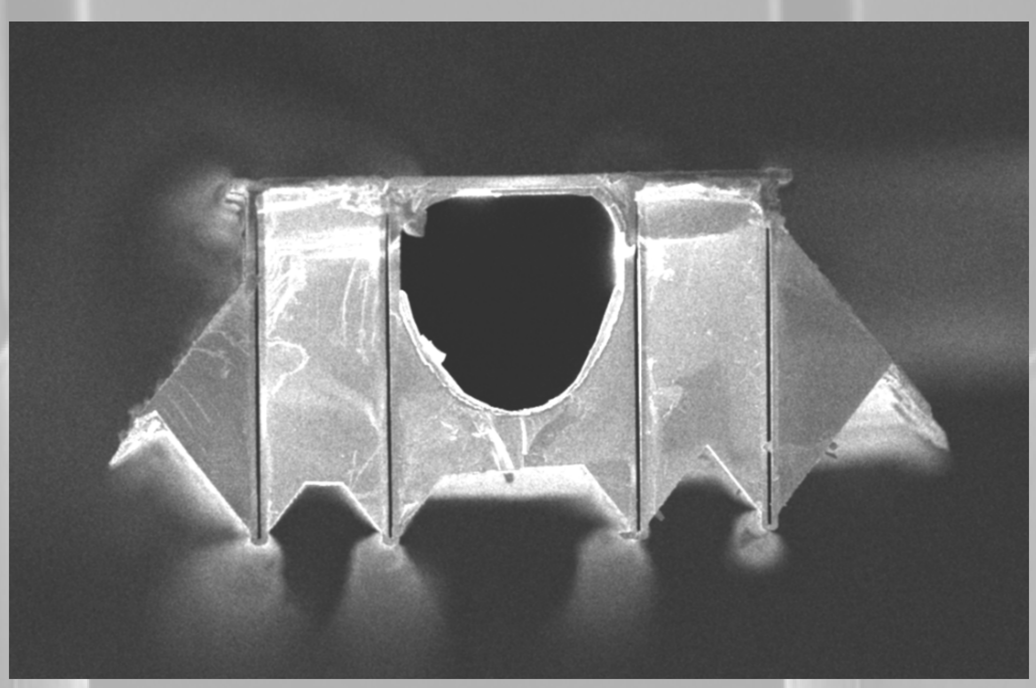




Master's Thesis - Electrical Engineering

Simplified Trench-Assisted Surface Channel Technology for High-Temperature Microfluidics



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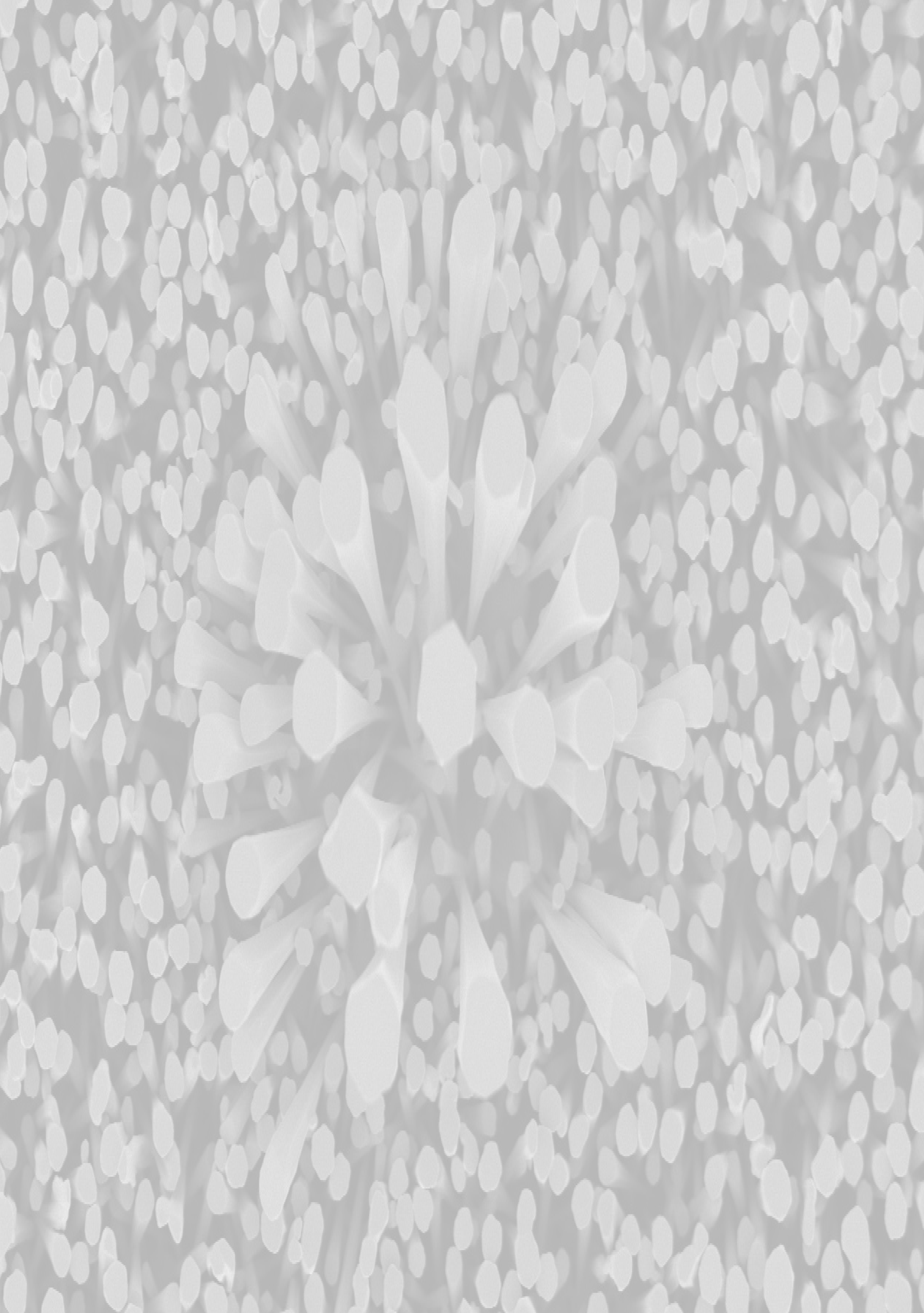

"There are few facts in science more interesting than those which establish a connexion between heat and electricity. Their value, indeed, cannot be estimated rightly, until we obtain a complete knowledge of the grand agents upon which they shed so much light."

James Prescott Joule

On the heat evolved by metallic conductors of electricity,
and in the cells of a battery during electrolysis.
1841, The London, Edinburgh, and Dublin
Philosophical Magazine and Journal of Science,
19(124), 260–277

Abstract

The Surface Channel Technology platform which is used for the fabrication of free-hanging microfluidic channels was advanced into newly technologies with integrated electrodes inside the bulk. This integration of electrodes leads to an improvement in design possibilities and functionalities. One promising solution for realizing this is called Trench-Assisted Surface Channel Technology. This technology enables the integration of highly-doped silicon sidewall heating elements parallel to the channel, whilst maintaining design freedom for microfluidic channel dimensions and for the placement of sensing elements. However, realizing actual devices with this technology is labour-intensive and requires hands-on skills. Due to the many micro-fabrication steps (>300), often complex optimization of problems was required. Together with problems in the release etch step, this called for the development of a new technology.

Therefore, in this work, a simplified Trench-Assisted Surface Channel Technology is presented. This technology is developed to realize a simpler yet still effective method to create highly-doped silicon sidewall heating elements, with a large cross-sectional area and parallel to the channel. This new technology introduces a novel way of creating pyramid-shaped vias to the microfluidic channels. The vias are formed simultaneously with the release of the microfluidic channels from the bulk silicon, leaving only a small membrane behind. This membrane ensures full enclosure of the microfluidic channels during and after the final release step. Therefore, this approach enables the usage of wet etching in KOH solution, since the contamination of residual insoluble floccules inside the microfluidic channels is avoided this way. After all the micro-fabrication steps are completed, the membranes can be punctured manually creating the final access to the outside world.

The main limitation of this simplified Trench-Assisted Surface Channel Technology showed to be a limitation for the electrode orientation, which can only be formed alongside the Si $\langle 110 \rangle$ directions on a Si $\{100\}$ wafer. Any deviation from this angle will result in significant undercutting of the silicon heaters. However, by optimizing the mask windows and etch times, this undercutting of the heaters can be minimized. Another limitation is the formation of residual silicon on the outer walls of the trenches. Also, from the fabrication, it became clear that V-grooves on the surface of the wafer should be minimized, as this can make successive lithography steps problematic. This can be resolved by avoiding complex trench junctions and by using tapered T-junctions.

Overall, this simplified Trench-Assisted Surface Channel Technology proved to be a simpler alternative to the existing Trench-Assisted Surface Channel Technology. This new technology can therefore be used to realize SCT-based devices, such as the Coriolis mass-flow sensors or Wobbe-index sensors. However, the performance of devices realized with this new technology has not yet been tested.

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Abbreviations

AlOx	aluminium oxide
BOX	buried oxide
CAD	computer-aided design
DRIE	deep reactive-ion etch
FEA	finite element analysis
HAR	high-aspect-ratio
KOH	potassium hydroxide
LPCVD	low-pressure chemical vapor deposition
MFC	mass-flow controller
NaOH	sodium hydroxide
PECVD	plasma-enhanced chemical vapor deposition
RIE	reactive-ion etch
S-TASCT	Simplified Trench-Assisted Surface Channel Technology
SCT	Surface Channel Technology
SHEs	sidewall heating elements
SiRN	silicon-rich nitride
SOI	silicon-on-insulator
STP	standard temperature and pressure
TASCT	Trench-Assisted Surface Channel Technology
TEOS	tetraethyl orthosilicate
TMAH	tetramethyl ammonium

Symbols

Symbol	Description	Unit
A	Area	m^2
C_p	Heat capacity at constant pressure	J/K
C_v	Heat capacity at constant volume	J/K
C_{fr}	Friction coefficient	µm
D_H	Hydraulic diameter	m
E	Bulk modulus of elasticity	Pa
H	Enthalpy	$J\,kg^{-1}$
I	Current	A
L	Channel length	m
Ma	Mach number	
P	Power	W
Q	Heat rate	W
R_{ref}	Reference resistance	Ω
Re	Reynolds number	
T_{ref}	Reference temperature	K
U_z	Underetch of hardmask	µm
U	Voltage	V
U	Internal energy	J
W	Work	J
$\Delta H_F°$	Heats of formation	kJ/mol
$\Delta H_{reaction}$	Heats of reaction	kJ/mol
ΔT	Temperature difference	K
Δx	Wall thickness	µm
$\dot{Q}$	Volumetric-flow rate	W
$\dot{m}$	Mass-flow rate	mg/h
ϵ	Emissivity of gray body	$W\,m^{-1}\,K^{-1}$
π	Geometrical value	
ρ	Density of fluid	kg/m^3
ρ	Resisitvity	Ω/cm^2
°C	Degree Celcius	°C
σ	Stefan-Boltzmann constant	$W\,m^{-2}\,K^{-4}$
h_t	Heat transfer coefficient	W/m^2
h	Height of channel	µm

Symbol	Description	Unit
j	Current density	A/cm^2
k_b	Boltzmann constant	J/K
k	Thermal conductivity	W m^{-1} K^{-1}
l	Length	µm
r	Radius	µm
v_0	Flow velocity	m/s
v_s	Velocity of sound	m/s
w_0	KOH via width at depth z	µm
w_m	Mask width	µm
w_z	Effective via width at depth z	µm
w_{tot}	New via width at depth z	µm
w	Channel width	µm
z	Etch depth	µm

Voor Mama, Papa, Rebecca en Bowie

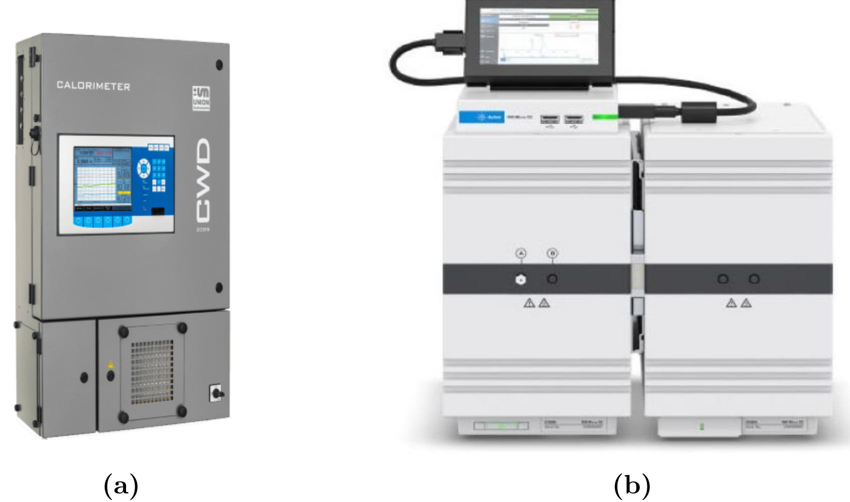
1 | Introduction

The research in this report is motivated by the desire for a simple technology to create microfluidic channels with integrated silicon sidewall heating elements (SHEs). Existing technologies that are able to create microfluidic channels with SHEs include extensive microfabrication steps, which result in minor and major problems, during and after fabrication. In this introductory chapter first, the background for the need for microfluidic channels with SHE's is explained. Secondly, the state-of-the-art technologies will be discussed. This ultimately leads to a section with new research goals and the chapter will be concluded with the outline of this thesis.

1.1 Background

Oil and gas keep the engine of the world economy running. Gas currently accounts for around 24.7% of the world's commercial energy mix [1]. Since gas is known for being a reliable and highly efficient source of power generation, it was after renewable energy sources, the fastest-growing primary energy source in the world [1]. However, one problem with natural gasses is that the composition of the gas my vary dependent on the location the gas is extracted from the ground. When comparing, for instance Groningen gas and North Sea gas, the different alkane, nitrogen and carbon dioxide contents lead to different amounts of energy inside the gas [2]. To measure the actual energy content in gaseous fuels either the complete composition of the gas must be known or the calorific value of the gas composition must be determined. The calorific value is the amount of heat evolved by the complete combustion of a unit certain volume of gas with air. To compare the calorific value of gaseous fuels on a unified scale, Goffredo Wobbe developed the "Wobbe-index" in 1926 [3]. The Wobbe-index is a measure of the interchangeability of fuel gas mixtures. Thus, a constant Wobbe-index ensures that the combustion energy of the gaseous fuel is also constant at a constant pressure.

Dutch consumers of gaseous fuels pay for the cost per unit volume of gas, based on the Wobbe index for Groningen gas. This ensures that the unit of energy inside of the gas stays constant. By mixing different (unknown) gasses the Wobbe index is not maintained. For this purpose, calorimeters are used, which first measure the gas and then relate its calorific value to the Wobbe-index [6]. Currently, devices the size of large cupboards and with prices of around €25.000 or higher are executing these measurements [4]. Alternatively, gas chromatography (GC) is used to determine the composition of the gas, hence the capability of determining the energy content of gaseous fuels [6]. These GC machines, are already offered as tabletop solutions but are still quite expensive [5]. Besides that, these measurements take a long time to complete due to multiple sensors and therefore do not offer direct measurement capabilities [7].



(a) (b)

Figure 1.1: Examples of machines currently used for calorific value determination. In **(a)** a combustion calorimeter for instant and continuous determination of the Wobbe index [4]. In **(b)** a table top gas chromatograph for non-continuous high quality, Wobbe index determination [5].

Over the years some efforts have been made to miniaturize calorific sensors, but these micrometer-scale solutions are far from ready for usage in commercial or industrial purposes. Nonetheless, miniaturizing these solutions on micrometer scale can offer huge benefits for the gas industry. The most valuable advantage is the continuous measurement capability, which highly reduces the consumption of gaseous fuels during the calorimetric measurements. This results in an enormous reduction of costs also due to significantly smaller device dimensions. In addition, more and more different sources for gaseous fuels are used, leading to different mixtures. This calls for more calorimeters to guarantee proper calorific values throughout gaseous fuel mixtures. These low cost micromachined calorimeters can offer a solution for the use at regional gas grid levels or maybe even at the end-of-line for consumers at home.

1.2 State of the art and motivation

In the last two decades new process technologies, such as Surface Channel Technology (SCT), developed at the University of Twente, enabled reliable integration of microfluidic channels [8]. This also led to the production of a micro-Coriolis mass-flow sensor, which is currently being commercialized by Bronkhorst High-Tech bv. The first envisioned calorific measurement system-on-chip based on this technology was presented by J. Lötters *et al.* [9]. This chip included both the micro-Coriolis mass-flow sensor and a calorific measurement part, as shown in figure 1.2. The calorific measurement system was realized and consisted of a pre-heater element, a reaction chamber with heaters, inlets and outlets. The heating elements and sensing elements in these systems were realized by applying a thin-film metal layer on top of the microfluidic channels. This heavily reduces the design freedom because all these metal features, both sensing and heating, must be placed in the vicinity of the channels. Moreover, using this thin-film metal layer for joule heating proved to be less than ideal. One of the main reasons for this is that thin-film heaters need an adhesion layer to make a proper binding to the commonly used MEMS materials such as silicon-rich nitride or silicon dioxide [10]. However, these adhesion layers degrade at high operating temperatures (500-1000 °C) [11]. This can result in delamination and buckling of the thin-film metal layer [12]. Therefore, several attempts have been made at extending

this SCT by integrating the heaters inside highly-doped silicon [13–15]. Because of this integration, more design freedom can be generated, more thermal stability can be offered and more efficient heat transfer can be realized with respect to SCT with metal heater elements on top of the channel.

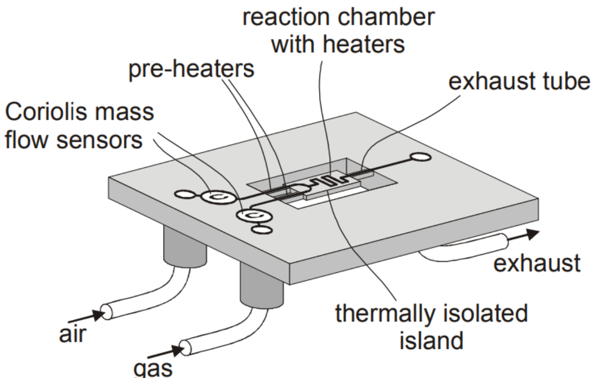
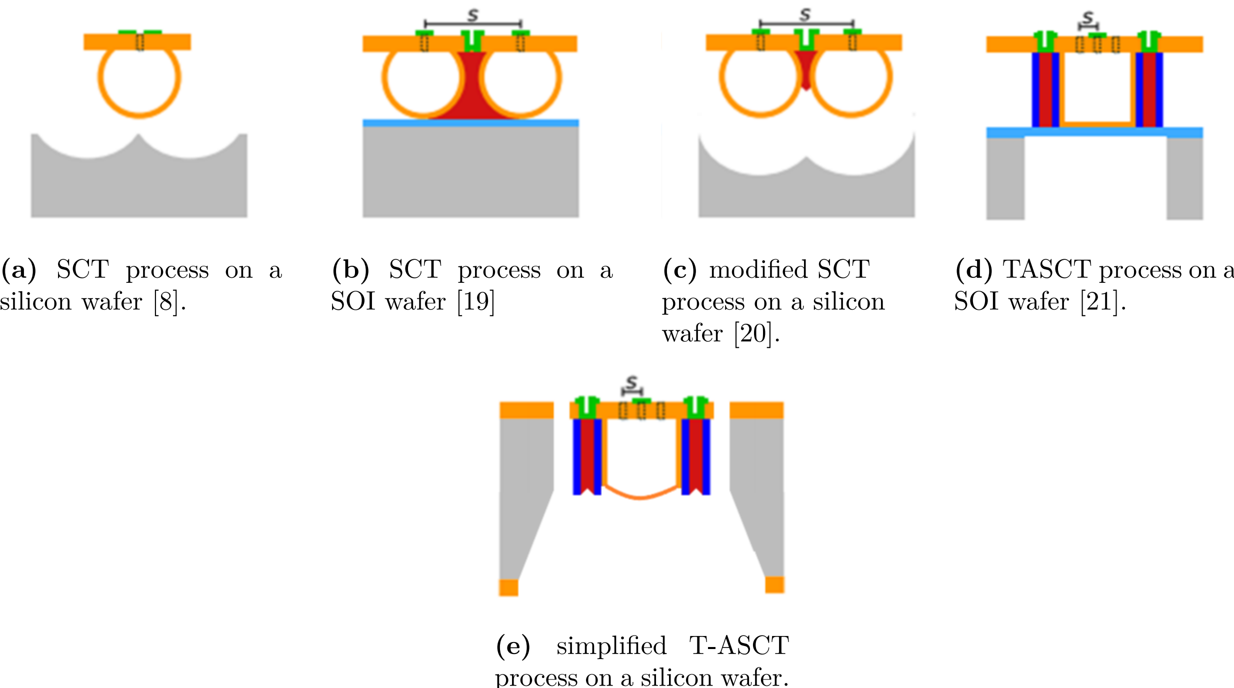


Figure 1.2: A schematic representation of the envisioned micro machined wobbe index sensor. The wobbe index sensors consistsof the already developed micro-Coriolis mass-flow sensor and a calorific measurement system. Image taken from original source [9].

In figure 1.3 an overview is given of the original SCT and more recently developed technologies. Figure 1.3a shows the original SCT process, where rows of slits are used to create micro-fluidic channels. Then, by depositing a thin-film metal layer on top, different functionalities such as sensing, heating, or actuation can be utilized [13, 16–19]. Because the previously stated functionalities are implemented in the same layer, the design freedom is severely limited. Therefore, attempts were made to make highly-doped silicon SHEs. In figure 1.3b with the same SCT technology and two rows of slits separated by a distance S on a silicon-on-insulator (SOI) wafer resulted in an isolated highly-doped silicon electrode between the channel walls. This method was demonstrated by using the isolated electrode as an inline relative permittivity sensor providing high accuracy results [19]. One downside was that this process was limited to the usage of SOI wafers.

Therefore, in figure 1.3c a modified SCT applied on a silicon wafer was proposed. By properly designing the release windows, in combination with an isotropic SF_6 reactive-ion etch (RIE) process, some highly-doped silicon resides between the channel walls. This highly-doped silicon was isolated from the bulk and could therefore be used as SHEs. A demonstrator device developed for this technology showed working SHEs used for Joule heating [20]. However, the produced heaters also showed non-uniform dimensions alongside the electrodes, which resulted in hotspots when used for joule heating. The main reason for the non-uniformity was ascribed to the wafer-scale non-uniformity or proximity effects during the isotropic SF_6 RIE and proposed was to investigate a backside release etch process, which should result in more uniform heaters with a higher cross-sectional area.

In figure 1.3d a new approach for creating highly-doped SHEs called TASCT is shown. By creating high aspect ratio trenches and refilling them with insulating material, in combination with etching stops from using the buried oxide (BOX) layer of a SOI wafer, insulated rectangular electrodes can be realized parallel to the channel [15, 21]. This technology offers a lot of design freedom and a very large electrode area. This allows higher currents to flow through the electrodes, which is crucial for Joule heating applications. A proof-of-principle device, which was developed to heat up an airflow, showed



(a) SCT process on a silicon wafer [8].

(b) SCT process on a SOI wafer [19]

(c) modified SCT process on a silicon wafer [20].

(d) TASCT process on a SOI wafer [21].

(e) simplified T-ASCT process on a silicon wafer.

Figure 1.3: Cross-sectional schematic illustrations of the SCT process and newly developed technologies. The original SCT process **(a)** on a silicon wafer. One or several rows of slits (dashed lines) closely together are used to create the microchannel. The metal layer on top (green) is used for sensing, heating or actuation. The SCT process applied on a SOI wafer **(b)**, now multiple rows with a spacing S results in two microchannels with residual silicon between the microchannels (red). The same principle applied on a silicon wafer results in **(c)**. A new approach in creating silicon side wall heaters by the Trench-Assisted Surface Channel Technology (TASCT) process **(d)** on a SOI wafer. Introducing a new release method to the TASCT on a silicon wafer results in **(e)**.The colors represent: Si SiO_2 SiRN Si Electrode Metal Refilled trenches. The dashed lines represent the slit outlines. Image adapted from its original source by adding **(e)** [14].

that the channels can easily be heated up by the silicon heaters to 400 °C at an operating power of 1.4 W. Higher temperatures were not reached due to an incomplete release etch. This caused silicon islands to remain under the channel which dissipated the heat via conduction to the bulk. Increasing the power resulted in a break-down of the proof-of-principle devices. The cause for the break-down was possibly due to induced stress caused by expansion of the channel. This expansion in combination with the under-etch of the tantalum adhesion layer during the XeF_2 release etch causes de-lamination of the platinum layer. Moreover, it was found that TASCT involves many complex micro-fabrication steps, in combination with using a SOI wafer. This results in a lot of process optimization, as every micro-fabrication step can introduce new complications.

Therefore, in this work, a Simplified Trench-Assisted Surface Channel Technology (S-TASCT) is presented, which is aimed to realize a simpler method to create highly-doped SHEs on a silicon wafer. This is done by introducing a new release method to the SCT platform, which offers a novel way to create pyramid-shaped vias to the microfluidic channels and release the devices in one micro-fabrication step. It is expected that the complications resulting from the release steps in the modified SCT and TASCT are prevented in this way. To test the viability of this technology a demonstrator device will be designed which should be able to heat up an airflow, supplied via a mass-flow controller (MFC), to at least 600 °C.

1.3 Research goals

The main goal of this work is to develop and characterize a new process technology called Simplified Trench-Assisted Surface Channel Technology. This new process technology integrates multiple facets of existing SCT-based technologies, with a novel way to create pyramid-shaped vias to the microfluidic channels, whilst simultaneously releasing the device structures from the bulk silicon. By combining the formation of vias to the channels, with the releasing of the devices in one process step, this new technology can be simplified significantly. This could ultimately result in a simpler yet reliable way of producing microfluidic channels with integrated SHEs, in comparison with the earlier developed TASCT. The newly developed S-TASCT will first be tested by simple test structures and the full capabilities will be tested by designing and modelling a demonstrator device. This device should be able to heat up an airflow to 600 °C. If the newly developed process technology results in usable devices, also characterization measurements can be conducted.

1.4 Thesis outline

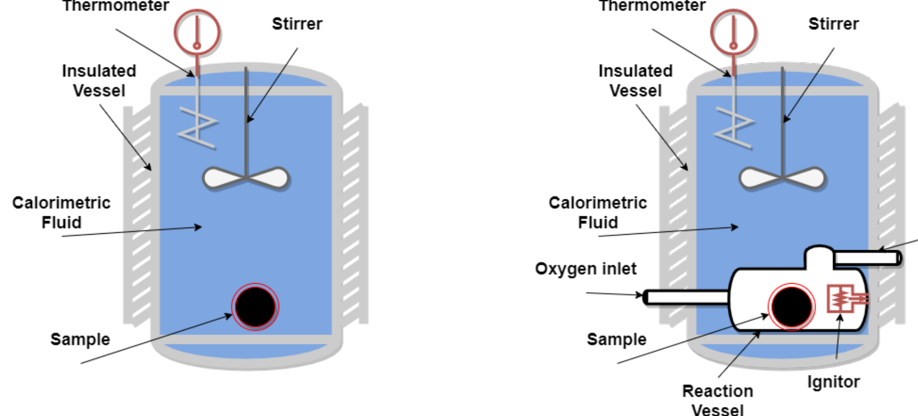
This report starts with an introduction to calorimetry in **chapter 2** and will advance into explaining the fundamental theory of a micro-scale calorific sensor. The combination of microfluidic channels with integrated heaters leads to the integration of physics from multiple domains. Hence, sections about thermodynamics, fluidics, and electronics provide all the basic formulas necessary for designing and modelling the demonstrator device in **chapter 3**. In that chapter also the S-TASCT process will be described in detail and the proof-of-principle design will also be verified with simulations in COMSOL Multiphysics 5.6. Once verified, the proposed design will be accompanied by mask designs and a process flow. This process flow is executed in **chapter 4** and all results will be described and discussed in detail. After the successful realization of the devices, measurements will be conducted in **chapter 5**. The fabrication will be evaluated and by comparing these results with the theory and design, a discussion section will be provided in **chapter 6**. In the case of successful fabrication of devices also a comparison can be made here between simulations and measurements. In **chapter 7** we reflect on all completed work, which will lead to several conclusions. This will help to form the future outlook of this new technology, including some recommendations that can improve the further development.

2 Theory

In this chapter fundamentals will be explained that are necessary for designing the demonstrator device in chapter 3. First, an introduction to calorimetry will be given to learn which physical models are required to successfully model the demonstrator device, this includes the trivial equations that are required for the verification of the finite element analysis (FEA) model in COMSOL Multiphysics 5.6. Moreover, key process steps for both the SCT and TASCT will be explained in more detail. Also the wet etching of silicon in potassium hydroxide (KOH), which is used for the novel way of creating vias to the microfluidic channels, is explained.

2.1 Introduction to Calorimetry

Calorimetry is defined as the measurement of heat. In which, heat is the amount of energy that is exchanged in a system due to physical processes or chemical reactions [22]. This means that heat can only be seen as a change of energy expressed as a heat flow within a certain time interval inside these systems. Calorimeters are the devices used for measuring this heat as can be seen by a simple schematic in figure 2.1. If a sample, providing an exothermal reaction is placed inside the liquid of a calorimeter, the heat will be absorbed by the liquid. This increases the temperature given by the thermometer, as shown in figure 2.1a.



(a) Basic calorimetric setup **(b)** Calorimetric combustion setup

Figure 2.1: Two calorimetric setups. In **(a)** a sample performing an exothermal reaction is placed inside the calorimeter, the heat will be absorbed by the liquid, resulting in an increase in temperature. In **(b)** the setup is modified to allow for combustion reactions to take place inside the calorimeter, the heat absorbed by the liquid will again result in a temperature increase.

Combustion reactions cannot take place inside this setup. Therefore an extra reaction vessel was placed inside the calorimetric liquid. In this new setup, shown in figure 2.1b, the reaction takes place inside this vessel. Again, the heat resulting from the reaction is absorbed by the calorimetric liquid, which increases the temperature. Two types of reaction vessels are used. The first one is fully closed, the so-called calorimetric bomb, and is used for the combustion of solid and liquid samples by using electronic ignition in an excess oxygen environment. The other one may contain a gas supply to the chamber, which is used for reacting one gas in a second gas, or using a solid or liquid sample inside the chamber for combustion, whilst supplying an oxygen stream.

2.2 Micro-scale calorific sensor

The envisioned calorific sensor described in the introduction as any basic calorimetric micro-sensor at least consists of an inlet, for the supply of fuel gas and air, a mixer, a combustion chamber, a heater (or ignitor), temperature sensor(s) and exhaust, as can be seen in the schematic of figure 2.2. Either fuel and air are supplied to a mixer, or a pre-mixed gas fuel mixture is supplied to a combustion chamber. The supplied flow is often regulated by a MFC. The gas fuel mixture flows through this chamber accommodated by heating elements alongside the chamber walls. If enough heat can be transferred to the supplied flow of gas fuel the auto-ignition temperature can be reached. Once this temperature is reached a combustion reaction takes place. This exothermic reaction provides extra heat release to the surroundings. The temperature of the combustion chamber is monitored and since the quality of the gas composition is dependent on the amount of extra heat released a relation can be made between the calorimetric value and the increase in temperature upon combustion.

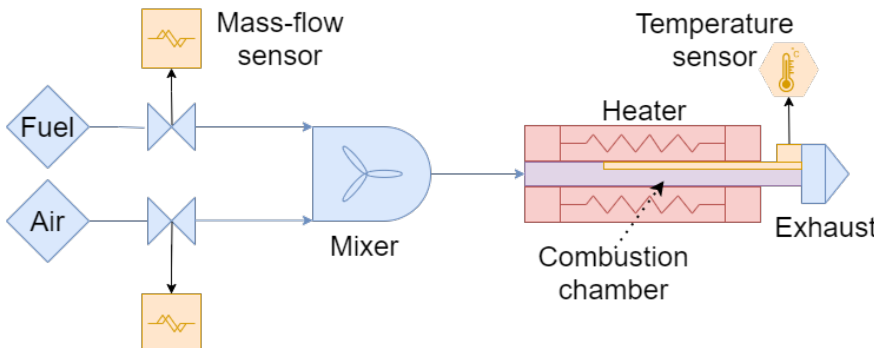


Figure 2.2: Different components of a micro calorific sensor. Fuel and air are regulated via MFCs and supplied to a mixer. This mixture is injected into the combustion chamber where it is heated until it reaches the auto-ignition temperature. The excess heat released from the combustion reaction is monitored by temperature sensors. The reacted gasses leave the combustion chamber via an exhaust.

2.2.1 Thermodynamics

When a temperature difference exists between two bodies, heat always flows from a warm body to a cold body. To get a better understanding of how the heat flows from the heaters to a gas inside the combustion chamber the three main forms of heat transfer will be explained, which are radiation, conduction and convection, as shown in figure 2.3. Also, the basic concepts of thermal transfer, such as the thermal capacity of materials and their corresponding intrinsic characteristic, will be explained.

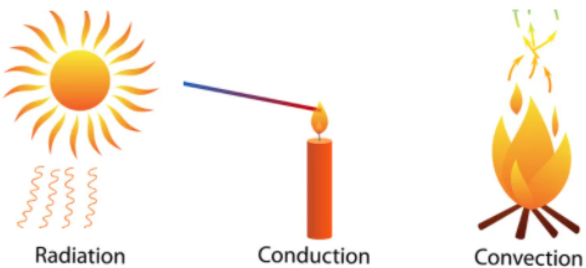


Figure 2.3: Three forms of heat transfer Radiative heat from a blackbody emitting electro-magnetic waves; Conduction of heat through a solid due to the vibration of molecules; Convective heating by the movement of free air molecules. Image adapted from original source by aligning the illustrations [23].

Three forms of heat transfer

Radiation is the transfer of heat by electromagnetic radiation (photons). A perfect blackbody radiator emits the maximum amount of thermal radiation possible for an object according to the temperature of that object [24]. However, all real objects do not radiate as much heat as a perfect black body and are therefore called gray objects. The total heat transfer rate (Q) by radiation of gray objects is given by equation 2.1, with ϵ the emissivity of the gray body, σ the Stefan-Boltzman constant, A the surface area of the object, T the temperature of the object and T_0 the ambient temperature.

$$Q = \epsilon \cdot \sigma \cdot A \cdot (T_0^4 - T^4) \tag{2.1}$$

Conduction is the transfer of heat by atom or molecule interactions, transferring its kinetic energy [24]. The total heat transfer is dependent on the transfer medium and its dimensions. To study the heat transfer in an object, the temperature difference, the geometry of the object and the physical properties must be known. The total heat transfer rate is described by equation 2.2, with k the thermal conductivity, Δx the thickness of the wall, ΔT the temperature difference and A the cross-sectional area.

$$Q = k \cdot A \cdot \frac{\Delta T}{\Delta x} \tag{2.2}$$

Convection is the transfer of heat via mixing and motion of a fluid flow passing a solid boundary [24]. A distinction can be made between two types of convection. First, there is natural convection. Due to temperature differences inside the fluid, the density of the fluid will vary, causing movement and mixing of the fluid. Second there is forced convection. Now the motion and mixing is caused by an external force (e.g. fans in a computer). A basic relation for the total heat transfer is given by equation 2.3, with h_t the convective heat transfer coefficient, A the surface area for heat transfer and ΔT the temperature difference. Typically, the convective heat transfer coefficient for natural convection will be around 2-20 and for forced convection this can range from 20-1000 [25].

$$Q = h_t \cdot A \cdot \Delta T \tag{2.3}$$

The heat transfer by convection is more complicated to analyse with respect to radiation or conduction. The convective heat transfer coefficient is dependent upon many physical properties of the fluid and it is also dependent on the physical situation where the flow is present in.

If we go back to the micro-scale calorific sensor, the main method to heat-up a supplied flow of gas, will be forced convection of the gas alongside the heater walls. From the total electrical power converted to heat, only forced convection will increase the temperature of the gas. All heat transfers that do not contribute to the convective heating of the supplied gas will be counted as losses. Because the convective heat transfer coefficient can vary from situation to situation and it can be chosen to use finite element analysis (FEA) tools for the simulation of convective heat transfer, which may also include conductive and radiative heat transfers in one model.

Thermal heat capacity

Thermal heat capacity, given by equation 2.4, is a measurable physical quantity equal to the amount of heat (Q) added to an object resulting in a certain temperature change (ΔT) [25]. This is an extensive property of matter and thus proportional to the size of the system. When this is expressed as intensive property, the heat capacity is divided by the volume or mass of the object, making the heat capacity independent of the size (e.g length) of the object. This specific heat capacity is the amount of heat needed to realize a heat change of 1 K for 1 kg of mass or 1 m^3 of volume.

$$C = \frac{Q}{\Delta T} \tag{2.4}$$

The relations between heat capacity and the thermodynamic energy states can be derived by looking at the internal energy (U) of a closed system. Heat can be added to (or removed from) the system or work (W) can be performed by the system, as shown by the first law of thermodynamics, in equation 2.5, with δQ as a small amount of heat added to the system and δW as a small amount of work performed by the system.

$$dU = \delta Q - \delta W \tag{2.5}$$

If the volume of the system increases, as a result of the delivered work, it can be written as $dU = \delta Q - PdV$. Now, at isobaric volume $dV = 0$, thus the second term can be removed. In this case, if the heat from conduction, radiation or Joule heating is added to the system, will result in equation 2.6. This is called the heat capacity at constant volume (C_V).

$$C_V = \left(\frac{\Delta U}{\Delta T}\right)_V = \left(\frac{\Delta Q}{\Delta T}\right)_V \tag{2.6}$$

From the definition of enthalpy as $H = U + PV$, then the change of enthalpy is given as $dH = dU - d(PV)$. If the volume of the system increases, as a result of the delivered work, we can plug in the term for dU, resulting in equation 2.7.

$$dH = \delta Q + Vdp + pdV - pdV = \delta Q + Vdp \tag{2.7}$$

Now at constant pressure, again the second term can be removed, resulting in equation 2.8 or the heat capacity at constant pressure (C_P).

$$C_P = \left(\frac{\Delta H}{\Delta T}\right)_P = \left(\frac{\Delta Q}{\Delta T}\right)_P \tag{2.8}$$

Both equations 2.6 and 2.8 are independent of the type of process, meaning that both the enthalpy and internal energy can change with an energy transfer in the system. This also means that a change

in enthalpy from, for instance, a combustion reaction, can cause a change in the temperature for a given C_P or C_V. Another equation derived from equation 2.8 is used to calculate the amount of heat change, necessary to induce a temperature difference (ΔT), for a given mass-flow ($\dot{m}$) is given by equation 2.9.

$$Q = \dot{m} C_P \Delta T \tag{2.9}$$

2.2.2 Fluidics

In this section, a physical foundation is laid for the fluid behaviour within micrometer dimensions. Micrometer dimensions are still much longer than the mean free path (λ) of the motion of the molecules (e.g. air molecules) [25]. The mean free paths can be calculated by equation 2.10, if each molecule is approximated to be a hard sphere with a diameter d, with pressure P, temperature T and k_b Boltzmann's constant. This means that in micrometer dimensions the laws of a continuous medium are still obeyed, thus, fluid properties such as density, pressure, and velocity stay constant at any defined point.

$$\lambda_{mfp} = \frac{k_b T}{\sqrt{2}\pi P d^2} \tag{2.10}$$

Therefore, basic fluid mechanics such as Poiseuille's law and Navier–Stokes–Fourier fluid dynamic models can still be used. For the Navier-Stokes equations, a distinction can be made between two forms of equations. One form is known as the incompressible form of equations and the other is known as the compressible form equations. Getting analytical solutions to the compressible form of the Navier–Stokes equation is complex. However, if the flow velocities are much smaller than the velocity of sound in the liquid, the fluid can be treated as being incompressible, which reduces the complexity of the Navier–Stokes equation. To determine whether a fluid is compressible or incompressible the Mach number can be used. The Mach number naturally is defined as the ratio of flow velocity (v_0) to the velocity of sound (v_s) in the same medium, which can be calculated according to equation 2.11. The fluid material-dependent Mach number is also given in equation 2.11, with E the bulk modulus of elasticity and ρ the density of the fluid. If the Mach number < 0.3 the fluid can be assumed to be incompressible. For air to be incompressible flow speeds should not exceed 100 m/s at room temperature.

$$Ma = \frac{v_0}{v_s} = \frac{v_0}{\sqrt{E/\rho}} \tag{2.11}$$

By introducing another dimensionless number, the Reynolds number (Re), the ratio between viscous force effects and inertial forces effects can be determined. The Reynolds number for liquid flow in a pipe can be calculated by using equation 2.12, with u the mean velocity of the fluid, D_H the hydraulic diameter, μ the dynamic viscosity, A the cross-sectional area of the pipe and $\dot{Q}$ the volumetric flow rate or $\dot{m}$ the mass-flow rate. In micrometer dimensions, viscous force effects start to become dominant in contrast to the inertial forces being dominant in macrofluidics. The resulting flow becomes laminar if $Re < 2300$. In the case of $Re < 1$ the non-linear Navier–Stokes equation can even be reduced to a linear Stokes equation. These equations can be used to get the pressure fields and velocity fields throughout a microfluidic channel. In the section below the Poiseuille's flow will be explained which has been used for modelling the flow in chapter 3.

$$Re = \frac{\rho \dot{Q} D_H}{\mu A} = \frac{\dot{m} D_H}{\mu A} \tag{2.12}$$

Poiseuille's flow

Poiseuille's analytical solutions to the Navier–Stokes equation, for a pressure-driven and steady-state flow in channels is known as Poiseuille's law or the Hagen–Poiseuille relation [25]. A typical Poiseuille's flow is the flow of fluid through a long straight channel, with zero fluid slip at the surface of the channel walls and increasing flow velocities toward the center of the channel. A direct consequence of this is, that for viscous fluids to be able to flow through the channel, a pressure difference (ΔP) must be applied between the inlet and outlet of the channel, no matter if the channel diameter varies throughout the length. Hagen and Poiseuille studied this flow in circular channels [26, 27], assuming a smooth channel and laminar flow and found the relation shown in 2.13, known as the Poiseuille's law or the Hagen–Poiseuille law [25], where L is the channel length, r the radius of the channel, μ the dynamic viscosity of the fluid

$$\Delta P = \frac{8\mu L\dot{Q}}{\pi r^4}. \tag{2.13}$$

However, the channels in microfluidic systems often have rectangular cross-sections, due to limited fabrication methods. Surprisingly, despite the symmetry in a rectangular cross-section, no analytical solution is known for the Poiseuille-flow problem for rectangular channels. Nevertheless, in the work of H. Bruus, a Fourier sum is used to get an analytical result. An approximate result for the volumetric flow rate $\dot{Q}$ is given in equation 2.14, with h the height of the channel, w the width of the channel, ΔP the pressure drop over the channel, μ the dynamic viscosity of the fluid and L the channel length [28]. In the worst case, for a square channel, with equal height (h) and width (w), the error is 13% and for rectangular channels at an aspect ratio of a half where the height is half the width, the error drops down to 0.2%.

$$\dot{Q} \approx \frac{h^3 w \Delta P}{12\mu L}\left[1 - 0.630\frac{h}{w}\right], \quad \text{for} \quad h < w. \tag{2.14}$$

For both geometries, it can be seen that the pressure drop is directly proportional to the viscosity of the fluids. In reality, if channels are not completely smooth but rough, roughness may introduce flow components that are different from the laminar flow. This will lead to an increased pressure drop over the channel. If a friction coefficient (C_{fr}) and a hydraulic diameter (D_H) are introduced into Poiseuille's law, the pressure drop can be rewritten to a more general form, as shown in equation 2.15. Typical values for C_{fr} are 64 for a circular cross-section and 96 for a rectangular cross-section [25]. However, C_{fr} is strongly influenced by the aspect ratio of the micro-channels and the width and length of the micro-channels. In the work of Z. Peng *et al.* a C_{fr} of 14.22, for a 30×30 µm microfluidic channel was reported [29].

$$\Delta P = C_{fr}\frac{\mu L\dot{Q}}{2AD_H^2} \tag{2.15}$$

Moreover, for laminar flow in the case of a circular channel, the velocity is zero at the walls of the channel and the velocity increases to its maximum value in the center of the channel, showing a parabolic velocity profile. For rectangular channels, this velocity just like the pressure drop is of course different. The exact profile is not necessary for this work, but the mean velocity ($\langle u\rangle$) and maximum velocity (u) are of interest. If the volumetric flow rate $\dot{Q}$ and the cross-sectional area A is known then the mean velocity is given by equation 2.16 and because of symmetry the maximum velocity corresponds to twice the mean velocity.

$$\langle u\rangle = \frac{\dot{Q}}{A} \tag{2.16}$$

2.2.3 Combustion and calorific value

In the micro-scale calorimetric sensor the combustion is initialized by reaching the auto-ignition temperature of a gas fuel mixture. Once the auto-ignition temperature point of a gas fuel mixture is reached many processes will occur at once. This can range from gas volume expansion, resulting in an increased flow speed, to surface reactions happening at the walls of the micro-channel, which can result in quenching of the flame [30]. Because of the complex gas kinetics the core focus will be on reaching the auto-ignition temperature, instead of maintaining a stable (continuous) combustion.
What is also of interest for this work, is to determine the amount of heat evolved from combustion of a known volume of gas fuel, often called the calorific value. This heat of combustion is often quantified as a higher heating value (HHV) or a lower heating value (LHV), which will be explained in the section below. The amount of heat generated should be large enough that it results in a measurable increase in the temperature of the sensors. The future micro-scale calorimetric sensor should be able to determine the calorific value of methane gas. Therefore the stoichiometric combustion of methane with air and the combustion of methane with excess air, are analyzed next. Both the heating values and air-fuel ratio (AFR) for this reaction are derived in the sections below.

Heating value

The energy released in a combustion reaction comes from the rearrangement of chemical bonds between reactants forming new products. The standard enthalpy change of formation ($\Delta H^0_{reaction}$) is used for quantifying the chemical bond energy of newly developed bonds at standard temperature and pressure (STP). The exact combustion reaction between methane and air is complicated to determine since many reactions steps are involved. However, a simple thermochemical equation that directly describes the combustion of methane with oxygen, is given by equation 2.17. The standard enthalpy change of combustion for this reaction is $-890.3\,\mathrm{kJ\,mol^{-1}}$ [30], where the minus sign indicates a release of heat.

$$CH_{4(g)} + 2O_{2(g)} \rightharpoonup CO_{2(g)} + H_2O_{(g)} \quad \Delta H^0_{reaction} = -890.3kJ/mol \tag{2.17}$$

The heating value of a fuel is normally used to quantify the heat that is can be released upon combustion with air. The maximum heat released is called the higher heating value, again at STP. However, if water is formed as the final reaction product, then the phase of the water can decrease the maximum heat that can be released because extra energy is released when water vapor condenses to a liquid. This is called the latent heat of vaporization and is included in the HHV. If the water stays in the gas phase, the standard enthalpy of formation for water vapor to water liquid must be subtracted from the HHV, this lower heat value is called the lower heating value. By using Hess's law, equation 2.17 can be decomposed in more reaction steps, with the standard enthalpy of formation (ΔH^0_f) for each reaction, as shown in 2.18. The LHV is then equal to $-890.3-(-44.016) = -846.284\,\mathrm{kJ\,mol^{-1}}$. For the micro calorific demonstrator devices used in this work, it is expected that due to the high operating temperature in combination with the small channel dimension the water will not be able to condensate in the vicinity of the temperature sensors [31]. The LHV should thus be used for calculating the total heat released upon combustion.

$$
\begin{aligned}
CH_{4(g)} \rightharpoonup C + 2H_2 \quad \Delta H_f^0 &= 74.81 kJ/mol \\
C + O_2 \rightharpoonup CO_2 \quad \Delta H_f^0 &= -393.51 kJ/mol \\
H_2 + \frac{1}{2}O_2 \rightharpoonup H_2O_{(g)} \quad \Delta H_f^0 &= -241.814 kJ/mol \\
H_2O_{(g)} \rightharpoonup H_2O_{(l)} \quad \Delta H_f^0 &= -44.016 kJ/mol
\end{aligned}
\tag{2.18}
$$

Air-to-fuel ratio

Stoichiometric combustion has the perfect amount of fuel and oxidizer material that after the combustion reaction all fuel and oxidizer materials have formed new products. This perfect mixture results in the highest flame temperature since all the energy released from combustion is used to heat the products [30]. For stoichiometric combustion of methane with air, if air is assumed to consists of only 21% O_2 and 79% N_2, the balanced reaction equation is given by

$$
CH_4 + 2(O_2 + 3.76N_2) \rightharpoonup CO_2 + 2H_2O + 7.52N_2 + heat. \tag{2.19}
$$

From equation 2.19 and the molecular weights for methane 16.0 g/mol and air 28.9 g/mol [32], the AFR can be calculated. However to ensure stoichiometric combustion and prevent soot forming, an excess of air is required. If an excess of 10% air is used the balanced reaction equation is then altered to

$$
CH_4 + 1.1 \cdot 2(O_2 + 3.76N_2) \rightharpoonup CO_2 + 2H_2O + 7.9N_2 + 0.1O_2 + heat. \tag{2.20}
$$

The AFR is then given by equation 2.21 and for every mass quantity of methane fuel a total of 18.8 mass quantities of air are required.

$$
AFR_{excess-air} = \frac{1.1 \cdot 2(1 + 3.76)}{1} \cdot \frac{28.9}{16.0} = 18.8 \tag{2.21}
$$

2.2.4 Electronics

Two types of electronics are described until now, electric heaters and electric sensors. Both types follow Ohm's law, but different characteristics are needed to efficiently fulfill its purpose.

Electric heaters

Electrical heaters produce the heat via Joule heating (Ohmic heating or resistive heating) [33]. This heating is caused by an electric current flow experiencing resistance passing through a conductor. For Joule heating as much as possible electrical power much be converted to heat. The formula for electrical power is given by equation 2.22.

$$
P = U \cdot I \tag{2.22}
$$

$$
U = I \cdot R \tag{2.23}
$$

Intuitively, by looking at Ohm's law (equation 2.23) it may seem that a very large resistance is needed to produce lots of heat. This of course is not true because a very high resistance limits the current.

By inserting Ohm's law into equation 2.22 we find Joule's first law

$$P = I^2 \cdot R \tag{2.24}$$

The power generated is proportional to the resistance, but it is also proportional to the square of the supplied current. To get the maximum power out of electrical heaters a good balance must be found between resistance and current. The current is often limited by the supply and the resistance is based on the resistivity and geometry of the wires. The resistance can be calculated by using equation 2.25 with, the resistivity (ρ), which is an intrinsic property of a material, A the cross-sectional area of a wire and l the length of the wire

$$R = \rho \frac{l}{A}. \tag{2.25}$$

Therefore, by changing the length, the cross-sectional area, or choosing a certain material a lot of design possibilities are available to realize the right amount of resistance for Joule heating. However, there is another factor that can put a limit on the current. If the current density (j), given by equation 2.26 becomes too high, phenomena such as electromigration might occur [34]. This can cause voids which can degrade the electrode performance over time.

$$j = \frac{I}{A} \tag{2.26}$$

Electrical sensors

The goal of the electrical sensors is to determine the temperature as accurately as possible. This is done by measuring the resistance (R), using the thermal coefficient of resistance (α), as shown in equation 2.27.

$$R = R_{ref}(1 - \alpha_r(T - T_{ref})) \tag{2.27}$$

With reference resistance (R_{ref}) which is measured at the reference temperature (T_{ref}). Due to the heating of the material the resistance increases. Hence, by supplying a fixed current, the potential across the sensor must also increase. To accurately determine the temperature, α_r must be large and the increase in resistivity vs temperature must be linear over a large temperature range. α_r is dependent on the deposition method, the thickness and microstructure [35]. Therefore, before the temperature can be related to a specific resistance calibration measurements are always necessary for each sensor.

2.3 Process technologies

The following section is used to get a better understanding of the underlying process technologies of the original SCT and TASCT processes. This is complemented by the theory of wet etching of silicon in KOH, which is a key process used in the newly developed S-TASCT.

2.3.1 Surface Channel Technology

The SCT, developed by M. Dijksta *et al.* [8] offers two main features. The first feature is the creation of low-stress Si_xN_y channels directly underneath the substrate. Subsequently, the channels are fully enclosed, which leaves the surface of the substrate intact. This enables the implementation of a second feature. Because the surface is still intact additional process steps, such as lithography, can still be used after the creation of the channels. These photomasks can then be used for patterning the outlines of sensing or actuation materials, without leaving residues behind inside the channel. The creation of micro-fluidic channels is done in a few steps as shown in figure 2.4. By applying a single mask containing segmented lines, holes can be etched into the silicon, using an isotropic etch step. This mask, often called a slit mask, is designed by using rectangles which are 2 µm in width and 5 µm(up to 15 µm) in length, including a 2-3 µm distance between the rectangles. By using low-pressure chemical vapor deposition (LPCVD) of silicon-rich nitride (SiRN), the sidewalls are created and the slits can be fully enclosed if the layer thickness is larger than these small slit dimensions. Because the channels are fully closed now, additional process steps can be included such as the deposition of metal layers on top or releasing structures from the bulk silicon by an isotropic under etching.

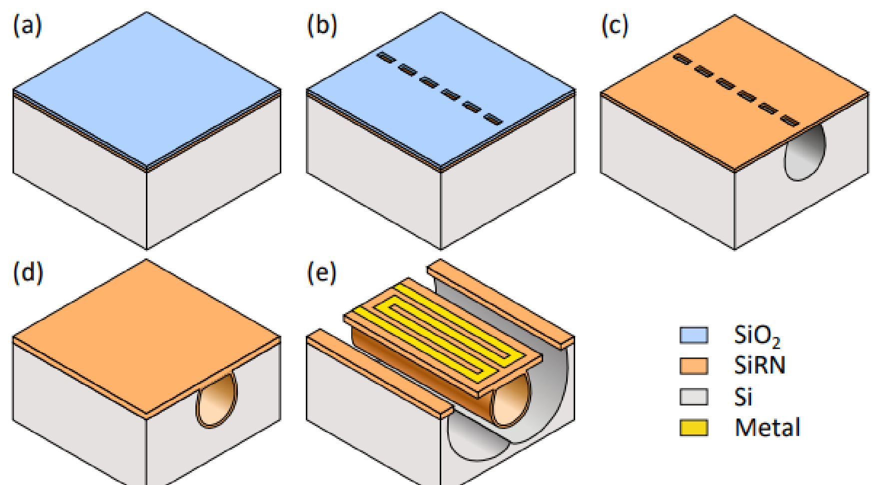


Figure 2.4: SCT fabrication process. **(a)** silicon wafer with 500 nm SiRN and a 500 nm SiO_2 hard mask; **(b)** Rectangular slits are patterned into the hard mask; **(c)** Channel etch and removal of SiO_2 hard mask channel; **(d)** Forming channel walls and closing of the slit openings; **(e)** Further processing possibilities e.g patterning of metal and release of the channel. Image taken from original source [16].

2.3.2 Trench-Assisted Surface Channel Technology

The core idea of TASCT is the creation of rectangular microfluidic channels by using refilled trenches, which act as etch stops in this process. The TASCT fabrication process is firstly introduced in the work of Veltkamp *et al.* for the fabrication of large-volume rectangular channels using a SOI substrate [15]. Simultaneously an introduction was made by Zhao *et al.* to use this technology for a miniaturized fuel gas combustion reactor [14]. Some years later Veltkamp *et al.* also published work about using the TASCT for the fabrication of high-power silicon sidewall heaters for fluidic applications [21]. The core of the TASCT in both works was the same but, the most recent work of Veltkamp *et al.* shows an improved version of the process. This TASCT process used to make microfluidic channels with integrated silicon SHEs is described in 3 main phases: Fabrication of microfluidic channel and heaters; Integration of the sensors and electrical connections; Release of the microfluidic channel.

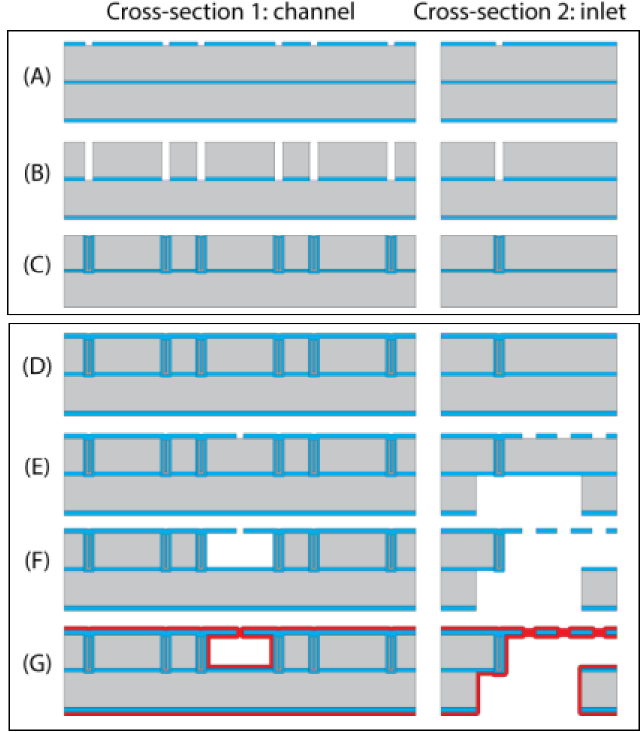


Figure 2.5: TASCT fabrication process phase 1 (A,B,C) and phase 2 (D,E,F,G). (A) silicon wafer with 1500 nm t-SiO_2 hard mask; **(B)** High aspect ratio trench etch; **(C)** Refilling of channel with SiO_2 and poly-silicon; **(D)** New 500 nm t-SiO_2 hard mask;**(E)** Slit patterned into hard mask; **(F)** Channel formation by etching the silicon with XeF_2; **(G)** Formation of the channel walls and closing of the slits by using LPCVD of SiRN. The colors represent: Si SiO_2 poly-Si SiRN. Image adapted from its original source by cutting the picture in half [21].

Fabrication of microfluidic channel and heaters

In figure 2.5 **(A)** the outline for the heaters and microfluidic channels is given. These outlines, which are 3 µm wide trenches, are patterned with broadband UV photolithography and etched into a thermal SiO_2 (t-SiO_2) hard mask using RIE. In **(B)** the trenches are etched using a high aspect ratio Bosch-based deep reactive ion etching (DRIE) process, until the BOX layer is reached at a depth of 50 µm. In **(C)** these trenches are then refilled, with first t-SiO_2 and second with low-stress poly-crystalline silicon, both via LPCVD. The excess p-Si and t-SiO_2 on the front and backside are

removed via RIE processes. In **(D)** a fresh layer of t-SiO_2 is deposited using LPCVD used as a front and backside hard mask. In **(E)** the slits of 1.6 µm by 3 µm are patterned with high accuracy using broadband UV photolithography. The slits are etched into the front mask using RIE. In the backside mask large inlet holes are patterned with broadband UV photolithography and etched using RIE in combination with a high-rate Bosch-based DRIE process. In **(F)** the channels are etched isotropically through the slits using vapour-phase XeF_2. During this step the t-SiO_2 in the trenches and in the BOX layer act as an etch-stop. In **(F)** the channel walls are created by depositing SiRN with LPCVD.

Integration of the sensors and electrical connections

In figure 2.6 **(H)** openings are patterned with broadband UV photolithography into the SiRN and SiO_2 layers, which are etched using RIE. After a vapor-phase HF treatment to remove native SiO_x, both 20 nm tantalum and 200 nm platinum are sputtered on the wafer. This is complemented by plasma-enhanced chemical vapor deposition (PECVD) of a 30 nm Si_xN_y pre-capping layer, which is used as a protection layer for the metal etching. The metal mask is patterned with broadband UV photolithography into the pre-capping layer using RIE. Ion beam etching (IBE) is used to remove the metal and pre-capping layer. A final PECVD Si_xN_y capping layer is deposited, used to protect the metal layers and to prevent oxidation. This layer is also patterned with broadband UV photolithography and etched using RIE.

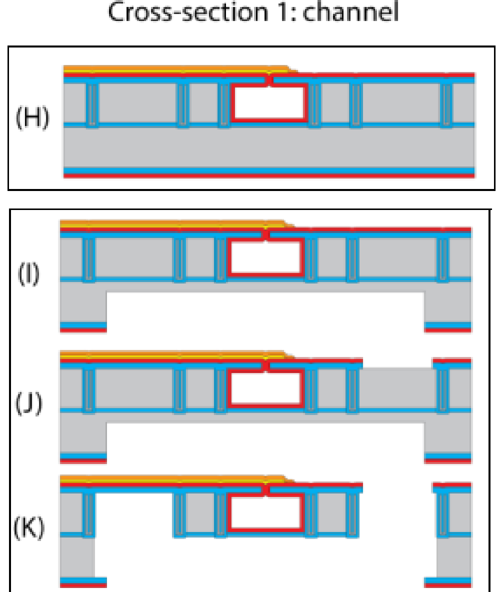


Figure 2.6: TASCT fabrication process phase 3 (H) and phase 4 (I,J,K). **(H)** Sensors and electronic connections created by depositing Ta/Pt, patterned via IBE and encapsulated by depositing PECVD Si_xN_y; **(I)** Cavity created by Bosch etching the backside for releasing structures; **(J)** Opening of frontside windows for releasing structures; **(K)** Final release step by etching the silicon with XeF_2. The colors represent: Si SiO_2 poly-Si SiRN metal capping. Image adapted from its original source by cutting the picture in half [21].

Release of the microfluidic channel

In figure 2.6 I-K, the microchannels are released in two steps using the Sacrificial Grid Release Technology [36]. First, a dry film resist foil (DuPont MX5020) is deposited on the backside and patterned with a cavity pattern using broadband UV photolithography. This pattern is etched into the SiRN and TEOS using RIE. Secondly, using a highly uniform Bosch-based process, the cavity pattern is etched to a depth of 300 µm. Next, the front side cavities are formed, via broadband UV photolithography, in the SiRN and annealed TEOS, and etched with RIE of in combination with gaseous-phase XeF2 etching of silicon. The remaining silicon in the handle-layer is etched by the same XeF2 recipe as the front side. This last step also include the releasing of the chips via dry etching release structures. The cross-sectional SEM image of the microfluidic channels and silicon heaters fabricated using TASCT can be found in figure 2.7.

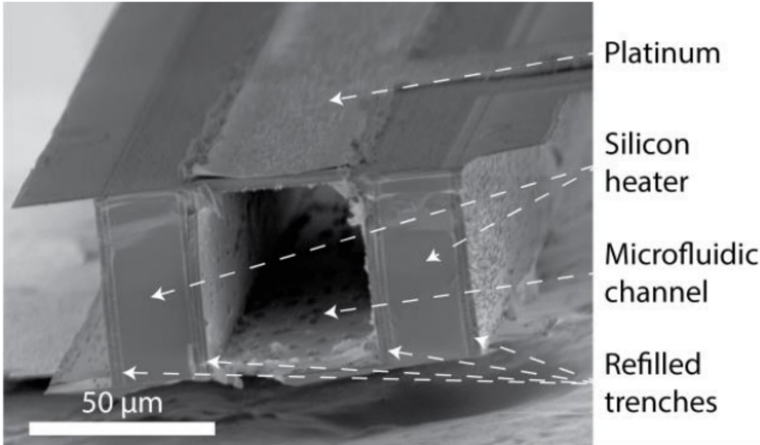


Figure 2.7: Cross-sectional SEM image of the microfluidic channels and silicon heaters using TASCT. Image taken from its original source [21].

2.3.3 Wet etching of silicon in potassium hydroxide solution

KOH among tetramethyl ammonium (TMAH) and sodium hydroxide (NaOH) can be used for etching crystalline silicon anistropically. The etching of KOH is favored in this work because it has been found that using TMAH solution results in a higher undercut rate and lower silicon ⟨100⟩etch rate with respect to KOH solution [37]. This will be explained more in the subsections below. The etching of silicon by KOH is described in a two-step process. The first step is a surface activation step, where a hydroxyl anion attacks the surface of the silicon and forms a SiH complex. The second step is the dissolution of the activated group, by oxidizing the complex. This forms SiOH and detaches from the surface. During this process also a new SiH complex is created for the next etching cycle due to released electrons [38]. The anisotropic nature of KOH etching is caused by different etch rates of the crystal planes. These different etch rates are a result of different atomic packing densities for the {100}, {110} and {111} planes. Crystal planes with lower packing densities etch faster with respect to other planes because less atoms have to be removed in order to remove a complete monolayer. The etch rates for the standard recipe of 25wt.% KOH at 75°C used in the MESA$^+$ cleanroom, are given in table 2.1 [39].

Table 2.1: Etch rates for the standard KOH etch recipe used at the MESA$^+$ cleanroom [39].

Material	Etch rate in 25wt.% KOH at 75 °C	Selectivity to ⟨100⟩ plane
Si ⟨100⟩	60 µm/h	1
Si ⟨110⟩	100 µm/h	0.6
Si ⟨111⟩	0.75 µm/h	80
t-SiO_2	0.18 µm/h	300
SiRN	$<$ 0.006 µm/h	10000

Etching of a ⟨100⟩ silicon wafer

When a mask containing rectangular squares is patterned onto a (100) silicon wafer and is exposed to KOH solution, a typical pyramid-shape will form. The reason for the shape is that etching along the ⟨100⟩ directions is faster than etching along the lateral ⟨111⟩ directions. The etching will almost stop when (111) planes meet in the top of this pyramid. If a cross section perpendicular to the wafer is taken, as shown in figure 2.8 then, the slope of the sidewalls is determined by the off-normal angle between the intersection of a ⟨111⟩ sidewall and a (110) cross-secting plane. This angle is exactly given by $\arctan(\frac{\sqrt{2}}{2})$ or 54.74°.

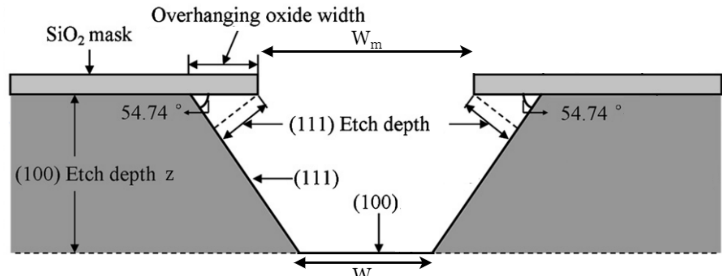


Figure 2.8: KOH etching in silicon, with a SiO_2 hard mask. By choosing a mask opening W_m, the width of the pit (pyramid) W_0 at an etch depth z can be calculated, because a typical slope of 54.74° forms between the mask and the Si (111) planes. Image adapted from its original source [37].

The end width, W_o, of the pyramid-shaped can then be determined by the total etch depth, z, the opening in the mask, W_m and the sidewall slope given above:

$$W_o = W_m \cdot 2\cot(54.74°) \cdot z \quad or \quad W_o = W_m - \sqrt{2} \cdot z \tag{2.28}$$

By looking at equation 2.28 it can be seen that how larger the opening in the mask the deeper the endpoint of the etch stop will be. KOH etchant can thus be applied to either release structures by wafer true etching if the opening in the mask is sufficiently large, or it can be used to create typical KOH pits (pyramids) inside the silicon to create small pyramid-shaped vias.

Under-etching

As explained before the etching characteristics of KOH etchant are orientation dependent. After a predetermined period of etching the mask opening, the structures will be formed according to the different etching rates of the different crystal planes. One unavoidable side issue is the under etching of the mask as shown in figure 2.8. If for a given etch time, the desired depth z is needed, then this is

determined by the window opening [40]. However, during the etching of the ⟨100⟩ direction, also the ⟨111⟩ direction will be etched, which enlarges the effective window opening. If we call the new mask width W_z, the effective mask width at a depth z. Then the relation between W_z and W_m will be given as shown in equation 2.29.

$$W_z = W_m + 2R_{<111>}\Delta t_z \tag{2.29}$$

with R_{111} the etch rate of the Si<111> plane and Δt_z the etch time to reach a depth z. The under etching (U_z) of the hard mask is then given by

$$U_z = R_{111}\Delta t_z. \tag{2.30}$$

The etch time to reach, a depth z is given by the R_{100} etch rate, and during this time the under etch will be formed with etch rate R_{111}. The new width of the pit (W_{tot}) at depth z (which was previously given by W_0) is now given by the sum of W_m plus twice the underetch for that same depth

$$W_{tot} = W_m - \sqrt{2} \cdot z + 2 \cdot \frac{R_{111}}{R_{100}} \cdot z. \tag{2.31}$$

In the work of S. Singh *et al.* [41], differences in etching characteristics of KOH were investigated. Another problem was found using KOH etchant on a silicon wafer. It was found the tolerance of the sidewall slope is determined by how well the flat of the wafer is aligned with respect to a ⟨110⟩ crystal direction. This is typically noted on the wafer specifications and often ranges between 0.5° to 1°. Any deviation from this angle will result in more undercutting of the mask. This also means that masks aligned to the flat of the wafer, hence, to the ⟨110⟩ crystal direction will also result in undercutting. An example of this is shown in figure 2.9. The extra undercutting (U), due to misalignment to the ⟨110⟩ direction, by an angle δ for a mask length l, can be calculated using the trigonometric relation, as shown in equation 2.32.

$$U = l \cdot \sin(\delta) \cdot \cos(\delta) \tag{2.32}$$

This extra undercut also influences the W_m and should be measured after the etching process. Moreover, because of free-hanging silicon heater structures, which are also aligned to a ⟨110⟩ crystal direction, hanging down inside the wafer, silicon that resides here will also be prone to the extra undercutting, due to misalignment to a ⟨110⟩ crystal direction. To calculate this undercut the same equation 2.32 can be used. However, this undercut can be minimized by optimizing the etching time, if these structures are etched last.

Other problems with KOH etching

Another problem with using KOH solutions is that organic photoresist dissolves rapidly [42]. Therefore, a hard mask with high selectivity to silicon is required, such as a silicon dioxide or a silicon nitride hard mask according to table 2.1. Another problem with wet etching in combination with releasing microfluidic channels is that KOH always leaves residual in-soluble floccules inside the microfluidic channels and on the wafer surface [43, 44]. For further processing after etching in KOH, the wafers need to be cleaned in RCA-2 to remove all KOH residues. This limits processing possibilities, as all materials which are affected by RCA-2, such as metals, cannot be used [8]. All These problems must be taken into account when incorporated into a micro-fabrication process flow.

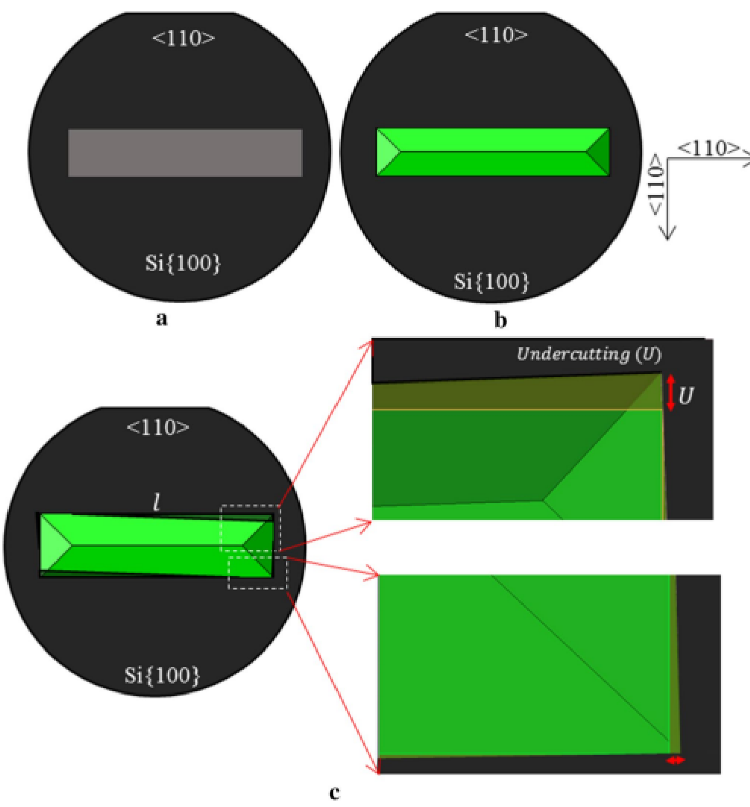


Figure 2.9: Effect of the misalignment in KOH etching of silicon. In **a**, a rectangle is patterned onto the mask using the wafer flat as reference for the alignment to the ⟨110⟩ crystal direction. In **b** the mask is perfectly aligned and no extra undercut will occur. In **c**, the mask is inaccurately aligned to the ⟨110⟩ direction, which will result in an extra undercut U. Image taken from its original source [41].

2.4 Conclusion

This chapter provided all the fundamentals necessary for designing the demonstrator device in chapter 3. Moreover, key process steps for both the SCT and TASCT were be explained in more detail. This revealed that no simplifications could be easily made in the integration of the sensors and electrical connections. By analysing the wet etching of silicon in potassium hydroxide solution it was made clear that etching in KOH solution can bring new complications to the TASCT platform. The first complication involved the undercutting of the hard mask openings due to a finite Si ⟨111⟩ etch rate of 0.75 µm/h. This also means that SHEs exposed to KOH solution will also be prone to undercutting. Another, more notable, influence is caused by misalignment of the masker windows to a Si ⟨100⟩ direction. For small angles (<1 °C) and dependent on the mask length, this undercut can already become very significant. It is expected that because the SHEs are only exposed to KOH solution briefly that this undercut will be minimal.

3 | Design

In this chapter, we start by describing the new S-TASCT in detail. The technology is explained in steps and critical parameters, which have an impact on the design and the micro-fabrication process, will be discussed. Next, the demonstrator device is explained. The theory from the previous chapter is applied here to determine the device dimensions, geometry, specifications and to verify the model in COMSOL Multiphysics 5.6. The analyses will be conducted on a basic model, which can therefore not be used for accurate quantitative measurements because not all the complex fluid kinetics involved are used in this model. The basic model will only be used for the analysis of two qualitative aspects. The first study will be done to determine the main heat loss mechanism when heating up an airflow to 600 °C using electrical heaters. The second study will investigate the influence of heat loss due to residual silicon on the outer sidewalls. Afterward, the resulting masks for the fabrication of test structures and demonstrator devices are shown and the process flow of the S-TASCT process is presented.

3.1 The S-TASCT process

The main goal of S-TASCT, as explained in chapter 1, is to reduce the amount of micro-fabrication steps compared to the TASCT. A second goal is to prevent release etch-related problems described in the TASCT process [21]. A possible solution to fulfill both goals is the usage of a KOH wet release etch process. Including a KOH wet etching process in the TASCT platform seems very contradicting, because this can introduce a lot of problems, as explained in section 2.3.3.

However, most of the problems resulting from a KOH wet etch can be avoided if the micro-fluidic channels are not exposed to KOH solution and if the KOH step is the final micro-fabrication so no additional cleaning is required, which still allows for metals to be used. Therefore an approach is presented to create the micro-fluidic channel and fully enclose them. After all micro-fabrication steps are completed, access to the micro-fluidic channels must be created manually by puncturing a thin membrane.

Moreover, by using KOH solution, the devices can be released from the bulk, whilst simultaneously allowing for the formation of pyramid-shaped vias to the channels. As opposed to the TASCT process which requires multiple extra masks for realising the same structures. Additionally, several device outlines can be specified, which can then also be released from the wafer in this step. Hence, including KOH wet etching process can offer a significant reduction in total micro-fabrication steps required to make functional devices. However, because of the typical etching characteristics of KOH solution, the final structures of the heater are different compared to the TASCT. All aspects concerning the KOH release are discussed in subsection 3.1.4.

Similarly to the TASCT process, the S-TASCT can be divided into several stages:

- Defining the silicon electrode and microfluidic channel dimensions;
- Fabricating microfluidic channels through a slit masker;
- Creating access to the electrodes and intergration of electronics;
- Creating pyramid-shaped vias to the microfluidic channels, releasing of microfluidic channel structures with heaters from the bulk and releasing devices from the wafer.

The first two stages include the most complex micro-fabrication steps and form the core of the TASCT. Fabrication steps in these stages have been optimized during the last two years. Together with the author of the original TASCT process [21], minor simplifications were added to these first two stages. Therefore, only the important micro-fabrication steps are discussed in subsections 3.1.1, 3.1.2. Also, no alternations have been made to the third stage and this stage is therefore briefly discussed in subsection 3.1.3.

3.1.1 Defining the silicon electrode and microfluidic channel dimensions

Stage 1 of the S-TASCT fabrication process, the outlines for defining the silicon electrodes and microfluidics is given in figure 3.1. In (A), we start by growing a 1.5 µm thermal oxide hard (t-SiO_2) mask layer, on a highly doped silicon wafer. This t-SiO_2 hard mask is very well suited for accurate transfer of the 3 µm wide trenches, using broadband UV photolithography and RIE of t-SiO_2. The electrode size can be determined by the spacing S between two closely placed trenches. The channel width can be determined by choosing a width W between two trench couples. In (B), the trenches with a depth of H_1 are etched using a high-aspect-ratio (HAR) Bosch-based deep reactive-ion etch (DRIE). Important for this etch is that no significant tapering (<1 µm) will exist throughout the trench and that the trench does not widen further (<500 nm). The H_1 for this work will be 75 µm because the aforementioned specifications can still be met with the available equipment. In (C), The t-SiO2 is removed using 50% HF solution and the trenches are cleaned and dried for several days in a heated drying vessel under a flow of nitrogen. The trenches are then filled with 2.4 µm SiRN in a LPCVD furnace. In (D), the trench width of 3 µm, in combination with this LPCVD process causes V-grooves, with a height H_2, to form on the surface. These V-grooves are dependent on the trench width, so the wider the trenches, the deeper these V-grooves will be. To further smoothen the surface and reduce the size of these V-grooves, the excess 2.4 µm layer will be removed and a fresh 500 nm SiRN will be deposited using LPCVD. This will reduce the V-grooves even more.

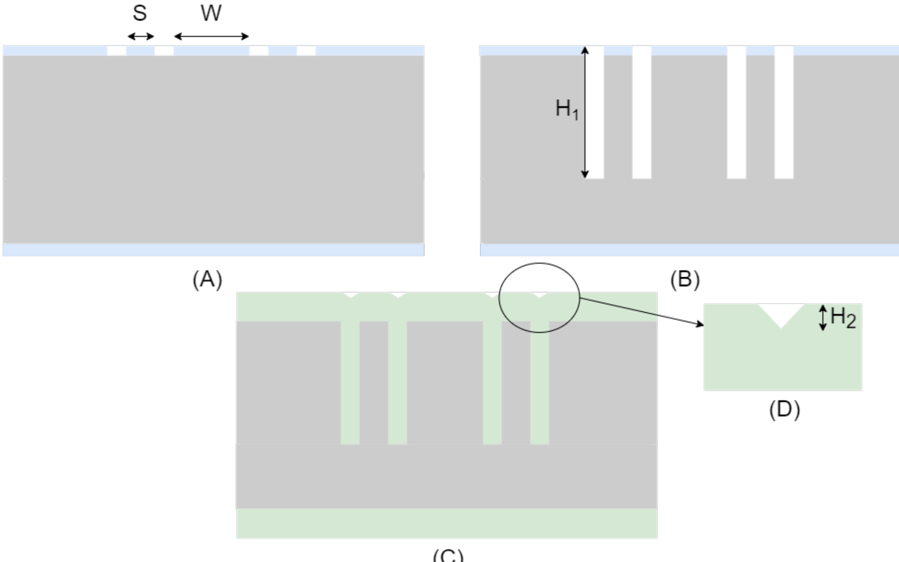


Figure 3.1: Stage 1 of the S-TASCT fabrication process. **(A)** 1.5 µm thermal oxide is grown on a highly doped silicon wafer. Mask openings with a width of 3 µm are etched into the t-SiO_2 by using RIE. The electrode size can be determined by the spacing S between two closely placed trenches. The channel width can be determined by choosing a width W between two trench couples; **(B)** HAR trenches are etched into the silicon via a Bosch-based DRIE etching process. The trench height H_1 determines the maximum possible electrode height and channel height; **(C)** The t-SiO_2 is removed and the trenches are filled with at least 2 µm SiRN in a LPCVD furnace. **(D)** This results in V-grooves with height H_2. The colors represent: Si t-SiO_2 SiRN

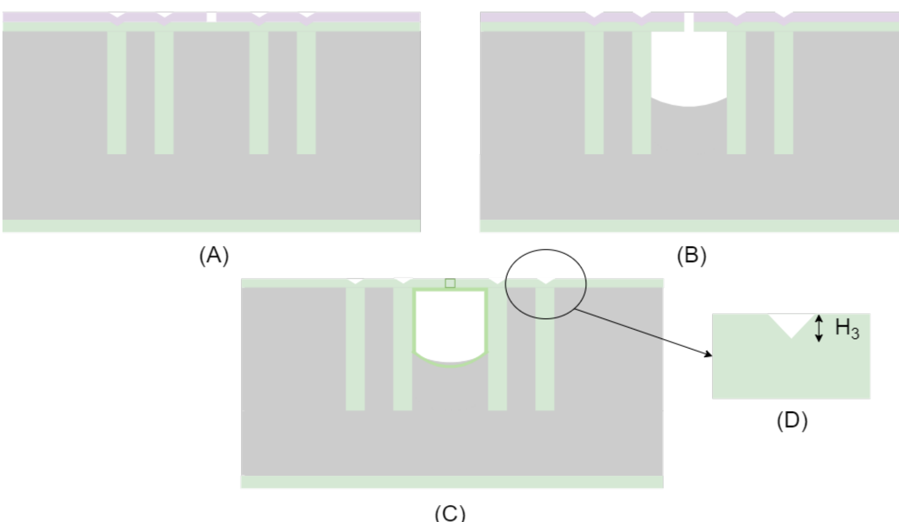


Figure 3.2: Stage 2 of the S-TASCT fabrication process. **(A)** The 500 nm SiRN is complemented by 100-200 nm aluminium oxide hard mask layer, which is deposited by evaporation. The slits are patterned into the AlOx. The AlOx layer prevents the slits from widening in the next step; **(B)** Channels are etched by first etching isotropical through the SiRN layer, subsequently anisotropical into the silicon **(C)**. The AlOx layer is removed prior to the forming of the channel walls and enclosing the slits which are done by depositing at least 1.6 µm LPCVD SiRN. In (D) the V-grooves with height H_3 remains to exist after these process step. The colors represent: Si SiRN AlOx

3.1.2 Fabrication of microfluidic channels

In stage 2 of the S-TASCT process, the microfluidic channels are formed as shown in figure 3.2. First in (A), a complementary 100-200 nm aluminium oxide (AlOx) hard mask layer is deposited by evaporation. This layer ensures that the slits do not widen throughout the channel etch. The slits of 1.6 µm by 3 µm are patterned with high precision into the AlOx using broadband UV photolithography and RIE. It is crucial that these slits are well defined, as this has a significant impact on the microfluidic channel dimensions. If slits are not fully transferred no channel can be created underneath that slit in the subsequent step. If the slits are smaller than 2 µm, then the etch time to reach a sufficient depth will be longer. If slits are too wide, they cannot be regrown. In (B), the SiRN hard mask is opened using a multi-layer RIE of SiRN, which ends with an isotropic strike. This strike creates a small round cavity in the silicon under the slit. This can be observed using an optical microscope and guarantees the slits in the hard mask layers are all opened properly. After this, the AlOx is removed and the channels are formed using an isotropic etch of silicon. In (C), the channel walls are formed and the slits are closed using LPCVD of 1.6 µm SiRN. The expected V-groove in (D) will now be < 400 nm.

3.1.3 Integration of on-chip electronics

Stage 3 of the of S-TASCT process involves the integration of on-chip electronics, as shown in figure 3.3 and a capping layer, as shown in figure 3.4. The first part of this integration in (A) is completed by patterning the contact-pad openings to the SHEs via broadband UV photolithography and opening the SiRN layer with RIE. In this step also the front release windows must be included already. In (B), native oxide on the contact pads is removed using vapor-phase HF to achieve good contact, which is directly followed by sputtering of 5 nm platinum. This Pt layer is annealed at 450 °C to form platinum silicides. This is done to improve the adhesion on SiRN layers. After the anneal in (C), a combination of 10 nm Ta and 200 nm Pt is sputtered on top. This is followed by a 30 nm thick Si_xN_y pre-capping layer using PECVD. In (D), the metal layer is patterned via broadband UV photolithography and RIE of the metal stack and pre-capping layer. The pre-capping layer ensures that during the etching of the metal layer no reflow will occur. The topview in (E) shows how the metal layer patterned across the device, the pre-capping layer is not visible in this picture. A final 70 nm thick Si_xN_y capping will be deposited in (F) via the same PECVD process. The capping layer will be patterned via broadband UV photolithography and opened with RIE of Si_xN_y in (G). The topside view shown in (H), reveals that only the bondpads have an exposed metal layer. The rest of the metal layer is covered by the capping layer.

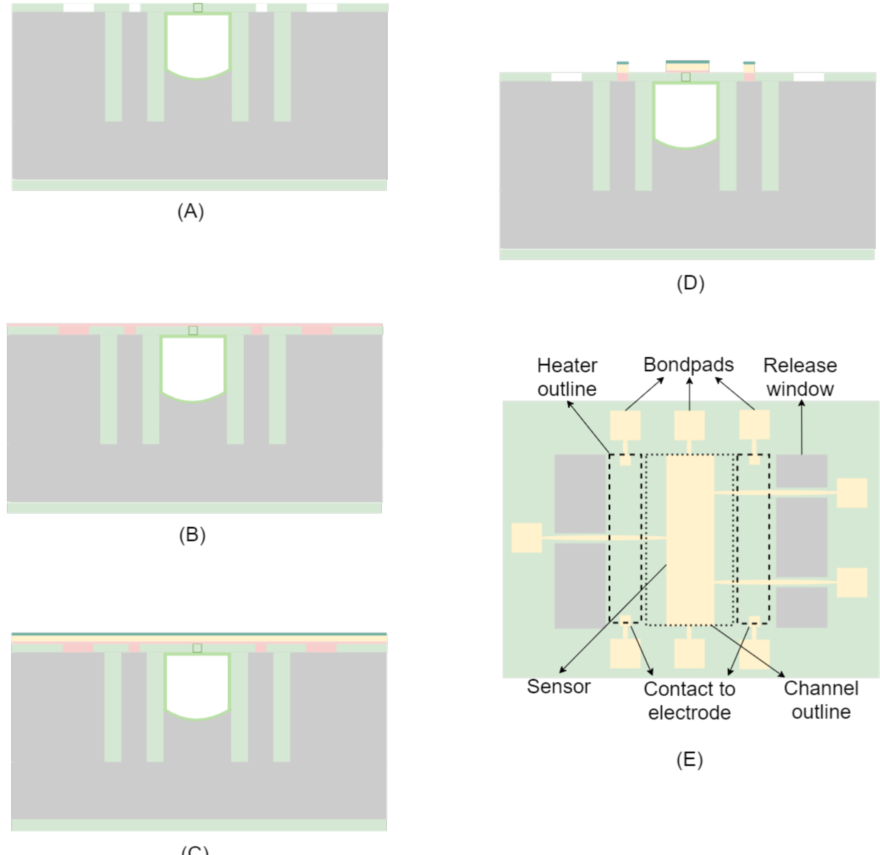


Figure 3.3: Stage 3.1 of the S-TASCT fabrication process **(A)** The contact-pad openings to the SHEs and front release windows are patterned in the SiRN via broadband UV photolithography and RIE. In **(B)**, native oxide on the contact pads is removed using vapor-phase HF, directly followed by sputtering of 5 nm platinum. The platinum is annealed in **(C)** and a combination of 10 nm Ta and 200 nm Pt is sputtered on top followed by a 30 nm thick Si_xN_y pre-capping layer using PECVD. In **(D)**, the metal layer is patterned via UV photolithography and RIE. In **(E)** the top-view shows how the metal layer is patterned across the device, the pre-capping layer is not visible in this picture. The colors represent: Si SiRN Pt Ta/Pt Si_xN_y

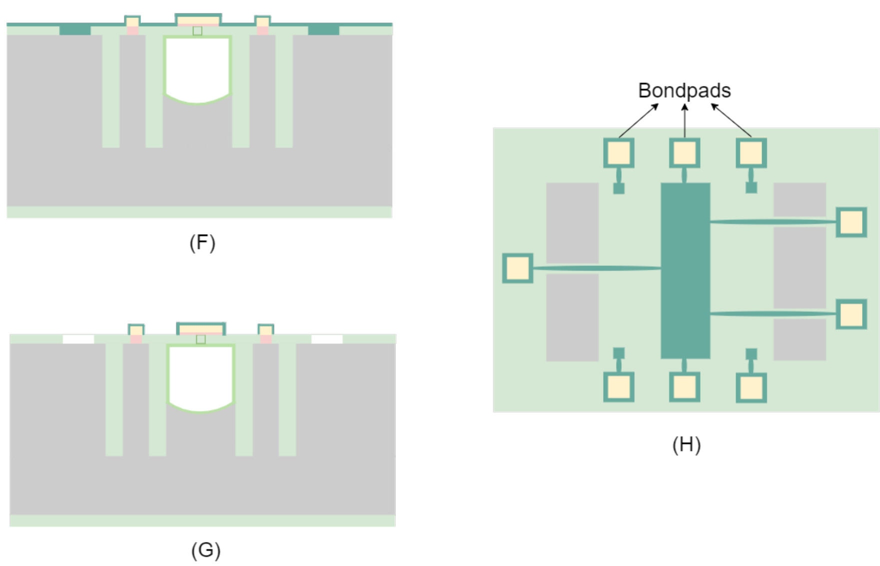


Figure 3.4: Stage 3.2 of the S-TASCT fabrication process. In **(F)** a 70 nm thick Si_xN_y capping layer is deposited via PECVD. In **(G)** the capping layer is patterned via broadband UV photolithography and opened with RIE of Si_xN_y. The topside view shown in **(H)**. The colors represent: Si SiRN Pt Ta/Pt Si_xN_y

3.1.4 Microchannel access and device release

The number of microfabrication steps with respect to TASCT can be highly reduced by combining the release of the devices from the bulk silicon with the fabrication of inlet and outlet vias. The approach taken to realize this is shown in figure 3.5. In the left column, the micro-fluidic channels are realized as designed, by using one row of slits (A) together with an isotropic plasma etch process (B). Once the walls of the channel have formed and the slits are closed again using LPCVD SiRN, the device can be released from the bulk using a front release window and a large back window. Simultaneously, in the right column, by increasing the number of slits on top of the wafer, deeper channels can be formed. However, if the amount of slits is doubled this will not mean that the microfluidic channel will become twice as deep for the same etch time. From earlier experiences, it is expected that by using 4 or 5 rows of slits with 3 µm separation, the channel will become 1.5 to 2 times deeper in contrast to using one row of slits. Once the microfluidic channel walls are formed in (C), again a small back release window can be used to create a small via to the membrane. This back window in (D) also needs to be designed in such a way that a needle can be inserted to manually puncture the membrane after all process steps have been completed.

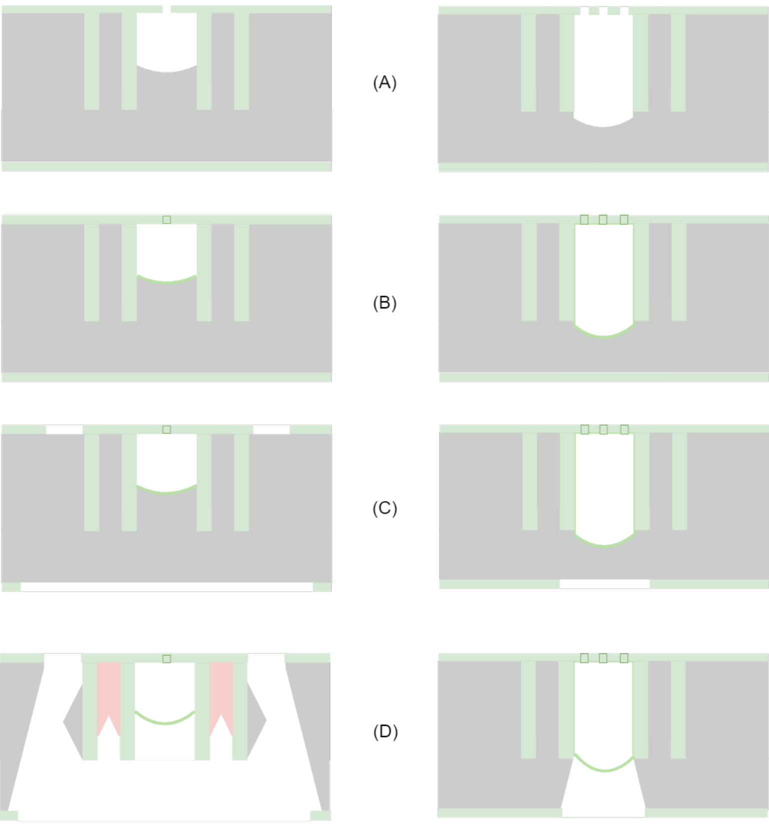


Figure 3.5: Stage 4 of the S-TASCT fabrication process. In the left column, the release steps are shown. In the right column, the access holes to the channel are formed. **(A)** One row of slits is used for the formation of channels, while multiple rows of slits are used for the formation of deeper channels. **(B)** LPCVD SiRN forms the channel walls and closes the slits. It also forms a membrane deeper in the silicon which seals the access holes for the final KOH release step. **(C)** Hard mask openings are made in the front side and back-side of the wafer. **(D)** Final release step by KOH etching, fully releasing the structures and creating a path to the buried microfluidic channel membrane. The colors represent: Si SiRN Si electrodes.

Because of the typical etching characteristic of KOH, the release windows must be designed carefully. For the front release windows, two situations can occur. The first situation as shown in figure 3.6, uses small release windows. These windows must have a minimum window size, to reach at least half the trench depth, else the devices will not be released from the bulk. The minimum window size can be calculated by solving equation 2.31. By filling in half the trench depth maximum trench of 75 µm, we find a W_r size of 52 µm. However, because much higher etch times are needed from the back of the wafer to reach the middle of the trenches, a significant undercut will occur in the top inverted pyramids. As an example, to reach the bottom of the trenches from the back-side, a distance Z_1 needs to be etched. This is equal to the total silicon wafer thickness of 75 µm minus the consumption of 1.5 µm silicon from oxidation, minus the depth of the trenches at 75 µm, which equals 448.5 µm. At this time the front side inverted pyramid has reached a depth of 35 µm plus an under etch in the ⟨111⟩ direction of $448.5 \cdot \frac{R_{100}}{R_{111}} = 5.1$ µm. The total etch depth left is Z_5, which will be equal to 35 µm. The total etch distance from the bottom of the wafer will be 483.5 µm. This will take a total etch time of 8 hours and 2 minutes.

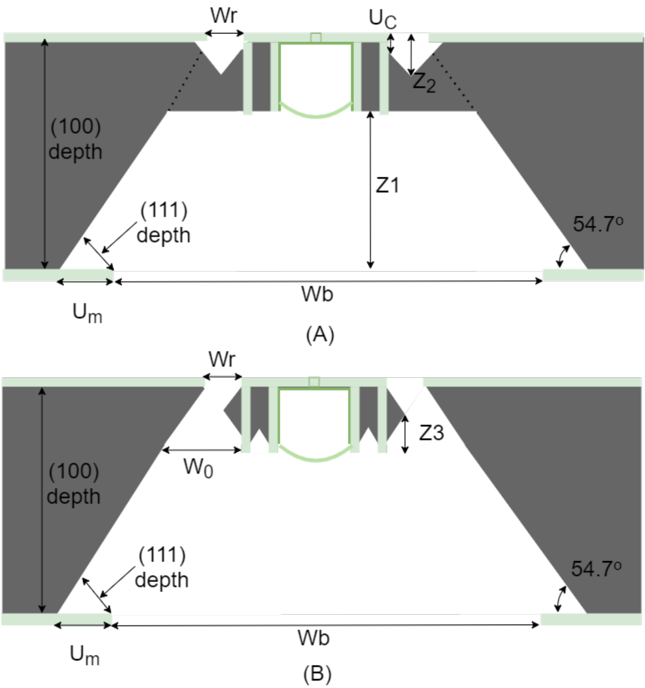


Figure 3.6: By using a small front release window W_r in (A), the upside pyramids end before the end of the trenches, with a depth of Z_2. Now the height Z_2 up to the silicon electrodes have to be etched. This leaves residual silicon on the outer walls of the trenches. Therefore it can be chosen to over etch (C), this also results in etching of the electrode. The colors represent: Si SiRN Si electrodes.

The second situation can occur if large front release windows are used, as shown in figure 3.7. The minimal release windows size can again be calculated by solving equation 2.31 By filling in the complete trench depth of 75 µm, we find a W_r size of 97.24 µm. By etching to a depth of Z_1 the front side pyramids already reach the end of the trenches. Now only a distance of Z_2 needs to be etched to completely release the devices from the bulk. The total etch depth from the back-side is thus given by Z_4 which again equals 448.5 µm. This requires a total etch time of 7 hours and 28 minutes. However, by making an example calculation for the residual silicon on the side of the heaters, as shown in figure 3.8, much larger residuals are present on the trench walls. Therefore, it can be chosen to

etch further with a depth Z_5, which also equals 35 µm. The total etch time is then again equal to 8 hours and 2 minutes. This also results in the same residuals in the case with smaller release windows. However, a benefit of using larger release windows is a much larger separation distance between the bulk silicon and the devices. This distance, in both scenarios, is determined by half the top window W_r size.

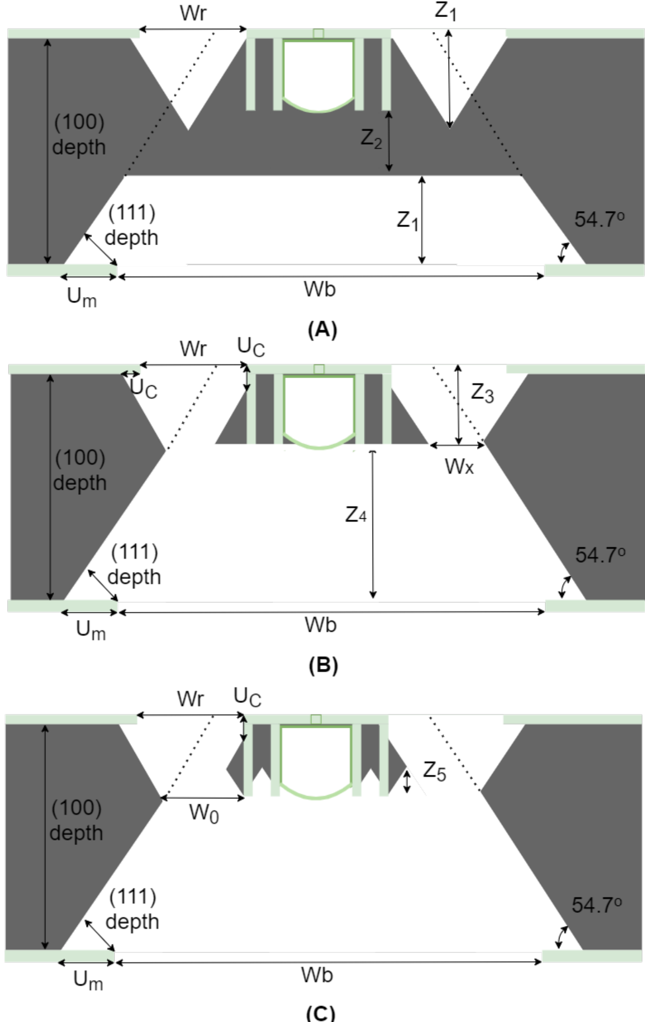


Figure 3.7: By using a front release window W_r larger than 97 µm in (A), the upside pyramids already reach past the trenches, after etching a depth of Z_1. Now the height Z_2 up to the silicon electrodes have to be etched. This leaves residual silicon on the outer walls of the trenches. Therefore it can be chosen to over etch (C), this also results in etching of the electrode, which will eventually create the residuals as in 3.6. The colors represent: Si SiRN Si electrodes.

There is also some design freedom for the back-side windows to create pyramid-shaped vias. Dependent on how deep the membrane is formed, the window depth and size can be adjusted. By using equation 2.31, the W_{tot} can be chosen at a certain depth, which will result in the required mask opening W_m. For example, if a window opening of 65 by 65 µm is required at the maximum trench depth of 75 µm, then by equation 2.31, this requires a back-side mask opening of 725 by 725 µm.

Another important aspect is that by using KOH, not all silicon can be removed in all places. This so-called, residual silicon, will be left behind on the outer sides of the outer trench walls. An example calculation for the residuals of the maximum trench depth of 75 µm can be found in figure 3.8.

In **(A)**, with a trench depth of 75 µm and heater width of 15 µm then by using small release windows of 50 µm and with an undercut (U_C) of 5.1 µm the silicon residual will be 860 µm^2.

This also means that for the case of figure 3.7 **(B)** this will lead to much larger residuals as no silicon is etched underneath the channel. This also may lead to complications if the heaters are not fully isolated from the (bulk) residuals.

However, if the channel depth is smaller than the trench depth, more residual silicon will be left behind as shown in figure 3.8 **(D)**, The total residual under the channel will be dependent on the channel width (W), trench to channel distance (D) and total etch time. By fully etching distance D, the residual under the channel can be approximated by using $(\tan 35.3° \times D)^2$. For a channel height of 50 µm and a maximum trench depth of 75 µm this would lead to 313.3 µm^2 extra residual under the channel.

For all cases, it is crucial that silicon used for the electrodes is fully isolated from any bulk silicon and dependent on the application of the device, residual silicon can have a significant influence on the performance. For example, if the fluid inside the channel needs to be heated, then a lot of heat will be dissipated through thermal conduction on the ends of the residual silicon sticking into the bulk silicon.

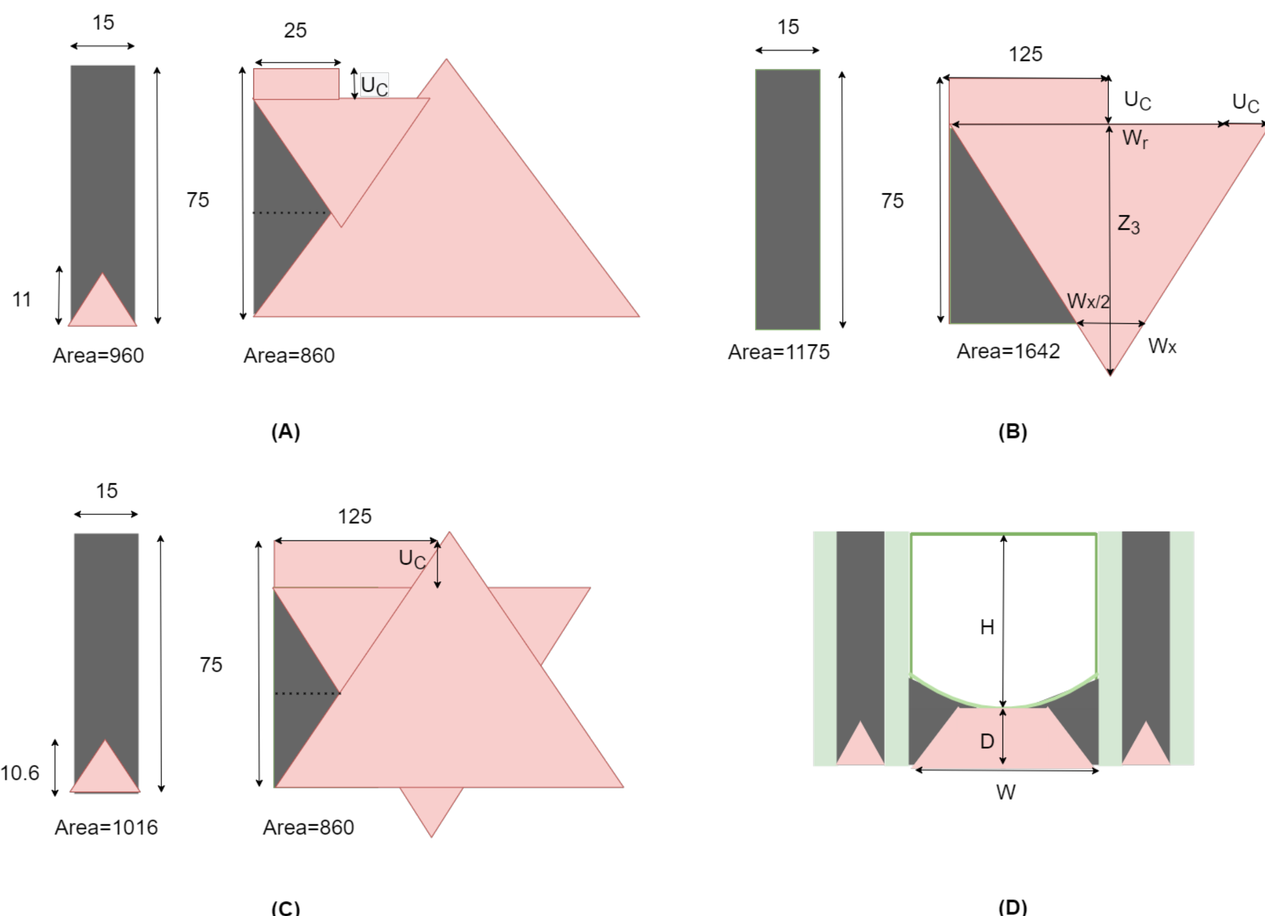


Figure 3.8: Example calculations for the residual silicon. In (A), with a trench depth of 75 µm and heater width of 15 µm by using small release windows of 50 µm and with an undercut (U_C) of 5.1 µm the silicon residual will be 860 µm^2. By only etching to the end of the trenches in (B) this residual will be 1642 µm^2. By using large release windows the same residual will be left in as in (A). In (D), if the channel height does not equal the trench height, then the residual under the channel can be approximated by $(\tan 35.3° \times D)^2$. The colors represent: Si SiRN Removed Si by KOH etching

3.2 Demonstrator device

Because the newly introduced S-TASCT includes a few process steps that are not used in similar technologies, such as TASCT, a demonstrator device is designed. This device is used to test the viability of the S-TASCT technology as a platform for microfluidic devices with integrated heaters and sensors. This device contains multiple domains: A microfluidic channel, two highly-doped silicon sidewall heaters; A metal sensor strip on the top side of the channel; Insulating SiRN channel walls. The main geometries such as channel dimensions and heater dimensions are based on the same dimension used for devices developed for the TASCT process, to have a good comparison for the device performance of both technologies. The newly designed devices should also be compatible with existing mounting boards for fluidic and electronic inputs and outputs to save time. From all design parameters, a computer-aided design (CAD) model is constructed in the CAD software SOLIDWORKS 2020. The CAD model is imported into the FEA software COMSOL Multiphysics 5.6. By using the flow package, the joule heating package and the heat-transfer package the demonstrator device's behaviour can be modelled. In order to verify the model, trivial calculations will be executed first, which are also described in the sections below. The model is used to investigate two important aspects. The first study is to determine the main heat loss mechanism when heating up an airflow to 600 °C using electrical heaters. The second study is about the influence of heat loss due to residual silicon on the outer sidewalls.

3.2.1 Microfluidic channels

In the following subsections all important aspects for modeling the microfluidic channels are described.

Dimensions

Although, the S-TASCT process offers a lot of design freedom for the channel dimensions, the final geometry will be mainly rectangular with one slightly circular side. Also, this new demonstrator device should be comparable to the TASCT demonstrator device. Therefore, rectangular channels with a width of 50 µm, a height of 50 µmand a length of 10 000 µm are desired. The main limitation for rectangular microfluidic channels according to the S-TASCT process description, will be the height of the channels, as this is dependent on the depth of the high aspect ratio trench etch. The maximum trench depth, using 3 µm wide trenches openings will be 75 µm and therefore the maximum channel height will be also 75 µm.

Mass flow input

The gas input for channels is regulated via mass flow controllers. The available mass flow controller is an EL-FLOW Select F-201CV, made by Bronkhorst High-Tech bv. [45], with a minimum flow range of 1.05 mg/h - 52.52 mg/h to a maximum flow range of 45.01 mg/h - 675.2 mg/h. From equation 2.9 it can be seen that higher mass-flow rates require more power to heat the gas to the same temperature. A future goal of S-TASCT is to heat an air-methane mixture to the auto-ignition temperature of around 600 °C. In order to react all methane present in this flow a good stoichiometric combustion is required with a slight excess of air to prevent sooth forming. According to the AFR (equation 2.21) for a stoichiometric combustion with 10% excess air, a combination of 10 mg/h methane with 188.415

mg/h of air can be used. 10 mg/h methane flow is close to the lower limit on the mass-flow controller and leads to a total flow of 198.415 mg/h. In the COMSOL model only air is simulated and because the heat capacities of a methane/air mixture and pure air are different, a corresponding airflow of 240.415 mg/h pure air is needed. The detailed calculations to convert a methane and air mixture to a corresponding pure airflow can be found in appendix C.

Pressure drop & flow velocity

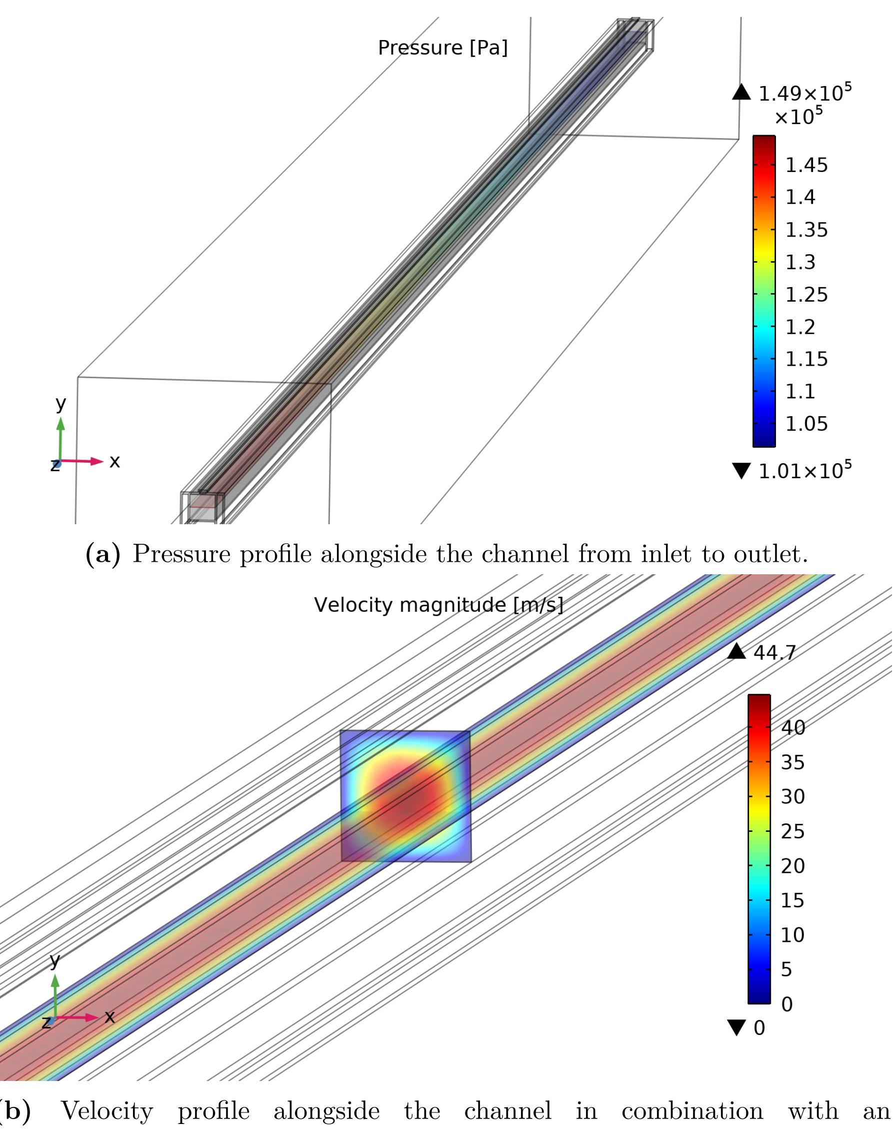
Since the mass flow rate is known, the Poiseuille flow approximation for a rectangular channel equation 2.14 can be used to calculate the pressure drop over the channel.

The relation between the mass flow rate ($\dot{m}$) and volumetric flow rate (Q) is the density of the material (ρ), as $\dot{Q} = \dot{m}/\rho$. The corresponding airflow is thus equal to a volume flow rate of $6.68 \cdot 10^{-8}$ m^3/s. By rewriting equation 2.14 and filling in the dynamic viscosity of air at room temperature, the height, width and length of the channel, gives a pressure drop of 63078 Pa over the channel. However, the pressure drop over the channel using equation 2.15, including the friction coefficient, shows a pressure drop of 13838 Pa for $C_{fr} = 14.22885$ and pressure drop of 93370 Pa for $C_{fr} = 96$. For the flow velocity, the volumetric flow rate Q is given by the product of the mean velocity and the cross-sectional area, as shown in equation 2.16. Filling in a cross-sectional area of the channel gives a mean velocity of 26.72 m/s. The maximum velocity is given as twice the mean velocity, which is 53.44m/s.

As shown in figures 3.9a and 3.9b, the values provided for the pressure drop and mean flow velocity by COMSOL are 48 kPa and 22 m/s respectively. This pressure drop is not within the 13% error range described in the work of H.Bruus [28]. However, the maximum flow velocity of the COMSOL analysis is within 13% error. The COMSOL value for the pressure drop is also between the lower and higher C_{fr} values used for calculating the pressure drop, which seems reasonable. The order of magnitude for the pressure drop and the flow velocities provided by COMSOL Multiphysics seem sufficient to provide qualitative results.

3.2.2 Heaters

Also for the heater dimensions, the S-TASCT process can offer a lot of design freedom and the final geometry will be a rectangle, with a triangular cut. One benefit of the S-TASCT is that the heater height is not limited by a BOX layer at a depth of 50 µm. In this case, the heater height is limited to a maximum trench depth of 75 µm in combination with potential undercutting due to mask miss-alignment to the Si ⟨110⟩ crystal directions. The width of heaters can be chosen freely by choosing a spacing between the trenches that encloses the silicon heater. This new demonstrator device is designed to be comparable to the TASCT demonstrator device, which used 20 µmby 50 µm heaters, with a length of 10 000 µm. Because the new heaters have triangular cuts and possible undercut the cross-sectional areas will decrease if the same dimensions are used. Therefore two heater dimensions are considered for this work. The first heater has a width of 15 µm, this results in a slightly bigger surface area of the channel wall, as compared to the TASCT heater. The second heater has a width of 25 µm and is used to create the same cross-sectional area and the same surface area to the channel wall, as used in de TASCT. The heights and allowed undercut to fabricate the same cross-sectional area as the TASCT heaters are calculated as shown in figure 3.10. For both designed heaters the



(a) Pressure profile alongside the channel from inlet to outlet.

(b) Velocity profile alongside the channel in combination with an cross-sectional profile.

Figure 3.9: Pressure & velocity profiles in micro-fluidic channel. In **(a)** the pressure drop over the channel is 48 kPa, from input to output. In **(b)** the velocity from 0 m/s at the walls to the maximum velocity of 44.7 m/s at the center.

undercut (U_C) is strongly dependent on the alignment of the masker to a Si⟨110⟩ orientation. If the masker is perfectly aligned to this crystal plane, U_C will be minimized and equal to the height of the pyramid times $\frac{R_{111}}{R_{100}}$, which equals 0.13 µm and 0.22 µm respectively, for figure 3.10 **B** and **(C)**. When the undercut is minimized the produced heaters will of course both have a much bigger cross-sectional area then the TASCT heaters, this can lead to different performance for Joule heating as the specific heat capacity is dependent on the volume of the heaters.

The resistivity of the P-type highly doped silicon wafer is specified from 0.001 Ω cm to 0.1 Ω cm on the wafer box ordered from Si-Mat Silicon Materials. However, a measurement done by H-W. Veltkamp [21] showed a resistivity of 0.012 Ω cm at 25 °C for wafers with the same specification. Also an increased resistivity of 0.019 Ω cm at 375 °C was reported. These values are used for further calculations. Now that the cross-sectional area, length and resistivity is known the resistance can be calculated using equation 2.25. The total resistance for one small heater will be 1600 Ω. The total resistance for one wide heater will be 1200 Ω. Typical electromigration effects start at current

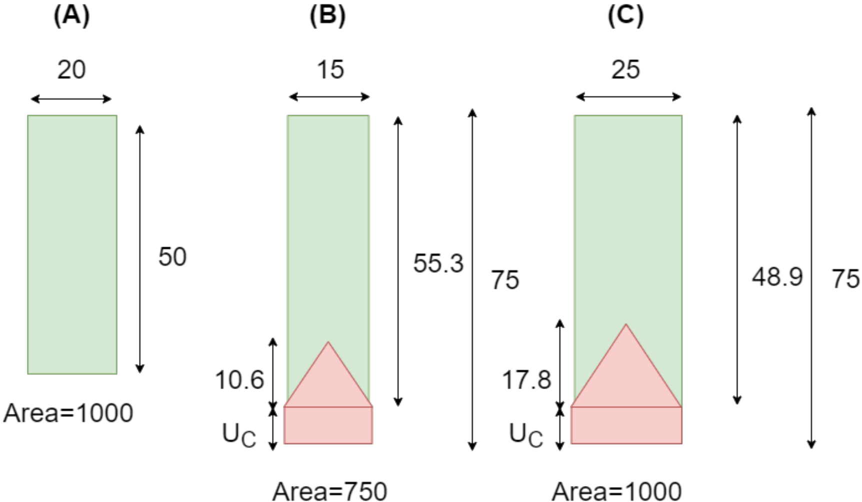


Figure 3.10: S-TASCT heater dimensions. In **(A)** The orginінal TASCT heater dimensions resulting in a cross-sectional area of 1000 µm^2. In **(B)** and **(C)** the heater dimensions considered for this work. In **(B)** a width of 15 µm and a height of 55.3 µm results in a cross-sectional area of 750 µm^2, but the surface area to the channel wall is bigger. The allowed undercut for this heater is 19.7 µm. In **(C)** a width of 25 µm with a height of 48.9 µm results in the same cross-sectional area as the TASCT heater. The allowed undercut for this heater is 26.1 µm

densities of >10^4 A/cm^2 [34]. To be on the save side, the limit for the maximum applied voltage on the heaters will be set at 100 V, which result in a maximum current density of 8333 A/cm^2 at 25 °C and 2627 A/cm^2 at 375 °C for the small heaters, the current densities for the wide heaters will be smaller, due to a smaller cross-sectional area.

3.2.3 Sensors

The usage of platinum in the TASCT process was mainly because its resistance depends linearly on temperature over a wide range of temperatures. As described in the S-TASCT process, first a small layer of platinum is sputtered and annealed which forms platinum silicides for proper adhesion to the SiRN. Then a metal stack combination of platinum with a small amount of tantalum was deposited. This alloy has a higher melting point than solely platinum [46]. This makes the sensor stack more stable at higher temperatures. Also, the chemical inertness and mechanical stability at elevated temperatures make it a perfect material when used as temperature sensor. However, at higher temperatures > 500 °C, degradation mechanisms are accelerated [11]. Therefore a pinhole-free Si_xN_y capping layer is required.

The dimensions of the sensor are bounded by both the electrode stack, which is 200 nm, and by the channel width, which is left between the release windows. Therefore, for this design the cross-sectional area will be $200\ nm \cdot 25\ \mu m = 5\ \mu m^2$. The resistivity of bulk platinum is $10.5 \cdot 10^{-8}\ \Omega \cdot m$ [11]. By choosing the length of a sensor at 2500 µm. The total resistance for a sensor will be around 210 Ω at room temperature. In the work of H-W. Veltkamp [21] a TCR (α_r) value was determined for the same electrode stack as used in this work. A TCR of around 0.0024 K^{-1} was found, which deviated from the bulk platinum TCR of 0.0039 K^{-1} [35]. This deviation was ascribed to thin-film effects (e.g grain boundaries or defects). Filling in equation 2.27 with the resistance at room temperature gives $R = 210 \cdot (1 + 0.0024(T - 25)$. By expanding this equation we find $R = 0.504\ T\ + 197.4\Omega$. So, an increase of 1 degree in the temperature results in an increase of around 0.5 Ω in resistance.

The heat released or LHV from the combustion reaction according to equation 2.17 and equation 2.18 will be −846.288 kJ/mol. The mass flow of methane was determined at 10 mg/h, which is $1.732 \cdot 10^{-7}$ mol/s. This will result in an energy release of 0.147 J/s. This is equivalent to 147 mW of power added to the system. The calculated power needed to heat up the corresponding airflow 600 °C, will be explained in the next section and corresponds to around 50 mW. The power generated upon a combustion reaction is three times as high. It is therefore expected that the combustion reaction results in a significant temperature increase to the surroundings, which therefore should be easily measurable by the sensors.

3.2.4 Electrical power to heat an airflow

As explained in the theory chapter, the amount of power needed to heat up an airflow is given by equation 2.9. Therefore, by using the mean heat capacity for air, which is 1.2480, the power needed to heat up the corresponding airflow of 240.415 mg/h by 600 K is 50 mW. However, this is not equal to the amount of electrical power needed because a lot of the generated heat is lost to natural convection of air around the device, radiative losses due to the high operating temperatures of the heaters, or conductive losses to the bulk silicon, which maintains a constant (room)temperature.

To get an estimate for the electrical power needed the main losses have to be taken into account. These are natural convection to the ambient air or all surface areas that make contact with the ambient air; Radiative heat loss which is emitted away from the channel, hence all outside surface areas pointing away from the microfluidic channel; Conductive heat loss to the bulk silicon, which mainly occurs at where the silicon electrodes make contact with the bulk, hence the cross-sectional areas at the end of the electrode.

Natural convection losses

The natural convection can be calculated by equation 2.3. Natural convection occurs at the surface area in contact with ambient air, which is the top and bottom side SiRN and the outer SiRN trench plane across the full length of the heater. The total surface area prone to natural convection for two small heater is $2.1\,\mathrm{mm}^2$, for the two wider heaters $2.5\,\mathrm{mm}^2$.

By using an approximation for h as $20.45\,\mathrm{W\,m^{-2}\,K^{-1}}$, which can be found using the work of M. Pap [47] and assuming a temperature increase of 600 K, the power loss for two small heaters is 25.8 mW. The power loss for two wider heaters is 30.7 mW. Both losses are very significant with respect to the power needed to heat up the corresponding airflow. However, the effect of heat loss due to natural convection can be omitted if a high vacuum environment can be created around the device.

Radiative losses

Due to the high temperatures involved the total heat generated by radiation also becomes significant, because the heat transfer by radiation scales with the T^4 as shown in equation 2.1. The generated radiation that is emitted away from the microfluidic channel are the same planes that are prone to natural convection. With $\sigma = 5.670367 \cdot 10^{-8} Js^{-1}\ m^{-2}\ K^{-4}$, the emissivity of silicon at 600 degree, which is 0.71 [48], the radiative heat loss is 34.6 mW for the small heaters and 37.39 mW for the wide

heaters. This again is very significant with respect to the power needed to heat a corresponding airflow from 293.25 K to 893.25 K. However, this calculation assumes that all silicon heater material has a ΔT of 600 K. This is not true, because a temperature profile will be present throughout the heater and only a fraction of the heaters will reach such high temperatures. To get an average from this temperature profile, a potential is applied to one heater to reach a center temperature of 600 °C. Then the average temperature from the total heater volume is taken. The value derived by COMSOL Multiphysics for the average temperature in the heater is 480 K. The new heat rate for the smaller heaters is therefore 5.86 mW, and for the larger heaters 6.33 mW. These are much lower and more realistic values as compared to the e.g. convective losses. Because of the high temperature of the heater body, this radiative heat loss is always present and therefore cannot be avoided.

Conductive losses

The edges of the heater, with cross-sectional areas of 750 μm^2 and 1000 μm^2 are insulated by 3 μm thick SiRN from the bulk silicon. An approximation can be made for the heat loss, which is generated as a point source at the center of the channel and moving to the edges. By using equation 2.2, with a ΔT of 600 K and a Δx of 5000 μm. The resulting heat loss for two small heaters will be 11.5 mW and for the wider heaters, the resulting heat loss will be 15.4 mW.

As shown in section 3.1.4, residual silicon will be present on the outer walls of the channel. Dependent on the etch time, these residuals will have a remaining cross-section of 860 μm to 1642 μm, which is very significant with respect to the heater cross-sectional areas. According to equation 2.2 the expected extra heat loss will be 13.2 mW for two small residuals and 25.2 mW for two larger residuals.

Total electrical power

The total required electrical power needed is thus, the power need to heat-up the corresponding airflow with 600 K and all heat losses. For small heaters excluding the residual silicon this will at least require 93 mW of electrical power. The wider heaters require at least 103 mW. The small heaters therefore require a current of 7.6 mA , which occurs by applying a voltage of 12.2 V. The wider heaters require a current of 9.3 mA, which occurs by applying a voltage of 11.1 V. These values seem reasonable and are well within the maximum voltage supply of 100 V. However, these values are a minimum power needed, because of conductive heating of the SiRN between the domains will lead to an increase of the effective surface areas hence, more radiative and conductive losses have to be taken into account.

3.2.5 COMSOL Multiphysics model analysis

In this section, the behaviour of the CAD models which have been imported in COMSOL Multiphysics will be investigated. The important domains are the Si heater domain, the micro-fluidic channel domain, the SiRN domain, the surrounding domain and possible Si residual domains. In the subsections below important analysis steps have been conducted.

Settings & Boundary conditions

The first important step using FEA simulations is verification of the model and ensuring that the correct boundary conditions are used. After the domains have been specified an according material

must be assigned to each domain. Due to different depositions methods used in the fabrication process, material properties (e.g thermal conductivity or resistivity) can vary a lot. Because not all materials are present in the COMSOL Multiphysics library, some material properties must be changed manually. Therefore for each material, all material properties were checked and altered if necessary. Secondly, the flow behavior in the channel was explored using the laminar flow package. This package required the definition of the reference pressure, the mass-flow inlet, outlet and wall conditions (e.g. slip or no slip). The resulting flow velocity and pressure drop over the channel were already verified in section 3.2.1. The model was complemented by the heat transfer in solids and fluids package. All domains must be assigned to either a fluid or a solid and all known boundary conditions must be applied. Those boundary conditions consisted of a constant outer shell temperature equal to room temperature or 293.15 K. Also, all surfaces areas that disappear in the bulk silicon are set to room temperature. For the heater surfaces pointing away from the micro-fluidic channel, a surface-to-ambient radiation source can be selected, this setting only requires the surface emissivity. Moreover, in the heat transfer package also a heat source can be assigned to the silicon heater domains to generate a certain heat flux (W/m^2). This can be used to verify the Joule heating package, which converts electric power to heat. In this Joule heating, all electrical conducting and insulating domains must be specified. Also, all electric potentials and grounds must be specified.

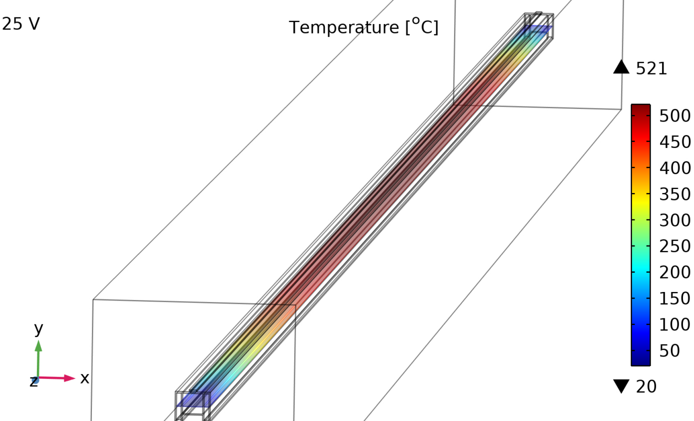
Heating up an airflow

A CAD model with two wider heaters, each with a cross-sectional area of 1000 μm^2, was used for this analysis. The first study included conductive, radiative and convective heat loss mechanisms. The applied voltage was started at around 10 V as calculated and increased with steps op 5 V to 25 V. From the temperature profile across the channel vs voltage graph in figure 3.11a it can be seen that at 10 V, the center temperature did not reach 600 °C. Only at 30 V, a temperature of607 °C was reached in the center, using a total electrical power of 1.1 W. This shows that the heat loss due to natural convection, radiation and conduction must be around 10.7 times higher than the calculated value of 103 mW. By switching off the surface-to-ambient radiation source only a few degrees of temperature change could be noticed across the channel. This indicates that the influence of heat loss via radiation is much less compared to natural convection and conduction combined.

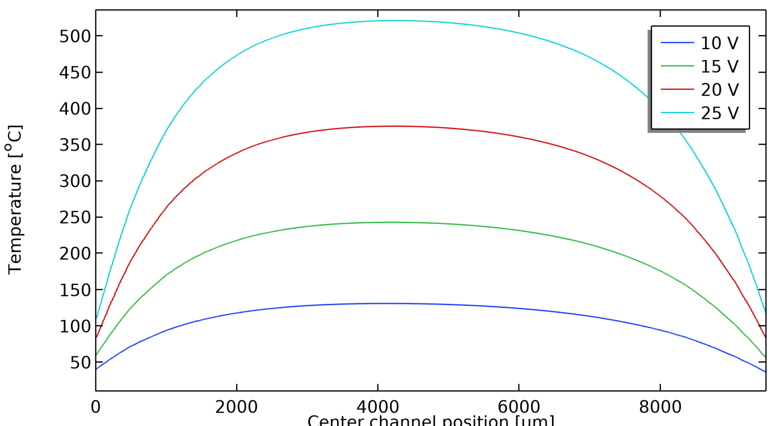
To further study the effect of convective heat losses, the same simulation was performed but the ambient was switched from air to vacuum. The results in figure 3.12 show a significant increase in temperature for lower applied voltages. This confirms that heat loss via convection is the most significant heat loss mechanism and is around 9 times higher as calculated. It is expected that the calculations only offer a minimal heat loss quantity and that the actual heat loss via convection is much higher due to a much larger surfaces area as opposed to the described surfaces areas, which are not directed towards the microfluidic channel. In order to reach much higher temperatures in the center of the microfluidic channel, without applying much higher voltages, it is recommended to place the devices inside a vacuum setup if possible.

Extra Heat loss due to residual silicon

Due to the residual silicon on the outer trench walls, more heat is lost via conduction to the bulk, so more electrical power must be converted to heat. If a vacuum environment is assumed, the convective term can be taken out, then, for the small heaters, a power of 80.5 mW or 92.5 mW is needed for small



(a) 2D Temperature profile after applying 25 V on the heaters



(b) 1D Temperature profile across the center from the beginning of the channel (10 000 µm) to the end of the channel (0 µm), for different applied voltages of 10-25 V.

Figure 3.11: In **(a)**, the resulting center temperature at 25 V did not reach 600 °C. In **(b)**, by increasing the voltage with steps of 5 V, higher temperatures were reached.

and large residuals respectively. This requires applied potentials of on the heaters 11.3 Vand 12.1 V. Two extra CAD models have been made. One contains a small residue with a cross-sectional area of 860 μm^2 and one with a large residue with a cross-sectional area of 1642 μm^2. For this study, the same two wider heaters, each with a cross-sectional area of 1000 μm^2 were used.

To study this effect of extra conductive heat loss in COMSOL, both the radiative and convective losses have now been turned off. In figure 3.13 the applied potential needed to reach a center temperature of 600 °C, for a device with small residuals **(a)** and one with large residuals **(b)** is given. The overall voltage must increase significantly to reach the same temperature as opposed to the scenario in figure 3.12, with no residual silicon. However, this gives a distorted picture because, if the cross-sectional area of the residual doubles, the conductive heat loss also doubles, but the voltage only needs to be increased from 13 to 15 V, to generate the same power to compensate for this extra heat loss.

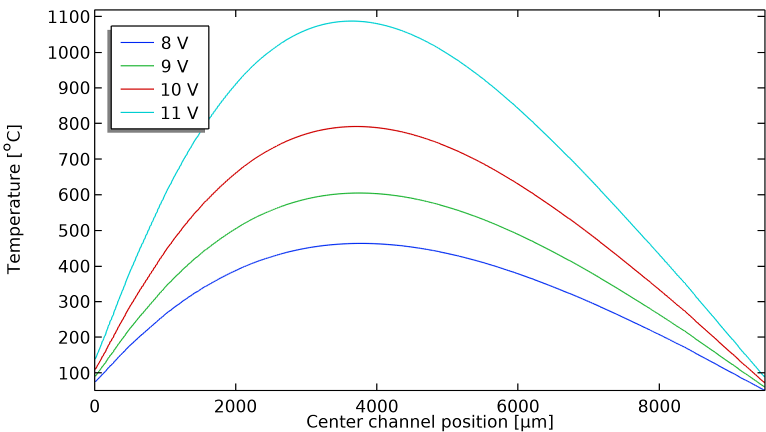
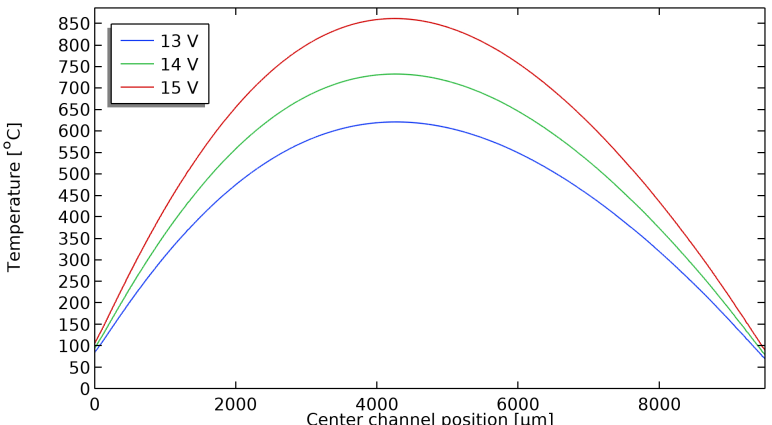
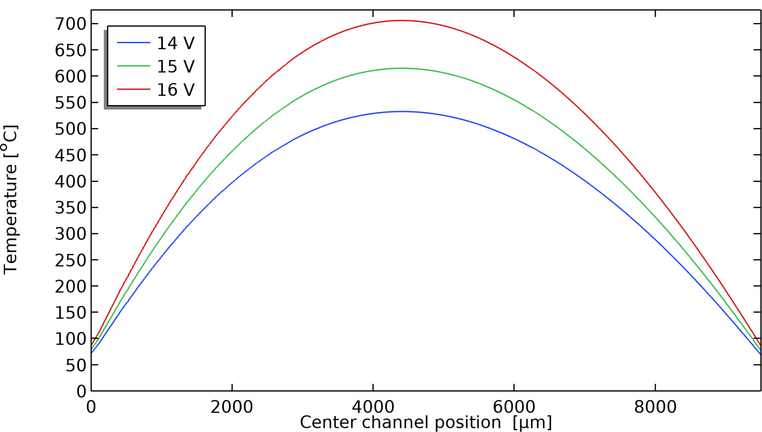


Figure 3.12: Applied potential vs temperature inside the channel from begin (10000) to end (0). A total electrical power of 81 mW is needed to reach a center temperature of 600 °C



(a) Applied voltages vs temperature alongside the channel for small residues



(b) Applied voltages vs temperature alongside the channel for large residues

Figure 3.13: In **(a)** Due to small residual silicon on the outside of the heaters a higher voltage of 13 V is required to reach a center temperature of around 600 °C. A slightly higher voltage just below 15 V is required for larger silicon residuals to reach the same center temperature of 600 °C.

3.3 Mask Design

This section will be used to explain what masks are needed for the test run and device. The according mask designs to realize the test structures and devices will be explained as well. All photo-lithography masks are designed by using the CAD software CleWin version 5.4.

3.3.1 Test run

In the test run the integration of the KOH wet etching process into the TASCT platform is tested. It is crucial that after the KOH wet etching step: the devices are fully released from the bulk silicon; access holes are created; Silicon electrodes are formed between the trench walls. In order to test the aforementioned a total of three masks are used, as shown in figure 3.14. The trench mask is used for all test structures. The back mask is designed for realizing two test structures. The first structure fully releases the devices from the bulk whilst leaving Si electrodes between the trench walls. This is realized by using large windows which can be used for wafer through etching. When smaller back windows are used, pyramid-shaped vias will be formed. The smaller back windows are patterned in an array setup. This is done to increase the chances of creating a cross-section through the middle of a pyramid-shaped via. An additional array mask is patterned to the front side of some wafers to create free-standing membranes, which can be punctured manually after fabrication. The complete mask design can be found in appendix A.3.1.

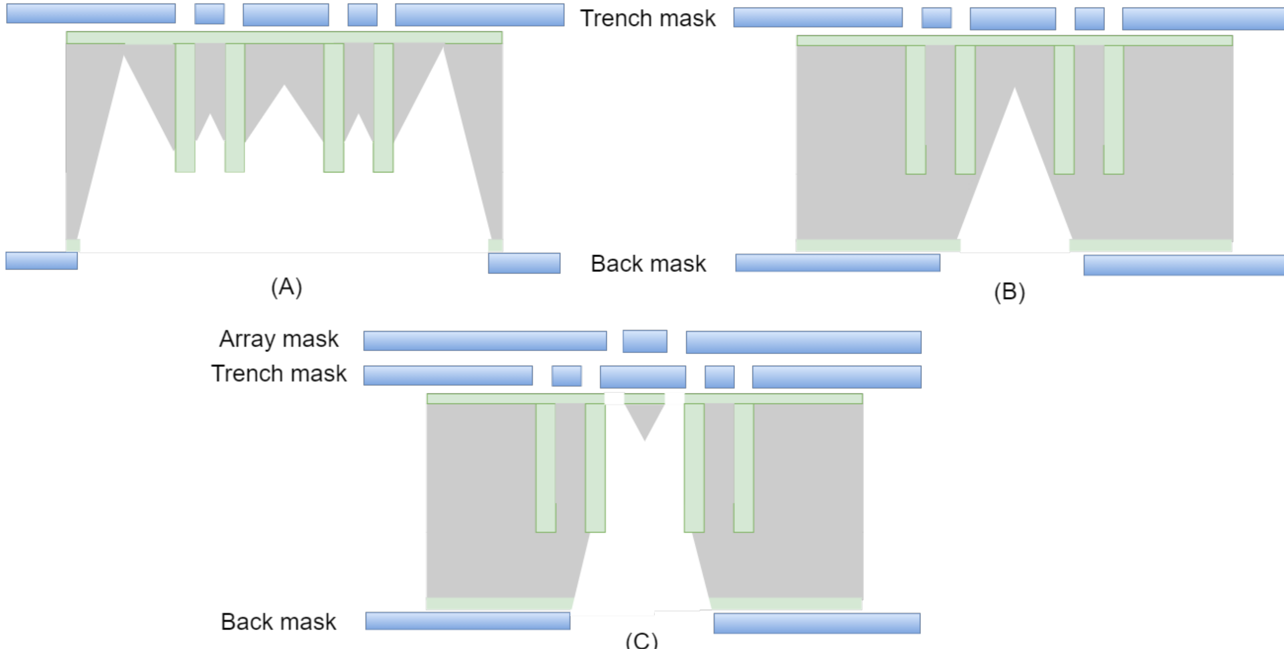


Figure 3.14: Masks needed for the realization of the S-TASCT test run process. **(A)** Test structure for fully releasing the devices from the bulk whilst leaving Si electrodes between the trench walls. Two mask are needed, a front trench mask and a back mask. The front trench mask is used for defining the electrode dimensions. The back mask should contain large windows which can be used for wafer through etching. **(B)** To test the fabrication of small access holes the back mask must also contain smaller windows. **(C)** To fabricate free-standing silicon membranes an extra front array mask is used. The mask is used to create openings in the front side SiRN hard mask. These openings allow free-standing membranes to form directly above the back-side access holes. The colors represent: Si Photo mask SiRN Si electrodes

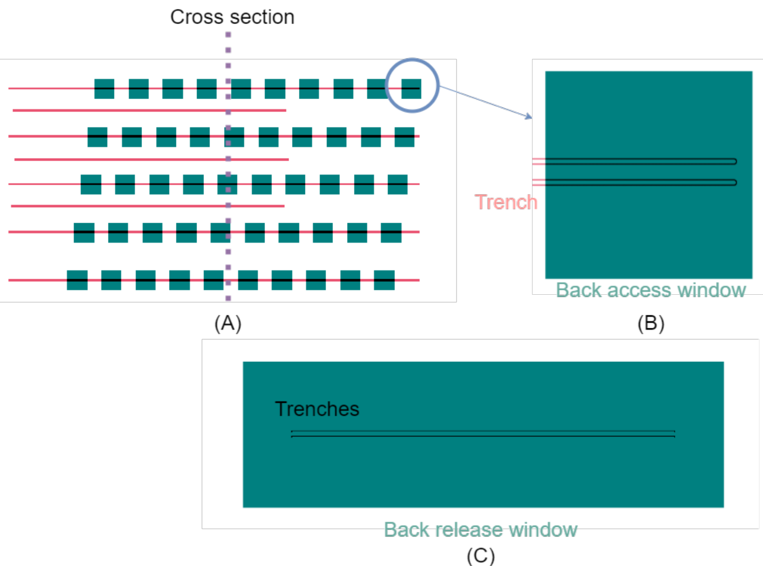


Figure 3.15: Masker design for test run structures. In (A), an array of inlets, this is used to increase the chances of cross-secting pyramid-shaped vias. In (B), a zoom-in on a small back access window in combination with the layout for the trenches. In (C), a large back window for releasing the devices from the bulk.

3.3.2 Device run

The full extent of the S-TASCT will be tested by realizing demonstrator devices. In order to create these devices, a total of six masks must be created, as shown in figure 3.16. The same mask set can be used to create devices fully isolated from the bulk, to create pyramid-shaped vias and to release the devices from the wafer. The combined masker design highlighting important segments is shown in figure 3.17.

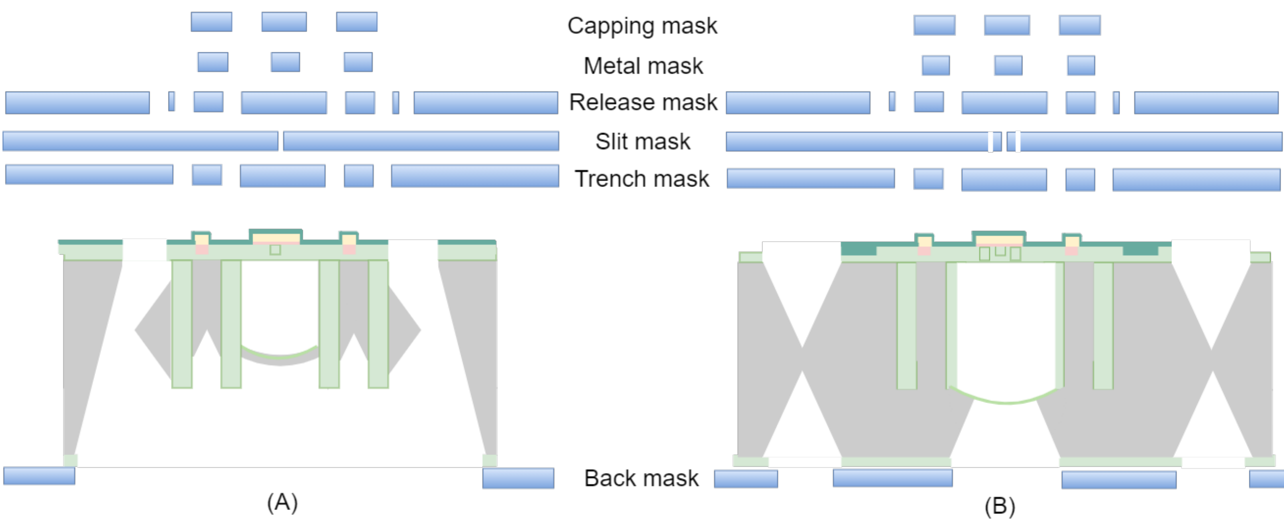


Figure 3.16: Masks needed for the realization of the S-TASCT device run process. In **(A)**, the device is released from the bulk silicon using a total of 6 masks. In **(B)**, the same mask set is used to realize the pyramid-shaped vias and release the devices from the wafer. The colors represent: Si Photo mask SiRN Pt Ta/Pt Si_xN_y

In this masker design the capping layer is omitted since this will only cover the metal mask with an identical 25 µm wider mask. In A, an electrical connection is made to the SHEs using 25×25 µm contact pads. The metal layer deposited on top is used to extend the electrical connection to the bond pads located at the edge of the device. The circular trench isolates bulk silicon from electrode silicon. In B, a sensor wire of 2000 µm is shown. The front release windows are directly located 10 µm next to the outer trenches. In C, 400×400 µm bond pads. In D, two trench walls with a spacing of 25 µm in between. The microfluidic channel is shown in the middle, with a metal sensor strip on top. A slit masker of 5×2 µm with 3 µm spacing. In E, an inlet/outlet segment containing several rows of slits in combination with a 712.5×712.5 µm back release mask. In F, a 150 µm device outline is drawn in the front release mask and in the back release mask, for releasing the devices from the wafer.

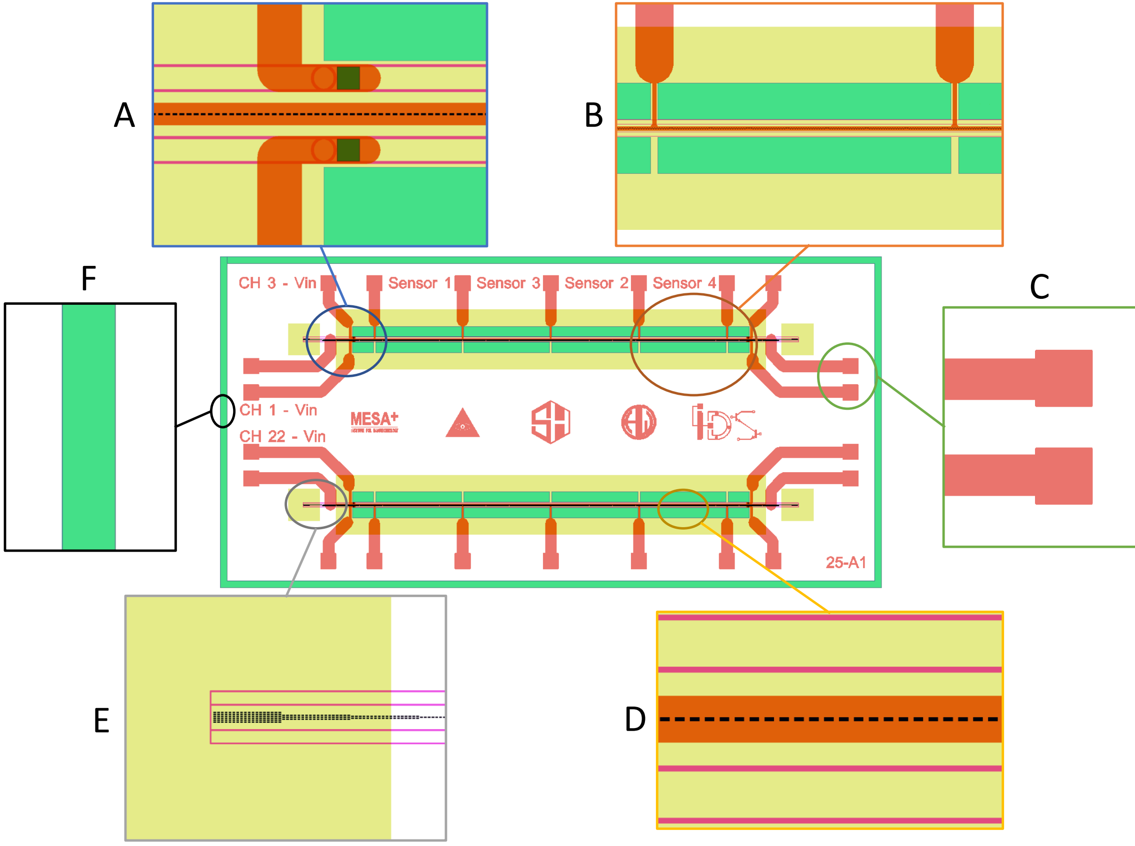


Figure 3.17: Mask design demonstrator device. In A, the contact pads to the SHEs and metal wires on top. In B, a sensor element and the front and back masker used for releasing the channels. In C, I/O metal contact pads. In D, a microfluidic channel element containing the trench outlines for the SHEs, the slit masker for the microfluidic channels and a metal wire on top as temperature sensor. In E, an inlet/out element containing more slits to create deeper channels in combination with a square back mask for the formation of the pyramid-shaped via. In F, on both the front release mask and back release mask a chip outline is drawn for releasing the devices from the wafer. The colors represent: ■ Back mask and front release mask overlapping ■ Metal mask ■ Metal mask ■ Back mask ■ Front release mask and metal mask overlapping ■ Slit mask ■ Trench mask

3.4 Process flow

To execute the newly developed technology two process flows are created, a test run process flows and a device run process flows. The test run process flow is executed first in order to test if the KOH wet etching release can be successfully integrated, to create the silicon sidewall electrodes and access holes via the puncturing of membranes. In the second process flow the devices described in section 3.3 will be realized.

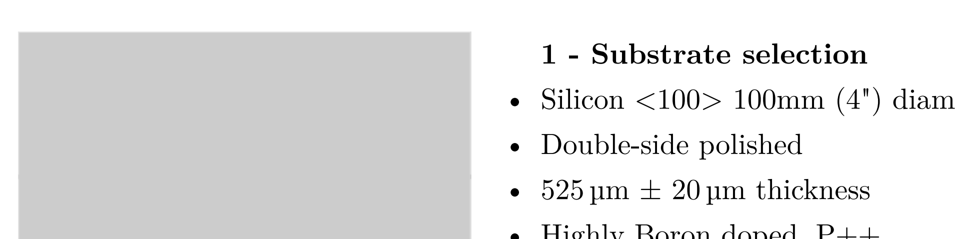
3.4.1 Test run

For the test run only steps 1-11 and 31-33 of table 3.1 are used for realizing the test structures.

3.4.2 Device run

For the device run all steps of table 3.1 are used for realizing the demonstrator devices. This process flow does not include the metrology steps. These steps mainly consist of layer thickness measurements and cross-sectional inspections. All crucial metrology steps are included in the full process flow given in appendix B.

Table 3.1: Complete S-TASCT process flow.
The colors represent: Si Photomask SiRN Pt Ta/Pt Si_xN_y t-SiO_2 AlOx.

	**1 - Substrate selection** • Silicon <100> 100mm (4") diameter • Double-side polished • 525 µm ± 20 µm thickness • Highly Boron doped, P++
	2 - Wet oxidation of silicon • Thickness: 1.5 µm • Time: 5h • Standby temperature: 700 °C • Temperature range: 1150 °C • O2 flow: 4 slm • Ramp: 10 °C/min

3 - Lithography Trench mask

- Priming HMDS
- Coating of Olin OiR 907-17 - 4000 rpm Dynamic
- Prebake of Olin OiR 907-17 (90 s)
- Alignment & exposure of Olin OiR 907-17

  vacuum + hard contact >800mbar

  pre-exposure delay 120 s

  Constant dose: 100 mJ/cm^2
- After exposure bake of Olin OiR resists (30 s)
- Development of Olin OiR resists (2x 30s)
- Quick Dump Rinsing (QDR) and Substrate drying

---

4 - Directional RIE of SiO2

- CHF3 flow: 100 sccm
- O2 flow: 5 sccm
- Pressure: 100 mTorr
- Power: 250 W
- Chamber clean
- Stripping of resist wet or dry

---

5 - High-Aspect Ratio Bosch-based Trench etch

- Temperature: 25 °C
- He pressure: 10 Torr

Etch / Deposit

- Time (sec): 2.4 / 3
- C4F8 flow (sccm): 200 / 10
- SF6 flow (sccm): 10 / 200
- APC (mTorr): 30 / 40
- ICP (W): 1300 / 1600
- CCP – LF (W) 0 / 16

---

6 - RCA-2 Cleaning

- Pour 1000ml of DI water into the beaker
- Turn on the stirrer
- Add 200ml of Hydrogen Chloride (HCl)
- Heat up the solution to 70 °C (setpoint: 80 °C)
- Slowly add 200ml of Hydrogen Peroxide (H2O2)
- Submerge your substrates as soon as the temperature is above 70 °C
- Time: 15 min
- Quick dump rinsing % Substrate drying

---

7 - HF etch 50%

- Cleaning in 99% HNO3 2x
- Quick Dump Rinsing
- Cleaning in 69% HNO3 at 95 °C
- Quick Dump Rinsing
- Etching in 50% HF
- Quick Dump Rinsing & Substrate drying

---

8 - LPCVD of low-stress SiRN

- Pre-furnace cleaning
- Overnight drying vessel (minimum 2 days)
- Thickness: 2x 1200 nm
- Time: 2x 4.5h
- Temperature: 820 °C - 870 °C
- Pressure: 150 mTorr
- SiH2Cl2 flow: 72 sccm
- NH3 flow: 22 sccm
- N2 low: 150 sccm

---

9 - Directional RIE of SiRN

- 2x 30 min per side
- CHF3 flow: 100 sccm
- O2 flow: 12 sccm
- Pressure: 40 mTorr
- Power: 250 W
- Chamber clean

---

10 - RCA-2 Cleaning

- Pour 1000ml of DI water into the beaker
- Turn on the stirrer
- Add 200ml of Hydrogen Chloride (HCl)
- Heat up the solution to 70 °C (setpoint: 80 °C)
- Slowly add 200ml of Hydrogen Peroxide (H2O2)
- Submerge your substrates as soon as the temperature is above 70 °C
- Time: 15 min
- Quick dump rinsing % Substrate drying

---

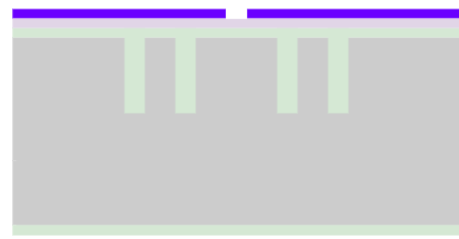
11 - LPCVD of low-stress SiRN

- Pre-furnace cleaning
- Overnight drying vessel (minimum 2 days)
- Thickness: 500 nm
- Time: 2h
- Temperature: 820 °C - 870 °C
- Pressure: 150 mTorr
- SiH2Cl2 flow: 72 sccm
- NH3 flow: 22 sccm
- N2 low: 150 sccm

---

12 - Evaporation of Al2O3

- Chamber preparation
- Glow discharge
- Base pressure: < 1e-6 mbar
- Target thickness: 100-200 nm
- Chamber cleaning



13 - Lithography slit mask

- Priming HMDS
- Coating of Olin OiR 908-35 - 5000 Dynamic
- Prebake of Olin OiR 908-35 (90 s)
- Alignment & exposure of Olin OiR 908-35

  vacuum + hard contact >800mbar

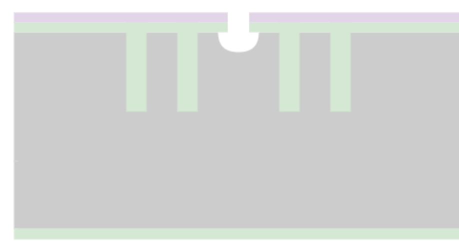
  pre-exposure delay 120 s

  Constant dose: 204 mJ/cm^2
- After exposure bake of Olin OiR 908-35 resists (30 s)
- Development of Olin OiR 908-35 resists (2x 30s)
- Quick Dump Rinsing & Substrate drying

---

14 - Etching of Al2O3

- time: 2-3 min
- BCl3 flow: 25 sccm
- HBr flow: 10 sccm
- Pressure: 3 mTorr
- ICP: 1750 W
- CCP: 20 W RF
- Table temperature: 2 °C
- He back-side: 10 Torr
- Chamber cleaning

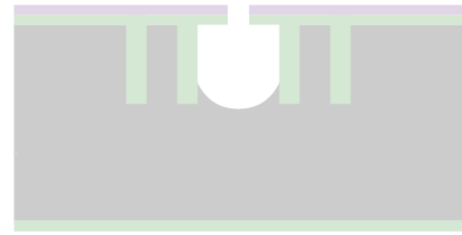


15 - Multilayer etch + iso strike

- Temperature: 25 °C
- He pressure: 10 Torr

Multi layer Etch / Iso strike

- Time (sec): 120 / 1
- C4F8 flow (sccm): 100 / -
- Ar flow (sccm): 100 / -
- SF6 flow (sccm): 0 / 800
- APC (mTorr): 100% / 15%
- ICP (W): 1500 / 4000
- CCP – LF (W): 150 / 50

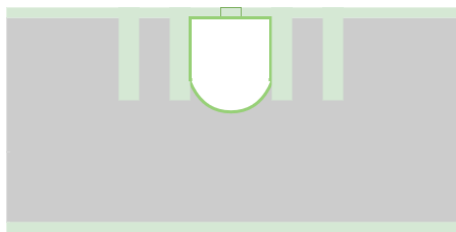


16 - Isotropic etch

- Temperature: 25 °C
- He pressure: 10 Torr
- Time (sec): 30
- C4F8 flow (sccm): -
- Ar flow (sccm): -
- SF6 flow (sccm): 800
- APC (mTorr): 90 mTorr
- ICP (W): 1500 / 4000 / 4000
- CCP – LF (W): 0
- Chamber clean
- Photoresist removal dry

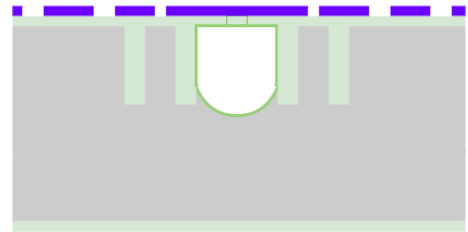
17 - RCA-2 Cleaning

- Pour 1000ml of DI water into the beaker
- Turn on the stirrer
- Add 200ml of Hydrogen Chloride (HCl)
- Heat up the solution to 70 °C (setpoint: 80 °C)
- Slowly add 200ml of Hydrogen Peroxide (H2O2)
- Submerge your substrates as soon as the temperature is above 70 °C
- Time: 15 min
- Cascade overflow rinsing & Substrate drying



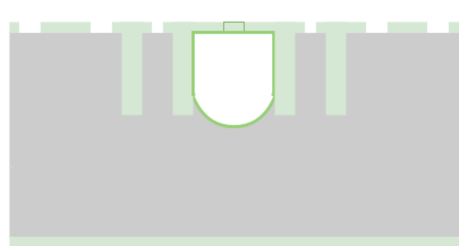
18 - LPCVD of low-stress SiRN

- Pre-furnace cleaning
- Overnight drying vessel (minimum 2 days)
- Thickness:1600 nm
- Time: 6h 15m
- Temperature: 820 °C - 870 °C
- Pressure: 150 mTorr
- SiH2Cl2 flow: 72 sccm
- NH3 flow: 22 sccm
- N2 low: 150 sccm



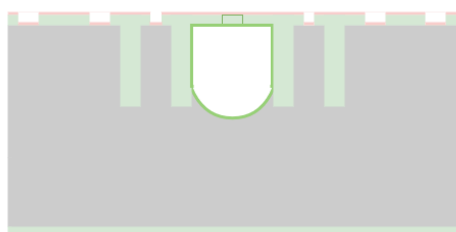
19 - Lithography front release mask

- Priming HMDS
- Coating of Olin OiR 908-35 - 5000 Dynamic
- Prebake of Olin OiR 908-35 (90 s)
- Alignment & exposure of Olin OiR 908-35
  vacuum contact >800mbar
  pre-exposure delay 120 s
  Constant dose: 204 mJ/cm^2
- After exposure bake of Olin OiR 908-35 resists (30 s)
- Development of Olin OiR 908-35 resists (2x 30s)
- Cascade overflow rinsing & Substrate drying



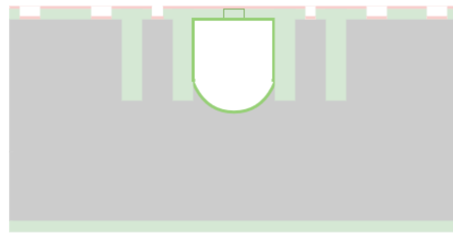
20 - Directional RIE of SiRN

- 2x 30 min per side
- CHF3 flow: 100 sccm
- O2 flow: 12 sccm
- Pressure: 40 mTorr
- Power: 250 W
- Chamber clean
- Photoresist strip wet or dry



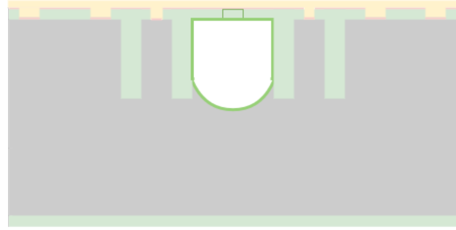
21 - Sputtering of Platinum

- Sample preparation - bake 120 °C for 5 min
- Base pressure: <1.0E-6 mbar
- Target: Pt
- Power: 200W
- pre-time: 30s
- process pressure: 6.6E-3 mbar
- target thickness: 5 nm



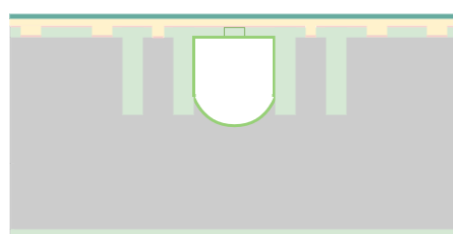
22 - Thermal anneal

- Cleaning in 99% HNO3 (2x)
- Cascade overflow rinsing & Substrate drying
- Standby temperature: 400 °C
- Time: 5h



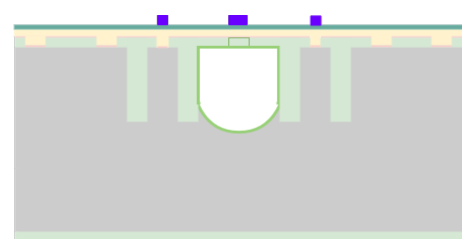
23 - Sputtering of Tantalum / Platinum

- Sample preparation - bake 120 °C for 5 min
- Base pressure: <1.0E-6 mbar
- Target: Ta / Pt
- Power: 200W / 200W
- pre-time: 1 min / 30s
- process time: 45s / 10 min
- process pressure: 6.6E-3 mbar / 6.6E-3 mbar
- target thickness: 5 nm / 200nm



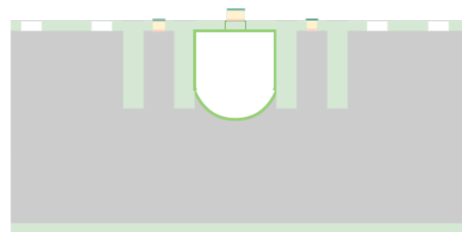
24 - PECVD of low-stress SiN

- Cleaning in 99% HNO3 (2x)
- Cascade overflow rinsing & Substrate drying
- Electrode temperature: 300°C
- Pressure: 650 mTorr
- Power: 20 W (7s LF/13s HF)
- 2% SiH4/N2 flow: 1000 sccm
- NH3 flow: 20 sccm
- Target thickness: 30 nm
- Chamber clean



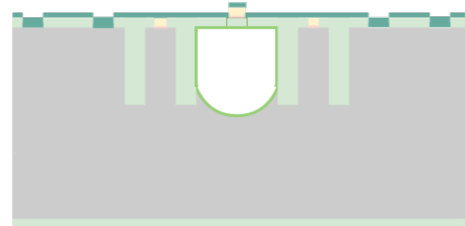
25 - Lithography metal mask

- Priming HMDS
- Coating of Olin OiR 908-35 - 5000 Dynamic
- Prebake of Olin OiR 908-35 (90 s)
- Alignment & exposure of Olin OiR 908-35
  vacuum contact >800mbar
  pre-exposure delay 120 s
  Constant dose: 204 mJ/cm^2
- After exposure bake of Olin OiR 908-35 resists (30 s)
- Development of Olin OiR 908-35 resists (2x 30s)
- Cascade overflow rinsing & Substrate drying



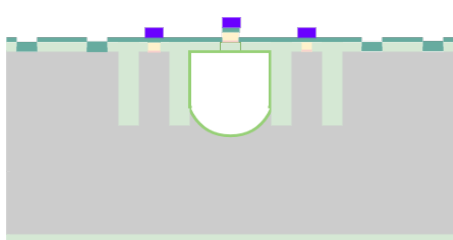
26 - Directional RIE of SiN

- T.B.D



27 - PECVD of low-stress SiN

- Cleaning in 99% HNO3 (2x)
- Cascade overflow rinsing & Substrate drying
- Electrode temperature: 300°C
- Pressure: 650 mTorr
- Power: 20 W (7s LF/13s HF)
- 2% SiH4/N2 flow: 1000 sccm
- NH3 flow: 20 sccm
- Target thickness: 70 nm
- Chamber clean



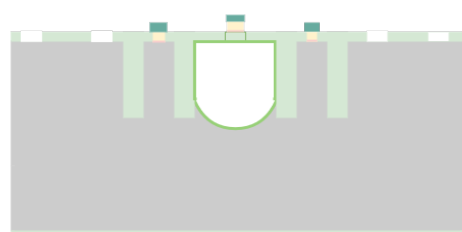
28 - Lithography capping mask

- Priming HMDS
- Coating of Olin OiR 908-35 - 5000 Dynamic
- Prebake of Olin OiR 908-35 (90 s)
- Alignment & exposure of Olin OiR 908-35

  vacuum contact >800mbar

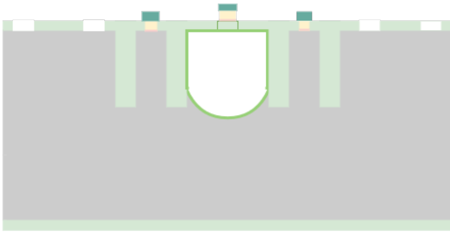
  pre-exposure delay 120 s

  Constant dose: 204 mJ/cm^2
- After exposure bake of Olin OiR 908-35 resists (30 s)
- Development of Olin OiR 908-35 resists (2x 30s)
- Cascade overflow rinsing & Substrate drying



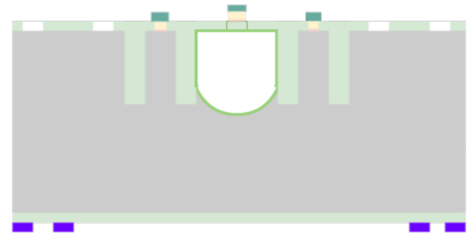
29 - Directional RIE of SiN

- T.B.D
- Photoresist strip wet or dry



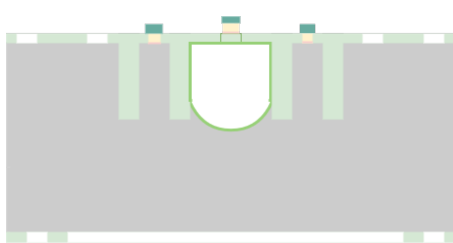
30 - Densification of PECVD SiN capping on Ta/Pt electrodes

- Cleaning in 99% HNO3 (2x)
- Cascade overflow rinsing & Substrate drying
- Thermal anneal: 250 °C
- Time: 48h



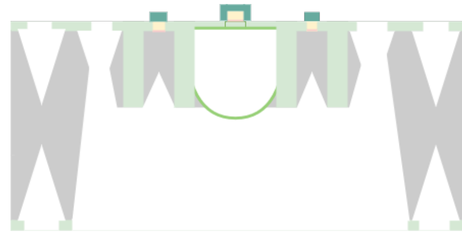
31 - Lithography back release mask

- Priming HMDS
- Coating of Olin OiR 907-17 - 4000 rpm Dynamic
- Prebake of Olin OiR 907-17 (90 s)
- Alignment & exposure of Olin OiR 907-17
  vacuum >800mbar
  pre-exposure delay 120 s
  Constant dose: 100 mJ/cm^2
- After exposure bake of Olin OiR resists (30 s)
- Development of Olin OiR resists (2x 30s)
- Cascasde overflow rinsing & Substrate drying



32 - Directional RIE of SiRN

- 2x 37 min back-side
- CHF3 flow: 100 sccm
- O2 flow: 12 sccm
- Pressure: 40 mTorr
- Power: 250 W
- Chamber clean
- Photoresist strip wet or dry



33 - KOH etch

- Etching in 1% HF
- Cascasde overflow rinsing & Substrate drying
- etching in 25wt.% KOH
- Temperature: 75°C
- Use stirrer
- Time: 8h 2min

3.5 Conclusion

The S-TASCT process was split into 4 stages and only minor changes were made to stages 1-3. Stage 4: Creating pyramid-shaped vias to the microfluidic channels, releasing microfluidic channel structures with heaters from the bulk and releasing devices from the wafer by using KOH solution was new to the TASCT platform and was therefore explained in detail. This section revealed that silicon residuals will form on the outer trench walls, residual silicon can remain underneath the microfluidic channel and SHEs will be etched. All tools and calculations to carefully design the frontside and backside release window sizes and to determine the etch time are provided in this chapter.

Also, a demonstrator device that is used for testing the viability of the S-TASCT platform is presented in this chapter. The demonstrator device is designed in such a way, that future characterization of the device can be compared very well to the demonstrator device made for the TASCT.

Two studies have been conducted using COMSOL Multiphysics. The first study showed that the main heat-loss mechanism when heating up an airflow to 600 °C, is natural convection on the outside of the microfluidic channel walls and outer trench walls. The second study about the influence of heat loss due to residual silicon on the outer sidewalls showed that if the cross-sectional area of the residual doubled, then also the power to compensate for this loss must be doubled.

The masks for realizing the test structures and devices were also provided and complemented by the complete process flow of the S-TASCT process.

4 | Fabrication

This chapter is split into two parts, a test run part and a device run part. In the first part the formation of KOH vias, the release of the device structures and the feasibility to puncture thin SiRN membranes are tested. In the second part, actual devices will be made and the results of important processing steps will be described in detail. All masks used for processing are printed on 5" in soda-lime glass photo-mask plates of 0.09" in thickness by Delta Mask bv, using a Heidelberg DWL-200 laser system. Before masks are used optical inspections are performed to guarantee proper resolution and quality. Etch rates for each etch process are determined via 24-points measurement, using a Woollam M-2000UI ellipsometer on a dummy wafer before and after the etching step. High-resolution scanning electron microscopy (SEM) pictures shown in this chapter were acquired with a JEOL JSM 7610FPlus.

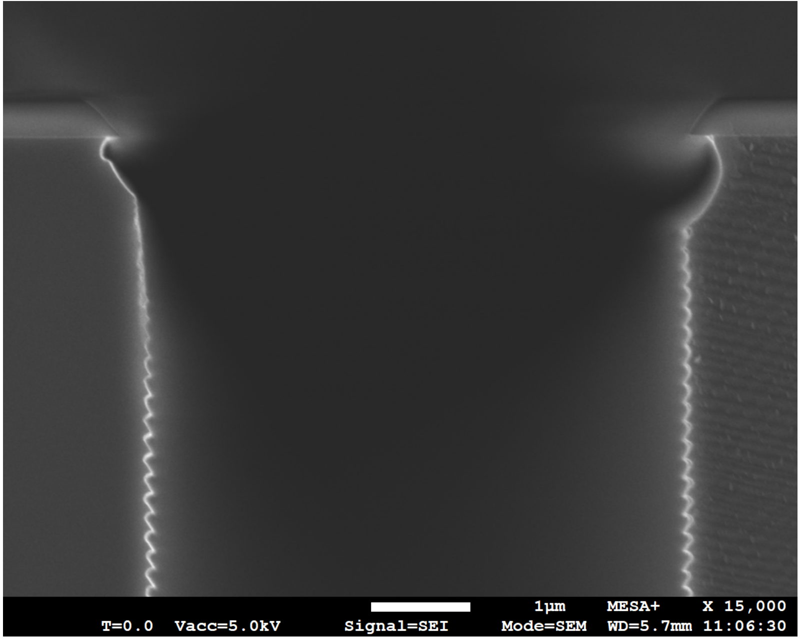
4.1 Test Run

The main goal of the test run is to create the test structures as designed in chapter 3. Another important aspect of the test run is to check whether the HAR etch recipe, as used in the TASCT process still reproduces sufficient results. This will be discussed in subsection 4.1.1. The other subsections will be used to show the results for filling the trenches, the creation of the test structures and the puncturing of thin SiRN membranes. The silicon wafers used for the test run had a 525 µm ± 20 µm thickness and a 4" diameter. The wafers are ⟨100⟩ orientated and double-side polished from Si-Mat Silicon Materials.

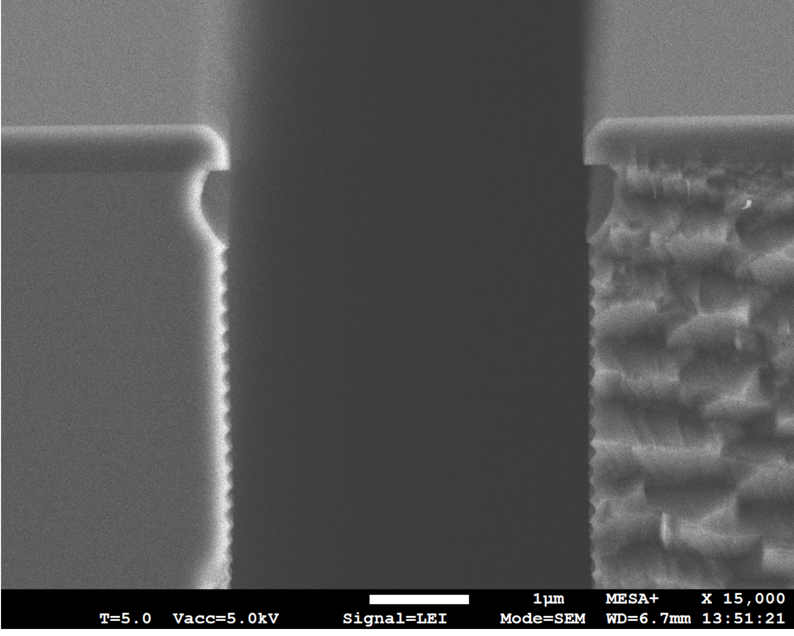
4.1.1 Silicon dioxide hardmask & high aspect ratio silicon trench etch

It may seem evident that silicon dioxide is an excellent choice of hardmask, as SiO_2 offers a great selectivity with respect to silicon, in directional plasma etching processes. However, the method chosen to grow SiO_2, e.g. via thermal oxidation, wet oxidation or formation of SiO_2 from the precursor tetraethyl orthosilicate (TEOS), each will result in hardmask layers with different etching characteristics. Both a thermal oxide (t-SiO_2) oxide hardmasks of 1.5 µm and a TEOS oxide hardmasks of 1.1 µm were used to create openings of around 3 µm ± 0.8 µm in the hard mask. The total cycles needed to reach a sufficient depth of 75 µm using the Bosch-based DRIE etch process were determined next. In figure 4.1, the trenches are shown which have been created. After 250 etch cycles, the trenches created using TEOS in **(a)** show a width of 5.7 um. The total depth after this etch time was 45 um. Also, 644 nm SiO_2 oxide was consumed during the etch which resulted in an etch rate of 2.57 nm/cycle. Because the edges of the mask openings are also etched the trenches became too wide to be fully refilled with SiRN in the subsequent step. The trenches created using a t-SiO_2 hardmask, after 500 cycles, are shown in **(b)**. The width measured 3.6 µm in combination with a depth of 75 µm,

as shown in figure 4.2. The total etched layer thickness was around $973 \pm 10\%$ nm, which results in an etch rate of 2.0 nm/cycle. These results are sufficient for usage in the device run. However, the trench also shows tapering throughout the trench as shown in figure 4.2, which can cause a void after refilling the trench. The size of this void is equal to the maximum trench width minus the minimum trench width. These voids are not expected to have a significant effect on the micro fabrication process, as the volume of these voids is much smaller then the total silicon volume surrounding the trenches.



(a) Trench opening using TEOS oxide hardmask. A sharp angle on the edge of the mask indicates consumption of SiO_2 during the etch.



(b) Trench opening using thermal oxide hardmask. The round angles on the edge of the mask indicates a better resistance during the etch.

Figure 4.1: Using TEOS oxide in **(a)**, after 250 cycles the trench width increased to 5.7 um. Note the sharp angle at the tip of the hardmask, which indicates a much higher consumption of SiO_2 during the HAR etch. Using t-SiO_2 in **(b)**, after 500 cycles the trench width remains around 3.6 µm. The tip of the hardmask is slightly rounded at the top.

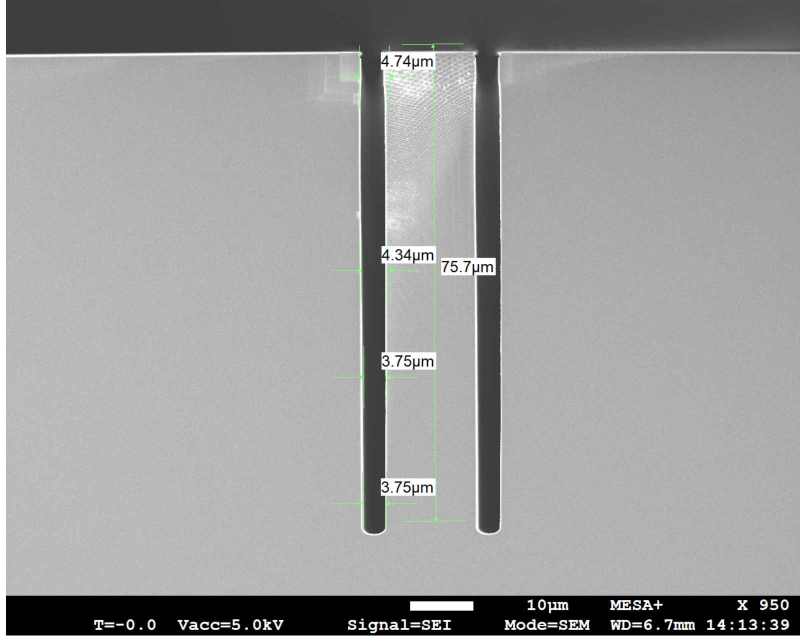


Figure 4.2: Resulting trench after 500 cycles of the HAR Bosch-based DRIE etch recipe, using a t-SiO_2 hardmask. The different widths along the channel indicate tapering of the channel. *The included measurements are indicative and the trench depth measurement is slightly misaligned.

4.1.2 Filling of trenches with silicon-rich nitride

Now, that the trenches are created they should be filled with LPCVD SiRN. The LPCVD process uses dichlorosilane gas in combinations with other gasses to uniformly grow SiRN from every surface the gas touches. The growth in the trench will thus be from the left, right, top and bottom sides of the trenches and also on top and bottom of the wafers. This means that e.g. trenches of 3 µm in width require a total SiRN layer growth of 1.5 µm. As shown in chapter 3, this way of filling the trenches will result in V-grooves to form. The V-grooves are dependent on the width of the channel and partially on the geometry around the top of the trench. For V-grooves with a height larger then 500 nm a photoresist with higher viscosity is required, in order to create smooth photoresist layers. Photoresist with too low viscosity will be expected to be thrown out of these V-grooves, during the photoresist spinning, which may lead to damaged photoresist surfaces. The LPCVD process is also limited to a maximum growth of 1.6 µm, which in our case leads to an effective growth of 3.2 µm inside the channel. This is not enough as had been observed that several trenches are wider than this specification. Therefore, two runs of 1.2 µm SiRN are grown, which leads to an effective growth of 4.8 µm, this must be amply sufficient for enclosing the trenches. The trench after the first deposition of 1.2 µm SiRN is shown in figure 4.3a. Here it can be observed that throughout the trench more SiRN is still required, then at the top of the channel to fill the trench. A zoom-in in of the top in figure 4.4a reveals that only around 1.2 µm is needed to fill this bottleneck. After growing another layer of 1.2 µm SiRN, the bottleneck has filled as shown in figure 4.4b. The voids formed in the underlying trench (figure 4.3b), varied from 400 nm to 1 µm in width. The V-grooves, as shown in figure 4.4a, varied from 400 nm to 1 µm in height, over multiple wafers. The excess 2.4 µm was removed on both sides of the wafer and the v-grooves were inspected again. The V-grooves were inspected both with a Bruker WLI Contour GT-I White light interferometry tool and SEM. The resulting V-grooves only measured heights around 400 nm at this time.

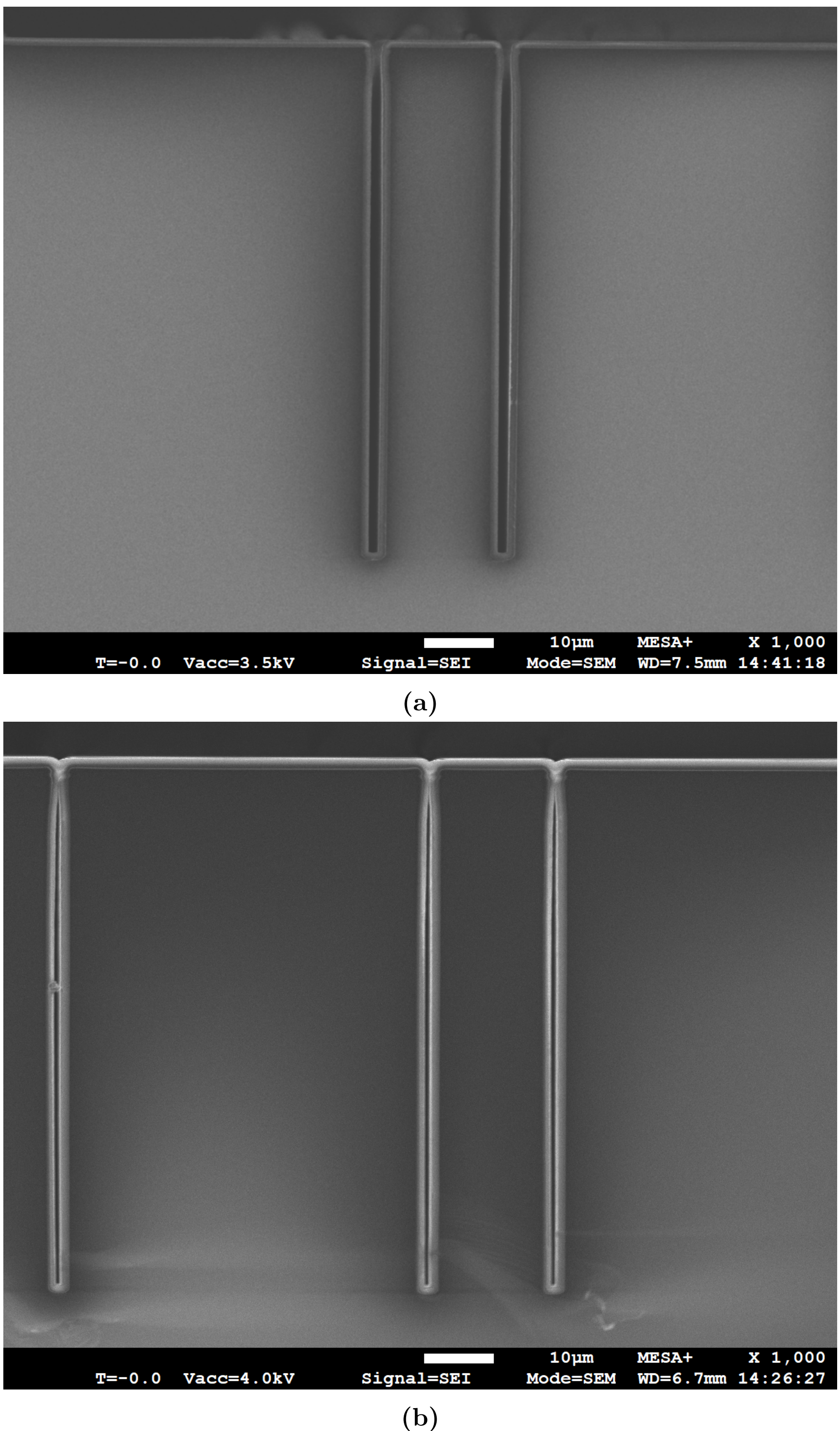


Figure 4.3: Trench filled with (a) 1.2 µm SiRN and (b) 2.4 µm SiRN. After the SiRN growth stopped due to the bottleneck in the top of the trench, a keyhole will be formed underneath.

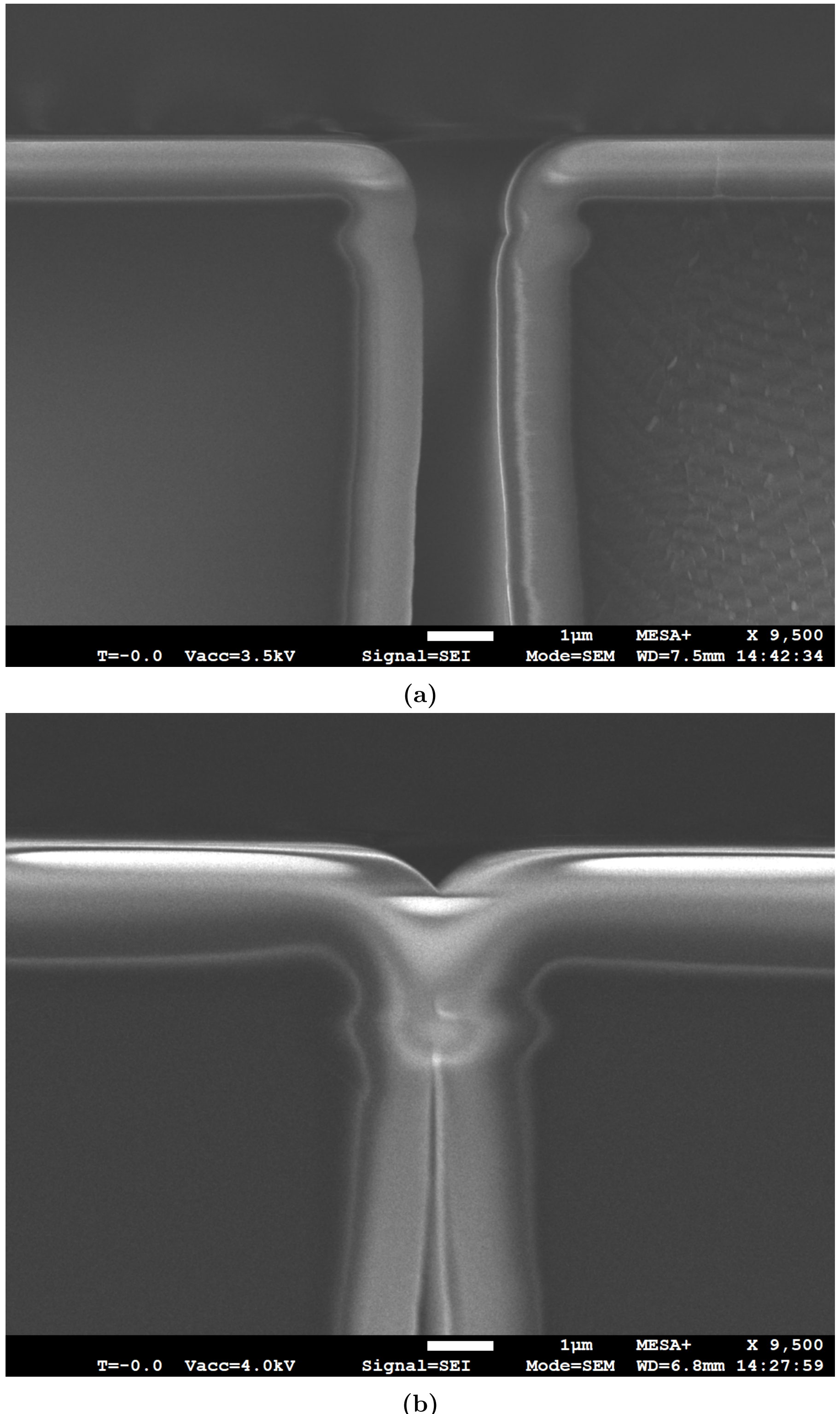


Figure 4.4: The zoom-in on topside trench filled with (a) 1.2 µm SiRN and 2.4 µm SiRN (b). The V-groove measureed in (b) is around 400 nm.

4.1.3 Potassium hydroxide etch

To avoid any contaminants present in the KOH solution, which can alter the typical etch rates, a new batch of KOH solution was made using the standard recipe of 25wt.% KOH at 75 °C. Since most test run wafers have no front release masks applied, the wafers needed more time in the KOH solution in order to fully etch through the wafer. The total etch time for wafer through etching was 8 hours and 45 minutes.

After the KOH etch cross-sections were prepared, revealing a pyramid-shaped via, in figure 4.5. The number 1 denotes the top of the pyramid, which was located at half the trench depth and the window size was around 65 µm at the bottom of the trench. Both values were as designed and this pyramid-shaped via can be used in the device run as an inlet or outlet.

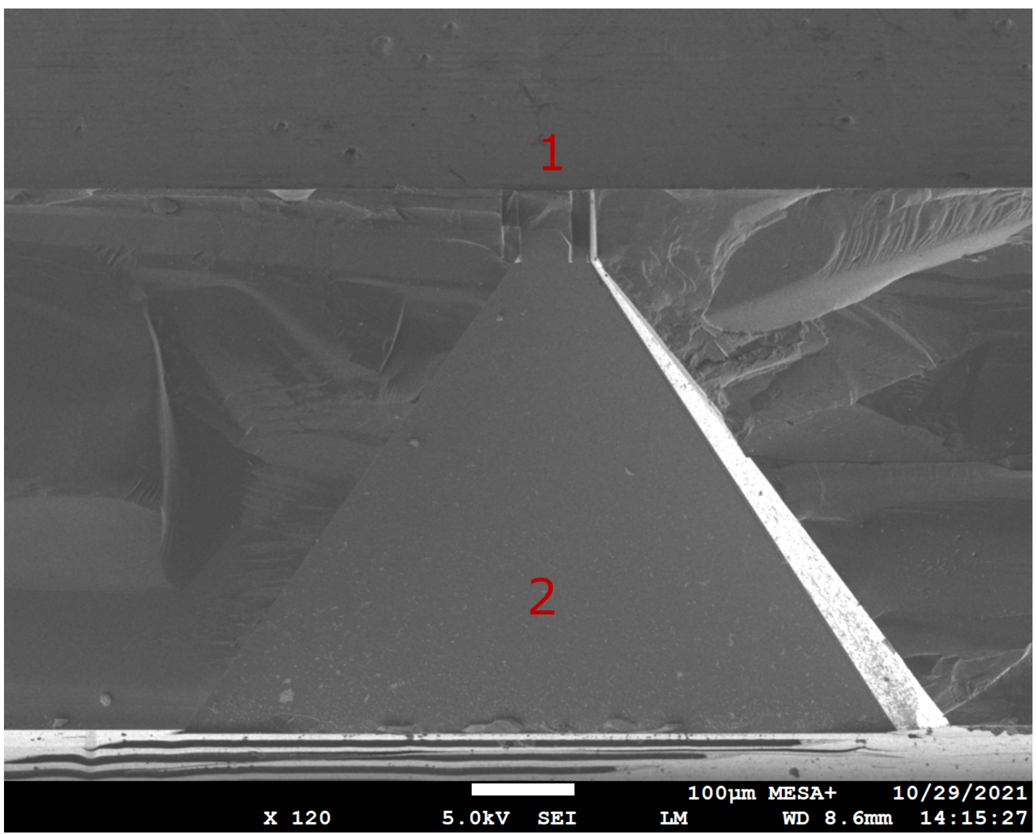


Figure 4.5: Cross-sectional SEM of a pyramid-shaped via. 1 indicates the trench outlines and 2 indicates the removed silicon, forming the pyramid-shaped via.

The fully released test structure from the bulk silicon can be seen in figure 4.6. At location 1, the bulk silicon is shown. At location 2, the removed bulk silicon can be seen. Locations indicated by 3-4-5 make up the device island. The first 3 and 4 seem a little it located behind the other parts of the island, as the left side broke off from the island. At location 3, the residual silicon on the outer trench walls is shown. This residual will become much smaller in the device run due to front mask openings. At location 4, the heaters are shown with a triangular cut on the bottom as expected. This shows that it is possible to fully release the devices from the bulk, while sufficient silicon will remain between the trench walls. At location 5, the microfluidic channel will be formed in the device run.

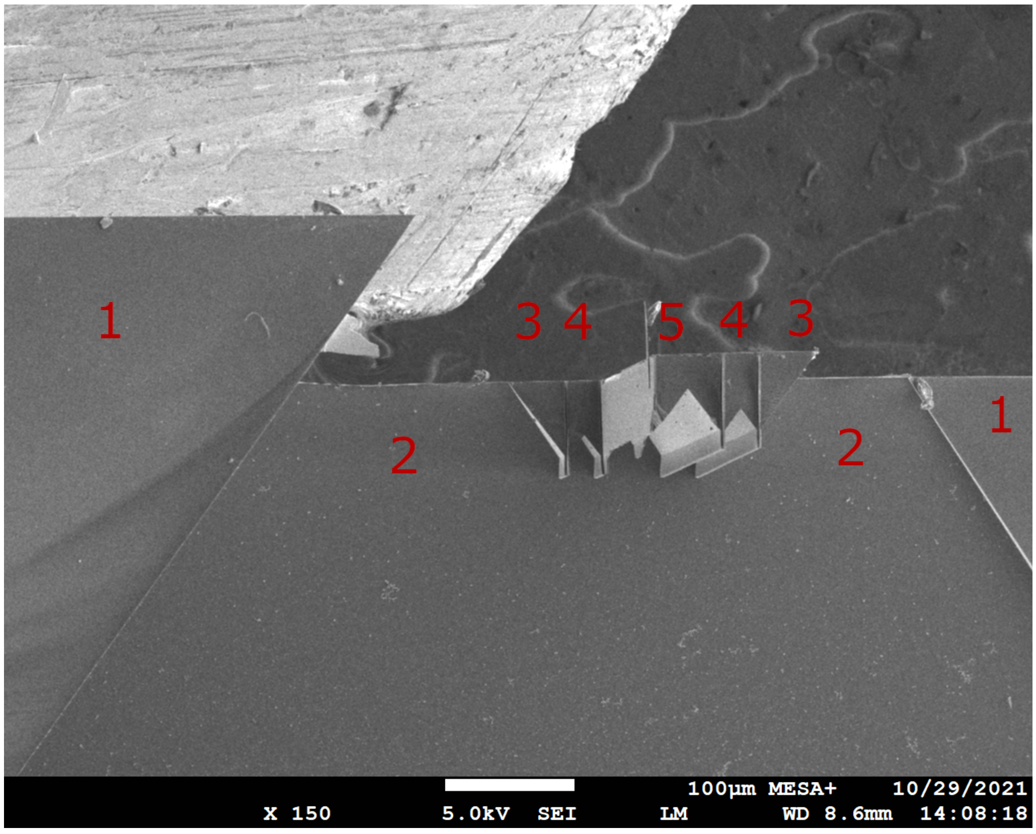


Figure 4.6: Cross-sectional SEM of the released test structure. 1 shows the bulk silicon, 2 shows the removed silicon outlines, 3 shows the residual silicon on the outer walls of the trenches, 4 shows the heater elements and 5 shows the future position of the microfluidic channel. The numbers 3-4-5 make up the total device. The left heater and residual appear behind the other structures, because the left part of device broke off.

4.1.4 Puncturing silicon nitride membranes

On two wafers, a front masker containing an array of 10 µm wide slits centered in the middle of the wafer, was patterned onto the front side of the wafer to create free-hanging membranes directly above the microfluidic channels, as was shown in figure 3.15. An attempt was made at puncturing these membranes by using a Seirin J-Type 0,20 mm x 30 mm dry needle. The needle can easily be inserted into the pyramid-shaped via, as shown in figure 4.5. A very small resistance in the needle was noticed before the membrane was punctured. When more pressure was applied the needle tip would resurface even further. Because these needles have a diameter of 200 µm it is expected that the trenches were damaged during the process. However, the membranes in the device run are buried 50 µm underneath the channel. Therefore, it is expected that this membrane can be punctured easily without damaging the trenches. It is advised that the puncturing of membranes must happen from the backside of the wafer while the wafer maintains an upright position, to avoid SiRN membrane parts to eject into the microfluidic channel. This method can be complemented by using a gas suction device (e.g. vacuum cleaner), forcing any debris out of the microfluidic channel inlet/outlet.

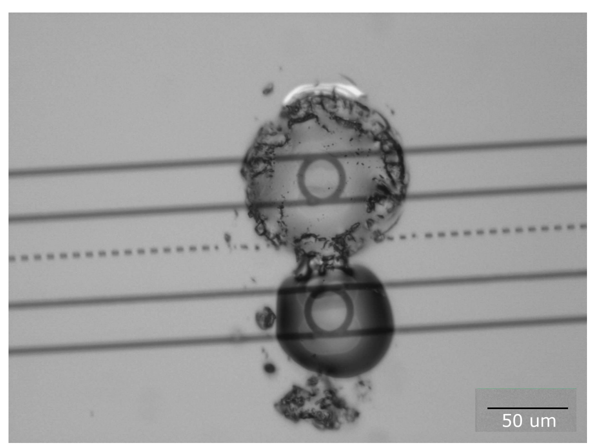
4.2 Device Run

For the device run, highly boron-doped (P++/B) ⟨100⟩ double-side polished silicon wafers from Si-Mat Silicon Materials were used. The following subsections will be used to describe the results from the device run. Stage 1 was already well discussed in the previous section, and the same 1.5 µm t-SiO_2 hard mask in combination with the HAR silicon trench etched was performed. Stage 3, crafting access to the electrodes and implementing electronics for sensing are not performed. Nonetheless, no crucial problems were expected here, as no alternations to the original TASCT had been made. The alignment marker set developed for this device run is shown in appendix A.2.

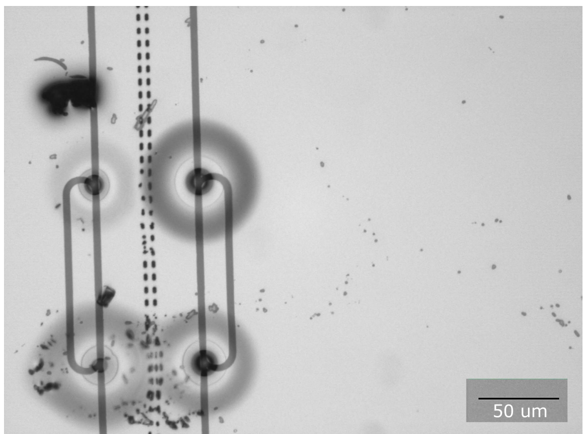
4.2.1 Fabricating microfluidic channels through a slit masker

After the fresh layer of 500 nm SiRN was deposited, olin OiR 908-35 was deposited on the wafer and spun at 4000 rpm. After developing, the wafers were inspected. This inspection revealed many circular spots to be present all over the wafer. It soon became clear that these circular spots recurred on the same spots each time. By zooming in on these spots as shown in figure 4.2.1(a), (b) and (c), it can be seen that the slits are not well defined. Also, one device used a tapered structure to combine the trenches, as shown in figure 4.2.1(d). Wherever this special trench geometry was used, no circular spots could be observed. The circular spots indicate a non-smooth photoresist layer. The transfer of the slits at these places was not good and resulted in defective or non-existing slits.

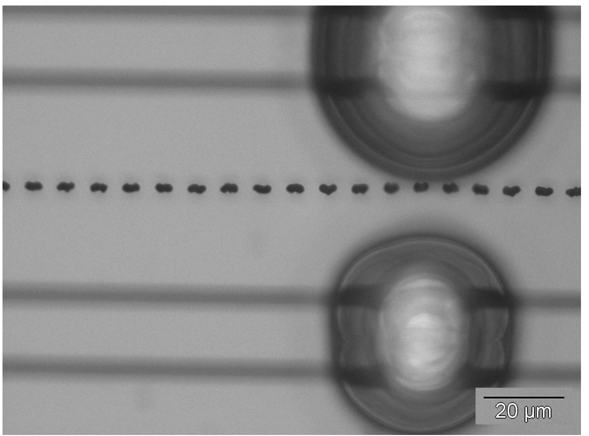
In order to still make use of the produced masks, the photoresist deposition was tried to be optimized. Stacking a layer of olin OiR 907-17 with olin OiR 907-12 at 3000-4000-5000 rpm did not improve the situation. Neither did spinning of olin OiR 908-35 at 3000 rpm or 3000 rpm with dynamic mode (dynamic starts at 400 rpm and increases to the set rpm). The best results were achieved by using olin OiR 908-35 at 5000 rpm with dynamic mode, as shown in figure 4.8. The number of devices with a proper slit pattern transfer was enough to continue with the process. It was noticed throughout the photoresist test that the tapered T-shaped locations still did not show any circular spots.



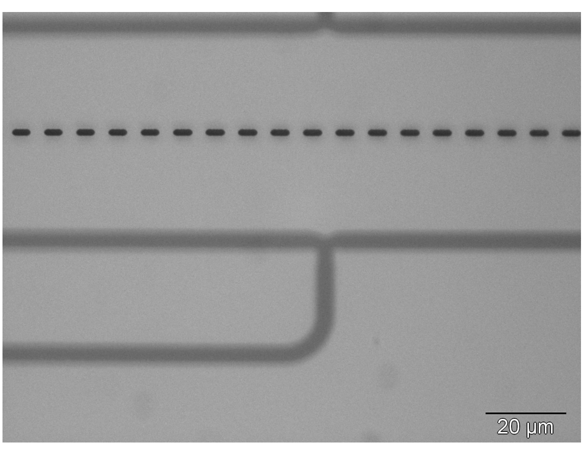
(a) Spots at circle shaped trench junction



(b) Spots at half-y junctions

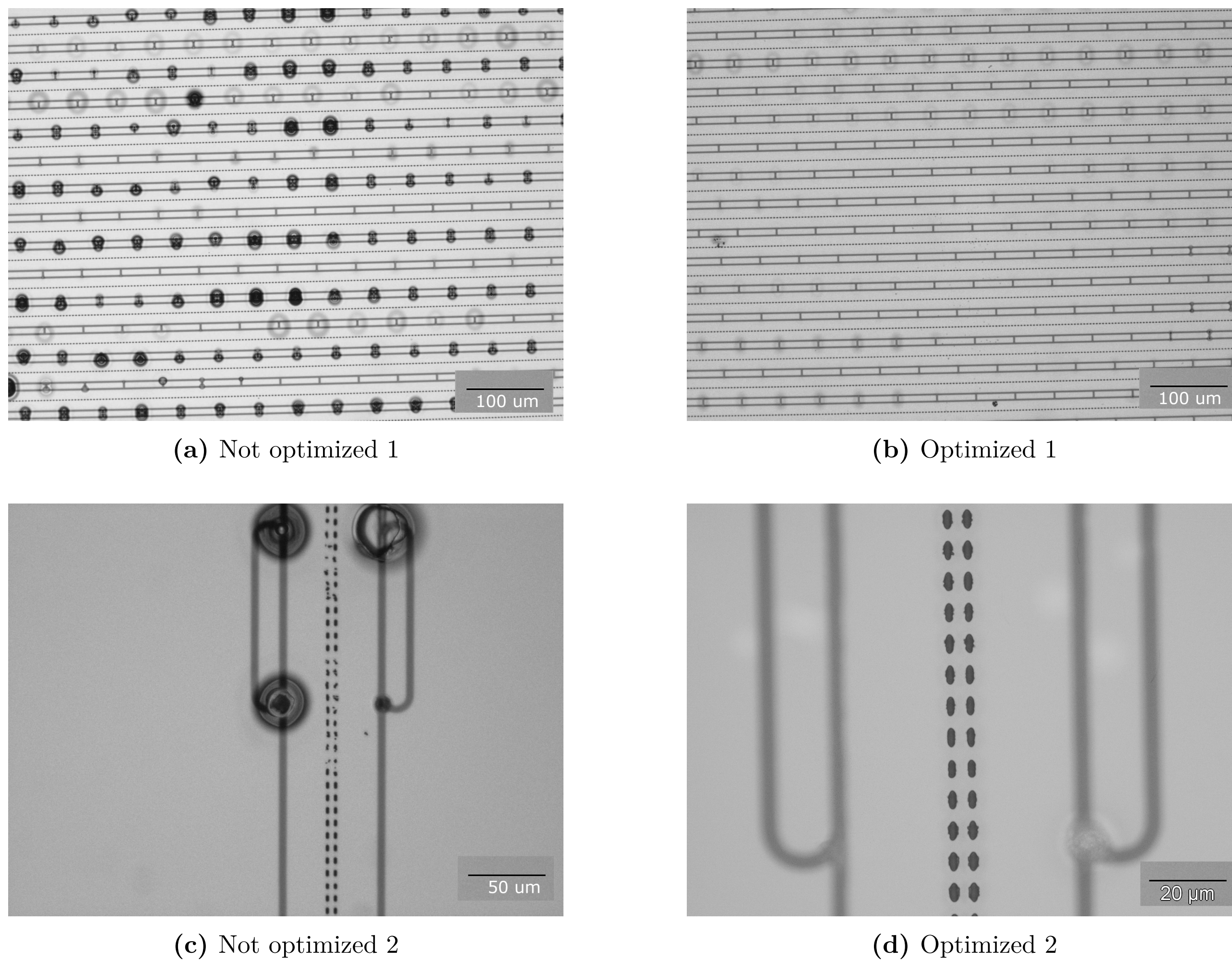


(c) Spots at T-shaped junctions



(d) No Spots at tapered T-shaped junctions

Figure 4.7: In (a), (b) and (c), circular spots can be noticed which will result in a low-quality slit transfer. In (d), a special tapered T-shape is used. No spots can be noticed here and also the quality of the slit transfer is much higher.



(a) Not optimized 1

(b) Optimized 1

(c) Not optimized 2

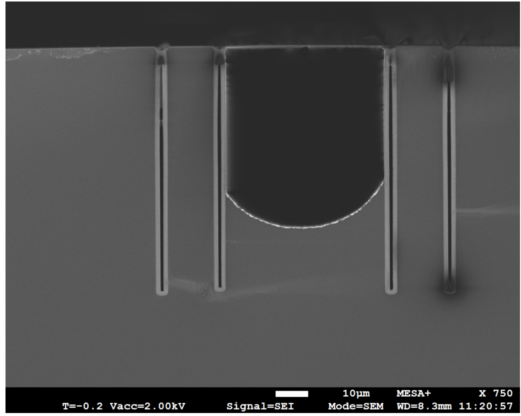
(d) Optimized 2

Figure 4.8: In (a), the photoresist deposition was not optimized. In (b) with an optimized recipe the circular spots are noticeably less and the slit transfer quality improved. In (c) the circular spots are also minimized but the slit quality is still not sufficient. In (d), at another complicated trench geometry, the spots also . No spots can be noticed here and also a good slit transfer.

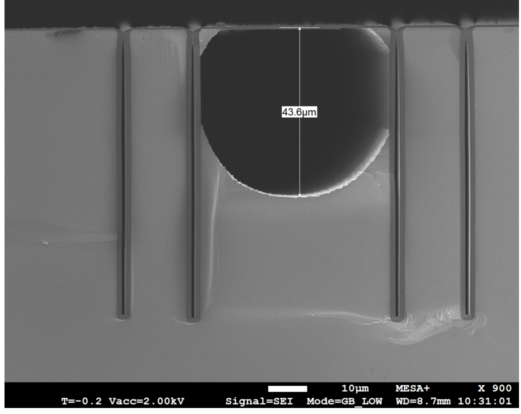
Table 4.1: Settings used on the SPTS Pegasus for etching the microfluidic channels.

- ICP power: 3000 W
- SF6 flow: 600 sccm
- Process pressure: 90 mTorr,
  with a 2 s 30 mTorr strike-up
- Temperature: −19 °C
- He BSC: 20 Torr
- Full auto matching
- Time: 40 min

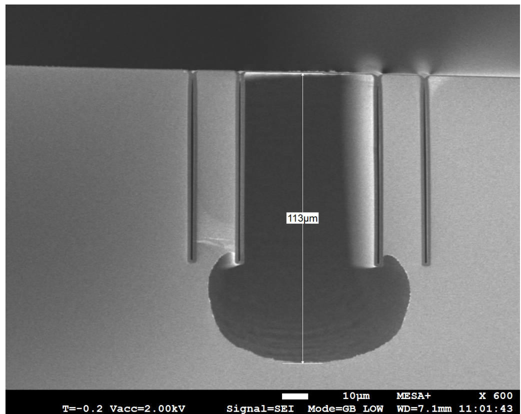
A SPTS Pegasus deep reactive ion etching system plasma was used for etching the microfluidic channels because the original etcher planned for this process was not available. The microfluidic channels were etched through the slits by using the settings given in table 4.1. After 40 minutes the microfluidic channels reached a depth of around 56 µm through the high-quality slits. The microfluidic channels etched through multiple slits on top reached a depth of 113 µm. The microfluidic channels etched through low-quality slits reached a depth between 0 to 50 µm. It was also observed that the microfluidic channels etched through 2 rows of slits reached the end of trenches at a depth of 75 µm for an etch time of 40 minutes. Another device which multiple microfluidic channels in parallel showed a large deviation in the microfluidic channel depth. Illustrations of the results described above can be found in figure 4.9.



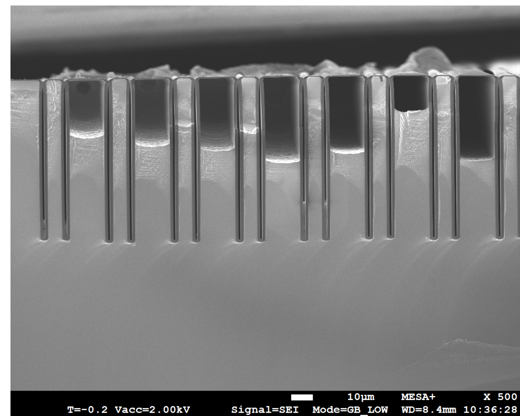
(a) 56 µm deep microfluidic channels and vertical sidewalls.



(b) 43 µm deep microfluidic channels and round sidewalls



(c) 113 µm deep microfluidic channel used for inlets and outlets.



(d) A large deviation in the microfluidic channel depth.

Figure 4.9: Microfluidic channels formed after etching 40 minutes. In (a), a high-quality slit transfer results in the desired depth. In (b), a low-quality slit transfer results in much smaller microfluidic channels. In (c), using multiple rows of slits results in much deeper microfluidic channels. In (d), all the parallel channels reached a different depth, showing the influence of the quality of the slit transfer.

4.2.2 Potassium hydroxide release step

First, a new batch of KOH solution was made using the standard recipe of 25wt.% KOH at 75 °C. After a 1% HF dip, the wafers were put into the KOH solution. The wafers were removed from the KOH solutions at three different times. The first time of removal was after 6 hours and 16 minutes. At this time, the pyramids formed through the large front release windows, were already past the trenches as shown in figure 4.11. The pyramids through the small front release windows are already closed into the Si (111) planes, as shown in figure 4.10. Both these result correspond very well with the design.

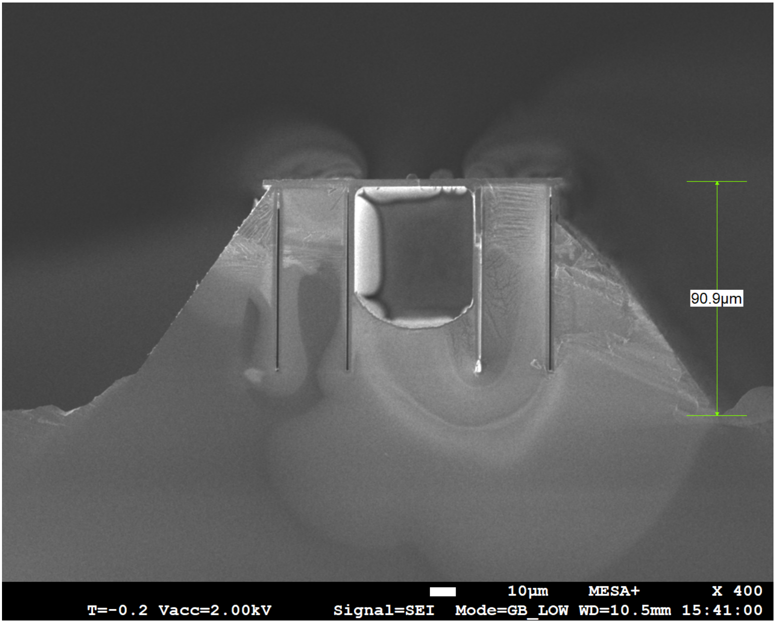


Figure 4.10: KOH etch 6 hours and 16 minute. By using large 250 µm front release windows the inverted pyramid moved past the end of the trenches.

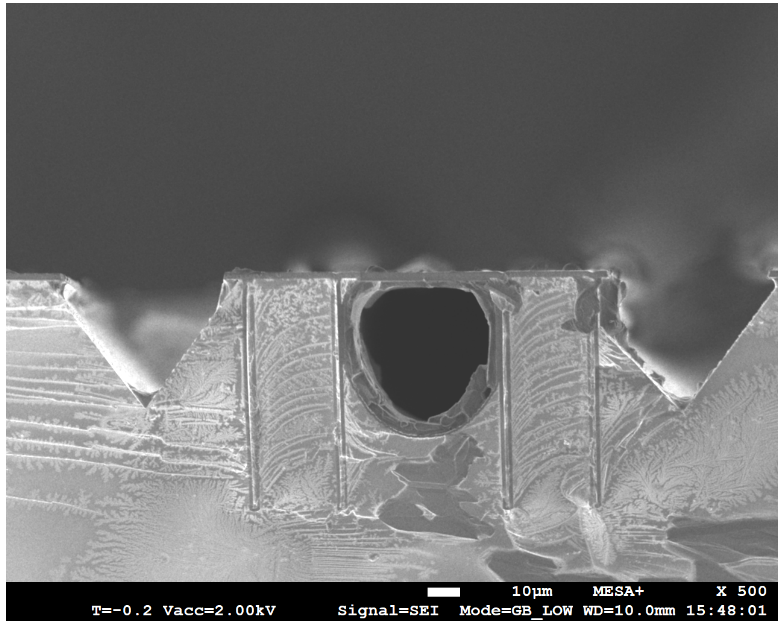


Figure 4.11: KOH etch 6 hours and 16 minutes. By using small 50 µm front release windows the inverted pyramid already stops before the end of the trenches.

The second time of removal was after 7 hours and 28 minutes. At this time, the pyramids formed through the large front release windows would meet the pyramid from the bottom of the trench, hence releasing the devices, as shown in figure 4.11. However, still much silicon is visible underneath the trench. As long as this silicon is present the SHEs are not isolated from bulk silicon. The pyramids through the small front release windows are still closed into the Si (111) plane and the backside pyramid has reached the trench. These devices are therefore not released yet, as shown in figure 4.10. Both these result also corresponded with the design. However, it was also noticed that many of the devices with large front release windows already started to etch the SHEs.

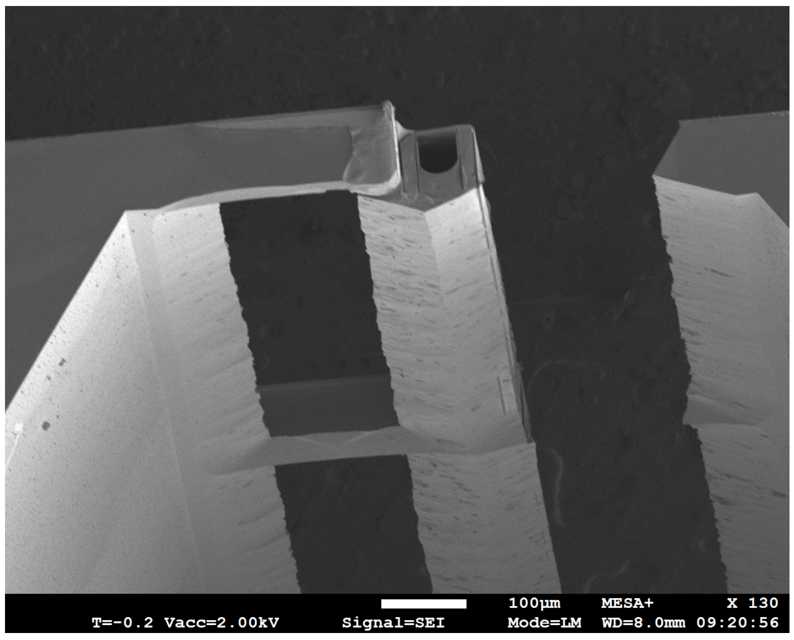


Figure 4.12: KOH etch 7 hours and 28 minutes. By using large 250 µm front release windows the devices are released from the bulk silicon, but silicon residue is still visible under the trench.

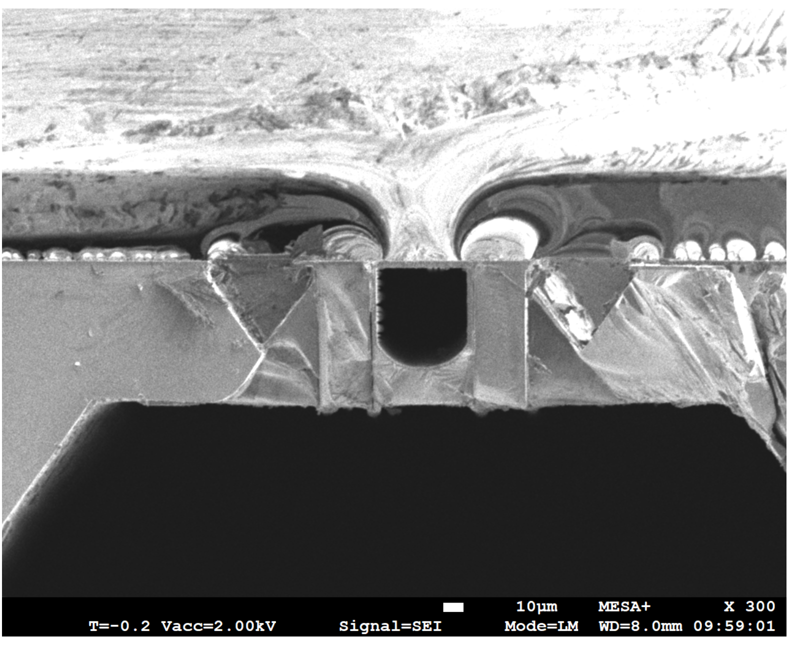


Figure 4.13: KOH etch 7 hours and 28 minutes. By using small 50 µm front release windows the inverted pyramids did not meet the backside pyramid.

The third time of removal was after 8 hours and 2 minutes. At this time, the backside pyramid would reach half the trench depth, minimizing the side wall silicon residual and releasing devices, both with small front release windows and large release windows. However, at this time only the devices with large front release windows were released as shown in figure 4.14. At this time also the SHEs have been fully isolated from any bulk silicon. On the other hand, the devices with small release windows were still not released in all cases. After extending the etch time with another 35 minutes, the devices were observed again and figure 4.15 showed that the devices are released this time. Also, these SHEs have been fully isolated from the bulk silicon. The bulk silicon is also very close to the device island.

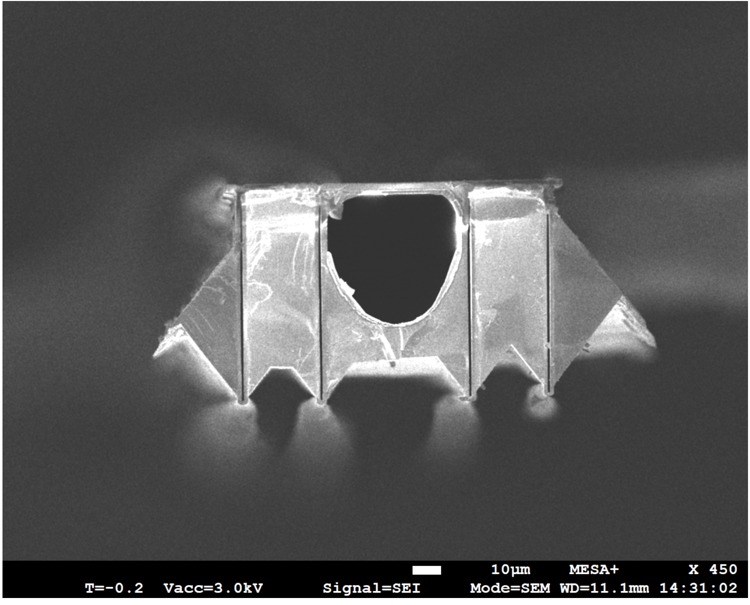


Figure 4.14: KOH etch 8 hours and 2 minutes. By using large 250 µm front release windows the devices are released from the bulk silicon and the silicon residues on the sidewall and under the microfluidic channel have been etched.

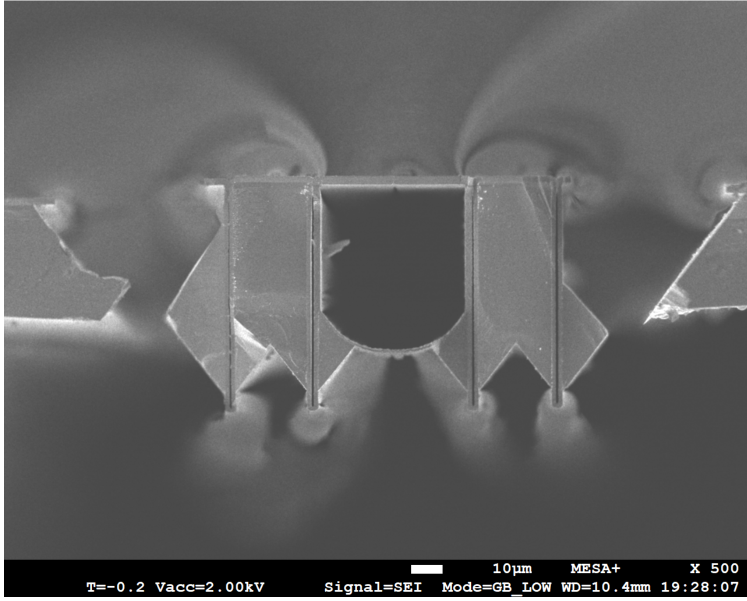


Figure 4.15: KOH etch 8 hours and 35 minutes. By using small 50 µm front release windows the inverted pyramid did not meet the backside pyramid.

4.3 Conclusion

This fabrication chapter was split into two sections, a test run part and a device run part. The test run part showed that it was possible to create SHEs, release the microfluidic channel with SHEs from the bulk silicon and create pyramid-shaped vias to the microfluidic channels. It also showed that t-SiO_2 is the prefered choice as hardmask for the HAR Bosch-based DRIE. This test run also confirmed the presence of V-grooves on top of the wafer and keyholes in the trenches.

The fabrication was extended in the device run and now included stage 1,2 and 4 of the S-TASCT process. Stage 1 was repeated as before. Stage 2, showed a problem with circular spots on the photomask. These circular spots are imperfections on the photomask and recurred at the same spots on each wafer. By analysing the problem it was shown that complicated trench junctions are the cause of these circular spots. It was also observed that tapered T-junctions did not have these circular spots.

This resulted in a low quality slit transfer and caused a huge spread in the microfluidic channel etch depth. This depth was very dependent on the slit quality. Multiple rows of slits were used to create deeper channels, behaviour was as designed.

By removing the wafers from the KOH at different times, the influence of the front mask window size could be monitored. The devices with small release windows of 50 µm were barely released after the calculated etch time. Also, the distance between the device island and the bulk silicon was very small. The devices with large release windows of 250 µm behaved as designed. After the desired etch time of 8 hours and 2 minutes these devices were fully released from the bulk silicon. The residual silicon on the outer walls of the trenches were minimized and the SHEs were fully isolated from the bulk silicon.

5 | Measurements

Two characterization test will be described in this chapter. First an electrical charactization will be done to test whether the S-TASCT technology resulted in silicon electrodes as designed in chapter 3. In the second characterization the demonstrator devices will be put up to the test. In the sections below the setup will be shown for each test and the protocols needed for executing the tests.

5.1 Electrical heater characterisation

In the following sections the schematic and protocol for the electrical characterisation tests is shown.

5.1.1 Setup & protocol

An attempt can be made at measuring the resistance of the heaters via the 20×20 µm contact pads. It can be tried to insert the probes through contact pad holes as shown in figure 5.1. Alternatively, the contact pads can be manually filled first with a conductive compound. After an electrical connection is made to the heaters, the voltage need to be stepped up from 1 to 5 V with steps of 1 V. The corresponding current for each voltage step needs be measured by an amperometer, and should be noted. The resistance can be determined by using Ohm's law (Eq. 2.23).

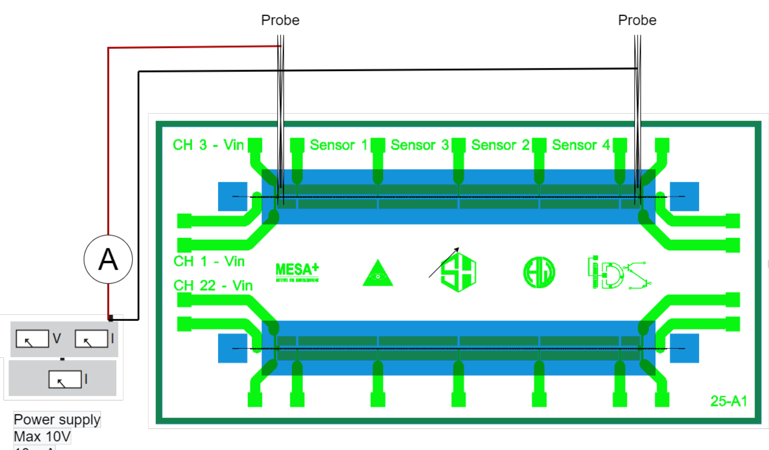


Figure 5.1: Electrical characterization setup. It can be tried to insert two probes in the 20×20 µm contact pads. The probes are connected to a power supply. An amperometer is used to measure the current, for each voltage step.

5.2 Demonstrator device characterisation

In the following sections are the schematic and protocol for the demonstrator device characterisation tests shown. The produced demonstrator devices are compatible with a universal modular fluidic and electronic interfacing platform for microfluidic devices [49]. The demonstrator devices can be glued in the center of these PCBs using a two component epoxy.

5.2.1 Setup & protocol

As explained before, for every platinum sensor a TCR measurement is required. Therefore, the produced devices containing 4 platinum sensing elements, shown by the green wires in figure 5.2, must be placed inside the Heraeus oven with customized temperature controller. The temperature is then increased from 65 °C to 85 °C with steps of 5 °C. By using Eq. 2.27, the temperature of the oven and the resistance, which is measured by a four-point probe method within the multiplexer Agilent 34970A data acquisition / data logger switch unit. A linear fit can be applied on all the measured data points. The slope of this linear fit can be used to determine the TCR of the sensor.

Once the TCRs of each sensor is known, the platinum sensors can be used to measure the ability of the silicon heaters to heat up an airflow inside the channel. An air flow of 240.415 mg/h can be supplied to the microfluidic channel via a EL-FLOW Select F-201CV MFC and different potentials, starting at 10 V, can be applied to the heaters. The four sensors can readily convert the measured potential to a temperature using available LabVIEW software. It can also be chosen to pump out the ambient air using a HiCube80 turbo molecular pump, by Pfeiffer-vacuum. The maximum applied voltage on the heaters cannot exceed 100 V.

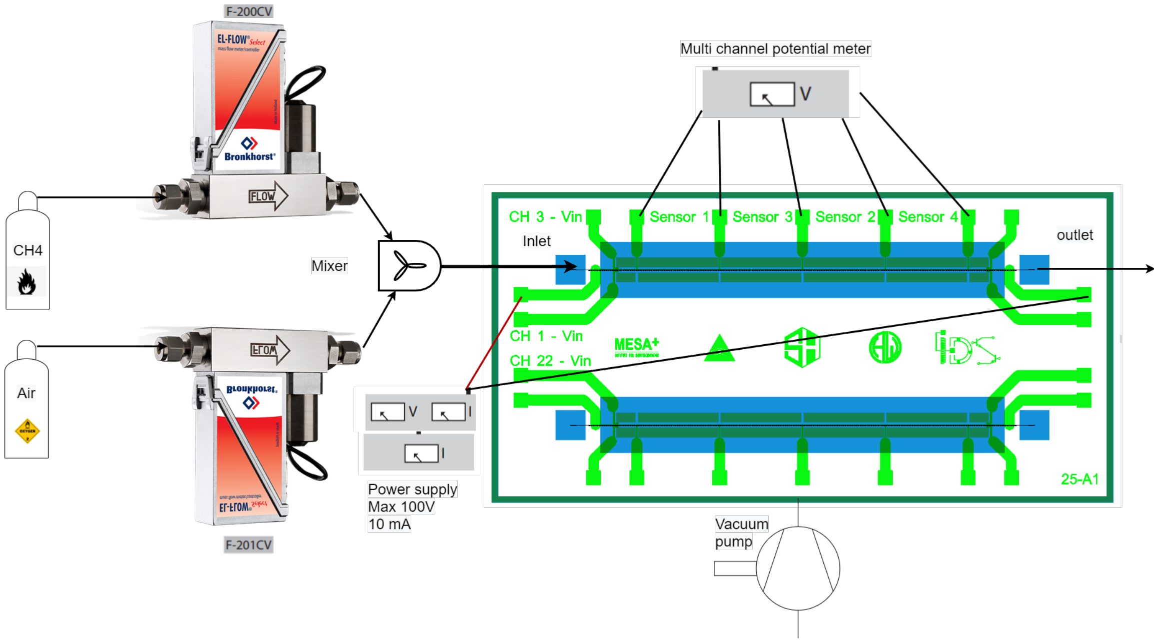


Figure 5.2: Demonstrator device characterisation setup. A single or mixed gas can be supplied to the inlet of the device by using MFCs. The gas in the microfluidic channel can be heated by applying power to the SHEs. The temperature on different locations on top of the channel can be measured by using thin-film platinum sensors. The gas flows out of the chip via an outlet. The device can be placed inside a vacuum setup, to clear out all ambient air around the microfluidic channels.

6 | Discussion

Theory, design and practice meet in this chapter. The strengths and limitations of the new simplified Trench-Assisted Surface Channel Technology will be highlighted here and unexpected findings are also discussed in this chapter.

6.1 The S-TASCT process

From chapters 2 & 3, it already became clear that some complications, such as the V-grooves on top of the wafer cannot be avoided in the new S-TASCT process. Besides that, S-TASCT also introduced a few new complications, such as undercutting of the -hardmask and -silicon heaters and the formation of residual silicon on the outer walls of the trenches. Also, silicon residuals would form underneath the channel, if channel dimensions were made shorter than the maximum trench depth. The results from the fabrication chapter can be used to further discuss these aspects in the subsections below.

6.1.1 Front release windows

Two front release windows were designed. From the fabrication, it was made clear that the larger release window, would fully release the microfluidic channels and heaters from the bulk silicon after 8h and 2 minutes. At this time also the devices with small front release windows should be just released. This was not the case and only happened after 8h and 35 minutes, which was 33 minutes longer than calculated. Maybe because the wafers were removed several times from the KOH solution it would take a few minutes to hit the described etch rates. This was not investigated further, as the small release windows proved to be far from ideal because of more problems which are described in subsections 6.1.3 and 6.1.4.

6.1.2 V-grooves

As explained in the design section, V-grooves will occur on top of the wafer trenches. It was determined that most of these V-grooves did not exceed a height of 400 nm. However, a smooth photoresist layer could not be created on top and recurring circular spots were visible at complex trench junctions, such as shown in figure 6.1. It was also noticed that these spots did not occur at tapered T-junctions. If we analyse the LPCVD growth behaviour in regular T-junctions versus tapered T-junctions, as shown in figure 6.2, it can be noticed that the tapered T-junctions prevent the formation of deep 75 µm pits. These pits make successive lithography steps problematic as no smooth surfaces can be created. This will obstruct a high-quality pattern transfer, which is crucial for the subsequent slit mask.

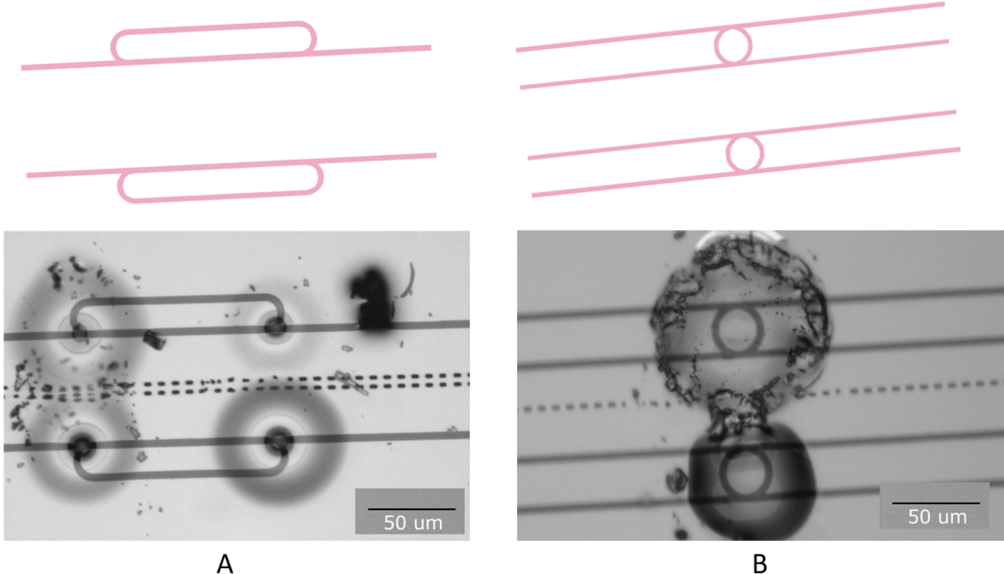
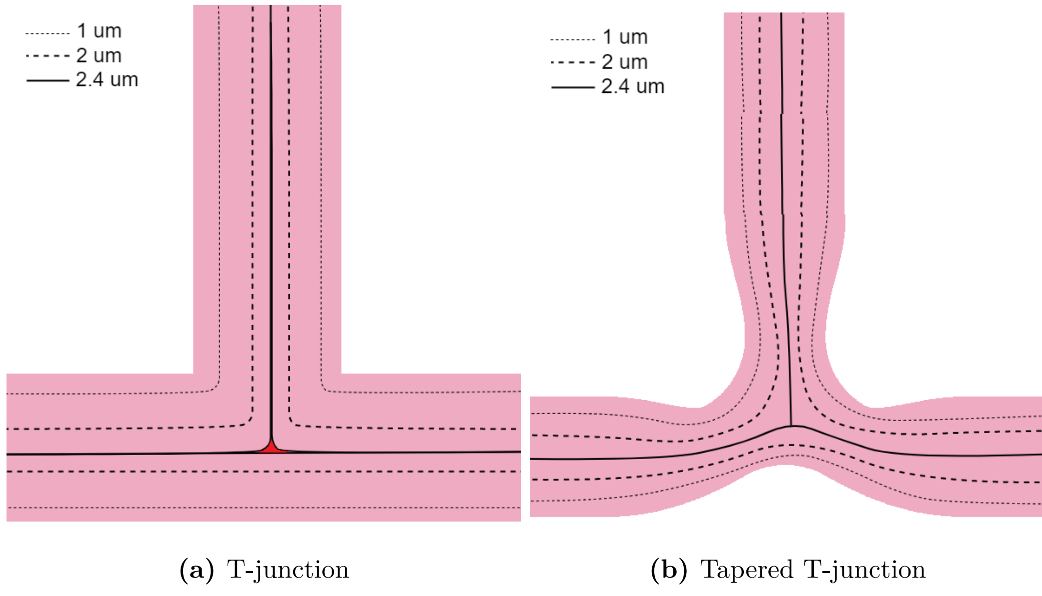


Figure 6.1: Circular spots on complex trench geometries. The top pictures show the trench mask. The bottom pictures show the developed photoresist layer with transferred slits. In A, at the half Y-junction circular spots can be noticed. In B, at the circular junctions more circular spots can be noticed.



(a) T-junction **(b)** Tapered T-junction

Figure 6.2: SiRN growth in complex trench junctions. Both trench junctions in (a) and (b) start with the same width of 3 µm. The lines indicate the SiRN layer thickness from the outer walls growing inwards to the center of the trench. In (a), by analysing the LPCVD SiRN growth pattern in this trench T-junction, it is highly likely that the red area will not be filled, which leaves a 75 µm deep pit behind. In (b), analysing the same growth pattern of a tapered trench T-junction, will result in no pit forming.

6.1.3 Undercutting

In the test run a total of 525 µm was etched from the backside of the wafer. After the KOH reached the trenches at a depth of 450 µm the heaters were exposed to KOH solution. Another 75 µm was etched to reach the top of the wafer, this resulted in an undercut of 0.95 µm. If we look at figure 6.3 position 2, the undercut measures around 10 µm. This means around 9 µm of undercut is due to the misalignment of the backside rectangular mask to a Si ⟨110⟩ direction. The total undercut on the backside masker as shown in figure 6.4 was 17.5 µm. If we subtract the undercut due to etching in the ⟨111⟩ direction, also around 9 µm of undercut due to misalignment is present. However, if we fill in the misalignment angle of 0.5° in equation 2.32, the undercut would be 87.3 µm. This is not the case and it seems that the rate at which this undercut (undercutting rate) forms is much slower than the Si ⟨100⟩ etch rate of 60 µm/min.

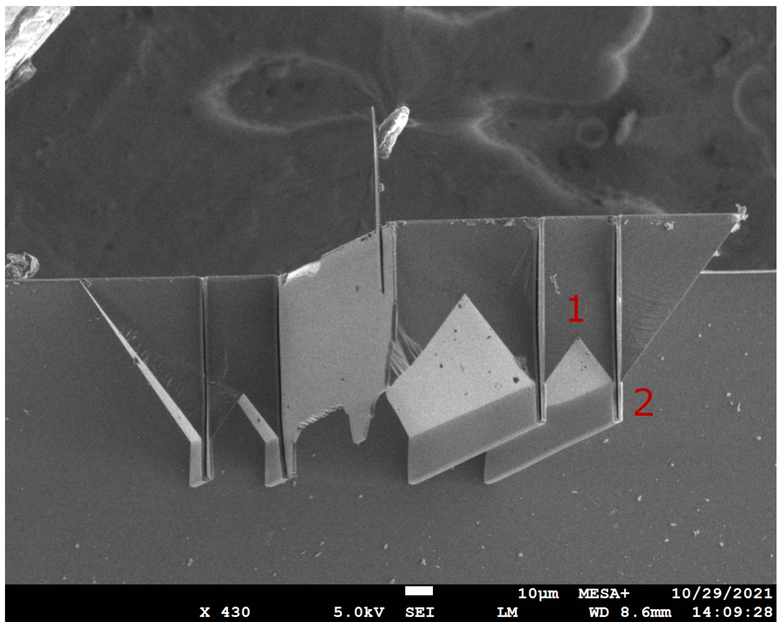


Figure 6.3: Cross-sectional SEM of the released test structure. At 1, the Si {111} planes meet at a height of 18 µm. The undercut, at 2, under the heaters measure around 10 µm

.

By also looking at the results from the device run, which have been removed from the KOH solutions at more optimal etching times, it can be noticed that after 8h and 2m only 2 µm of under etch can be noticed in figure 6.5, with almost the same misalignment angle of the backside mask of around 0.5°. This confirms that the undercutting rate indeed must be much less than 60 µm/min.
More distinct effects of the undercut due to misalignment could be noticed on the front side of the wafer. Again by looking at figure 6.5, an undercut on the left and right top side can be noticed. This undercut measured 16.8 µm. By looking at the etch time only 5.5 µm was caused by etching in the Si ⟨111⟩ direction, the remaining 11.3 µm is thus caused by misalignment of the front mask to a ⟨110⟩ direction. The measured misalignment angle of the front mask was 0.36°, by filling in a front mask length of 2500 µm and the angle in equation 2.32, this would lead to an undercut of 15.7 µm which is much closer than expected but still much more than reality. A probable explanation for this undercutting rate is given in the work of S. Singh et al. [41]. It is mentioned that the undercutting rate is dependent on the angle, and the position of the masker opening on the wafer. However, no

actual etch rates are specified for positions on the wafer or misalignment angles. Because the front and back release masks in this work are aligned to the alignment markers, which are not accurately aligned to a Si ⟨110⟩ direction, there is also the possibility that some mask openings are better aligned to a ⟨110⟩ direction than other mask openings. To investigate this undercutting effect more, requires the alignment markers of the trench mask to be accurately aligned to a Si ⟨110⟩ direction. A method to do this is described in the work of S. Singh et al. [41]

Figure 6.4: Undercut of the back mask. The misalignment angle, or the angle between the black square and light outlines, showed to be 0.5°, the undercut from top to bottom measured 17.5 µm, the undercut from right to left measured 10 µm.

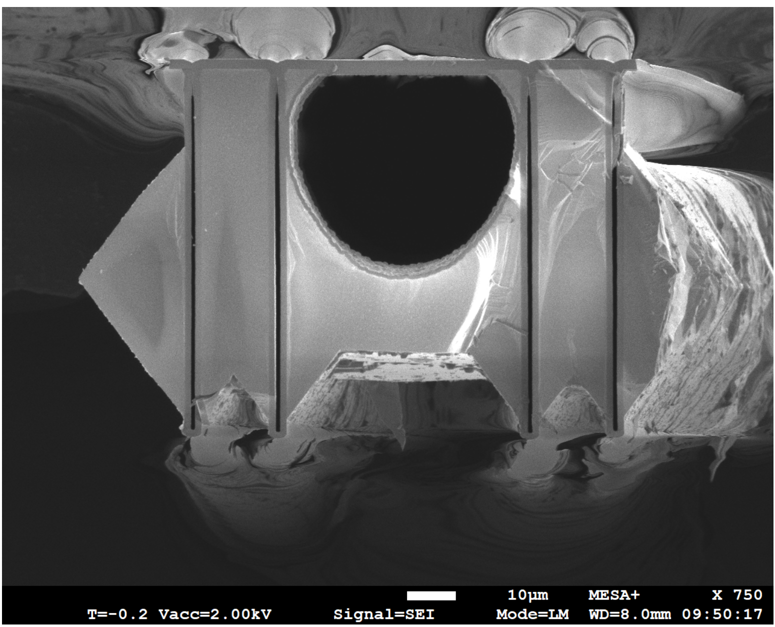


Figure 6.5: After an optimal etching time of 8h and 2m only, only an undercut of 2 µm can be noticed on the bottom of the heaters.

6.1.4 Residual silicon

As explained in the design section, residual silicon will be left on the outer trench walls and under the microfluidic channel if the channel height and trench height are not equal. The largest residual silicon on the outer trench wall having used a large front release window, as shown in figure 6.6, measured around 800 μm^2. This residual had an undercut close to the calculated 5.1 µm and therefore matched the design very closely. The largest observed residual found, after using small release windows, was close to 600 μm^2, as shown in figure 6.7.

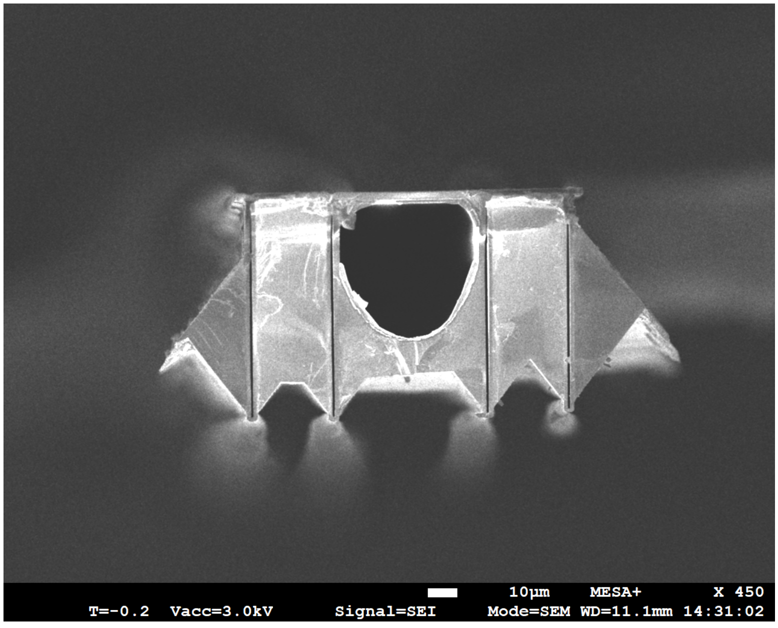


Figure 6.6: Using large release windows the bulk silicon is spaced 125 µm away from the device island. It can also be noticed that on the top left and top right side the residual silicon is not symmetrical.

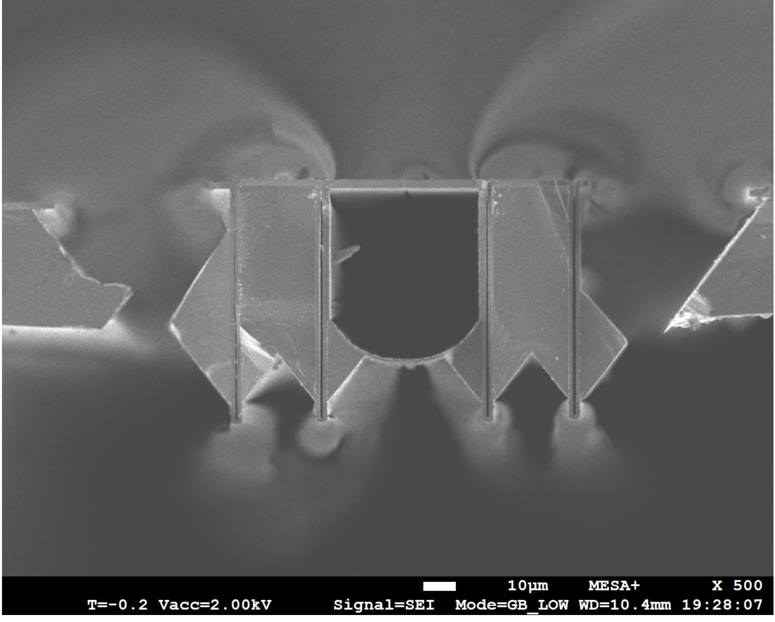


Figure 6.7: Using small release windows the bulk silicon is spaced only 10 µm away from the device island. It can also be noticed that on the top left and top right side the residual silicon is not symmetrical.

The silicon residuals formed left and right, were not symmetrical in many cases. It was already expected that due to misalignment to a $\langle 110 \rangle$ direction different undercut rates can be present on different parts of the wafer. This extra undercut will lead to more etching of the residual silicon. This effect can either be beneficial as the cross-sectional area on one side is decreased significantly, or it can be disadvantageous because a non-symmetry is introduced.

Because the microfluidic channel has not the same height as the trenches, residual silicon was left under the channel as shown in figure 6.7. The calculated area is 312.5 μm^2, the area due to a D of 25 µm via the approximation $(\tan 35.3° \times D)^2$ equals 313.3 μm^2, which shows this is a very close approximation. The residual underneath the microfluidic channel can easily be prevented by etching the microfluidic to the same depth as the trenches.

6.1.5 Opening the SiRN membrane

The fabricated test run structures enabled us to test the manual puncturing of SiRN membranes on top of the wafer through a pyramid-shaped via. The needle with a diameter of 200 µm could be inserted in the via with ease. Only a small touch to the membrane was needed to puncture it. A slight resistance was felt through the needle as the membrane was punctured occuring once per via.

This method was also tested on the devices from the device run. Here again a small resistance was noticed through the needle after the needle was inserted into the via. This resistance could only be felt once per via and no damage was visible on the top of the wafer. In combination with the cross-sectional SEM results of the pyramid-shaped vias in the fabrication process it is certain that this resistance comes from the formed SiRN membrane. However, the quality of the membranes in the pyramid-shaped vias have not been observed.

6.1.6 Minor problems

Throughout the fabrication process some minor issues came to light, which can be resolved by making alternations to the mask design. These additions can improve the quality of the micro-fabrication. The first problem was that the front release mask was spaced only 4 to 5 µm from the outer trench walls. By slight misalignment of the front release mask it would overlap the heaters. This opened the heaters on top and exposed the heaters during the etch in the KOH solution, as shown in figure 6.8. To resolve this the distance between the outer trench walls and release windows should be increased to at least 10 µm.

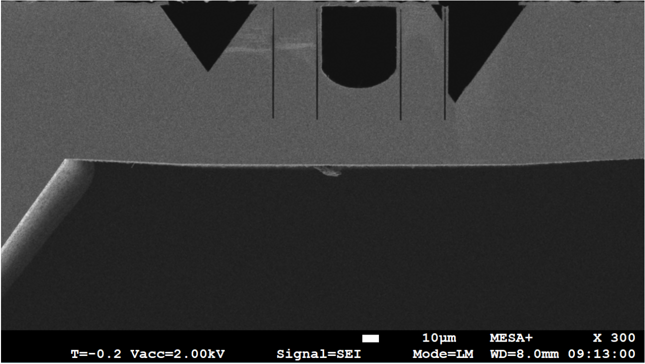


Figure 6.8: Due to misalignment of the front mask on one wafer the heaters got etched in the KOH solution.

The second problem involved the SiRN bridges, used to guide the electrical wires to the microfluidic channel island. These SiRN bridges were connected to the microfluidic channel parallel to a Si ⟨110⟩ direction. This leaves a lot of residual silicon underneath these trenches, as shown in figure 6.9. This residual silicon can result in problems if this is not fully isolated from the silicon between the trenches. By attaching the SiRN bridges under a slight angle of 5 to 10° more silicon will be etched away. If no silicon is desired at all underneath, the SiRN bridges can be placed under an angle of 45°.

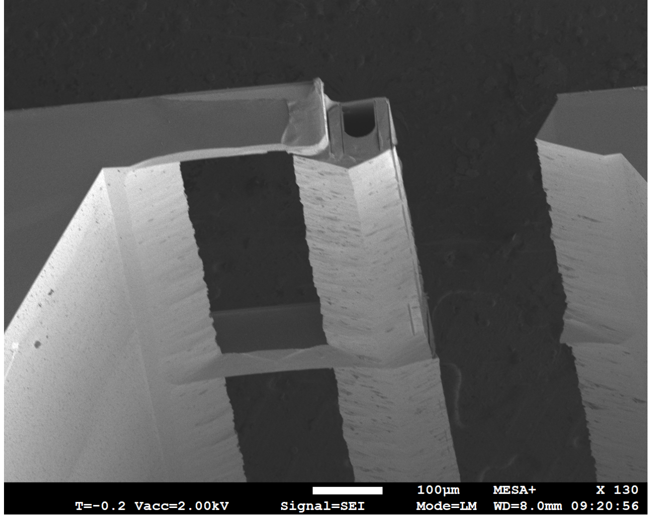


Figure 6.9: Because the SiRN bridges are aligned close to a Si ⟨110⟩ direction residual silicon will remain under SiRN bridges

A third problem, which is caused as a direct result of an incomplete or low-quality slit transfer, is the final depth and geometry of the microfluidic channel. The microfluidic channel was designed to reach a depth of 50 µm by using one row of slits. This should have created microfluidic channels with complete vertical sidewalls. However, this was only the case for devices which used the tapered T-junction and had a high-quality slit transfer, as shown in figure 6.7. Therefore, it again is very crucial that the slit transfer is of high quality.

A fourth problem is that multiple devices were released from the wafer during careful handling of the wafer. The front- and back-side outlines used for releasing the devices were made 300 µm wide. This would result in a height of 215.95 µm for both the back-side pyramid and a front side pyramid, leaving only 93 µm silicon between the pyramid tips. This was not enough silicon to keep the devices in the wafer. Moreover, if we look at the wafer thickness specification of 525 ± 20 µm, the silicon thickness between the pyramids can even become smaller than 93 µm. It is therefore advised to decrease the maximum outline width to 250 µm, this would always leave a minimum of 165 µm silicon between the pyramid tips.

6.2 Demonstrator device analysis

Despite the insightful findings of the COMSOL Multiphysics analysis, no verification could be performed on real S-TASCT demonstrator devices. However, it is still very likely that the main heat loss is caused by natural convection on the outer walls of the microfluidic channels and heaters. The simulated value of around 1.1 W to reach a center temperature of 600° seems very reasonable, if we compare this to the results of the demonstrator device developed for the TASCT, which needed 1.4 W to reach a temperature of 450°, in the sensor strip on top of the channel [21]. A higher power was needed for this device, to reach a temperature lower than 600°. This can be due to the higher mass-flow of 1 g h^{-1} used in this device or the location of the sensor strip, which can be placed away from the hottest area.

The total calculated power needed to reach a center temperature of 600 °C was 103 mW. This is 10.7 times lower than the simulated value of 1.1 W. The conductive heat loss was in the right order as calculated and the applied power on the heaters scaled linearly with an increased cross-sectional surface area of the residual silicon. The simulations also showed that the radiative power loss was negligible compared to the heat loss via natural convection.

Overall, by looking at the performance of the older TASCT demonstrator device and the results from the simulation, a center temperature of 600° in the microfluidic channel of the new S-TASCT demonstrator device can easily be reached if the demonstrator devices are placed in a vacuum setup. Without this vacuum setup, it is still possible to reach 600°, but much higher voltages must be applied on the heater, which may eventually lead to unforeseen complications due to much higher current densities.

7 | Conclusion and outlook

In this chapter all conclusions from previous chapters are summarized. The conclusion helps to provide all key aspects which can be used for the future outlook for this simplified Trench-assisted Surface Channel Technology. The outlook also contains the recommendations, which should be taken into account when further research is conducted on this technology platform.

7.1 Conclusions

In this work, a simplified Trench-Assisted Surface Channel Technology was presented. The main goal was to introduce a simpler yet still effective method to create highly-doped silicon sidewall heating elements, with a large cross-sectional area parallel to the channel. Introducing a KOH wet etch step to the TASCT platform enabled us to form pyramid-shaped vias to the microfluidic channels and releasing of the microfluidic channels from the bulk silicon in one micro-fabrication step. This reduced the new process flow by around 100 micro-fabrications steps. However, from the theory, we learned that using KOH solutions can bring new complications to the platform as well. One of the complications is the contamination of residual insoluble floccules, which will be left on the wafer and in the microfluidic channels. This requires an extra RCA-2 cleaning step which putd a limit on the RCA-2 compatible materials for the devices. However, this can be avoided by encapsulating the microfluidic channels with a thin SiRN membrane buried under the channel. This membrane can then be punctured manually through the pyramid-shaped via after all micro-fabrication steps are completed.

Another problem from using the KOH solution is the under etching of the hard masks and SHEs. The anisotropic form of the KOH etch comes from the limited etch rate in the Si ⟨111⟩ direction. However, this etch rate is still 0.75 µm/h thus resulting in undercutting, hence widening of the mask windows. If the SHEs are exposed to KOH solution, then they will also be prone to undercutting. In addition to this undercut, there will also be an undercut due to misalignment of the masker window with a Si ⟨110⟩ direction. This extra undercut is dependent on the mask window length and the misalignment angle. Even for misalignment angles $<1°$, this undercut is already very significant compared to the undercut created by the Si ⟨111⟩ etch rate. However, it was observed that this undercutting rate is much slower than the typical Si ⟨100⟩ etch rate. Since the SHEs will only be etched from the backside of the wafer, it takes a lot of time before the SHEs are reached. By carefully designing the front- and back-release windows and by optimizing the etch time, only a slight undercut of 2 µm will be present under the SHEs. This undercut also ensures that the SHEs are fully released from the bulk silicon and is therefore much desired.

Because of the typical etching characteristic of KOH yet another unavoidable side-effect will be present, the formation of residual silicon on the outer trench walls. Calculations presented in this work can estimate the cross-sectional areas of the residual silicon very accurately, but these calculations only hold if the undercut due to misalignment with a Si ⟨110⟩ direction is minimal. If the misalignment with a Si ⟨110⟩ direction increases, non-symmetrical residuals will form on the left and right sides of the outer trench walls. This can be beneficial if a smaller cross-sectional area of the residue is desired. By carefully aligning the first alignment markers with a Si ⟨110⟩ direction, will result in symmetrical residuals as calculated and minimize the extra undercutting due to misalignment.

One problem that arose during the fabrication process were circular spots on the photomask. These circular spots are imperfections on the photomask and recurred at the same spots on each wafer. By analysing the problem it was shown that complicated trench junctions are the cause of these circular spots. It was also observed that tapered T-junctions did not have these circular spots. By analysing the SiRN growth process in the trench junctions it became clear that the circular spots are caused by 75 µm deep pits. These pits made subsequent lithography steps very problematic as no smooth photomask layer could be made around those pits.

Overall, this simplified Trench-Assisted Surface Channel Technology proved to be a simpler alternative to the existing Trench-Assisted Surface Channel Technology. By using tapered T-junctions and by designing the windows in combination with optimizing the etch time, this new technology can already be used to realize SCT-based devices, such as the Coriolis mass-flow sensors or Wobbe-index sensors. However, no performance of devices realized with this new technology has been tested yet.

7.2 Outlook & Recommendations

The S-TASCT platform is near to its completion and from the conclusion of this work, it is clear that by integrating tapered T-junctions for the trench mask in combination with fine-tuning the front release windows and etch times, this platform is ready to be used for the realization of SCT-based devices. A first step can be to incorporate the solutions provided to the common problems and complete a new device run with demonstrator devices equivalent to the ones designed in this work. These devices can provide insightful information about this platform.

However, some aspects may require some further research to fully prove the viability of this platform. One of these aspects is a closer inspection of the SiRN membranes formed beneath the microfluidic channels. Cross-sectional SEM images can be taken to verify the quality of these membranes and to distinguish if these membranes fully encapsulate the channel during the KOH etch. An optimal result of this research will be a before puncture and after puncture image of a SiRN membrane.

Another aspect is the investigation of the undercutting rate due to misalignment with the Si ⟨110⟩ direction. By first determining the exact Si ⟨110⟩ direction, followed by the patterning of trenches and front release masks on various degrees of misalignment. The undercutting rate for each misalignment angle can be determined. This helps to understand to which extent SHEs can still be formed and may limit this technology.

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Appendices

A | Mask design & Allocation

A.1 Masks

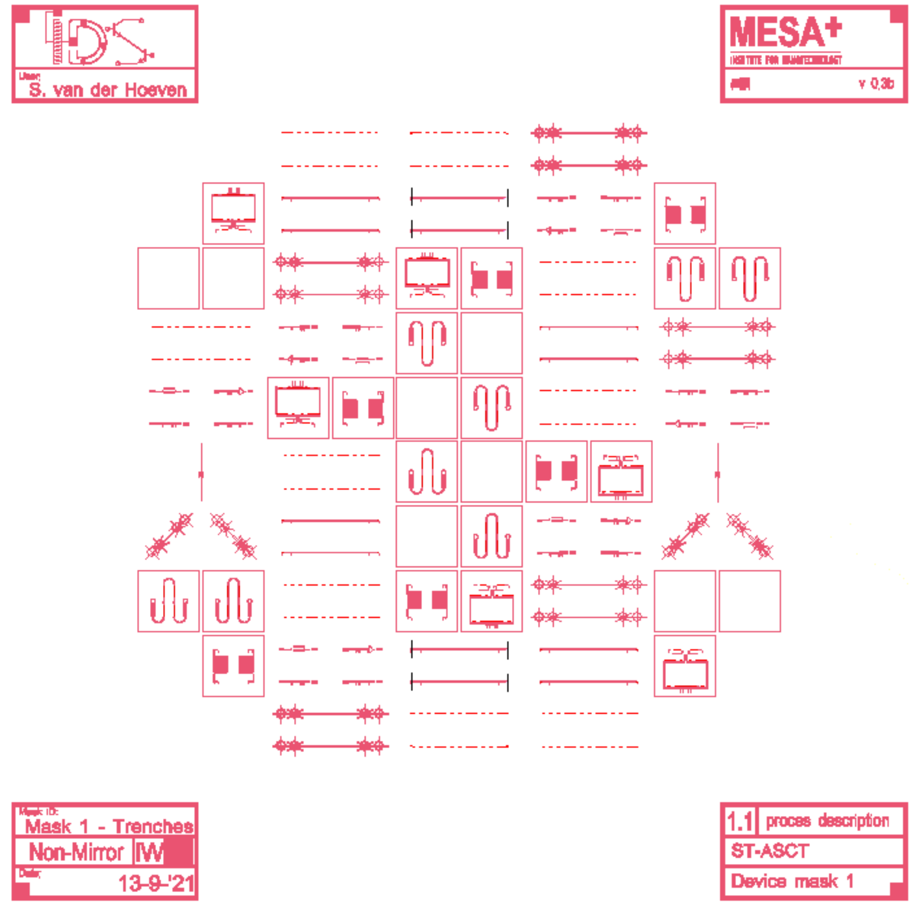


Figure A.1: Trench mask

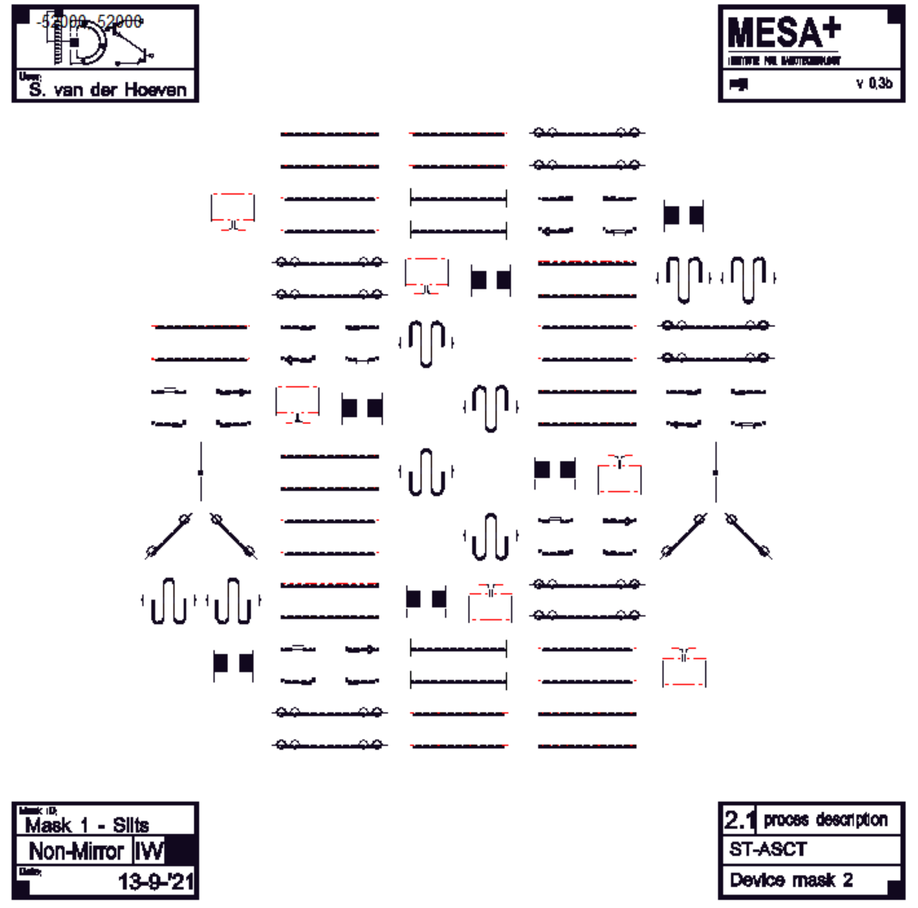


Figure A.2: Slit mask

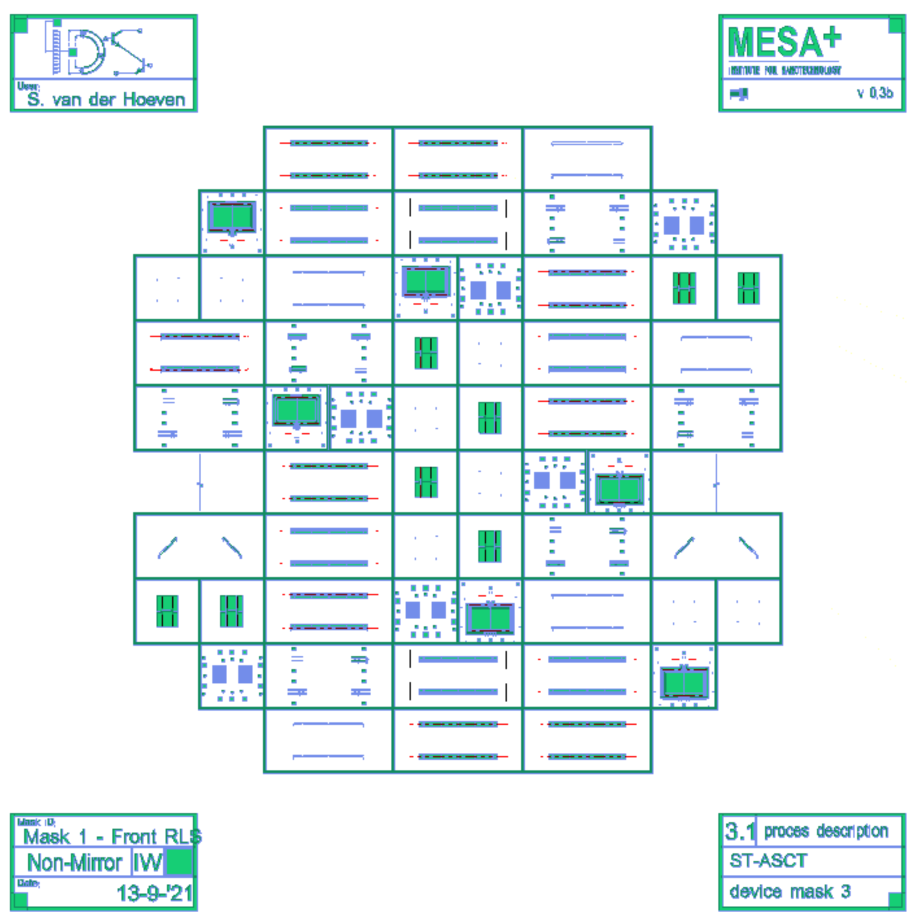


Figure A.3: Front release mask

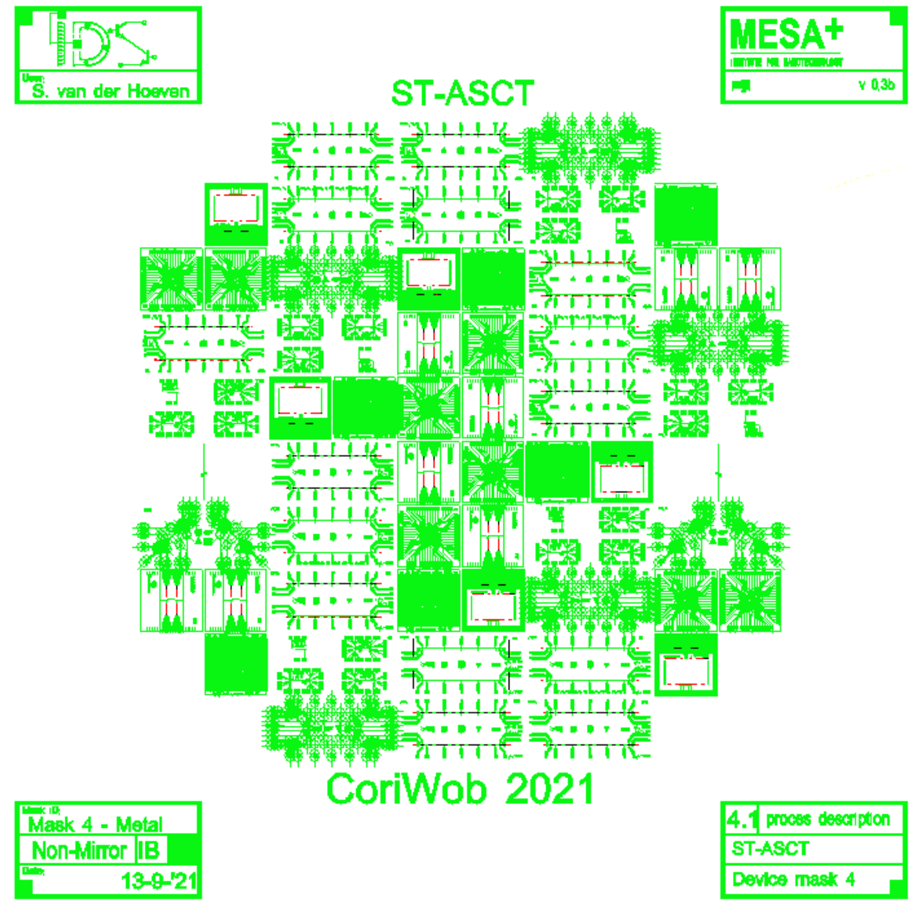


Figure A.4: Metal mask

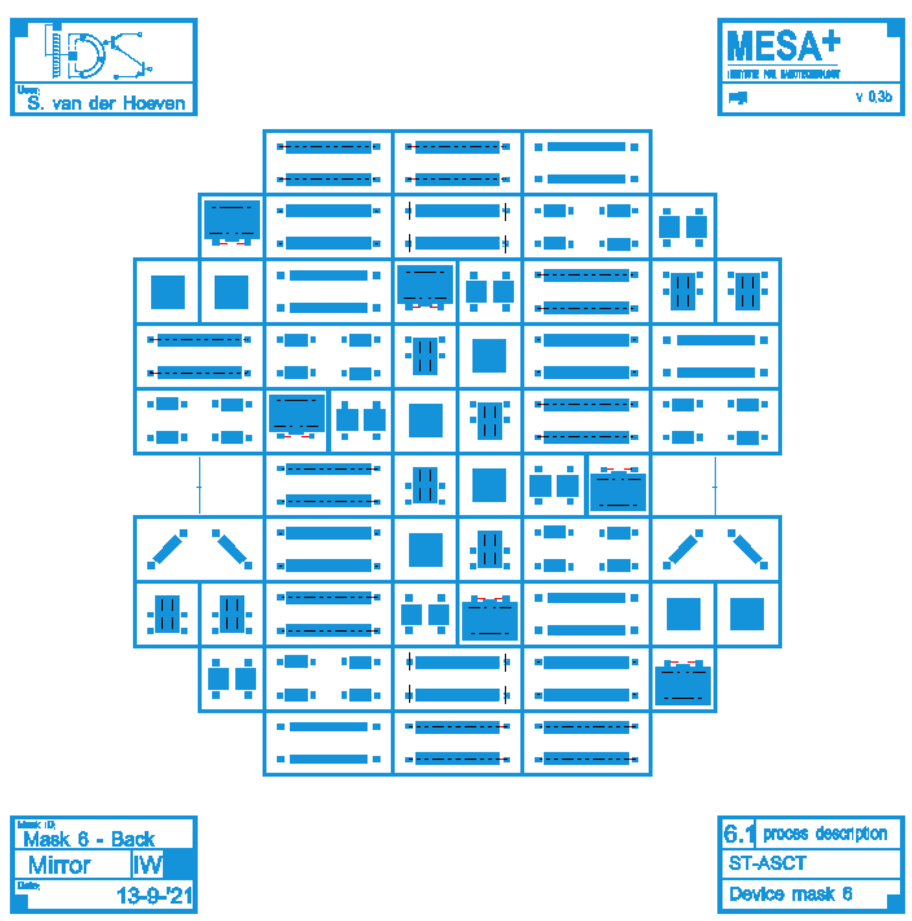
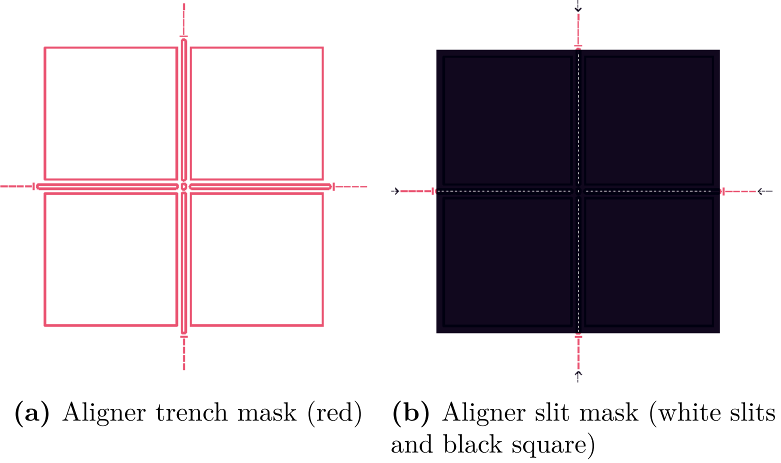


Figure A.5: Back Mask

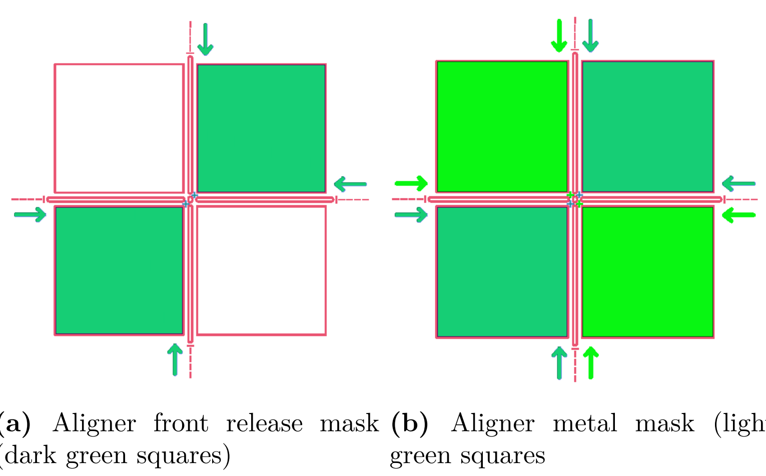
A.2 Alignment marker set

The trench mask of A.6(a) is the first mask used and therefore contains all outlines for subsequent alignment markers. The slit mask of A.6(b) should be aligned exactly in the center. However, the mask in A.6(b) is inside-white, which means that all black will be transparent in the masker. Therefore, it should be noted that in combination with positive photoresist the squares will be opened on the wafer. This means all these alignment markers must be covered with kapton tape during the etching steps. After the kapton tape is removed again, the squares of figure A.7 can be placed inside the outlines. Because the metal layer must be covered by a capping layer, the crosses of figure A.8(a) can be placed inside the metal squares. The final back release masker, is a cross that must be centered in the middle of the outline.



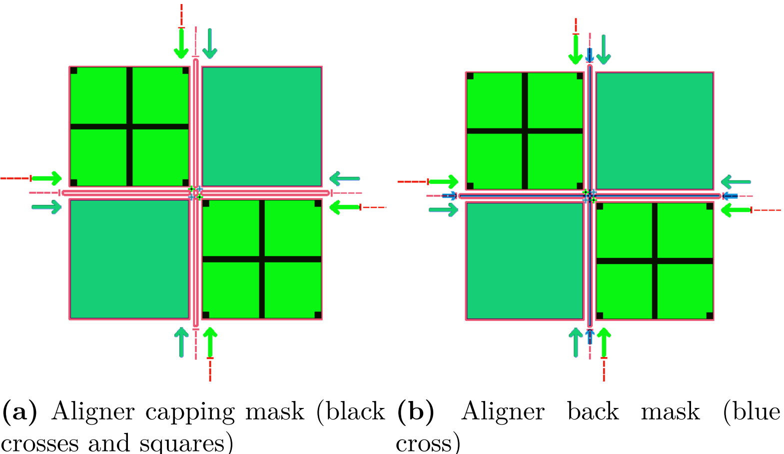
(a) Aligner trench mask (red) **(b)** Aligner slit mask (white slits and black square)

Figure A.6: The trench mask **(a)** is the first mask used and therefore contains all outlines for subsequent alignment marks. The slit mask **(b)** is inside-white, which means that all black will be transparent in the masker.



(a) Aligner front release mask (dark green squares) **(b)** Aligner metal mask (light green squares

Figure A.7: Both aligners **(a)** and **(b)** can be placed inside the squares.



(a) Aligner capping mask (black crosses and squares)

(b) Aligner back mask (blue cross)

Figure A.8: The capping mask alignment markers **(a)** should be placed exactly over the metal squares. The back mask **(b)** must be placed exactly in the center.

A.3 Wafer Allocation

A.3.1 Test run

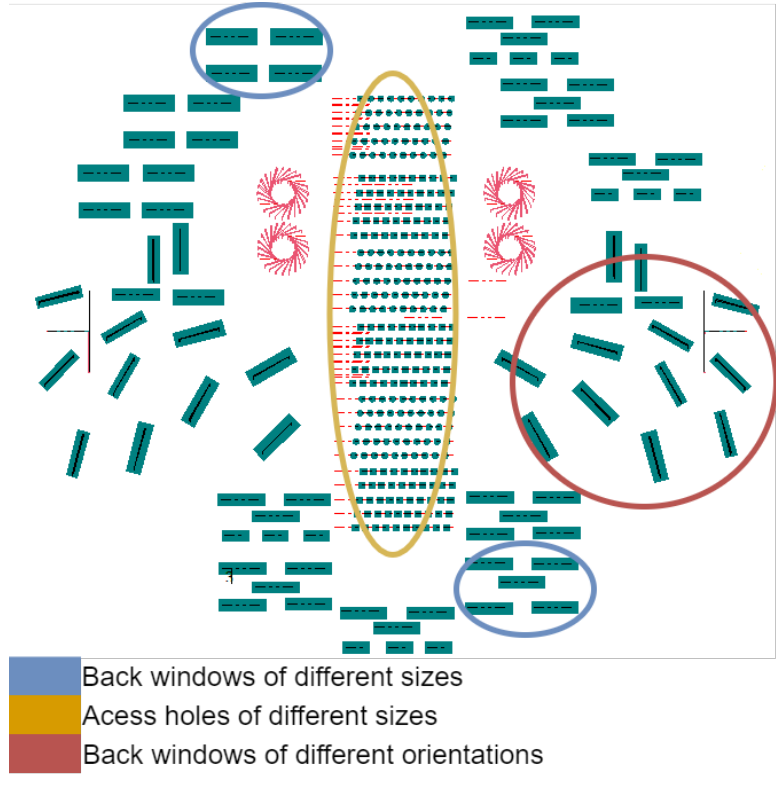


Figure A.9: Complete wafer position allocation used in the test run. Blue: different sizes of large windows result in more bulk silicon removal; Yellow: different sizes of small windows result in different final pit sizes, these are used for determining the optimal access hole windows; Red: Windows placed on a angle result in a undercut of which the significance is tested.

A.3.2 Device run

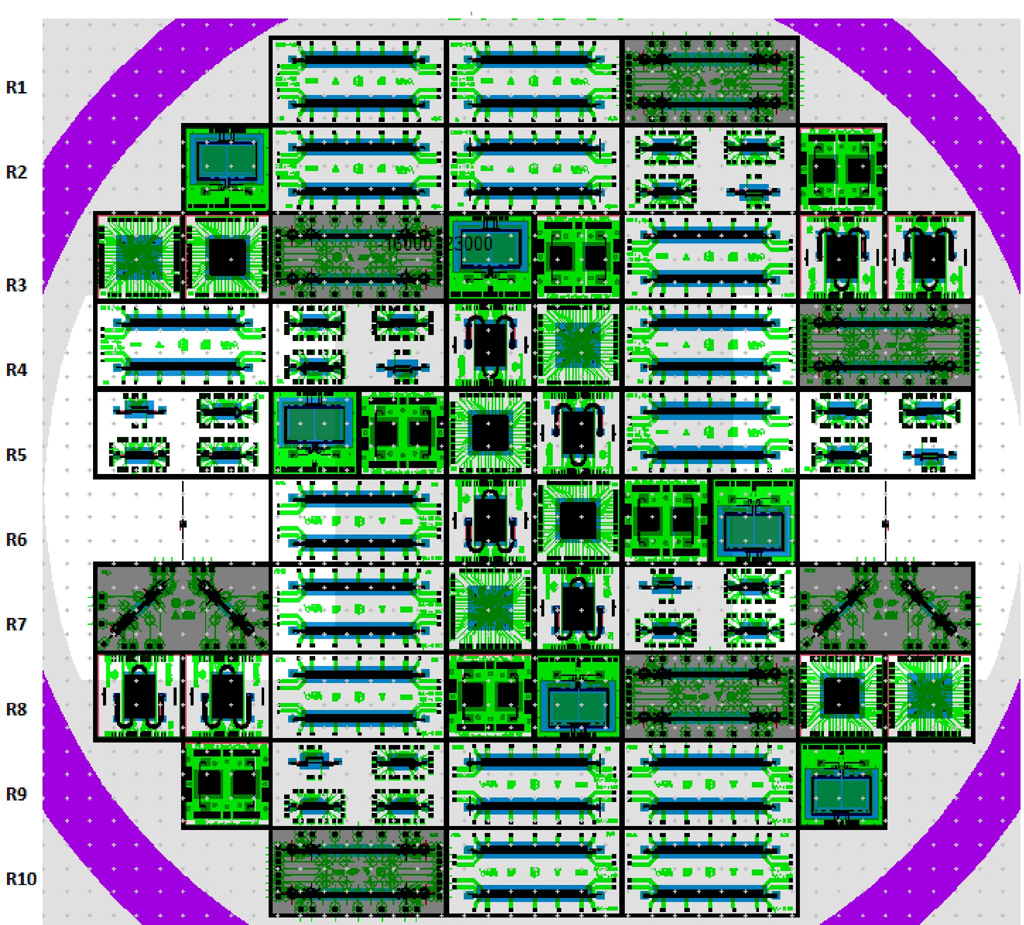


Figure A.10: Complete wafer allocation used in the device run. Only one of each device is placed per row according to the row numbers.

B | S-TASCT process flow

Print date: 2022-02-01

Name of process flow:	S-TASCT2021_SvdH
Platform:	Fluidics
Creation date:	2021-09-06
Personal information	
User name:	Hoeven, S. van der
Email address:	s.vanderhoeven@student.utwente.nl
Company/Chair:	Masterstudenten
Function:	Student
Project:	Simplified trench-assisted surface channel technology
Name of supervisor:	Henk-Willem Veltkamp
Process planning	
Process start:	2021-09-14
Process end:	2021-12-24
Status	
Name of advisor:	
Last revision:	2021-11-03
Approval:	
Approval date:	
Expiration date:	

ILP: In-line Processing	MFP: Metal-free Processing	UCP: Ultra Clean Processing	Removal of Residues

Step	Level	Process/Basic flow		User co
1		**Substrate Silicon** (subs104)	**NL-CLR-Wafer storage Cleanroom** Orientation: <100> Diameter: 100 mm Thickness: 525µm +/- 15µm Polished: double side (DSP) Resistivity: 0.01-0.025Ωcm Type: p+/ boron	
		film1903: Wet Oxidation of Silicon or polySi (A3)		
2	MFP	**Cleaning in 99% HNO3** (#clean001)	**NL-CLR-WB14 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	Finished
3	MFP	**Cleaning in 99% HNO3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
4	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
5	MFP	**Cleaning in 69% HNO3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO3 • Temperature: 95°C • Time: 10min	
6	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
7	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** **Optional drying step**. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples).	

Step	Module	Process	Instructions	Comments
			Batch drying of substrates: Use the Semitool for drying up to 25 substrates at once.	
8	MFP	**Etching in 1% HF** (#etch127)	**NL-CLR-WB15 1% HF BEAKER** Purpose: remove native SiO2 from Silicon. Chemical: 1% HF • Temperature: room temperature • Time: 1min **Optional etching step. This step is obligatory for the MESA+ monitor wafer.**	
9	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
10	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	
11	MFP	**Wet Oxidation of Silicon or polySi (MFP)** (#film903)	**NL-CLR-A3 FURNACE** Application: wet oxidation of Silicon or polySi. Programs: WET750, WET800, WET900, WET1000, WET1150 Settings: • Standby temperature: 700°C • Temperature range: 750-1150°C • O2 flow: 4slm • Ramp: 10°C/min Please mention the following settings in the User Comments: • Program: ….. • Target thickness: ..... nm • Time: .....min	Target thi Temperat Time:app
12	ILP	**Particle inspection** (#metro201)	**NL-CLR-COLD LIGHT SOURCE (SEM ROOM)** Shine light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a coating from one of the furnaces contains (a lot of) particles! Contact Christaan Bruinink for questions.	
13	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
14	ILP	**HMDS priming** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 HOTPLATE** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Primer: HexaMethylDiSilazane (HMDS) Settings: • Temperature: 150°C • Pressure: 25inHg • Dehydratation bake: 2min • HMDS priming: 5min CAUTION: let the substrates cool down before handling with your tweezer!	
15	ILP	**Coating of Olin OiR 907-17** (#litho101)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 907-17 Spin program: 4000	

Step	Type	Process	Details	Comments
			Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s	
16	ILP	**Prebake of Olin OiR 907-17** (#litho003)	**NL-CLR-WB21 PREBAKE HOTPLATE** Purpose: removal of residual solvent from the resist film after spin coating. Settings: • Temperature: 95°C • Time: 90s	
17	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	**NL-CLR-EV620 AND EVG6200NT MASK ALIGNERS** Settings:(EVG620) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: constant time/…/... • Exposure time: 4sec This exposure time is based on the Hg lamp with a power of 12mW/cm2. Settings:(EVG6200NT) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: UV-LED GHI-line 100 mJ/cm2 • Exposure setting needs to be optimized for optimal result, depending on structures on the mask! This exposure is based on UV-LED light source.	Mask 1: T Vacuum c
18	ILP	**After exposure bake of Olin OiR resists** (#litho005)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 60s	
19	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21 DEVELOPMENT BEAKERS** Developer: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
20	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
21	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
22	ILP	**Postbake of Olin OiR resists** (#litho008)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 10min	No post b tapering t
23	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
		etch1774: Directional RIE of SiO2 and Si3N4 by CHF3/O2 Plasma (PT790)		
24	UCP	**Etching of SiO2 and Si3N4** (#etch221)	**NL-CLR-PT790** Application: etching of thin layers of oxides and nitrides. Settings: CHF_3 flow: 100sccm O_2 flow: 5sccm Pressure: 40 mTorr Power 250W Etch rate SiO2: 32 nm/min Etch rate Si3N4: 30nm/min	46 min = 92 min = 2x4 wafer wafers +45min c 5h
25	UCP	**Chamber clean (PT790)** (#etch199)	**NL-CLR-PT790** Application: removal of organic and fluorocarbon residues from the chamber wall. • Graphite electrode • O_2 flow: 100sccm • Pressure: 100mTorr • Power: 400Watt Note: always clean the chamber after etching!	
26	ILP	**Stripping of Resists** (#strip101)	**NL-CLR-TePla360** Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041	1h r04 for or r16 for

on the TePla360 (strip1130)!

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

27 | Rem Res | **Removal of metal traces in RCA-2** (#residue504) | skip

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

28 | ILP | **Rinsing** (#rinse001) | skip

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

29 | ILP | **Substrate drying** (#dry001) | skip

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

clean1002: In-line cleaning (WB16-ILP)

30 | ILP | **Cleaning in 99% HNO3** (#clean005)

NL-CLR-WB16 BEAKER 1
Purpose: removal of organic traces.
Chemical: 99% HNO3

• Time: 5min

NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!

31 | ILP | **Cleaning in 99% HNO3** (#clean006)

NL-CLR-WB16 BEAKER 2
Purpose: removal of organic traces.
Chemical: 99% HNO3

• Time: 5min

32 | ILP | **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

33 | ILP | **Substrate drying** (#dry001)

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

etch1803: High-Aspect Ratio (<40) BOSCH - BASIC (Oxford Estrelas)

34	ILP	**High-Aspect Ratio (<40) BOSCH** (#etch803)	**NL-CLR-Oxford Estrelas** Application: high-aspect ratio etching of trenches in Silicon. Recipe: #B-HAR114 @25 deg [#etch803] Settings: • Temperature: 25°C • He pressure: 10Torr	Custom r 500 cycle

Step (in order)	Deposition	Break	Etch
Time (sec)	2.4		3
C4F8 flow (sccm)	200		10
SF6 flow (sccm)	10		200
APC (mTorr)	30		40
ICP (W)	1300		1600
CCP – LF (W)	0		16

Check the process sheet for settings and details:
https://mesaplusnanolab.ewi.utwente.nl/mis/generalinfo/downloads/usermanuals/425/Process%20sheet%20High%20Aspect%20Ratio%20[etch803]%20%20v2.pdf

35 ILP **Removal of Fluorocarbon** (#etch809) — 30min

NL-CLR-Oxford Estrelas
Application: removal of Fluorocarbon after BOSCH etching in the Oxford Estrelas.
Recipes: #C - FC removal @10degC, #C - FC removal @25degC

WARNING - PLEASE READ
This recipe is effective in stripping of Fluorocarbon in microstructures with aspect ratios up to 15. Contact the administrator in case you want to strip Fluorocarbon in nanostructures. This recipe attacks silicon and nitride coatings on the nanometer scale!

Settings:
• Platen temp: 10°C or 25°C (see recipe name)
• He pressure: 10Torr
• Pressure: 10mTorr
• O2 flow: 100sccm
• ICP: 2000W
• CPP: no CCP (50W at plasma ignition)
• Time: 5min*

* You can increase the time in case you want to completely remove the resist.

36 ILP **Stripping of Resists** (#strip101) — skip

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

37 Rem Res **Removal of metal traces in RCA-2** (#residue504) — skip

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

38 ILP **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Step	Type	Process	Description	Comment
			Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
39	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		etch1204: HF etch 50 % (WB15)		
40	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO_3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO_3!	
41	MFP	**Cleaning in 99% HNO_3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO_3 • Time: 5min	
42	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
43	MFP	**Cleaning in 69% HNO_3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO_3 • Temperature: 95°C • Time: 10min	
44	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
45	MFP	**Etching in 50% HF** (#etch129)	**NL-CLR-WB15 50% HF BEAKER** Application: stripping films prior to high-temperature processing. Chemical: 50% HF • Temperature: room temperature • Time: until the silicon is hydrophobic • LPCVD SiRN (G3) = 3.1 - 3.5 nm/min • SiO_2 = 1 µm/min • LPCVD Si_3N_4 (H2) = 11.6 nm/min	remove S beaker
46	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
47	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	
		film1205: LPCVD of low-stress SiRN (G3-50 MPa)		
48	MFP	**System monitoring** (#spc001)	**NL-CLR-FURNACES** Purpose: monitoring the stability of the furnaces in terms of deposition rate, non-uniformity and optical parameters. Procedure: 1. Take a Silicon wafer from the wafer box with monitor wafers 2. Fill in the digital logbook and write down the last 4 digits of the waferID in the User Comment 3. Write down the run number on the lid of the waferbox	
49	MFP	**Cleaning in 99% HNO_3** (#clean001)	**NL-CLR-WB14 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO_3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO_3!	

No.		Step	Procedure	Comments
50	MFP	**Cleaning in 99% HNO3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
51	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
52	MFP	**Cleaning in 69% HNO3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO3 • Temperature: 95°C • Time: 10min	
53	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
54	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** **Optional drying step**. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	
55	MFP	**Etching in 1% HF** (#etch127)	**NL-CLR-WB15 1% HF BEAKER** Purpose: remove native SiO2 from Silicon. Chemical: 1% HF • Temperature: room temperature • Time: 1min **Optional etching step. This step is obligatory for the MESA+ monitor wafer.**	
56	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
57	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	Process w drying ve overnight
58	MFP	**Loading of wafers** (#film217)	**NL-CLR-LPCVD FURNACES** Program: UN-/LOAD **RESTRICTION**: the maximum loading capacity of process wafers is 25 (excl. the boat fillers). Procedure: 1. Start the UN-/LOAD program after cleaning 2. Let the filler wafers cool down for 5 minutes 3. Load your wafers within 30 minutes 4. Place the monitor wafer in the center of the wafer carrier 5. Always use a full wafer load	Early in tl
59	MFP	**LPCVD of SiRN (50 MPa)** (#film205)	**NL-CLR-G3 FURNACE** Application: deposition of low-stress Silicon Nitride. Program: SIRN04 **RESTRICTION**: maximum thickness is 1.6µm. Settings: • Temperature: 820°C (zone 1), 850°C (zone 2), 870°C (zone 3) • Pressure: 150mTorr • SiH2Cl2 flow: 72sccm • NH3 flow: 22sccm • N2 low: 150sccm	fill 3um t completel 1.2 um

Please mention the following settings in the User Comments:
• Target thickness: ..... nm
• Time: .....min

60 ILP **Particle inspection** (#metro201)

NL-CLR-COLD LIGHT SOURCE (SEM ROOM)

Shine light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a coating from one of the furnaces contains (a lot of) particles!

Contact Christaan Bruinink for questions.

61 ILP **Layer thickness measurement** (#metro401)

NL-CLR-WOOLLAM-2000UI ELLIPSOMETER

Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.

metro1102: SEM inspection

62 ILP **SEM inspection** (#metro103)

NL-CLR-SEM

• JEOL JSM 7610FPlus FEG SEM (cleanroom)

• High resolution SEM LEO (Mark Smithers)

cross sect
inspect if
are filled

etch1772: Directional RIE of Si3N4 or SiRN by CHF3/O2 Plasma (PT790)

63 UCP **Directional RIE of Si3N4 or SiRN** (#etch185)

NL-CLR-PT790
Program: Etch

• Graphite electrode
• CHF3 flow: 25sccm
• O2 flow: 5sccm
• Pressure: 20mTorr
• Power: 350Watt

Mask Olin 907-17: ... nm/min
Si3N4/SiRN: 34 nm/min
Silicon: 32 nm/min
SiO2: 32 nm/min

2400/50 =
FIRST B
= 1h = 2x
SECOND
2x30min
2h per 4 v
cleaning =

64 UCP **Chamber clean (PT790)** (#etch199)

NL-CLR-PT790
Application: removal of organic and fluorocarbon residues from the chamber wall.

• Graphite electrode
• O_2 flow: 100sccm
• Pressure: 100mTorr
• Power: 400Watt

Note: always clean the chamber after etching!

65 ILP **Stripping of Resists** (#strip101)

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

66 Rem Res **Removal of metal traces in RCA-2** (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)

			• Slowly add 300ml* of Hydrogen Peroxide (H_2O_2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.
67	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
68	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
		film1205: LPCVD of low-stress SiRN (G3-50 MPa)	
69	MFP	**System monitoring** (#spc001)	**NL-CLR-FURNACES** Purpose: monitoring the stability of the furnaces in terms of deposition rate, non-uniformity and optical parameters. Procedure: 1. Take a Silicon wafer from the wafer box with monitor wafers 2. Fill in the digital logbook and write down the last 4 digits of the waferID in the User Comment 3. Write down the run number on the lid of the waferbox
70	MFP	**Cleaning in 99% HNO3** (#clean001)	**NL-CLR-WB14 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO_3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!
71	MFP	**Cleaning in 99% HNO3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO_3 • Time: 5min
72	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
73	MFP	**Cleaning in 69% HNO3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO_3 • Temperature: 95°C • Time: 10min
74	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
75	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** **Optional drying step**. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO_2 in 1% HF (WB15). **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.
76	MFP	**Etching in 1% HF** (#etch127)	**NL-CLR-WB15 1% HF BEAKER** Purpose: remove native SiO_2 from Silicon. Chemical: 1% HF • Temperature: room temperature • Time: 1min **Optional etching step. This step is obligatory for the MESA+ monitor wafer.**
77	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates

			Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
78	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	
79	MFP	**Loading of wafers** (#film217)	**NL-CLR-LPCVD FURNACES** Program: UN-/LOAD **RESTRICTION**: the maximum loading capacity of process wafers is 25 (excl. the boat fillers). Procedure: 1. Start the UN-/LOAD program after cleaning 2. Let the filler wafers cool down for 5 minutes 3. Load your wafers within 30 minutes 4. Place the monitor wafer in the center of the wafer carrier 5. Always use a full wafer load	
80	MFP	**LPCVD of SiRN (50 MPa)** (#film205)	**NL-CLR-G3 FURNACE** Application: deposition of low-stress Silicon Nitride. Program: SIRN04 **RESTRICTION**: maximum thickness is 1.6µm. Settings: • Temperature: 820°C (zone 1), 850°C (zone 2), 870°C (zone 3) • Pressure: 150mTorr • SiH2Cl2 flow: 72sccm • NH3 flow: 22sccm • N2 low: 150sccm Please mention the following settings in the User Comments: • Target thickness: ..... nm • Time: .....min	new unifc hardmask
81	ILP	**Particle inspection** (#metro201)	**NL-CLR-COLD LIGHT SOURCE (SEM ROOM)** Shine light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a coating from one of the furnaces contains (a lot of) particles! Contact Christaan Bruinink for questions.	
82	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		metro1102: SEM inspection		
83	ILP	**SEM inspection** (#metro103)	**NL-CLR-SEM** • JEOL JSM 7610FPlus FEG SEM (cleanroom) • High resolution SEM LEO (Mark Smithers)	inspect ne layers
		film1068: Evaporation of Al2O3 (BAK600)		
84	ILP	**Chamber preparation** (#film146)	**NL-CLR-Balzers BAK600** Application: Removal of material from the vacuum chamber walls. Use the vacuum cleaner to scrape off and remove material from the walls and door. Remove the shutter, clean the inside with the vacuum cleaner. Wipe with a dry wipe to remove fine dus (check and repeat if necessary). Remove the copper shield from above the pockets, use a razor blade and the chisel to remove deposits but do not scrape the rim! It will damage the part. Use a dry wipe to remove fine dust.	
85	ILP	**Glow discharge** (#film147)	**NL-CLR-Balzers BAK600** Application: Removal of organic traces through glow discharge in argon or oxygen gas (optional). Settings: • Base pressure: <2x10-6 mbar • Gas: Argon or Oxygen • Current: 0 – 200mA • Time: 0 – 600s • Rotation: on or off depending on next step	
86	ILP	**Evaporation of Al2O3** (#film118)	**NL-CLR-Balzers BAK600** Application: deposition of Aluminium Oxide • Base pressure: < 1e-6 mbar • Beam voltage: - • Beam sweep: - • Emission current: see MIS logbook (indicative!) • Deposition rate: check MIS logbook Material reference (KJ Lesker) • Crucible: Tungsten • Performance: Excellent e-beam performance • Other: Sapphire excellent in E-beam; forms smooth, hard films	100-200n

• MP 2072°C | -°C for 10-6Torr vap. press. | 1550°C for 10-4Torr vap. press.

litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)

Step	Lab	Process	Details	Notes
87	ILP	**HMDS priming** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 HOTPLATE** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Primer: HexaMethylDiSilazane (HMDS) Settings: • Temperature: 150°C • Pressure: 25inHg • Dehydratation bake: 2min • HMDS priming: 5min CAUTION: let the substrates cool down before handling with your tweezer!	
88	ILP	**Coating of Olin OiR 907-17** (#litho101)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 907-17 Spin program: 4000 Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s	
89	ILP	**Prebake of Olin OiR 907-17** (#litho003)	**NL-CLR-WB21 PREBAKE HOTPLATE** Purpose: removal of residual solvent from the resist film after spin coating. Settings: • Temperature: 95°C • Time: 90s	
90	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	**NL-CLR-EV620 AND EVG6200NT MASK ALIGNERS** Settings:(EVG620) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: constant time/…/... • Exposure time: 4sec This exposure time is based on the Hg lamp with a power of 12mW/cm2. Settings:(EVG6200NT) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: UV-LED GHI-line 100 mJ/cm2 • Exposure setting needs to be optimized for optimal result, depending on structures on the mask! This exposure is based on UV-LED light source.	Mask 2: S Vacuum c
91	ILP	**After exposure bake of Olin OiR resists** (#litho005)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 60s	
92	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21 DEVELOPMENT BEAKERS** Developer: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
93	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
94	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	

95	ILP	**Postbake of Olin OiR resists** (#litho008)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 10min	No postba
96	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	

etch1823: Etching of Al2O3 (Oxford Cobra)

97	ILP	**Etching of Al2O3 films** (#etch823)	**NL-CLR-OXFORD PLASMAPRO 100 COBRA** Application: etching of 3-8 µm wide Al2O3 waveguides on t-SiO2 and mask layouts for MicroCoriolis. Status of basic flow: operational Process name: #C-Al2O3 etch @2deg #etch823 Settings: • BCl3 flow: 25sccm • HBr flow: 10sccm • Pressure: 3mTorr • ICP: 1750W • CCP: 20W RF • Table temperature: 2°C • He backside: 10Torr Performance: • Etch rate: 60mm/min and 65nm/min (@25W CCP) • Selectivity: 1.15 (with respect to Olin OiR resists) • Etch uniformity: ±0.7% (at 5mm edge exclusion) • Profile control: 75-80° Results by OS (@80% loading, 4-inch wafer). Ref. document: OIPT reference (PT6677,8,9,6684.1)	AlOx etcl overlegge dikte ??
98	ILP	**Chamber cleaning Cl2/SF6** (#etch820)	**NL-CLR-OXFORD PLASMAPRO 100 COBRA** Application: two-step chamber cleaning to remove etch deposits of materials e.g. Ti, TiO2, Al, AlOx and mask layers using a Cl2/SF6-based plasma (step 1) followed by a 100% SF6 plasma clean (step 2). Process name: #A-Cl2/SF6 clean @20deg #etch820 (2x10min) CAUTION: always load a dummy wafer with 2µm t-SiO2 into clamped systems before plasma etching. Set the backside Helium pressure to zero. Settings (step 1): • Cl2 flow: 40sccm • SF6 flow: 20sccm • Pressure: 10mTorr • ICP: 2500W • CCP: 150W @13.56MHz RF • Table temperature: 20°C • He backside pressure: 0Torr • Time: 10min Settings (step 2): • SF6 flow: 50sccm* • Pressure: 10mTorr • ICP: 2500W • CCP: 150W @13.56MHz RF • Table temperature: 20°C • He backside pressure: 0Torr • Time: 10min * To ignite the SF6 plasma, start with an Argon/SF6 plasma using a flow of 25 sccm for both gases.	
99	ILP	**Stripping of Resists** (#strip100)	**NL-CLR-TePla300** Application: stripping of resists by O2 plasma after plasma etching. **PLEASE NOTE** **1. RESTRICTION**: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041). **2. BACKUP**: TePla300 down? Contact the administrator if you can continue your processing in the TePla360.	skip

Step	O2 (sccm)	N2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	500	1.0	800	0:10:00
Stripping of resist	500	0	1.0	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time.

Program 01: time = 10 min
Program 02: time = 30 min
Program 04: time = 60 min

etch1814: Multilayer + isotropic etching BHT (Oxford Estrelas)

100	ILP	**Multilayer + isotropic etching** (#etch814)	**NL-CLR-Oxford Estrelas** Applications: multistep etching prior to DRIE or channel etching (Bronkhorst) Recipe: #C-Multilayer+Iso @20degC Settings: • Temperature: 20°C • He pressure: 10Torr	#C-Iso et 90mTorr 4000W IC recept res rij slits m etsen in e van 55um dummy te

Step (in order)	Multilayer	Iso (strike)	Iso
Time (sec)	120	1	30
CHF3 flow (sccm)	100	-	-

Ar flow (sccm)	100	-	-
SF6 flow (sccm)	0	800	800
APC (pos/mTorr)	100%	15%	90mTorr
ICP (W)	1500	5000	5000
CCP – RF (W)	150	50	0

101 ILP **Stripping of Resists**
(#strip101)

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

102 Rem Res **Removal of metal traces in RCA-2**
(#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

103 ILP **Rinsing**
(#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

104 ILP **Substrate drying**
(#dry001)

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

metro1102: SEM inspection

105 ILP **SEM inspection**
(#metro103)

NL-CLR-SEM

• JEOL JSM 7610FPlus FEG SEM (cleanroom)

• High resolution SEM LEO (Mark Smithers)

Check ch
dimensio

film1205: LPCVD of low-stress SiRN (G3-50 MPa)

106 MFP **System monitoring**
(#spc001)

NL-CLR-FURNACES
Purpose: monitoring the stability of the furnaces in terms of deposition rate, non-uniformity and optical parameters.

Procedure:
1. Take a Silicon wafer from the wafer box with monitor wafers
2. Fill in the digital logbook and write down the last 4 digits of the waferID in the User Comment
3. Write down the run number on the lid of the waferbox

107 MFP **Cleaning in 99% HNO3**
(#clean001)

NL-CLR-WB14 BEAKER 1
Purpose: removal of organic traces.
Chemical: 99% HNO3

			• Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	
108	MFP	**Cleaning in 99% HNO3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
109	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
110	MFP	**Cleaning in 69% HNO3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO3 • Temperature: 95°C • Time: 10min	
111	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
112	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** **Optional drying step**. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	
113	MFP	**Etching in 1% HF** (#etch127)	**NL-CLR-WB15 1% HF BEAKER** Purpose: remove native SiO2 from Silicon. Chemical: 1% HF • Temperature: room temperature • Time: 1min **Optional etching step. This step is obligatory for the MESA+ monitor wafer.**	
114	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
115	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **NOTE:** load your wafers within 4 hours after cleaning! **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.	process w drying ve overnight
116	MFP	**Loading of wafers** (#film217)	**NL-CLR-LPCVD FURNACES** Program: UN-/LOAD **RESTRICTION**: the maximum loading capacity of process wafers is 25 (excl. the boat fillers). Procedure: 1. Start the UN-/LOAD program after cleaning 2. Let the filler wafers cool down for 5 minutes 3. Load your wafers within 30 minutes 4. Place the monitor wafer in the center of the wafer carrier 5. Always use a full wafer load	Early in tl
117	MFP	**LPCVD of SiRN (50 MPa)** (#film205)	**NL-CLR-G3 FURNACE** Application: deposition of low-stress Silicon Nitride. Program: SIRN04 **RESTRICTION**: maximum thickness is 1.6μm. Settings: • Temperature: 820°C (zone 1), 850°C (zone 2), 870°C (zone 3)	regrow sl channel w

• Pressure: 150mTorr
• SiH2Cl2 flow: 72sccm
• NH3 flow: 22sccm
• N2 low: 150sccm

Please mention the following settings in the User Comments:
• Target thickness: ..... nm
• Time: .....min

118 ILP **Particle inspection** (#metro201)

NL-CLR-COLD LIGHT SOURCE (SEM ROOM)

Shine light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a coating from one of the furnaces contains (a lot of) particles!

Contact Christaan Bruinink for questions.

119 ILP **Layer thickness measurement** (#metro401)

NL-CLR-WOOLLAM-2000UI ELLIPSOMETER

Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.

litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)

120 ILP **HMDS priming** (#litho600)

OPTION 1 Liquid HMDS priming

NL-CLR-WB21/22 HOTPLATE
Purpose: dehydration bake

Settings:
• Temperature: 120°C
• Time: 5min

After the dehydration bake, perform the liquid priming with minimum delay!

NL-CLR-WB21 Primus SB15 Spinner
Primer: HexaMethylDiSilazane (HMDS)

Settings:
• Spin mode: static
• Spin speed: 4000rmp
• Spin time: 30s

OPTION 2 Vapor HMDS priming

NL-CLR-WB28 Lab-line Duo-Vac Oven
Primer: HexaMethylDiSilazane (HMDS)

Settings:
• Temperature: 150°C
• Pressure: 25inHg
• Dehydratation bake: 2min
• HMDS priming: 5min

CAUTION: let the substrates cool down before handling with your tweezer!

121 ILP **Coating of Olin OiR 907-17** (#litho101)

NL-CLR-WB21 PRIMUS SB15 SPINNER
Resist: Olin OiR 907-17
Spin program: 4000

Settings:
• Spin mode: static
• Spin speed: 4000rpm
• Spin time: 30s

Olin 35 a

122 ILP **Prebake of Olin OiR 907-17** (#litho003)

NL-CLR-WB21 PREBAKE HOTPLATE
Purpose: removal of residual solvent from the resist film after spin coating.

Settings:
• Temperature: 95°C
• Time: 90s

123 ILP **Alignment & exposure of Olin OiR 907-17** (#litho301)

NL-CLR-EV620 AND EVG6200NT MASK ALIGNERS

Settings:(EVG620)
• Separation: 50µm
• Contact mode: proximity/soft contact/hard contact/vacuum contact
• Exposure mode: constant time/…/...
• Exposure time: 4sec

This exposure time is based on the Hg lamp with a power of 12mW/cm2.

Settings:(EVG6200NT)
• Separation: 50µm
• Contact mode: proximity/soft contact/hard contact/vacuum contact
• Exposure mode: UV-LED GHI-line 100 mJ/cm2
• Exposure setting needs to be optimized for optimal result, depending on structures on the mask!

This exposure is based on UV-LED light source.

Mask 3: h
contacts
+ front re
vacuum c

124 ILP **After exposure bake of Olin OiR resists** (#litho005)

NL-CLR-WB21 POSTBAKE HOTPLATE
Purpose:

Settings:
• Temperature: 120°C
• Time: 60s

125 ILP **Development of Olin OiR resists** (#litho200)

NL-CLR-WB21 DEVELOPMENT BEAKERS
Developer: OPD4262

• Beaker 1: 30sec
• Beaker 2: 15-30sec

126 ILP **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

127 ILP **Substrate drying** (#dry001)

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

128 ILP **Postbake of Olin OiR resists** (#litho008)

NL-CLR-WB21 POSTBAKE HOTPLATE
Purpose:

Settings:
• Temperature: 120°C
• Time: 10min

no postba

129 ILP **Inspection by Optical Microscopy** (#metro101)

NL-CLR-Nikon Microscope

Use the Nikon microscope for inspection.

etch1771: Directional RIE of SiRN by CHF3/O2 Plasma (PT790)

130 UCP **Etching of SiRN** (#etch223)

NL-CLR-PT790
Application: directional etching of thin layers of SiRN.

Settings:
CHF_3 flow: 100 sccm
O_2 flow: 12 sccm
Pressure: 40 mTorr
Power 250W

Etch rate: Si3N4: 40 nm/min, SiO2: 32 nm/min, SiRN: 42nm/min

opening f
+ contacts

1.6um+5(
= 42min f
200% = 8
min clean
= 2h per 4
8 wafers =

131 UCP **Chamber clean (PT790)** (#etch199)

NL-CLR-PT790
Application: removal of organic and fluorocarbon residues from the chamber wall.

• Graphite electrode
• O_2 flow: 100sccm
• Pressure: 100mTorr
• Power: 400Watt

Note: always clean the chamber after etching!

132 ILP **Stripping of Resists** (#strip101)

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

1h-r04 fo
r16 for te

133 Rem Res **Removal of metal traces in RCA-2** (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)

skip

• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

134 ILP **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

skip

135 ILP **Substrate drying** (#dry001)

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

skip

clean1002: In-line cleaning (WB16-ILP)

136 ILP **Cleaning in 99% HNO3** (#clean005)

NL-CLR-WB16 BEAKER 1
Purpose: removal of organic traces.
Chemical: 99% HNO3

• Time: 5min

NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!

137 ILP **Cleaning in 99% HNO3** (#clean006)

NL-CLR-WB16 BEAKER 2
Purpose: removal of organic traces.
Chemical: 99% HNO3

• Time: 5min

v-HF %?

138 ILP **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

139 ILP **Substrate drying** (#dry001)

NL-CLR-WBs (ILP)

Single substrate drying:
1. Use the single-wafer spinner
   Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

film1635: Sputtering of Platinum (TCOathy)

140 ILP **Sample preparation** (#film631)

NL-CLR-T´COathy
Purpose: reduce outgassing and pump time.

- Use a dehydration bake (120°C, 5 mins) in WB22 after wet processing.
- Use only Kapton tape for fixing samples on a carrier wafer or a shadow mask* on a process wafer.

*TCO is the preferred supplier of shadow masks.

5nm pt

141 ILP **Sputter rate verification** (#film632)

NL-CLR-T´COathy
Purpose: optional step to determine the sputter rate with the Woollam Ellipsometer. One material per monitor wafer!

Use the standard process parameters underneath or calibrate according to the process parameters when using other pressure / power settings.

Layer	Target	Power (W)	Pre-time	Proc-time	P (x10-3) mbar
1	Au	200	1:00	0:30	6.6
1	Pt	200	1:00	1:00	6.6
1	Cr	200	1:00	2:00	6.6
1	Ta	200	1:00	2:00	6.6
1	Ti	200	1:00	2:00	6.6

• Follow calibration instructions in the equipment manual!

142 ILP **Sputtering of Pt** (#film637)

NL-CLR-T´COathy
Application: deposition of Platinum

• Base pressure: <1.0E-6 mbar

Layer	Target	Power (W)	Pre-time	Proc-time	P (x10-3) mbar
	Pt	200	0:30	…	6.6

• Estimated deposition rate ~ 20 nm/min

bond1103: Wafer bonding silicon-glass with Pt structures (B3)

143 ILP **Cleaning in 99% HNO3** (#clean005)

NL-CLR-WB16 BEAKER 1
Purpose: removal of organic traces.
Chemical: 99% HNO3

skip

			• Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	
144	ILP	**Cleaning in 99% HNO3** (#clean006)	**NL-CLR-WB16 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	skip
145	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	skip
146	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	skip
147	ILP	**Wafer bonding** (#bond128)	**NL-CLR-E2 FURNACE** Application: silicon-glass bonding with Pt structures. Programs: ANOX900, ANOX950, ANOX1000 Settings: • Use the horizontal wafer boat for this process. • Standby temperature: 400°C • Temperature range: 900-1000°C • N2 flow: 4slm* • Ramp: 10°C/min Please mention the following setting in the User Comments: • Program: ….. • Time: .....min * Check that the time for O2 is set to 0:00:00.	Thermal a deg C

film1683: Sputtering of Ta/Pt conductor (TCOathy)

148	ILP	**Sample preparation** (#film631)	**NL-CLR-T´COathy** Purpose: reduce outgassing and pump time. - Use a dehydration bake (120°C, 5 mins) in WB22 after wet processing. - Use only Kapton tape for fixing samples on a carrier wafer or a shadow mask* on a process wafer. *TCO is the preferred supplier of shadow masks.	
149	ILP	**Sputter rate verification** (#film632)	**NL-CLR-T´COathy** Purpose: optional step to determine the sputter rate with the Woollam Ellipsometer. One material per monitor wafer! Use the standard process parameters underneath or calibrate according to the process parameters when using other pressure / power settings. (see table below) • Follow calibration instructions in the equipment manual!	

Layer	Target	Power (W)	Pre-time	Proc-time	P (x10-3) mbar
1	Au	200	1:00	0:30	6.6
1	Pt	200	1:00	1:00	6.6
1	Cr	200	1:00	2:00	6.6
1	Ta	200	1:00	2:00	6.6
1	Ti	200	1:00	2:00	6.6

150	ILP	**Sputtering of Ta/Pt conductor** (#film698)	**NL-CLR-T´COathy** Application: deposition of a Ta/Pt conductor for high temperature applications • Base pressure: <8.0E-7 mbar Program subsequent layers in the T'COathy program: (see table below) Typical thickness: Ta: 5-10nm Pt: 200nm	10nm Ta Don´t bre

Layer	Target	Power (W)	Pre-time	Proc-time	P (x10-3) mbar
1	Ta	200	1:00	0:45	6.6
2	Pt	200	0:30	10:00	6.6

film1403: PECVD of low-stress SiN (Oxford80)

151	ILP	**Cleaning in 99% HNO3** (#clean005)	**NL-CLR-WB16 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	
152	ILP	**Cleaning in 99% HNO3** (#clean006)	**NL-CLR-WB16 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3	

			• Time: 5min	
153	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
154	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
155	ILP	**PECVD of low-stress SiN** (#film403)	**NL-CLR-OXFORD PLASMALAB80+** Application: Program: Low-stress SiN Settings: • Electrode temperature: 300°C • Pressure: 650mTorr • Power: 20W (7s LF/13s HF) • 2% SiH4/N2 flow: 1000sccm • NH3 flow: 20sccm • Deposition rate= 12nm/min • Stress: 90MPa (tensile) Note: Apply purge sequence before and after use Purge sequence: 1 min N2, pump down, apply three times. Please mention the following settings in the User Comments: • Target thickness: ..... nm • Time: .....min	30 nm pr -> moet d IBE
156	ILP	**Chamber Clean** (#film400)	**NL-CLR-OXFORD PLASMALAB80+** Cleaning the chamber is compulsory in the following cases: - after deposition of PECVD SiN - after a total deposition of 15-20µm of PECVD SiO2 Run the following programs in sequence: **1. Program: Oxford Clean** Settings: Temperature: 300°C Pressure: 1400mTorr Power: 150Watt (LF) + 300Watt (HF) CF4/O2 flow: 100sccm **2. Program: Final Clean** Settings: Temperature: 300°C Pressure: 550mTorr Power: 50Watt (LF) + 150Watt (HF) CF4/O2 flow: 150sccm	
157	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
158	ILP	**Particle inspection** (#metro201)	**NL-CLR-COLD LIGHT SOURCE (SEM ROOM)** Shine light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a coating from one of the furnaces contains (a lot of) particles! Contact Christaan Bruinink for questions.	
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
159	ILP	**HMDS priming** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 HOTPLATE** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming**	

#	Module	Step	Equipment / Instructions	Comments
			NL-CLR-WB28 Lab-line Duo-Vac Oven Primer: HexaMethylDiSilazane (HMDS) Settings: • Temperature: 150°C • Pressure: 25inHg • Dehydratation bake: 2min • HMDS priming: 5min CAUTION: let the substrates cool down before handling with your tweezer!	
160	ILP	**Coating of Olin OiR 907-17** (#litho101)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 907-17 Spin program: 4000 Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s	
161	ILP	**Prebake of Olin OiR 907-17** (#litho003)	**NL-CLR-WB21 PREBAKE HOTPLATE** Purpose: removal of residual solvent from the resist film after spin coating. Settings: • Temperature: 95°C • Time: 90s	
162	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	**NL-CLR-EV620 AND EVG6200NT MASK ALIGNERS** Settings:(EVG620) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: constant time/…/... • Exposure time: 4sec This exposure time is based on the Hg lamp with a power of 12mW/cm2. Settings:(EVG6200NT) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: UV-LED GHI-line 100 mJ/cm2 • Exposure setting needs to be optimized for optimal result, depending on structures on the mask! This exposure is based on UV-LED light source.	Mask 4: s heater co hard cont
163	ILP	**After exposure bake of Olin OiR resists** (#litho005)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 60s	
164	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21 DEVELOPMENT BEAKERS** Developer: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
165	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
166	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
167	ILP	**Postbake of Olin OiR resists** (#litho008)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 10min	10m @ 1 voor beet om reflow gaan.
168	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
169				Cobra Et Ta(10nm) (500nm)

film1403: PECVD of low-stress SiN (Oxford80)

#	Module	Step	Equipment / Instructions	Comments
170	ILP	**Cleaning in 99% HNO3** (#clean005)	**NL-CLR-WB16 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	
171	ILP			

		Cleaning in 99% HNO3 (#clean006)	**NL-CLR-WB16 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
172	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
173	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
174	ILP	**PECVD of low-stress SiN** (#film403)	**NL-CLR-OXFORD PLASMALAB80+** Application: Program: Low-stress SiN Settings: • Electrode temperature: 300°C • Pressure: 650mTorr • Power: 20W (7s LF/13s HF) • 2% SiH4/N2 flow: 1000sccm • NH3 flow: 20sccm • Deposition rate= 12nm/min • Stress: 90MPa (tensile) Note: Apply purge sequence before and after use Purge sequence: 1 min N2, pump down, apply three times. Please mention the following settings in the User Comments: • Target thickness: ..... nm • Time: .....min	70 nm fin layer
175	ILP	**Chamber Clean** (#film400)	**NL-CLR-OXFORD PLASMALAB80+** Cleaning the chamber is compulsory in the following cases: - after deposition of PECVD SiN - after a total deposition of 15-20µm of PECVD SiO2 Run the following programs in sequence: **1. Program: Oxford Clean** Settings: Temperature: 300°C Pressure: 1400mTorr Power: 150Watt (LF) + 300Watt (HF) CF4/O2 flow: 100sccm **2. Program: Final Clean** Settings: Temperature: 300°C Pressure: 550mTorr Power: 50Watt (LF) + 150Watt (HF) CF4/O2 flow: 150sccm	
176	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
177	ILP	**Particle inspection** (#metro201)	**NL-CLR-COLD LIGHT SOURCE (SEM ROOM)** Shine light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a coating from one of the furnaces contains (a lot of) particles! Contact Christaan Bruinink for questions.	
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
178	ILP	**HMDS priming** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 HOTPLATE** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp	

#	Lab	Step	Equipment / Settings	Comments
			• Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Primer: HexaMethylDiSilazane (HMDS) Settings: • Temperature: 150°C • Pressure: 25inHg • Dehydratation bake: 2min • HMDS priming: 5min CAUTION: let the substrates cool down before handling with your tweezer!	
179	ILP	**Coating of Olin OiR 907-17** (#litho101)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 907-17 Spin program: 4000 Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s	
180	ILP	**Prebake of Olin OiR 907-17** (#litho003)	**NL-CLR-WB21 PREBAKE HOTPLATE** Purpose: removal of residual solvent from the resist film after spin coating. Settings: • Temperature: 95°C • Time: 90s	
181	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	**NL-CLR-EV620 AND EVG6200NT MASK ALIGNERS** Settings:(EVG620) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: constant time/…/... • Exposure time: 4sec This exposure time is based on the Hg lamp with a power of 12mW/cm2. Settings:(EVG6200NT) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: UV-LED GHI-line 100 mJ/cm2 • Exposure setting needs to be optimized for optimal result, depending on structures on the mask! This exposure is based on UV-LED light source.	Mask 5 L bond pad front rele windows Front side hardconta
182	ILP	**After exposure bake of Olin OiR resists** (#litho005)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 60s	
183	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21 DEVELOPMENT BEAKERS** Developer: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
184	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
185	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
186	ILP	**Postbake of Olin OiR resists** (#litho008)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 10min	
187	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
		therm1102: Densification of PECVD Oxford 80 capping on Ta/Pt electrodes (B3)		
188	ILP	**Cleaning in 99% HNO3** (#clean005)	**NL-CLR-WB16 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	
189	ILP	**Cleaning in 99% HNO3**	**NL-CLR-WB16 BEAKER 2**	

Step	Lab	Process	Description	Comments
		(#clean006)	Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
190	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
191	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
192	ILP	**Densification of PECVD coatings** (#therm139)	**NL-CLR-E2 FURNACE** Application: densification of PECVD capping on Ta/Pt electrodes. Program: ANOX950 Settings: • Standby temperature: 400°C • Temperature: 950°C • N2 flow: 4slm* • Ramp: 10°C/min Please mention the following setting in the User Comments: • Time: .....min * Check that the time for O2 is set to 0:00:00.	Anneal 4ε degree C
193				Cobra Etc in 100nm capping la
		clean1002: In-line cleaning (WB16-ILP)		
194	ILP	**Cleaning in 99% HNO3** (#clean005)	**NL-CLR-WB16 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min NOTE: only dry wafers are allowed to enter this beaker in order to prevent dilution of the 99% HNO3!	
195	ILP	**Cleaning in 99% HNO3** (#clean006)	**NL-CLR-WB16 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
196	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
197	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
		litho1801: Lithography of Olin Oir 907-17 (positive resist - ILP)		
198	ILP	**HMDS priming** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 HOTPLATE** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner** Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Primer: HexaMethylDiSilazane (HMDS) Settings: • Temperature: 150°C	

			• Pressure: 25inHg • Dehydratation bake: 2min • HMDS priming: 5min CAUTION: let the substrates cool down before handling with your tweezer!	
199	ILP	**Coating of Olin OiR 907-17** (#litho101)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 907-17 Spin program: 4000 Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s	COAT BC SIDES: First Fron protectior second ba mask
200	ILP	**Prebake of Olin OiR 907-17** (#litho003)	**NL-CLR-WB21 PREBAKE HOTPLATE** Purpose: removal of residual solvent from the resist film after spin coating. Settings: • Temperature: 95°C • Time: 90s	
201	ILP	**Alignment & exposure of Olin OiR 907-17** (#litho301)	**NL-CLR-EV620 AND EVG6200NT MASK ALIGNERS** Settings:(EVG620) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: constant time/…/... • Exposure time: 4sec This exposure time is based on the Hg lamp with a power of 12mW/cm2. Settings:(EVG6200NT) • Separation: 50µm • Contact mode: proximity/soft contact/hard contact/vacuum contact • Exposure mode: UV-LED GHI-line 100 mJ/cm2 • Exposure setting needs to be optimized for optimal result, depending on structures on the mask! This exposure is based on UV-LED light source.	Mask 6: I Release + channel Backside hard conta
202	ILP	**After exposure bake of Olin OiR resists** (#litho005)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 60s	
203	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21 DEVELOPMENT BEAKERS** Developer: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
204	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
205	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
206	ILP	**Postbake of Olin OiR resists** (#litho008)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 10min	
207	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.	
		etch1771: Directional RIE of SiRN by CHF3/O2 Plasma (PT790)		
208	UCP	**Etching of SiRN** (#etch223)	**NL-CLR-PT790** Application: directional etching of thin layers of SiRN. Settings: CHF_3 flow: 100 sccm O_2 flow: 12 sccm Pressure: 40 mTorr Power 250W Etch rate: Si3N4: 40 nm/min, SiO2: 32 nm/min, SiRN: 42nm/min	1.6um+5(SiRN + 100nm = 2200/5(for 100% 130% = 5 wafers, 8 wafers = + 45 min = 2h 39m
209	UCP	**Chamber clean (PT790)** (#etch199)	**NL-CLR-PT790** Application: removal of organic and fluorocarbon residues from the chamber wall. • Graphite electrode • O_2 flow: 100sccm • Pressure: 100mTorr	

• Power: 400Watt

Note: always clean the chamber after etching!

210 ILP **Stripping of Resists** (#strip101)

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

tepla300

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

211 Rem Res **Removal of metal traces in RCA-2** (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

skip

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.

212 ILP **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

skip

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

213 ILP **Substrate drying** (#dry001)

NL-CLR-WBs (ILP)

skip

Single substrate drying:
1. Use the single-wafer spinner
Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge)
2. Use the nitrogen gun (fragile wafers or small samples)

etch1001: KOH etch - standard (WB17) with RCA-2 post cleaning (WB09)

214 ILP **Etching in 1% HF** (#etch192)

NL-CLR-WB16 1%HF BEAKER
Purpose:
Chemical: 1% HF

• Temperature: 20 °C
• Time: depends on application

215 ILP **Rinsing** (#rinse001)

NL-CLR-WBs QDR
Purpose: removal of traces of chemical agents.

Choose one of the two rinsing modes:
QDR = Quick dump rinsing mode
Cascade = Overflow rinsing mode for fragile substrates

Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.

216 ILP **Silicon etching in KOH** (#etch138)

NL-CLR-WB17 Beaker KOH-1 or KOH-2
Chemical: 25wt.% KOH

525 minu
45m

Application: anisotropic etching of crystalline silicon.

Settings:
• Temperature: 75°C
• Use stirrer

Step	Type	Process	Details	
			Etch rates: Si <100> = 1µm/min Si <111> = 12.5nm/min SiO2 (thermal) = 180nm/hr SiRN < 0.6nm/hr	
217	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
218	ILP	**Substrate transport in demi-water** (#trans003)	**NL-CLR-WB17 > WB09** Purpose: transport of wafers for cleaning in RCA-2 after etching in KOH (WB17). Wet transport of substrates in a beaker with demi-water. After transport, return the quartz wafer carrier back to WB17.	skip
219	Rem Res	**Removal of residues in RCA-2** (#residue501)	**NL-CLR-WB09** Purpose: removal of residues after wet-chemical processing (e.g. KOH and metal stripping) in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue: • cleaning in the Pre-Furnace Clean (WB14-MFP) • processing in the Ultra-Clean Line - Front End (WB12-UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) . Chemicals: HCl:H_2O_2:H_2O (1:1:5 vol%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	skip
220	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	skip
221	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	

C | Flow calculations

Flow calculation chip-based

Henk-Willem Veltkamp

Introduction

In the microfluidic channel, we would like to apply two flows:

1) A pure air flow
2) A mixture of air and methane with 5% excess air with regard to stoichiometric combustion

The mass-flows of both flows should result in an equal amount of power required to heat up the flow to 600°C:

Power to heat up air flow = power to heat up mixture flow

For dry air, only the four major components in the following ratios are taken into account:

Component	Percentage	Fraction
N_2	78.0840	0.780840
O_2	20.9476	0.209476
Ar	0.93650	0.009365
CO_2	0.03190	0.000319
Total:	**100**	**1**

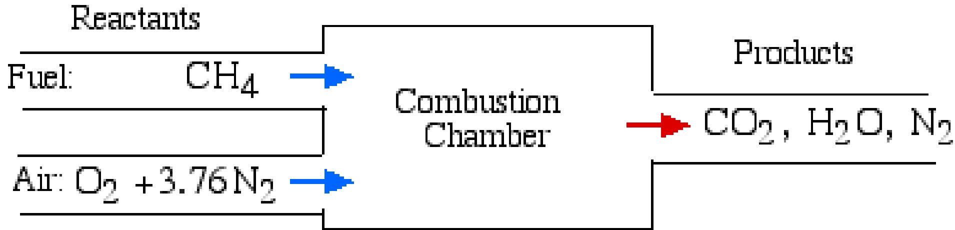
Besides this, we also need the atomic or molecular weights:

- Methane: 16.04246 g mol^{-1}
- Air: 28.8503972 g mol^{-1}

Stoichiometric combustion

For simplicity, air is considered as a mixture that contains 79% N_2 and 21% O_2 only. Other components are neglected. Normalizing this for oxygen gives:

$$0.21O_2 + 0.79N_2 = 0.21(O_2 + 3.76N_2)$$



The stoichiometric combustion of methane with air results in the following overall chemical reaction:

$$CH_4 + a * (O_2 + 3.76N_2) \rightarrow b * CO_2 + c * H_2O + d * N_2 \cancel{+ e * O_2} + heat$$

Where a is known as the stoichiometric coefficient for the oxidizer (air). Stoichiometric combustion assumes that no excess oxygen exists in the products, thus e = 0. We obtain the other four equations from balancing the number of atoms of each element in the reactants (carbon, hydrogen, oxygen and

nitrogen) with the number of atoms of those elements in the products. This means that no atoms are destroyed or lost in a combustion reaction.

Atom	Amount in reactants	=	Amount in products	Reduced equation
H_2	4	=	$2c$	$4 = 2c$
O_2	$2a$	=	$2b + c$	$a = b + c/2$
C	1	=	b	$b = 1$
N_2	$2(3.76)a$	=	$2d$	$d = 3.76a$

Making:

$$CH_4 + 2(O_2 + 3.76N_2) \rightarrow CO_2 + 2H_2O + 7.52N_2 + heat$$

For theoretical stoichiometric combustion (complete combustion) of fuel we can calculate the required air by using the equation of stoichiometry of the oxygen/fuel reaction, the air/fuel ratio (AFR):

$$AFR = \frac{air\ mass\ flow\ [\mathrm{kg\ s^{-1}}]}{fuel\ mass\ flow\ [\mathrm{kg\ s^{-1}}]}$$

Besides the AFR, we also have the $\overline{AFR}$, the ratio on molar basis:

$$\overline{AFR} = \frac{moles\ of\ air\ [moles]}{moles\ of\ fuel\ [moles]}$$

The relate to each other via the molecular weights (M):

$$AFR = \overline{AFR}\frac{M_{air}\ [\mathrm{g\ mol^{-1}}]}{M_{fuel}\ [\mathrm{g\ mol^{-1}}]} = \overline{AFR}\frac{28.8503972}{16.04246} = \overline{AFR} * 1.798377$$

The theoretical/stoichiometric AFR is:

$$AFR = \frac{moles\ of\ air\ [moles]}{moles\ of\ fuel\ [moles]} * \frac{M_{air}\ [\mathrm{g\ mol^{-1}}]}{M_{fuel}\ [\mathrm{g\ mol^{-1}}]} = \frac{2(1 + 3.76)}{1} * \frac{28.8503972}{16.04246} = 17.12055$$

So, for every mass quantity of fuel (CH_4) a total of 17.12055 mass quantities of air are required to achieve stoichiometric combustion.

Excess air

Actual combustion also depends on the assumed air excess, based on the stoichiometry ratio:

$$\lambda = \frac{actual\ air}{stoichiometric\ air}$$

Or similarly, the equivalence ratio, in which the subscripts S is for stoichiometric and A is for actual:

$$\phi = \frac{(moles\ of\ air/moles\ of\ fuel)_S}{moles\ of\ air/moles\ of\ fuel} = \frac{AFR_S}{AFR_A} = \frac{1}{\lambda}$$

Based on these two parameters, the following summary can be made:

Type of flame/type of mixture

Rich	Stoichiometric	Lean
$\lambda < 1$	$\lambda = 1$	$\lambda > 1$
$\phi > 1$	$\phi = 1$	$\phi < 1$

To prevent soot forming, an excess of air is required, meaning a rich mixture. The air excess becomes:

$$\% \; of \; theoretical \; air = \frac{100\%}{\phi} = \lambda * 100\%$$

And:

$$\% \; of \; excess \; air = \frac{1-\phi}{\phi} * 100\% = (\lambda - 1) * 100\%$$

For combustion we assume an AFR with a 10% excess of air. The overall equation for combustion:

$$CH_4 + a * (O_2 + 3.76N_2) \rightarrow b * CO_2 + c * H_2O + d * N_2 \cancel{+ e * O_2} + heat$$

Becomes:

$$CH_4 + \mathbf{1.1} * 2(O_2 + 3.76N_2) \rightarrow CO_2 + 2H_2O + \mathbf{7.9 N_2} + \mathbf{0.1 O_2} + heat$$

With the following air excess:

$$\% \; of \; excess \; air = 1 = (\lambda - 1) * 100\% \Longrightarrow \lambda = 1.1$$

And:

$$\% \; of \; theoretical \; air = \frac{100\%}{\phi} = 1.1 * 100\% = 110\% \Longrightarrow \phi = 0.9091$$

With its AFR:

$$AFR = \frac{moles \; of \; air \; [moles]}{moles \; of \; fuel \; [moles]} * \frac{M_{air} \; [\mathrm{g \; mol^{-1}}]}{M_{fuel} \; [\mathrm{g \; mol^{-1}}]} = \frac{1.1 * 2(1 + 3.76)}{1} * \frac{28.8503972}{16.04246} = 18.83261$$

Summarizing, this would give the following ratios for stoichiometric combustion and combustion with an excess of air:

Type	Air [M t^{-1}]	Fuel [M t^{-1}]	Air [%]	Fuel [%]
Stoichiometric	17.12055	1.0	94.48	5.52
Excess (10%)	18.83261	1.0	94.96	5.04

These values can represent any flow, kg h^{-1}, mg s^{-1}, etc. As long as the units are the same for both flows. Therefore, they are denoted with mass per time (M t^{-1}). The corresponding percentages are also given.

Now we know the ratio of the required flow. The next step is to calculate the corresponding pure air flow.

For this, two methods are compared. The first one uses the equation:

$$P = \dot{m} C_p \Delta T$$

In which, P is the power in W, $\dot{m}$ is the mass flow in g s^{-1}, C_p is the heat capacity at constant pressure in J $mole^{-1}$ K^{-1} or kJ $kmole^{-1}$ K^{-1}, and ΔT is the required temperature increase in K.

The second method only compares the C_p of both flows.

Method 1

We use:

$$P = \dot{m}C_p\Delta T$$

However, this equation assumes that C_p is constant over the temperature increase. This is only possible when small temperature increases are used. For large temperature differences, the equation is modified by using the mean heat capacity at constant pressure:

$$P = \dot{m}\frac{\int_{T_1}^{T_2} C_p dT}{T}$$

As equation for C_p we use the NASA 7-term polynomial [B. J. McBride, S. Gordon, M.A. Reno. "Coefficients for calculating thermodynamic and transport properties of individual species" NASA Technical Memorandum 4513, 1993]:

$$C_p = R(a_1 + a_2T + a_3T^2 + a_4T^3 + a_5T^4)$$

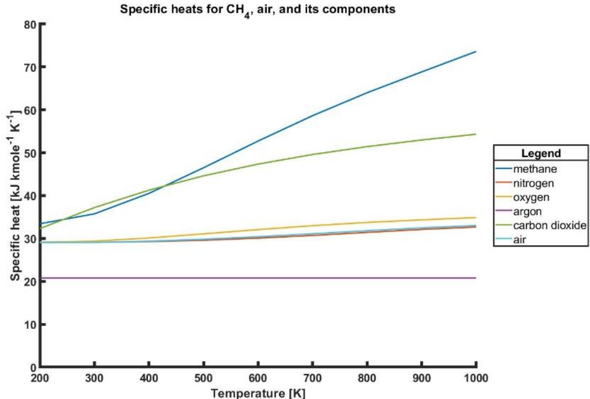
In which, R is the universal gas constant (8.31446261815324 J mole^{-1} K^{-1}), a_i are specie-specific coefficients. For the NASA 7-term polynomials, these are:

Coefficient	T range [K]	CH_4	N_2	O_2	Ar	CO_2
a_1	200-1000	5.14987613E+00	3.53100528E+00	3.78245636E+00	2.50000000E+00	2.35677352E+00
	1000-6000	1.63552643E+00	2.95257626E+00	3.66096083E+00	2.50000000E+00	4.63659493E+00
a_2	200-1000	-1.36709788E-02	-1.23660987E-04	-2.99673415E-03	0.00000000E+00	8.98459677E-03
	1000-6000	1.00842795E-02	1.39690057E-03	6.56365523E-04	0.00000000E+00	2.74131991E-03
a_3	200-1000	4.91800599E-05	-5.02999437E-07	9.84730200E-06	0.00000000E+00	-7.12356269E-06
	1000-6000	-3.36916254E-06	-4.92631691E-07	-1.41149485E-07	0.00000000E+00	-9.95828531E-07
a_4	200-1000	-4.84743026E-08	2.43530612E-09	-9.68129508E-09	0.00000000E+00	2.45919022E-09
	1000-6000	5.34958667E-10	7.86010367E-11	2.05797658E-11	0.00000000E+00	1.60373011E-10
a_5	200-1000	1.66693956E-11	-1.40881235E-12	3.24372836E-12	0.00000000E+00	-1.43699548E-13
	1000-6000	-3.15518833E-14	-4.60755321E-15	-1.29913248E-15	0.00000000E+00	-9.16103468E-15

For air, the C_p can be calculated based on the fractions (f_i) and their corresponding C_p:

$$C_{p,air} = f_{N_2}C_{p,N_2} + f_{O_2}C_{p,O_2} + f_{Ar}C_{p,Ar} + f_{CO_2}C_{p,CO_2}$$

For the different species, the following C_p graphs apply:



The same applies for the two mixtures (stoichiometric and excess air mixture):

$$C_{p,St} = f_{air}C_{p,air} + f_{CH_4}C_{p,CH_4} = 0.9448 * C_{p,air} + 0.0552 * C_{p,CH_4}$$

$$C_{p,Ex} = f_{air}C_{p,air} + f_{CH_4}C_{p,CH_4} = 0.9473 * C_{p,air} + 0.0527 * C_{p,CH_4}$$

To calculate the C_p in kJ kg^{-1} K^{-1} the C_p has to be divided by the molecular weight:

$$C_{p,St,kg} = \frac{C_{p,St,mole}}{MW_{St}} \qquad C_{p,Ex,kg} = \frac{C_{p,Ex,mole}}{MW_{Ex}} \qquad C_{p,air,kg} = \frac{C_{p,air,mole}}{MW_{air}}$$

Where the molecular weights of the mixtures are based on their fractions:

$$MW_{St} = 0.9448 * MW_{air} + 0.0552 * MW_{CH_4} = 0.9448 * 28.8503972 + 0.0552 * 16.04246 = 28.14339906656$$

$$MW_{Ex} = 0.9496 * MW_{air} + 0.0504 * MW_{CH_4} = 0.9496 * 28.8503972 + 0.0504 * 16.04246 = 28.20487716512$$

For convenience we use a mass flow of 20 mg h^{-1} of methane.

Using the ratios, this will give the following mass flows:

Mixture	**Mass flow CH_4**	**Mass flow air**	**Mass flow total**
Stoichiometric	20 mg h^{-1}	342.32 mg h^{-1}	362.32 mg h^{-1}
10% excess	20 mg h^{-1}	376.83 mg h^{-1}	396.83 mg h^{-1}

Both mass-flows are roughly in the middle of their mass-flow controller range.

Now, using:

$$P = \dot{m}\frac{\int_{T_1}^{T_2} C_p dT}{\Delta T}$$

We get:

$$P = \dot{m}\left(\frac{R\int_{T_1}^{T_2}(a_1 + a_2T + a_3T^2 + a_4T^3 + a_5T^4)dT}{\Delta T}\right) = \dot{m}\left(\frac{R\left(a_1(T_2 - T_1) + \frac{a_2(T_2^2 - T_1^2)}{2} + \frac{a_3(T_2^3 - T_1^3)}{3} + \frac{a_4(T_2^4 - T_1^4)}{4} + \frac{a_5(T_2^5 - T_1^5)}{5}\right)}{\Delta T}\right)$$

More specific, for the mixtures:

$$P_{mixture} = \dot{m}\frac{\int_{T_1}^{T_2} C_{p,mixture}dT}{\Delta T} = \dot{m}\frac{\int_{T_1}^{T_2}\left(f_{air}C_{p,air} + f_{CH_4}C_{p,CH_4}\right)dT}{\Delta T}$$

With:

$$C_{p,air} = f_{N_2}C_{p,N_2} + f_{O_2}C_{p,O_2} + f_{Ar}C_{p,Ar} + f_{CO_2}C_{p,CO_2}$$

We would like to increase the temperature from 293.15 K to 893.15 K (ΔT of 600 K).

Here we use that the integral of sums is the sums of integrals. For only N_2 this would become:

$$\frac{\int_{293.15}^{893.15} f_{N_2} C_{p,N_2} dT}{\Delta T} = \frac{f_{N_2} R \left(a_1(T_2 - T_1) + \frac{a_2(T_2^2 - T_1^2)}{2} + \frac{a_3(T_2^3 - T_1^3)}{3} + \frac{a_4(T_2^4 - T_1^4)}{4} + \frac{a_5(T_2^5 - T_1^5)}{5} \right)}{\Delta T} \approx 14171.044$$

Putting this in WolframAlpha can be done by using:

0.78084 * 8.31446261815324 * (3.53100528E+00 (893.15-293.15)+(-1.23660987E-04 (893.15^2-293.15^2))/2+(-5.02999437E-07 (893.15^3-293.15^3))/3+(2.43530612E-09(893.15^4-293.15^4))/4+(-1.40881235E-12 (893.15^5-293.15^5))/5)

The rest of the integration is done using MATLAB and results in the following C_p values:

Gas	**C_p [kJ kmole^{-1} K^{-1}]**	**$C_{p,kg}$ [kJ kg^{-1} K^{-1}]**
Stoichiometric	40.2228	1.4292
10% Excess	40.2269	1.4262
Air	36.0056	1.2480

These values are slightly different from earlier values, as the integral is taken instead of a linear C_p.

Now we plug in these values into

$$P = \frac{\dot{m}}{1000 * 3600} \frac{\int_{T_1}^{T_2} C_p dT}{\Delta T}$$

Assuming a ΔT of 600 K and the mass-flow rates described earlier gives us:

Gas	**$\dot{m}$** [mg h^{-1}]	**P [W]**
Stoichiometric	362.3188	0.1256
10% Excess	396.8254	0.1373

This are reasonable values ☺

The last step of method 1 is calculating the corresponding air flow to heat up to the same temperature while using the same power. This can be calculated using:

$$\dot{m} = \frac{P * 1000 * 3600}{\frac{\int_{T_1}^{T_2} C_p dT}{\Delta T}}$$

Original gas	**Original $\dot{m}$** [mg h^{-1}]	**Original P for ΔT = 600 K [W]**	**Corresponding air flow [mg h^{-1}]**
Stoichiometric	362.3188	0.1256	414.9230
10% Excess	396.8254	0.1373	453.4961

Method 2

Instead of using the power, we directly compare C_p values. We have the following values:

Gas	**Original $\dot{m}$** [mg h^{-1}]	**$C_{p,mg}$ [mJ mg^{-1} K^{-1}]**
Stoichiometric	362.3188	1.4292
10% Excess	396.8254	1.4262

Using the following ratio we can calculate the required air flow:

$$\dot{m}_{air} = \dot{m}_{mix} * \frac{C_{p,mix}}{C_{p,air}}$$

Which gives, using $C_{p,air} = 1.2480\ [\text{mJ mg}^{-1}\ \text{K}^{-1}]$:

Original gas	**Original $\dot{m}$** [mg h^{-1}]	**Original $C_{p,mix}$ [mJ mg^{-1} K^{-1}]**	**Corresponding air flow [mg h^{-1}]**
Stoichiometric	362.3188	1.4292	414.9230
10% Excess	396.8254	1.4262	453.4961

Which is exactly the same as the values in method 1 ☺.

Samenvatting

Surface Channel Technology dat wordt gebruikt voor de fabricage van vrijhangende microfluïdische kanalen, heeft zich doorontwikkelt tot technologieën met geïntegreerde elektroden in de bulk. Deze integratie van elektroden leidt tot een verbetering van ontwerpmogelijkheden en functionaliteiten. Een veelbelovende oplossing om dit te realiseren is de zogenaamde Trench-Assisted Surface Channel Technology. Deze technologie maakt de integratie van zwaar gedoteerde silicium zijwandverwarmers parallel aan het kanaal mogelijk, terwijl de ontwerpvrijheid voor microfluïdische kanaalafmetingen en voor de plaatsing van sensoren behouden blijft. Het realiseren van daadwerkelijke apparaten met deze technologie is echter arbeidsintensief en vereist aardige praktijk vaardigheden. De vele microfabricagestappen (> 300) vereiste vaak complexe optimalisatie van problemen. Samen met problemen die zich voordeden bij het vrijetsen van de microfluïdische kanalen vroeg dit om een nieuwe technologie.

Daarom werd in dit werk een vereenvoudigde Trench-Assisted Surface Channel-technologie gepresenteerd. Deze technologie wordt gebruikt om een eenvoudigere maar nog steeds effectieve methode te realiseren om silicium zijwandverwarmers te maken met een hoge doping concentratie en met een groot dwarsdoorsnede-oppervlak, evenwijdig aan het kanaal. Deze nieuwe technologie introduceert een nieuwe manier om piramidevormige toegangen naar de microfluïdische kanalen te creëren. Deze toegangen worden gelijktijdig gevormd met het vrijetsen van de microfluïdische kanalen uit de bulksilicium, waardoor er slechts een klein membraan achterblijft. Dit membraan zorgt voor volledige omsluiting van de microfluïdische kanalen, tijdens en na de laatste microfabricage stap. Deze benadering stelt ons instaat om nat te etsen in een KOH-oplossing, aangezien de verontreiniging van onoplosbare vlokken in de microfluïdische kanalen wordt vermeden. Na alle microfabricage-stappen kunnen de membranen handmatig worden doorgeprikt, waardoor de definitieve toegang naar de buitenwereld ontstaat.

De belangrijkste beperking van deze vereenvoudigde Trench-Assisted Surface Channel Technology bleek een beperking te zijn voor de oriëntatie van de elektrode, deze kan alleen worden gevormd parallel aan de Si $\langle 110 \rangle$ richtingen op een Si $\{100\}$ wafer. Elke afwijking van deze hoek zal resulteren in een aanzienlijke onderets van de silicium zijwandverwarmers. Door de masker vensters en etstijden te optimaliseren, kan deze onderets van de zijwandverwarmers echter drastisch worden verminderd. Een andere beperking voor deze technology is het achterblijven van bulksilicium op de buitenwanden van de elektroden.

Deze nieuwe vereenvoudigde Trench-Assisted Surface Channel-technologie blijkt een makkelijker alternatief te zijn voor de bestaande Trench-Assisted Surface Channel-technologie. Uit de fabricage werd duidelijk dat complexe trench juncties voorkomen moeten worden, omdat dit opeenvolgende lithografiestappen zeer problematisch kan maken. Een oplossing voor dit probleem is om trench T-juncties met een vernouwing te gebruiken.