Optical Sciences group

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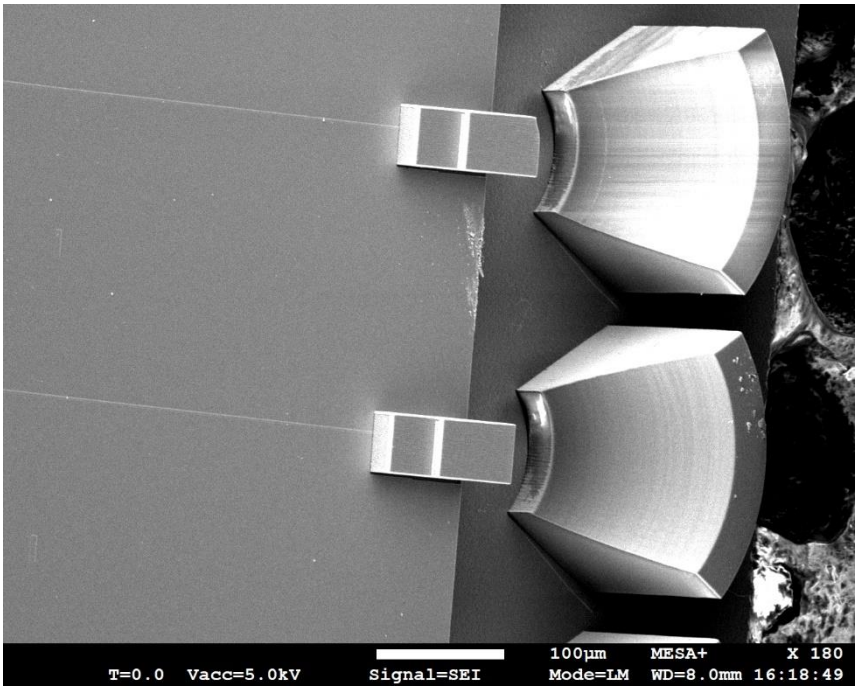
3D printed on-chip parabolic mirror for chip-to-fiber and chip-to-chip coupling



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Enschede

Abstract

Reflection of light by a 3D printed parabolic mirror overcomes the in-plane limitation of end facet coupling between two photonic devices (such as on-chip waveguides, optical fibers). With a 3D printed parabolic mirror, light can leave the wafer-plane. This enables wafer-level optical testing, where we can identify problematic devices easily and do not need to waste assembly on them. Furthermore, with the proper curvature design, the mirrors generate a bigger beam waist than the mode sizes at the waveguide end facet, which reduces requirements on the alignment accuracy[1]. Depending on the reflection coating, a parabolic mirror can work over a very large wavelength range (e.g. from the UV to the infrared for an Al coating) compared to a grating coupler, which typically spans only a few tens of nano-meters[2]. In this study, a parabolic mirror base is 3D printed using a 3D-Nanoscribe two-photon polymerization printer. The reflection layer is formed by Al coating. Details of the design, fabrication, and preliminary characterization of the mirrors will be presented.

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1 Introduction

As science and technology evolve, the rapid growth of internet and cloud computing applications has led to network bandwidth demands in data center that exceed Moore's Law[3]. According to the Cisco Global Cloud Computing Index, annual Internet Protocol (IP) traffic in data center exceeds 20 Zettabytes (i.e. 20x1024 bytes) in 2021[4]. Therefore, at the wafer scale, higher demands are placed on the energy consumption and heat dissipation of electronic and photonic chips. And gradually the optical chip is showing more advantages in this process: especially in the field of the silicon photonics, where more and more research teams are exploring the limits. Accordingly, wafer-level testing (for rapid inspection to reduce production and packaging costs) is gradually expanding from electronic chip testing to optical chip testing. In this chapter, we first introduce the background knowledge of the electrical chip testing and it limitations. We then introduce why optical connections on chip level is desired to solve the problems. At the end, we introduce the outline of this thesis which is about our contribution to this field.

1.1 Electronic chip testings

The purpose of chip testing is to reject failed and potentially failed chips in the production process and to prevent defective products from flowing to customers. Therefore we need to increase the evaluation of the chip test level during the selection process by communicating with the original manufacturer as well as the packaging and testing factory to obtain the key parameters and indicators of the chip design verification → inspection → wafer-level testing → finished chip test stages to make a comprehensive evaluation[5].

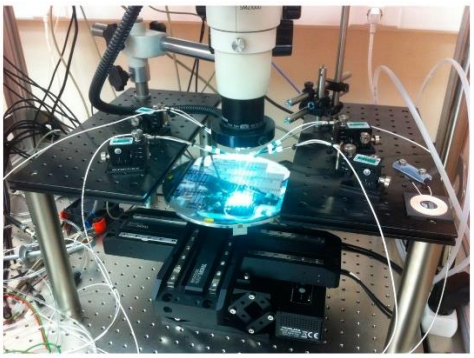


Figure 1.1 Example of a semi-automatic probes for electric wafer-level testing[6]

Electrical testing is a technique originally borrowed from the traditional integrated circuit industry, whereby an electrical signal is injected into a structure using a microprobe and the resulting electrical signal is then measured with another probe, from which some mechanical properties can be derived[7, 8].

The performance of electronic chips is very dependent on the stability of the production process. It is therefore necessary to check the process parameters that affect microfabrication. As process parameters affect their operational function, it is possible to select probe with sensors with good performance and map some key parameters along the wafer plane to determine if there is something wrong[8]. In

addition, the cost of the package is a large part of the overall chip cost: wafer-level testing prevents chip damage before package.

In fact, the problem of wired connections changes qualitatively once we get to the information processing system itself[9]. Because there, space is not infinite and all available space is filled with wiring. And competing with the space for the interconnection of wires is the space required to power and dissipate heat from the system. As a result, information processing systems are often limited by power and the wiring density[10].

The performance of electronic chip information processing systems is increasingly limited by the energy available on earth. Chips today cannot easily consume more power, e.g. the power saturation of each chip is at ~100 - 200 W[11]. Of course there are many sources of energy dissipation in information processing: reading and writing to memory; sending and receiving information through interconnections within the system and to the outside world; all these operations must consume energy[10].

1.2 Demands and developments of optical interconnect

As communication distance reducing to even shorter distances even to 50 nm, limitations imposed on interconnect systems have changed significantly[12]. Optics offer significant advantages in terms of interconnect density, interconnect power and other aspects such as improved signal integrity and timing compared to electrical chips here, and possibly also switching and routing via optics[10, 13].

Optics can provide particularly precise signal timing because optical channels: e.g. optical fibers, optical waveguides, etc. have low dispersion, allowing short pulses to be propagated over relatively long distances (for fiber around 10 m) without broadening them[12]. Compared with electrical signals, the propagation speed of optical signals in the optical path is not highly dependent on temperature. Photonic interconnect networks can now provide higher bandwidth and lower latency, while significantly reducing power consumption[10, 13].

Advanced computers and data centers require extremely low power consumption and dense integration to achieve higher interface bandwidth densities. And silicon photonics integration is an enabling technology for power and cost-effective optical interconnects in exascale computers and data centers[14]. Figure 1.2 shows an optical transceiver using silicon photonics.

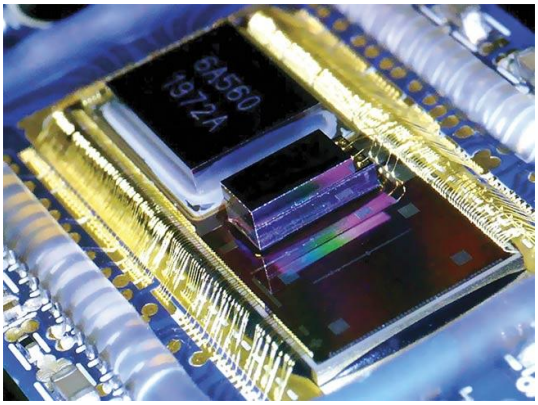


Figure 1.2 An optical transceiver built using silicon photonics[15]

To reduce costs, the packaging of optoelectronic components is also turning to wafer-level packaging. However, mass production of photonic integrated circuits (PIC) requires high-throughput wafer-level testing as shown in Figure 1.3 early in the manufacturing process before entering expensive and complex manufacturing steps such as chip separation, anti-reflective coatings, and packaging to evaluate device performance[16].

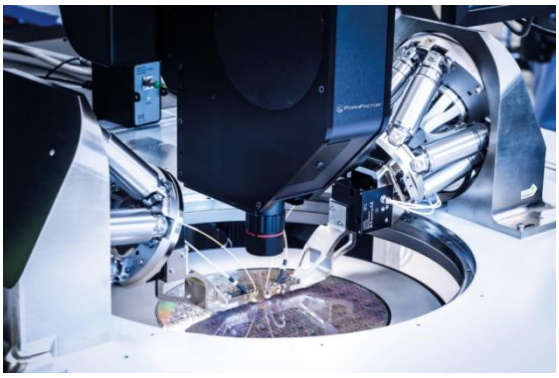


Figure 1.3 Example of an optical wafer-level testing setup[17]

Currently, wafer-level testing of PICs mainly relies on surface coupling through grating structures or use of waveguide tap couplers to couple a small fraction of light from the PIC, which can lead to permanent total optical losses in the system[18]. Because this approach relies on evanescent or diffractive excitation of light, the waveguide core must be exposed at the test location by etching in the waveguide cladding. This technique therefore leads to excessive scattering losses. In addition, today's PIC designs increasingly rely on edge coupling (EC), so PIC designers must make a difficult trade-off between minimizing optical losses and ensuring adequate test site accessibility[18, 19]. Furthermore, wafer-level testing of edge-emitting devices of vertical planes on deeply etched trench sidewalls remains a significant challenge.

In the Si waveguide platform, grating couplers have been used to couple the light out of the wafer plane for wafer-level testing[20]. However, it is challenging to use grating coupler in lower contrast waveguide material platforms due to the relative small bandwidth (i.e., typically spanning only a few tens of nanometers) [21].

1.3 Thesis outline

In order to avoid harming the waveguide and increasing scattering losses; to attenuate the inconvenience of edge coupling; and to increase the bandwidth of wafer-level testing, In this project we propose an on-chip parabolic mirror for optical interconnect and wafer-level testing. The overall coupling system design is presented in chapter 2. Chapter 3 discusses the fabrication processes. Chapter 4 discusses its optical performance with different testing condition. Finally, conclusions are presented in chapter 5, along with an outlook for future research. Many practical details are included in the Appendix.

2 Coupling System Design

This chapter introduces the system design, components design and corresponding Gaussian beam knowledge related to the design. Figure 2.1 shows the coupling system designed in the project. The light exit from the waveguide diverge to the mirror then is collimated and reflected 90 degree by the mirror. The reflected light is 90 degree out of the wafer plane and has an enlarged mode size for relaxed coupling requirement. Coupling light into the chip can follow the reversed way.

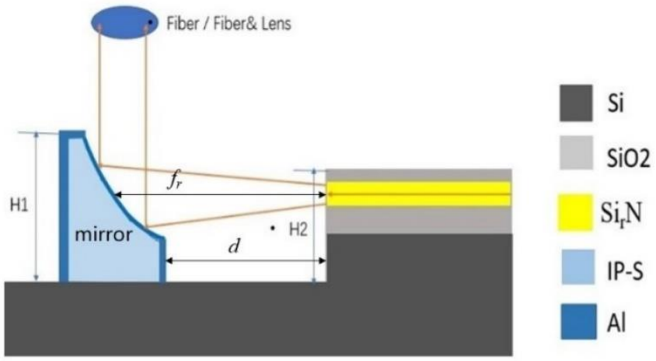
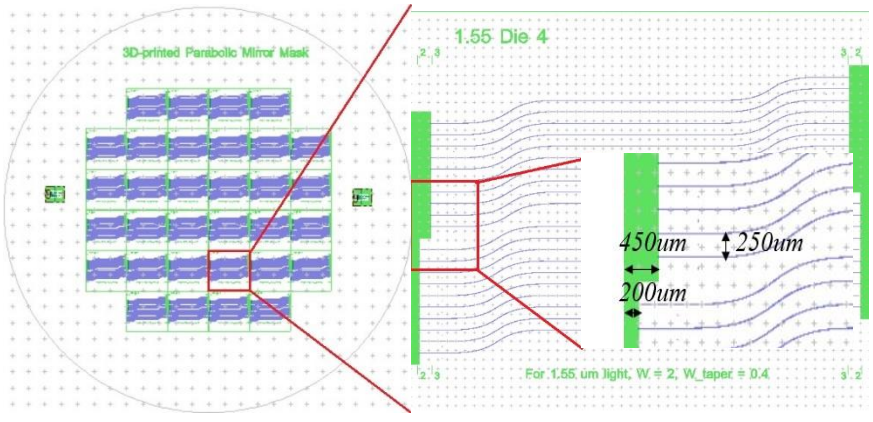


Figure 2.1 Sketch of target chip-to-fiber coupling system

2.1 Chip & Waveguide Design

A mask was designed in the software CleWin, shown in the Figure 2.2 : It consists of 32 chips. The purple part is the waveguide (the spacing 250 μm), where the waveguide taper at the end face has three widths: 400 nm, 250 nm, and 150 nm, yielding different mode profiles. They all have the same height (200 nm). The green part is the etched platform for placing the parabolic mirror, they have 450 μm or 200 μm width.



(a) (b)

Figure 2.2 The mask layout of the whole wafer (a) and a single die (b)

We plan to place the mirrors in the wide grooves so that there is more freedom in designing the size of the mirrors.

In Lumerical, those parameters (mentioned above) are used to simulate the mode profiles at wavelength of 980 nm, 1380 nm, 1550 nm. The results are shown in Figure 2.3 . In this fabrication focused study, we approximate these modes as Gaussian modes. This helps to simplify the mirror shape design (instead freeform shape, we could use parabolic shape, which will be discussed in chapter 2.4).

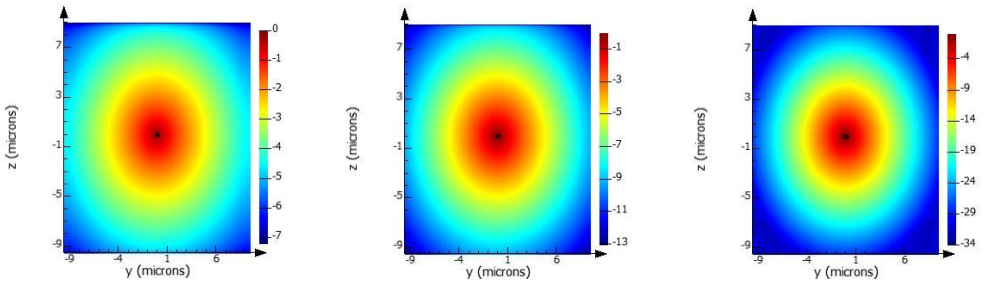


Figure 2.3 Mode profile with taper width of (a) 150 nm,(b) 250 nm, and (c) 400 nm at wavelength 980 nm

2.2 Gaussian Beam

The light from a single-mode fiber can be well approximated as a fundamental Gaussian beam[22]. The light exited from our waveguide taper is also approximated as a Gaussian mode in this thesis. Even through this approximation is not as close as the case of a single mode fiber, it is good enough to discuss the concepts for this fabrication focused thesis.

The introduction of the Gaussian beam in this section (until equation (6) is summarized from[23]) The E field in a fundamental Gaussian beam is:

$$E(r,z) = E_0 \hat{x} \frac{\omega_0}{\omega(z)} \exp\left(\frac{-r^2}{\omega(z)^2}\right) \exp\left(-i\left(kz + k\frac{r^2}{2R(z)} - \psi(z)\right)\right) \quad (1)$$

Where $\mathbf{w_0}$ is the beam waist;

$\mathbf{Z_R}$ is the Rayleigh range;

r is the radial distance from the center axis of the beam;

z is the axial distance from the beam's focus (or "waist");

k = 2πn/λ is the wave number (in radians per meter) for a free-space wavelength λ, and n is the index of refraction of the medium in which the beam propagates;

$\mathbf{E_0}$ = E(0, 0), the electric field amplitude (and phase) at the origin (r = 0, z = 0);

R(z) is the radius of curvature of the beam's wavefronts at z;

ψ(z) is the Gouy phase at z, an extra phase term beyond that attributable to the phase velocity of light.

As shown in Figure 2.4.

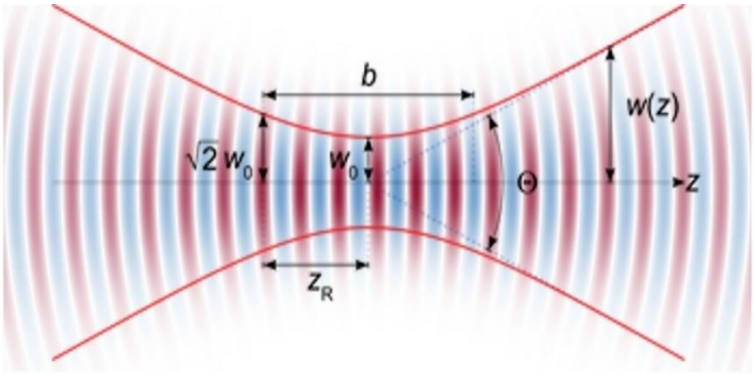


Figure 2.4 Electric field distribution around the focus of a Gaussian beam[23].

Rayleigh range Z_R is obtained from Equation (2)

$$z_R = \frac{\pi \omega_0^2 n}{\lambda} \tag{2}$$

where λ is the wavelength of the light, n is the index of refraction. The Gaussian beam width w(z) as a function of the distance z along the beam forms a hyperbola.

$$\omega(z) = w_0 \sqrt{1 + (\frac{z}{z_R})^2} \tag{3}$$

$$\omega(z) = \frac{FWHM(z)}{\sqrt{2\ln 2}} \tag{4}$$

b is the depth of focus; Θ is total angular spread and we usually define $\Theta/2$ as divergence angle θ. The beam divergence angle is a measure of the speed at which the beam diverges from the beam waist. Beams with a very small divergence angle, such as a beam radius that is close to constant over long travel distances, are called collimated beams. Due to the wave nature of light, some divergence in the beam is unavoidable (assuming light travels in an isotropic medium).

Then we know that:

$$\omega_0 = \frac{\lambda}{\pi\theta} \tag{5}$$

$$\theta = \frac{\lambda}{\omega_0 \pi} \tag{6}$$

2.3 Parabolic mirror

Both spherical and parabolic mirror are commonly used to collimate a point source of focus a parallel beam. Ray tracing pictures are shown in Figure 2.5. Figure 2.5(a) shows a small spherical mirror (the mirror diameter is relative small compare with its focal length) where, the parallel incoming light essentially crosses at a common point. Figure 2.5(b) shows a large spherical mirror (the mirror diameter is relative large

compare with its focal length) cannot make the light cross at one single point but creates multiple focal points, collectively known as a *focal volume*. Parallel light reflected by a parabolic mirror, it will cross at a single point, focal point, regardless of the incoming beam diameter respect to the focal length, as shown in Figure 2.5(c). The distance along the optical axis from the mirror to the focal point is the focal length f of the mirror[24].

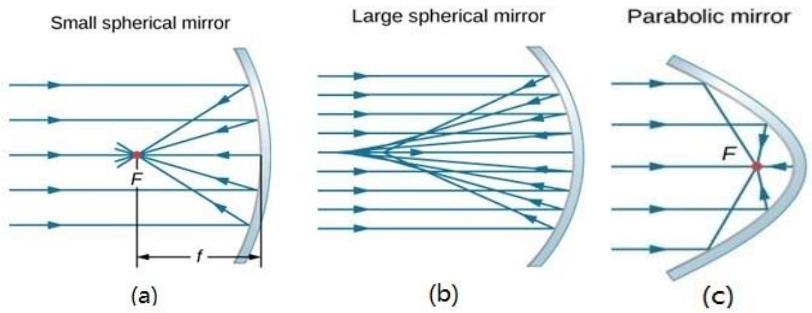


Figure 2.5 (a) Light reflected by a spherical mirror that is small compared to its radius of curvature. (b) Parallel light reflected from a large spherical mirror. (c) Parallel light reflected from a parabolic mirror[24].

Compared to spherical mirrors, spherical aberration increases with the ratio of beam diameter to focal length, while parabolic mirrors can be made to accommodate beams of any width. However, if the incident beam is at a non-zero angle to the axis (or if the emitting point source is not placed in focus), the parabolic mirror suffers from an aberration called ***coma***. This is mostly discussed in telescopes though, as most other applications do not require sharp resolution off the parabolic axis. In this project, we can effectively avoid the problem of ***coma*** by putting the waveguide end facet at the focal point of parabolic mirror[25].

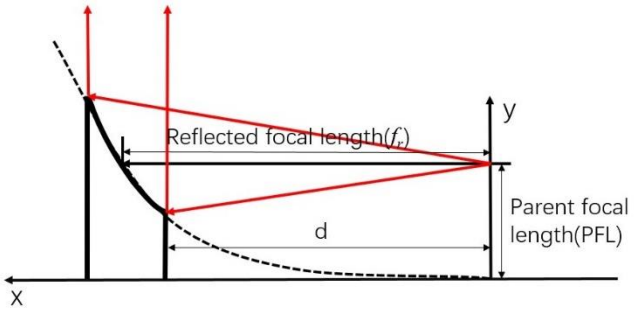


Figure 2.6 Sketch light reflected by parabolic mirror

If we want the light from the waveguide be reflected vertically by the parabolic mirror, the required parabolic segment is shown in Figure 2.6. Every ray starting from the focus point will become parallel light after parabolic reflection

The parabolic line in Figure 2.6 is described with

$$x^2 = 2py \tag{7}$$

The corresponding Parent focal length (PFL) f is:

$$f = \frac{p}{2} \tag{8}$$

Where p is focal quasi-distance. The Reflected focal length f_r in case of 90 degree reflection can be calculated with $y = f$ (the line between center of mirror and the focal point is parallel to x axis):

$$\begin{aligned} f_r^2 &= 2*2f*f \\ f_r &= 2f \end{aligned} \tag{9}$$

The waveguide mode size and desired beam waist after the parabolic mirror determines the reflected focal length f_r , the width of the mirror, and the distance d between the waveguide facet and parabolic mirror. The parabolic function is defined by:

$$y(f_r) = \frac{x^2}{2f_r} \tag{10}$$

2.4 Parabolic mirror parameter design

From chapter 2.2-2.3: that is to say, the maximum reflected focal length (from Figure 2.2.b and 2.6) should not exceed 460 µm there are other limiting factors which are discussed below.

In Lumerical, mode of 3 different widths of waveguide 150 nm, 250 nm, 400 nm were simulated with height 200 nm. Silicon nitride waveguides have an index of refraction of 1.994 and the SiO_2 cladding has an index of refraction around 1.45 at a wavelength of 1 µm. Related scripts & files are detailed in the appendix A. Figure 2.7 shows the mode diameter at different distance from the waveguide end facet.

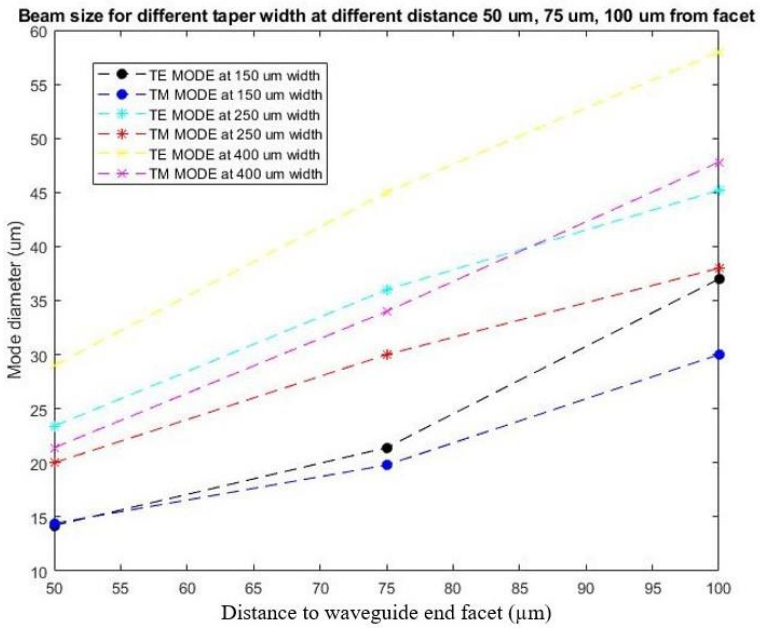


Figure 2.7 mode diameter under different taper width 150 nm, 250 nm, 400 nm at different distance 50 µm, 75 µm, 100 µm from the waveguide end facet.

And Figure 2.8 shows the mode profile of a waveguide taper width 150 nm.

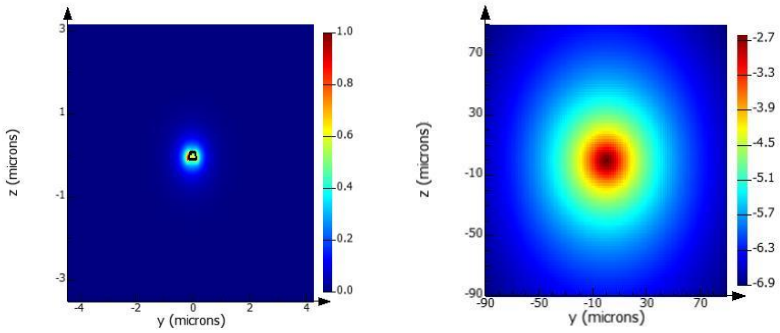


Figure 2.8 (a) Mode profile of a waveguide taper with 150 nm width and (b) its mode profile format at a distance of 50 µm from the waveguide end facet.

In this project, we would like to enlarge the beam waist to reduce the translation alignment requirement. However, at a given wavelength, increasing Gaussian beam diameter, means reducing its divergence angle. This leads to a trade-off between reduced translation alignment requirement and increased angular alignment requirement. The relationship between w_0 and the divergence angle θ of a Gaussian beam is shown in Figure 2.9. We use 4 quadrants to indicate different alignment requirement. Quadrant I has low translation and low angular alignment requirement; Quadrant II has high translation and low angular alignment requirement; Quadrant III is opposite to Quadrant I, has high translation and high angular alignment requirement; Quadrant IV is opposite to Quadrant II, has low translation and high angular alignment requirement.

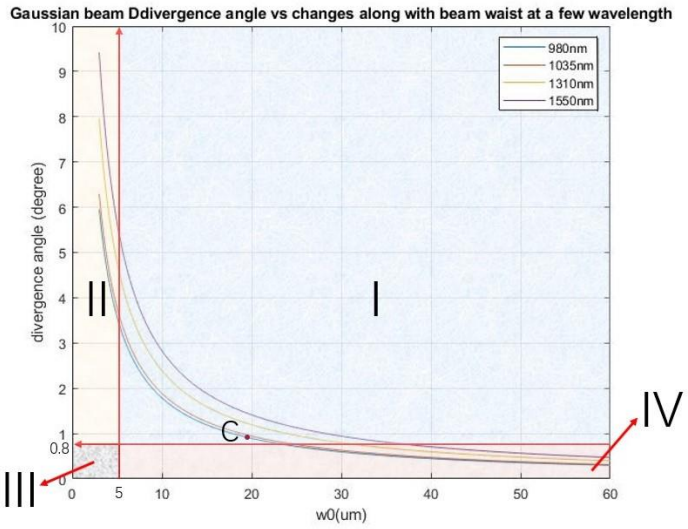


Figure 2.9 Gaussian beam divergence angle vs beam waist at a few wavelength.

In this project, we choose a reflected focal length, f_r, of 100 µm to demonstrate the fabrication process. The waveguide end face will be positioned at the focal point of the mirror, thus in average, the waveguide end facet to mirror distance is f_r (100 µm). In case of a 150 nm wide 200 nm thick waveguide, the corresponding mode size is 37

μm (i.e. w_0 of 18.5 μm). After reflected by the mirror, the 'collimated' beam waist is approximately the same as the beam size incident on the mirror, which is marked in Figure 2.9 with C: a red dot. C is in the Quadrant I shows that it is easy for alignment during the experiment.

The parabolic mirror modal is designed with Solidworks. A sketch of the mirror is shown in Figure 2.10. The mirror center is designed to face the waveguide end facet. As described above, the reflected focal length, f_r, is chosen to be 100 μm, which means the parent focal length f is 50 μm. Thus,

$$x^2 = 2*100*y \tag{11}$$
$$f_r = 2f = 100$$

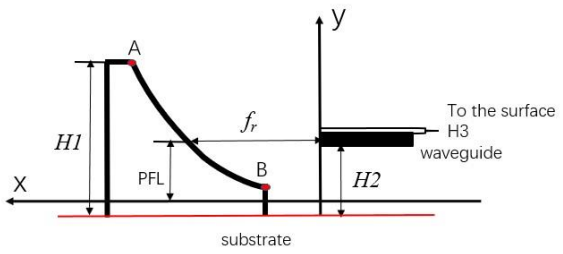


Figure 2.10 Introduce mirror design to chip

In Figure 2.10, usually H2 is bigger than PFL that means the bottom of the mirror will be raised (depending on actual height of groove) to ensure that the center of the parabolic mirror can be aligned to the waveguide end facet. And the parameter of H3 is detailed in Appendix B.

Since the mirror surface should be bigger than the mode size (37 μm) incident on it, the point A and B have coordinate of (-50, 30.5) μm and (-150, 130.5) μm respectively.

In Solidworks, the y-axis is the rotation axis, since we want a maximum beam diameter around 40 μm(2*w_0), which means that the surface of the parabolic mirror should cover it. The sketched mirror rotates 35 degrees in both of the left and right directions to make sure the lateral width can also cover the maximum beam diameter as shown in Figure 2.11.

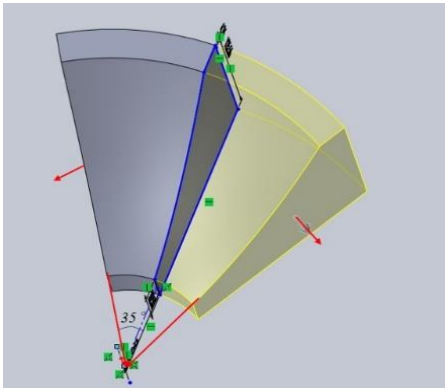


Figure 2.11 Sketch and modal show lateral width

3 Fabrication processes

In this chapter, we first describe the full fabrication process flow. We then discuss a few key steps (3D printing, aluminum deposition, and aluminum etching) in details. All the instruments involved in this project are from the laboratories of the Nanolab and optical science group at University of Twente.

3.1 Fabrication process flow

This process flow of fabrication micro mirror couplers on SirN waveguide chips is shown in Figure 3.1. It consist of 7 main steps:

Step 1: Spin coating UV lithography and then development.

Step 2: Using reactive ion etching to create a platform (depth around 60 µm). This platform is needed to position the mirror in front of the waveguide;

Step 3: Printing parabolic mirrors aligned to the end facet of the waveguides;

Step 4: Aluminum deposition on the whole surface;

Step 5: In order to remove the Al layer apart from the mirror, positive resist is coated over the surface;

Step 6: After exposure, wet etching away unwanted Al;

Step 7: Remove the resist covered on the mirror.

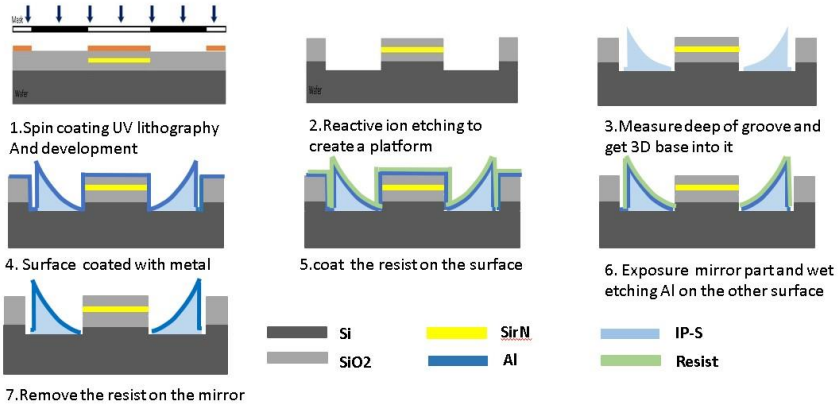


Figure 3.1 Process flow of the whole fabrication

There are also other fabrication possibilities to have the Al coating only on the mirror, such as lift off or shadow mask deposition. Due to the limited time, we could not try them all. However, the idea is described in Appendix B as well as whole process flow for step 1 and step 2.

3.2 3D printing

3.2.1 Two-photon polymerization for printing

Laser 3D direct writing based on two-photon polymerization provides is currently the most effective technology for nanoscale 3D printing[26]. Different from traditional micro-stereolithography (which is a single-photon micro-stereolithography process), laser direct writing 3D printing is based on the principle of two-photon polymerization (or multiphoton absorption).

Two-photon polymerization is a photopolymerization process initiated by a substance after two-photon absorption; two-photon absorption means that a molecule of a substance absorbs two photons at one time, and two-photon absorption occurs mainly in the focus of a super-intense laser generated by pulsed laser.

Except for the focal point, the intensity of the laser light elsewhere along the optical path is not sufficient to produce two-photon absorption, and because the selected light has a longer wavelength and lower energy, the corresponding single-photon absorption process cannot occur. This nonlinear two-photon absorption effect makes 3D printing at the micro-nano scale possible: the two-photon absorption effect occurs only when the light intensity reaches a certain value(threshold), then when the laser is focused, the reaction area can be localized in an extremely small area inside the focal point[27].

Through the nano-scale precision moving stage and galvo scanning mirror, the focus is moved in the photosensitive material, and the position where the focus passes, the photosensitive material is denatured and cured, and 3D objects of any shape and size can be printed. The 3D printer (Photonic Professional GT) developed by Nanoscribe has been used in many fields such as photonics, micro-photonics, micro-channels, life sciences, micro-nano technology, etc. The basic idea and printer are shown in Figure 3.2[28].

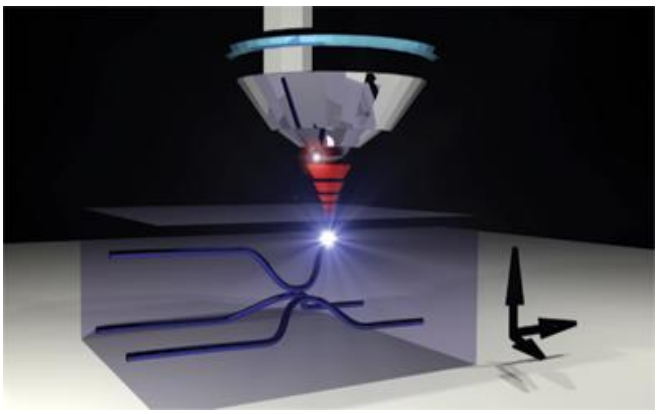


Figure 3.2.1 Schematic diagram of the principle of two-photon laser direct writing[28]

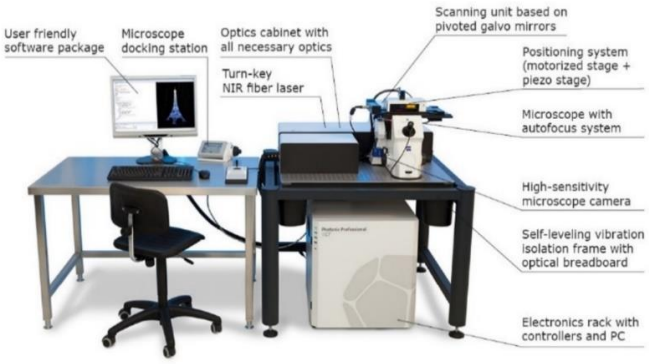


Figure 3.2.2 Nanoscribe Photonic Professional GT basic configuration stage[29]

3.2.2 Mirror model and working flow

From Chapter 2.4, 2 different rotations combine together and the structure is drawn in Figure 3.3.

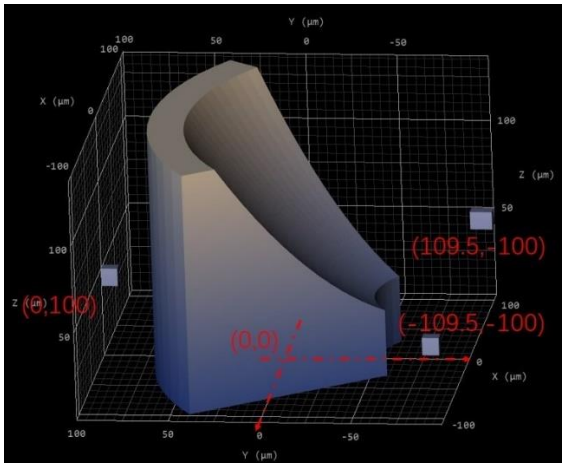


Figure 3.3 3D model with 3 markers

In Figure 3.3, 3 markers are used for determining exact distance(reflected focal length) between the center of mirror and the end facet of waveguide.

A generalized work flow for creating a structure with the printer is as follows:

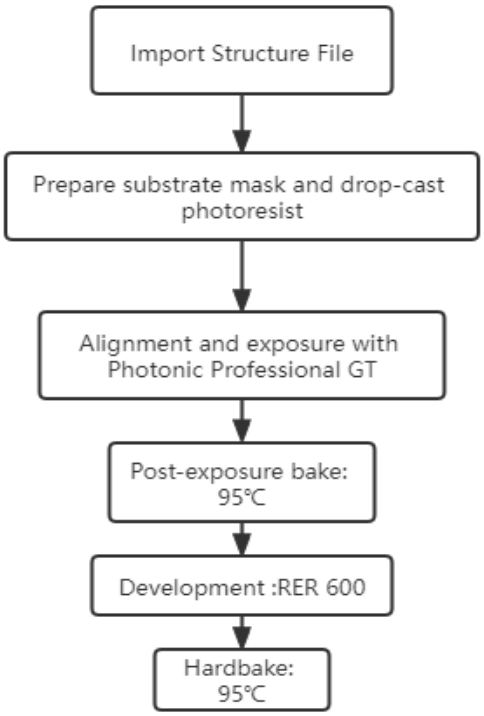


Figure 3.4 Nanoscribe working flow

For our project, some special settings are needed. The 100 µm reflected focal length with markers is to ensure that the center of the mirror is exactly 100 µm from the cross section of the waveguide. Therefore, in the Nanoscribe execution command, we put the center cursor exactly at the end facet of waveguide, the interface on PC is shown in Figure 3.5.

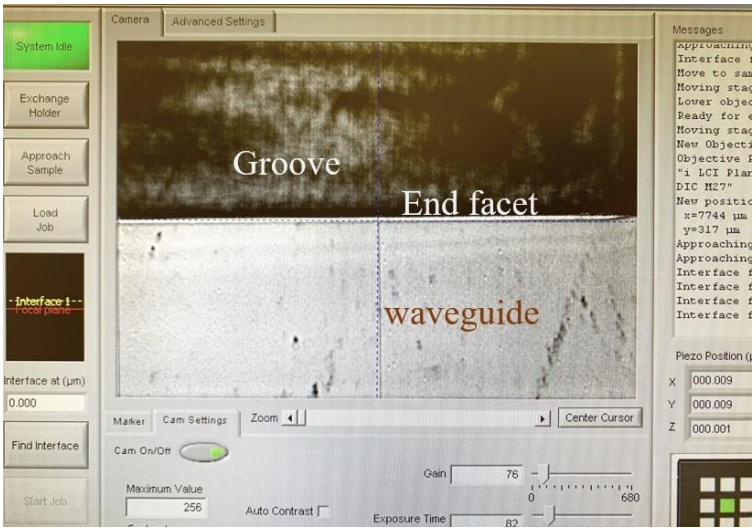


Figure 3.5 Microscope top view before printing with center cursor

Then try to give the code to move the stage position(x, y, z)axis. Working flow is shown in Figure 3.6.

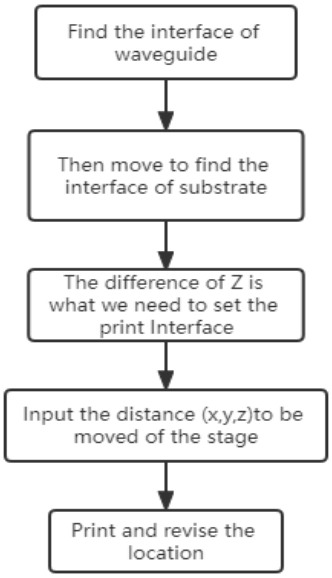


Figure 3.6 Working flow for locate the print center

3.2.3 Nanoscribe parameters

According to Yuchen's work[30], 25x objective lens is chosen for smooth surface and precise size of structure. At the same time, some other printing parameters are given in detail. There are summarized in Table 1. Related scripts are in Appendix C.

Resist	IP-S	Objective	25X	Work mode	Dip-in	Slicing Mode	Adaptive
Hatching AngleOffset	90	Fix Self Intersections	on	Surface Normals	0	Distance Max(μm)	0.1
Scanspeed(μm/s)	100000	Hatching Distance(μm)	0.2	Voxel Aspect Ratio	3.6	Distance Min(μm)	0.1
Laserpower(%)	60	Hatching Angle	0	SimplificationTolerance	0.05	Slope Evaluation	1

Table 1. Printing parameters

IP-S photoresist is widely used in Mechanical metamaterials, microoptics, integrated photonics, microfluidics. Because through it the 3D structure could have smooth surfaces during micro- and mesoscale fabrication with optical-quality surface roughness and shape accuracy[31].

And among those parameters, **scanspeed** is particularly important. If the **scanspeed** is faster than 100000 μm/s, the printed surface roughness increases. Comparison between 2 different **scanspeed** is shown in Figure 3.7. The faster the scanning speed is, the more clear line shape traces on the mirror surface.

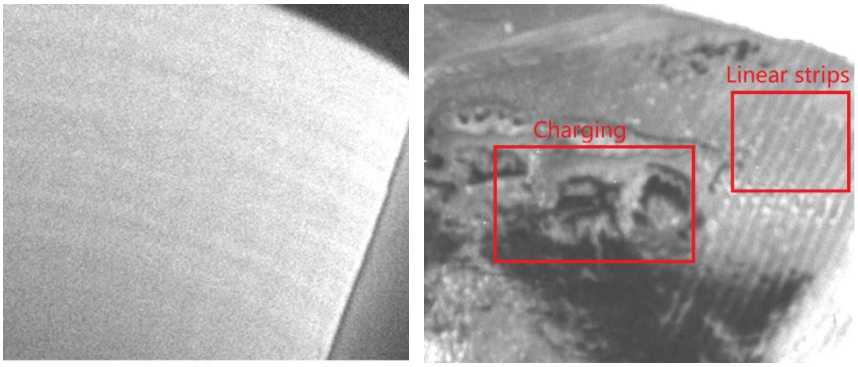


Figure 3.7 (a). Scanspeed 100000, (b). Scanspeed 160000

Then put those printed mirrors into RER600 15 mins for development and 2-Propanol VLSI 5 mins for cleaning.

Before printing parabolic mirror on chips, those mirrors are printed on the Silicon dummy wafer to see whether the shape and size are correct. Figure 3.8 shows 3*3 array mirrors with nice shape under microscope. Details about how to measure it are put into Appendix C.

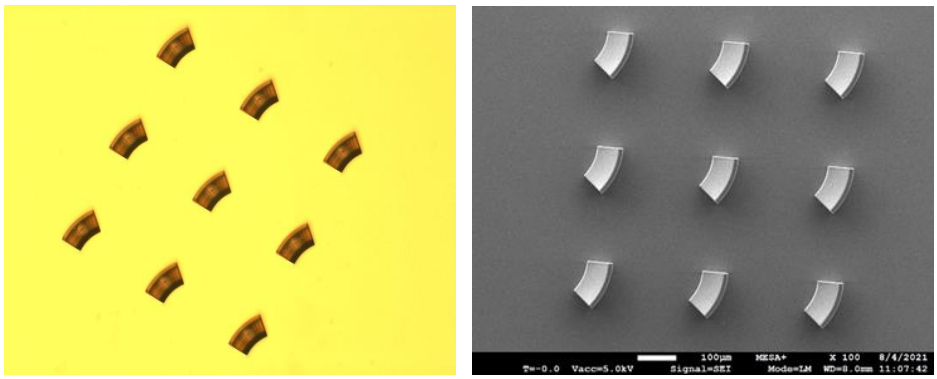


Figure 3.8 3*3 array printed parabolic mirrors (a)without coating;(b) with coating

3.3 Aluminum layer Deposition

A parabolic mirror printed on a silicon substrate wafer using the 2-PL method, then Al coating is given in this section. They are also the third and fourth steps in the process.

Al layer has been chosen to be the reflection coating in order to achieve high reflection over a very large wavelength range(UV to the infrared)[32]. The reflectance curve for several metal coatings (Al, Gold, Silver) as shown in Figure 3.9. The reflectivity of metallic aluminum films remains around 80%-90% over a wide range of wavelengths and has a good stability. Two different deposition methods are available in the MESA+ Nanolab for aluminum film deposition: one is sputtering; the other is evaporation. Both deposition methods are investigated and discussed below.

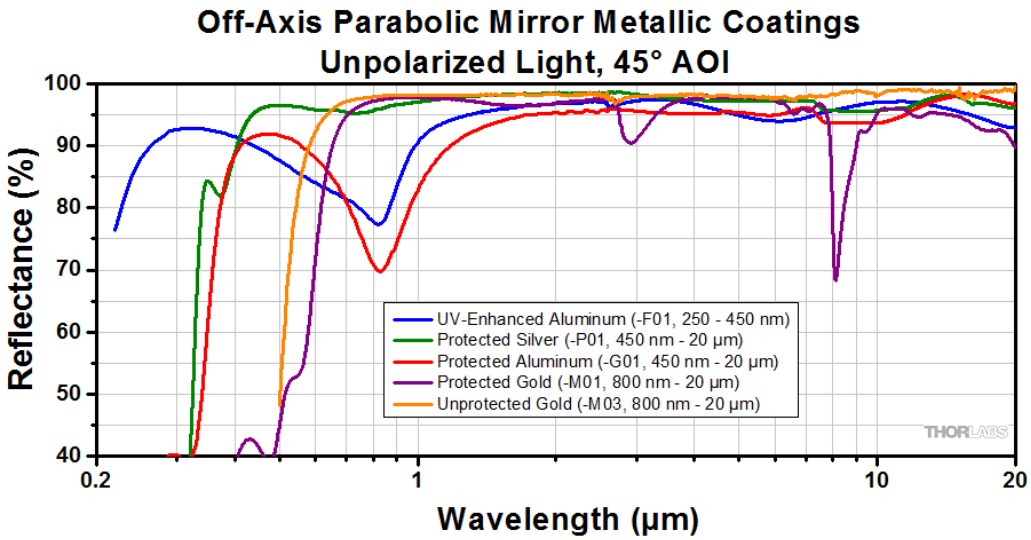


Figure 3.9 Typical reflection curves of metal coated mirrors from UV-IR range(45 degree)[33]

3.3.1 Sputtering

Sputtering is a phenomenon in which microscopic particles of a solid material are ejected from the surface of the material after it has been bombarded by energetic particles from a plasma or gas[34]. In the Nanolab, Sputterke is a multipurpose sputter coater for deposition of conductive materials. Sputterke consists of Pirani, Penning vacuum gauges, providing high base vacuum around 2.0 e-6mbar. A picture of the machine is shown in Figure 3.10.

Figure 3.10 Sputterke overview in the Nanolab

In order to investigate the reflectivity as a function of film thickness, aluminum films with thicknesses from 10 nm to 1 µm are deposited. As the Al layer thickness increases, the surface roughness increases, thus the sample looks milky when the Al layer more than ~ 300 nm thick as shown in Figure 3.11. The corresponding SEM pictures are shown in Figure 3.12 in the next section to compare with the evaporation deposited layers.

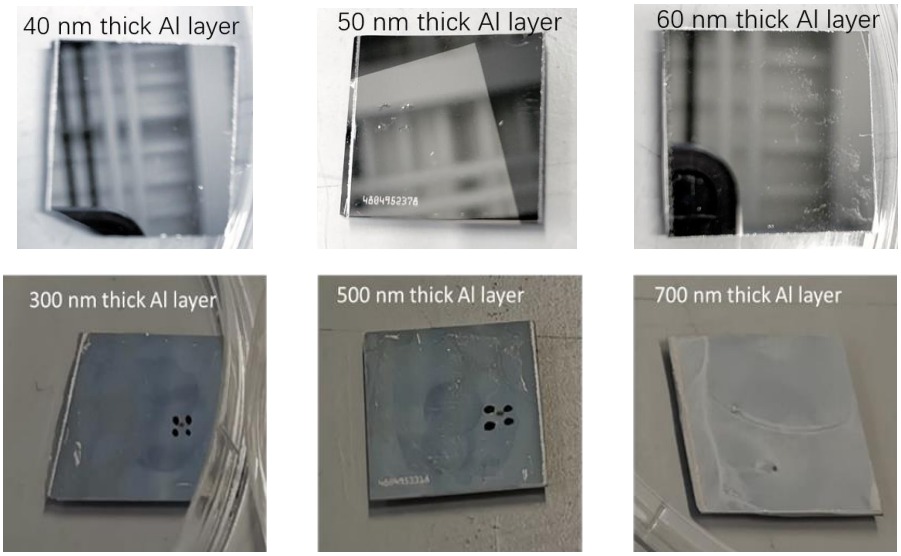


Figure 3.11 Al coating on Si substrate surface view at different thicknesses 40 nm, 50 nm, 60 nm, 300 nm, 500 nm, 700 nm

These results indicate that sputtered Al layer does not act as a very good mirror (visible wavelength) when its thickness exceed more than ~ 300 nm.

3.3.2 Evaporation

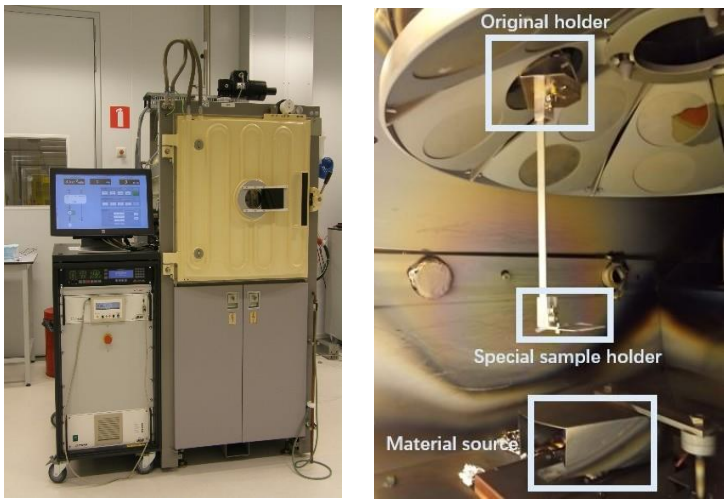


Figure 3.12 BAK600 in the Nanolab(a), and its vacuum chamber with special holder(b)

BAK600 is an e-beam evaporator for deposition of various materials under high vacuum conditions. The evaporator uses a high voltage electron beam for resistive heating of materials[35]. When using its stranded wafer holder, the maximum Al thickness it could deposit is around 500 nm which cannot meet the desired 1 µm thick testing range. Thus, one special holder is introduced as shown in Figure 3.12 (b). In this way, sample will be more close to material source and deposits thicker thickness in the same amount of time. The actual thickness is approximately 7 times the PC set thickness. Details are explained in Appendix D.

The evaporated layers show mirror like surface at a Al thickness as large as ~800 nm as shown in Figure 3.13. It is much thicker than the sputtering case. SEM images of the sputtered layers and evaporated layers have been compared in Figure 3.14.

These results lead to a conclusion that evaporation process is more suitable to deposit thick smooth layer than the sputtering process. The reason of this roughness difference is not clear to us, one possible caused could be the Al particle anergy difference during the deposition process. Sputtering is more energetic, which may resulting in a greater tendency to produce large grains.

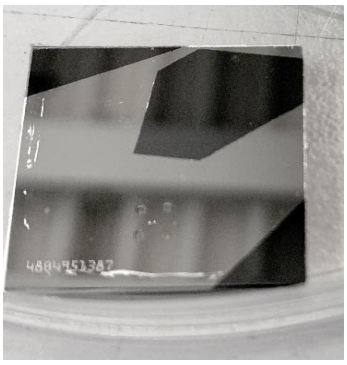


Figure 3.13 BAK600 : Al coating on Si substrate surface view at 800 nm thickness

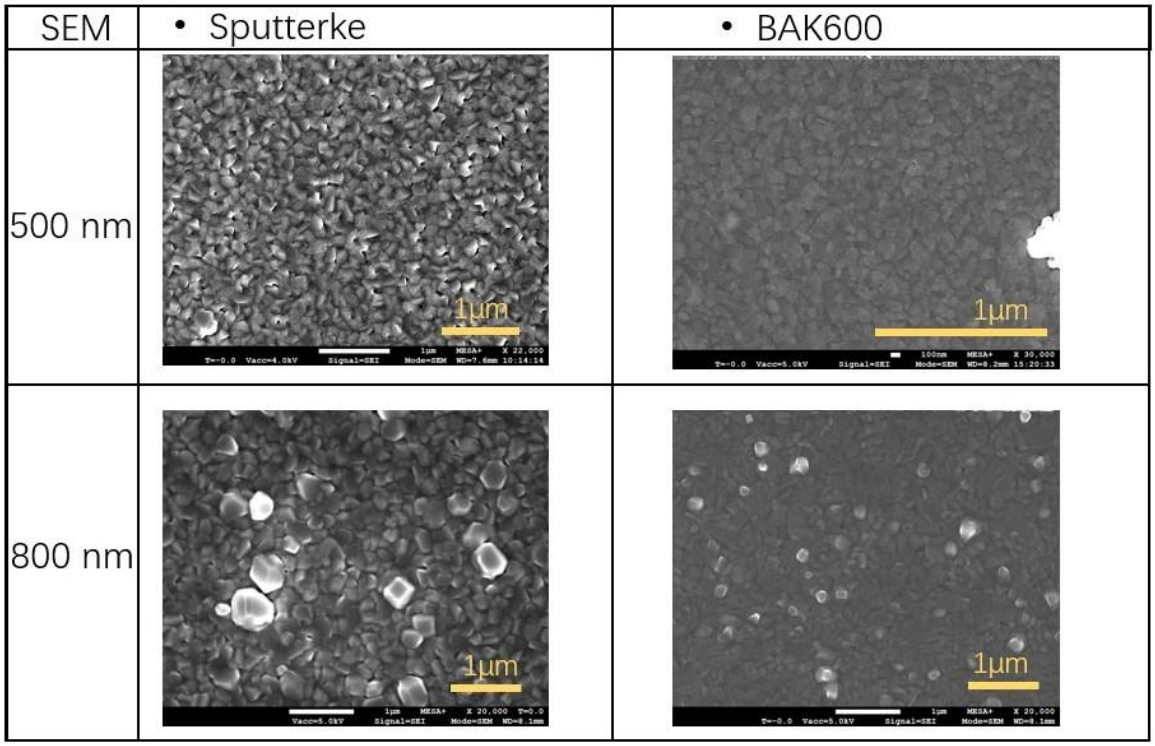


Figure 3.14 SEM images of the sputtered layers and evaporated layers at 500 nm, 800 nm thickness

At 50 nm thickness, the evaporated one also has smaller grain size than the sputtered one as shown in Figure 3.15. However, the sputtered one is smooth enough for our testing light wavelength of 980 nm..

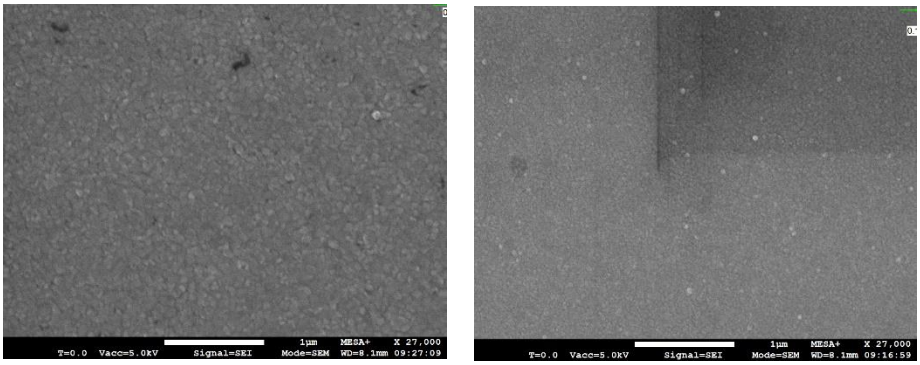


Figure 3.15 SEM for sputtering substrate (a)and evaporation substrate (b)

3.4 Aluminum layer pattering

In this section, we going to describe the processes to keep the Al coating on the mirror surface (also on the platform bottom) and remove it from all other places as shown in Figure 3.1. In order to cover all surfaces of this large 3D profile, spray coating resist is used instead of standard spin coating. A wet Al etching and cleaning is then applied to remove the Al layer and resist layer.

3.4.1 Spray coating and lithography

Step 5 in Figure 3.1,spraying is applied to the surface of the object by means of a spray gun or disc atomizer, which is dispersed into uniform and fine droplets by means of pressure or centrifugal force. AltaSpray coater is used for spraying positive photoresist: AZ4999, which is a coating of highly transparent photoresists tailored to special coating equipment such as the SUSS Delta AltaSpray, and provides a defect-free and conformal coating on structure with severe topography[36]. Therefore for parabolic mirrors this is a good choice. Sample chips are put onto the wafer stage for all-round spraying from 4 different angles as shown in Figure 3.16. This results a ~5 µm thick resist layer.

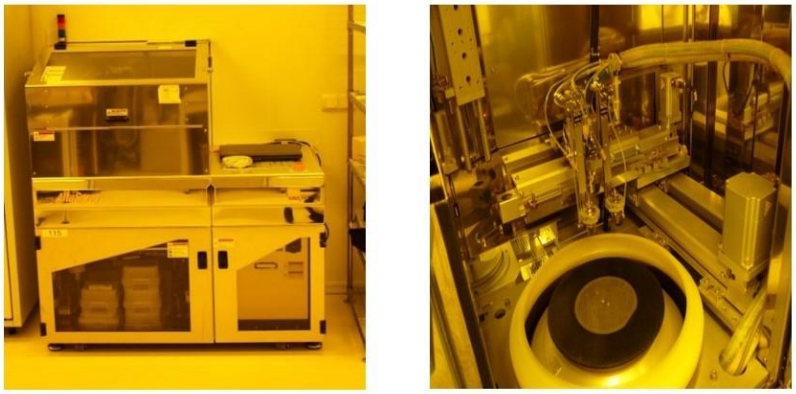


Figure 3.16 Altaspray coater in the Nanolab (a) and its wafer stage inside (b)

The wafer is then transferred to hotplate for baking at 100 ℃ for 70 seconds. According to Figure 3.17, there is no gap between substrate and hotplate should be applied, otherwise, the temperature may not reach 100℃ within 70 seconds.

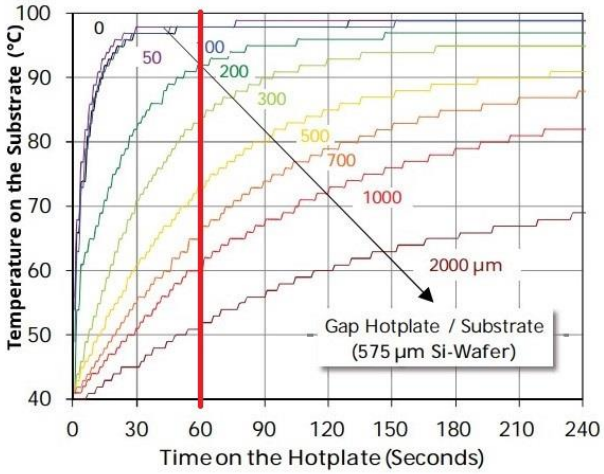


Figure 3.17 The temperature on the substrate (Si wafer)measured as a function of time on a hotplate set to 100 °C with different gaps between the hotplate and substrate[37].

Step 6 in Figure 3.1 needs a mask to block the UV light on top of the mirror (in case of positive resist) as shown in Figure 3.18.

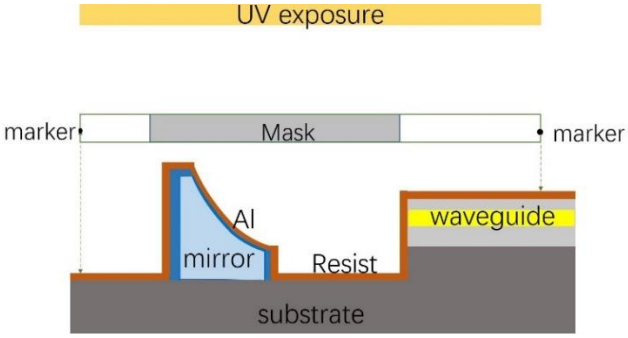


Figure 3.18 Schematic light exposure for 3d printed mirror

The mask is aligned to the wafer in Mask aligner EVG6200NT then apply UV exposure for 3 seconds. Then, place the chip in the developer OPD4262 Beaker 1 for 30 seconds and Beaker 2 for 15-30 seconds. After that, use QDR to clean the surface, the work flow is shown in Figure 3.19. The resist is then covered on the parabolic mirror only, ready for the wet Al etching step.

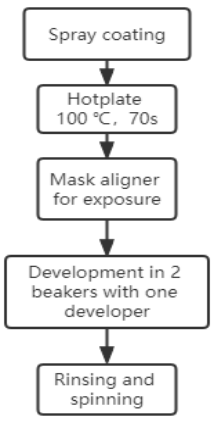


Figure 3.19 Steps for exposure and development in Nanolab

In order to check that the mirror is still covered by resist after development, it is placed under a fluorescent microscope, as shown in Figure 3.20: the red part indicates the presence of resist, while the green part indicates that the resist above Al has been washed away.

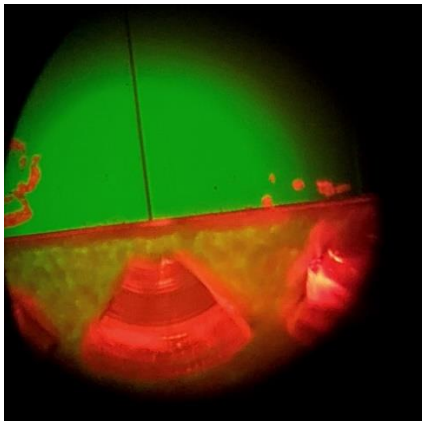


Figure 3.20 Mirrors covered with resist after development

3.4.2 Al layer wet etching and cleaning

According to Nanolab basic flow recipe as shown in Figure 3.21, Aluminum etchant is used to remove the Al layer(step 6 in Figure 3.1). The etching time depends on the thickness of Al film. The etching is usually considered to be complete when the Al color has faded.

ILP: In-line Processing	MFP: Metal-free Processing	UCP: Ultra Clean Processing	Removal of Residues

etch1211: Etching of Al or Al2O3 (WB10-private use)

Step	Level	Process		Comment
1	ILP	**Etching of Aluminium** (#etch142)	**NL-CLR-WB10** Use a Quartz beaker with Aluminium etchant Settings: • Temperature: 45°C Etch rate = 0.4µm/min	
2	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR** = Quick dump rinsing mode **Cascade** = Overflow rinsing mode for fragile substrates Rinse until message 'End of rinsing process' is shown on the touchscreen of the QDR, else repeat the rinsing process.	
3	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	

Figure 3.21 Wet etching recipe for Al

Then, acetone is introduced for removing residual resist on the mirrors. Samples are immersed in the solution for approximately 5 minutes. Figure 3.22 shows mirror after the whole process.

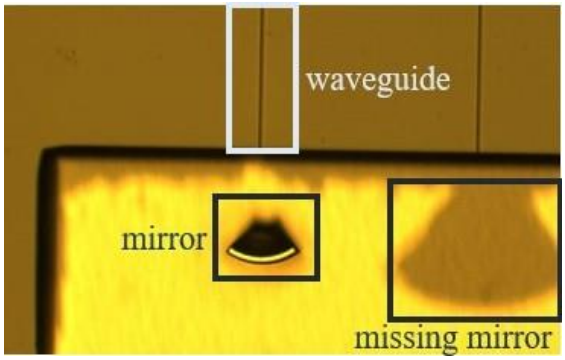


Figure 3.22 Focusing on the top surface of mirror after wet etching

From this image, we could see the color of the mirror top surface is as the same as the bottom of the etched platform, which means they are all covered by Al after wet etching. The parabolic mirror surface itself is black, this is due to the facet that the illumination light is reflected to the waveguide direction thus not reaching the microscope camera.

During this fabrication process, we notice some mirrors are missing, and we could not verify yet if there are any Al layer left at the waveguide end facet. This needs more time in the future to optimize and check. Thus the chips fabricated in this method is not ready for optical measurement at this moment. However, we will introduce an alternative way to fabricate and measure the mirror with a waveguide at chapter 4.2.

4 Optical measurement

4.1 Mirror testing with a bare fiber

In order to test the mirror performance without the complexity of a waveguide mode, standalone mirrors (i.e., without waveguide) have been fabricated on a flat Si wafer. Mirrors are printed at the edge of Silicon substrate and facing outside. This make it easy to align the bare fiber with the mirror. Basic set up in the OS lab is shown in Figure 4.1.

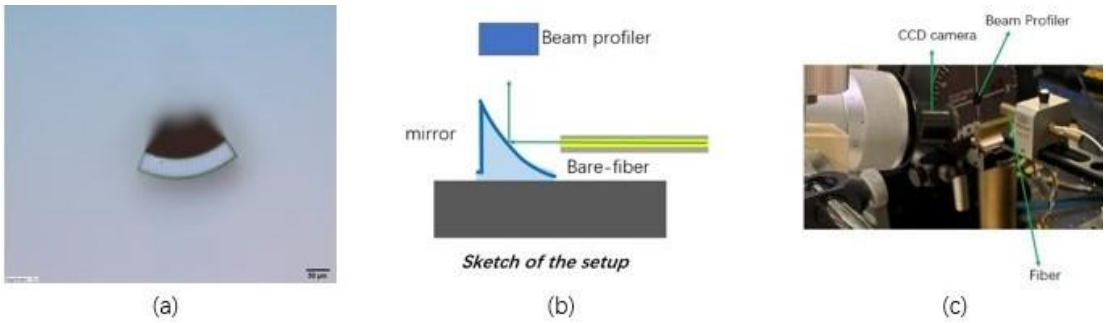


Figure 4.1 (a)Printed mirror with Al film, (b)setup sketch, (c) Picture of setup in OS lab. Unlike the in figure (b), the beam profiler (Thorlabs BP209IR1(/M)) is facing the bare fiber to measure the beam without the chip.

The measurement is performed with a laser wavelength of 980 nm. Bare-fiber beam, side view of the mirror and reflected beam are shown in Figure 4.2.

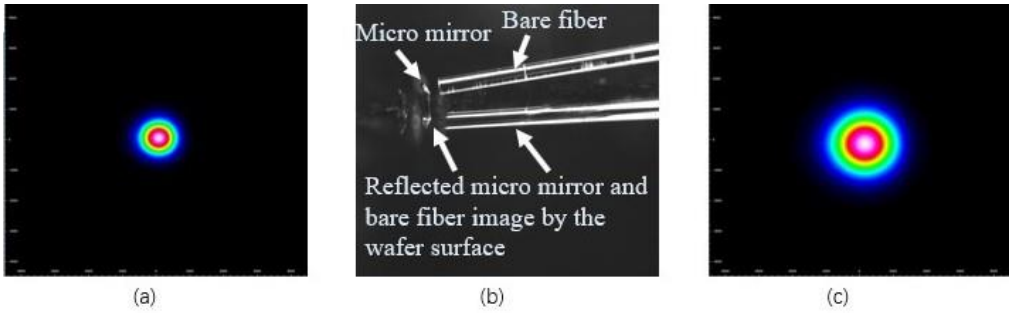


Figure 4.2 (a)Bare fiber beam detected by profiler,(b)Side view of the fiber aligned to the mirror, (c) beam reflected by the mirror.

From Figure 4.2, nice beam shape after reflecting is detected by the beam profiler, which means parabolic mirror here is working as expected and ready for being printed on waveguide chips.

In order to measured mirror reflectivity as a function of Al layer thickness, mirrors with different Al film thickness have be fabricated by evaporation. Figure 4.3 shows simulated reflectivity and experimental results. This is measured with the setup described in Figure 4.2. Where the power reflectivity R is calculated by the power measured with the mirror divide by the power measured without the mirror.

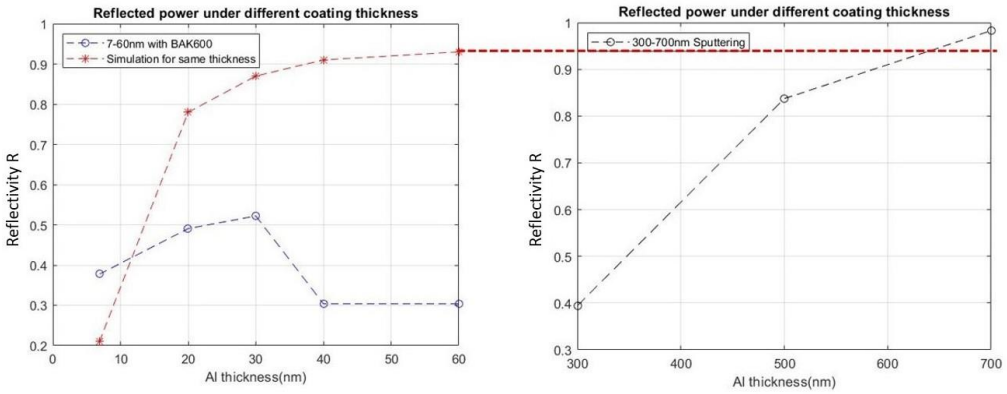


Figure 4.3 Variation of reflectivity at different aluminum film thicknesses: from 7 nm to 700 nm at a wavelength of 980 nm.

When the Al film thickness increases to 30 nm and above, the simulation reflectivity is close to 90%. Unlike the simulation results, the experimental results is quite different: there are large ups and downs. Even with a thickness of 300 nm, reflectivity of 40% may occur which is much lower than simulation results.

At a late stage of this project, we notice the beam profiler we used is not suitable to measure the absolute power of a mode since it has large dependency (~10% - 20%) on the beam location and is divergence angle. Thus the measured results we present in Figure 3.4 is not very conclusive. Its error margin is too large to conclude anything. More reliable power measurement is needed in the future.

4.2 Mirror on-chip with cap

4.2.1 3d printed shadow mask fabrication

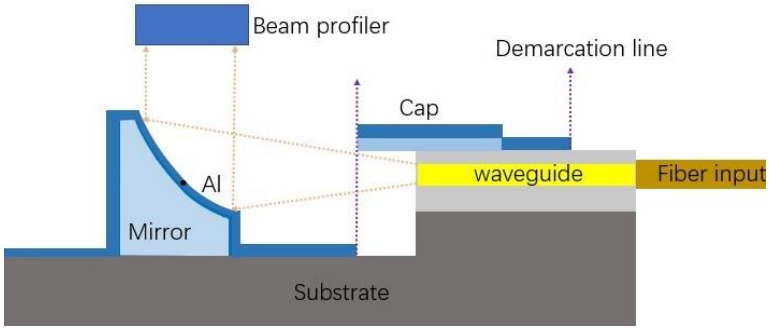


Figure 4.4 Schematic setup for beam detecting

As mentioned in chapter 3.4.2, optical measurements are difficult to conclude anything due to non-optimized fabrication results. Specifically, the waveguide end facet may have Al layer not fully removed, and the mirror surface may not have full Al coverage in case of a bad resist protection. Therefore in order to measure the optical performance of the waveguide and mirror combination, a temporary solution is applied. This is based on a concept of shadow mask deposition, which is a common method used in sputtering and evaporation deposition if a particular local area was wanted to be deposited. This is all based on the fact that sputtering and evaporation are directional from the material source and therefore the area covered by a shadow mask will not have deposition. The basic idea in this project is shown in Figure 4.4.

Instead of making a separate shadow mask, one printed “cap” is introduced to every waveguide end point as shown in Figure 4.5 and Figure 4.7. It extend further than the waveguide end facet to prevent Al deposition on the waveguide end facet. This makes sure that light can exit from waveguide and strike the parabolic mirror. At the same time no further etching process near the mirror could damage the mirror. In this way, caps don’t need to be removed after Al deposition which is a lot less hassle.

For testing proposes, we coupled the light into the waveguide with end facet coupling on one side and measure the output beam reflected by the mirror. Thus the Al on the other end of the waveguide could be removed by dipping half of the chip into the Al etchant as shown in Figure 4.5. Details of the cap shape and how to etch are in Appendix E.

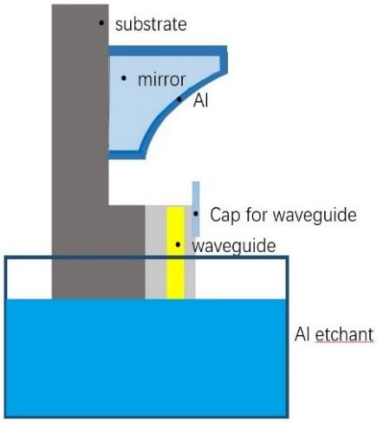


Figure 4.5 Schematic illustration of the approach in vertical position

Overview after deposition is shown in Figure 4.6, Figure 4.7 shows positions of mirrors and caps facing the waveguide.

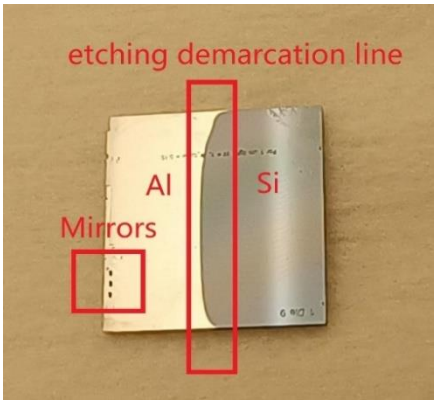


Figure 4.6 Mirrors with caps covered by Al

Another way to protect the other waveguide end is using Kapton tape during deposition to cover half of the chip and extend over the edge of the chip.

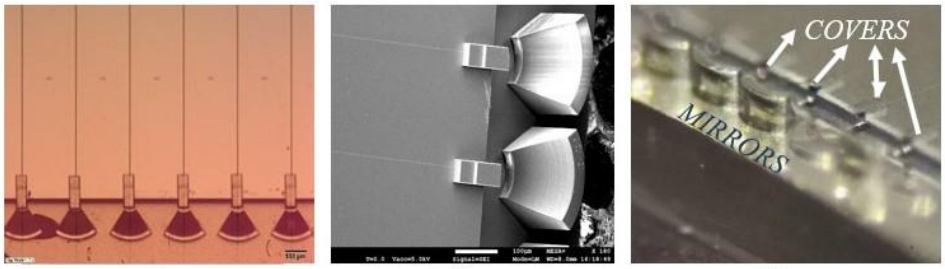


Figure 4.7 (a) Microscope image of mirrors with caps and (b) its SEM image, (c) sideview microscope image

4.2.2 Optical measurement

Light from fiber is coupled into the waveguide as shown in Figure 4.8.

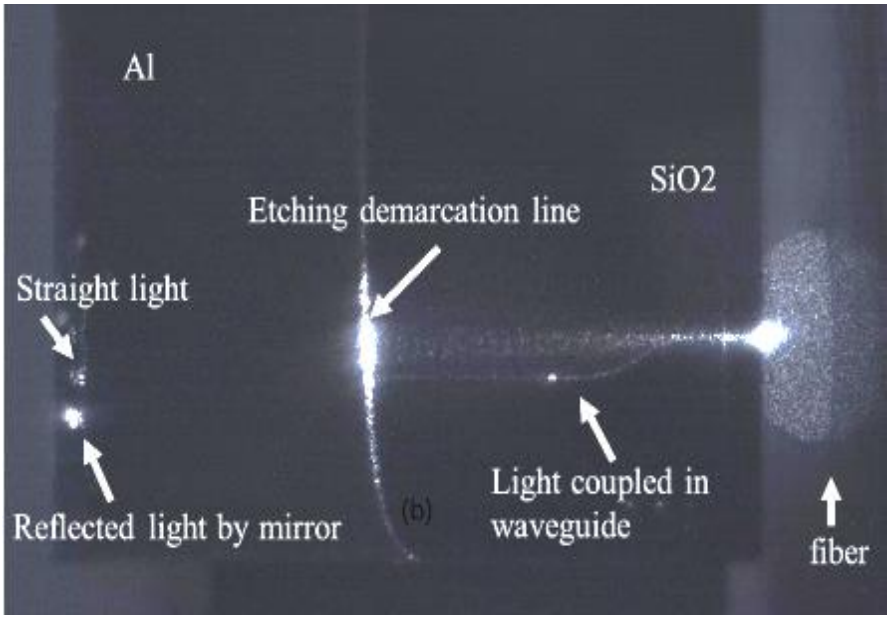


Figure 4.8 Light coupled into waveguide of the chip

A side view (with a shallow angle) is shown in Figure 4.9.

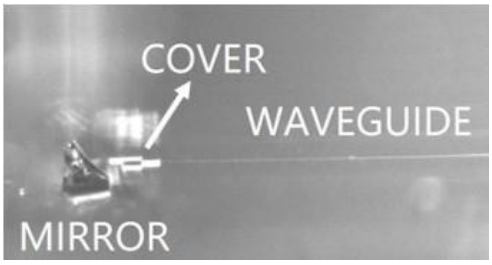


Figure 4.9 Side view of mirrors printed on the substrate with caps without laser on

At wavelength 980 nm, a beam profiler was used to measure the beam shape. The result is shown in Figure 4.10. The shape of the reflected beam is slightly distorted compared to that obtained in figure 4.2 (c). This may be caused by a non-smooth end facet of the etched waveguide.

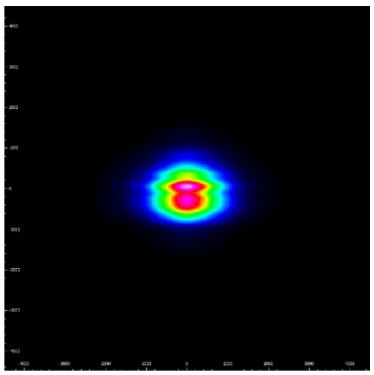


Figure 4.10 Beam shape measured at one distance from the mirror

Then, according to the principle of reversibility of the light path, the light source is directed vertically from the top of the mirror. The light when is reflected by the mirror and enters the waveguide, the other end facet is connected to the power meter. When

laser on, the original power sets at 10 mW, and after transmission through the fiber and an adjustable fiber collimator (Thorlabs CFC2-C), the optical power exiting the fiber is approximately 2mW. Then the light is reflected by the parabolic mirror and coupled into waveguide. On the other side of waveguide, the optical power is measured around 600 µW - 800 µW. This measurement only mean to indicate that the mirror could be used to coupling light into the waveguide but not good enough to determine the best possible coupling efficiency. This is due to the large mode mismatch (about 5 times different between the mode produced by the mirror and the mode produced by the fiber collimator) and may unknow losses, such as mirror reflection losses; end-coupling losses; waveguide taper loss; and waveguide transmission losses, etc. This is why it's needed a more convenient and accurate instrument later to measure the corresponding power and get the desired result.

5 Conclusion and outlook

In this work, we demonstrate the fabrication process and preliminary characterization results of 3D printed micro parabolic mirror on a Si3N4 waveguide chip. It shows the potential to be used for wafer-level testing and inter-chip optical connections.

5.1 Conclusion

The project started with the theoretical structure and fixes the position of the parabolic mirror as well as the equation of the curve by analyzing the various parameters of the Gaussian beam and combining them with the parabolic curve to find the right focal length. The base of the parabolic mirror was also raised according to the depth of the chip groove to ensure that the center of the mirror is roughly at the same level as the end facet of the waveguide.

In chapter 3 by mapping the fabrication process flow, the overall direction of the fabrication and the experimental steps were roughly defined. These included starting by learning Nanoscribe, importing the prepared STL model file; finding the position to be printed by the command; setting the relevant parameters and get the desired and accurate polymer parabolic mirror. The desired aluminum film is then deposited on the parabolic mirror and the chip, either by sputtering or evaporation. Before wet etching, AZ4999 photoresist is sprayed on the mirror surface to protect it from etching. The final chip is obtained with aluminum on the parabolic mirror only, completing the whole fabrication process.

Although the SEM revealed that the positive resist protecting aluminum was not perfectly laminated on the mirror surface and not ideal for optical measurements, it proved the feasibility of the project. Of course, the Nanoscribe will later be too inefficient for mass production of parabolic mirrors on wafer, so a 3d-imprint technique may be introduced to ensure the accuracy of the parabolic shape. We are also confident that these shortcomings will be improved in subsequent studies.

Chapter 4, we build a few optical setups in the OS lab. Measurement results for the beam profile of bare *fiber + the mirror* and *waveguide + mirror* were prosected. The results indicated further waveguide end facet etching optimization is needed to improve the beam shape in case of waveguide + mirror. The mirror reflectivity measurement is not very conclusive at this moment due to photo detectors have large dependency on the beam location and divergence. Better measurement method is need in the future.

5.2 Outlook

Many new ideas have been thought during the project. However, it is not possible to try them all due to the limited time. They are organized in outlook for future projects.

At present, this project has only been completed for structures where the mirror is printed on one side of the waveguide and light coupled into the waveguide on the other side. To achieve true wafer-level testing, mirrors should be present on both sides of the waveguide so that the probes above the chip can scan the array without contact to determine if there is a problem with the waveguide. Therefore, the improvement and detection of the efficiency of the optical coupling after bilateral printing of parabolic mirrors is also one of the directions for future research. For example, beam size collimators, which are more in line with reflections from parabolic mirrors, will be used. New specially designed set-ups will also be built to the measurement group for bilateral mirrors.

When choosing between sputtering and evaporation, we chose evaporation simply by looking at the size of the grain through SEM as shown in Chapter 3.3.2. Although kinetic theoretical calculations show that the deposition rate of Torr at a high pressure and high thickness rate is approximately one tenth of the number of residual gas atoms per second hitting the substrate as aluminum atoms. However, the main component of the residual gas is certainly water vapor, which reacts readily with aluminum to form aluminum oxide and hydrogen gas. In order to reduce the possibility of oxidation during deposition, the deposition of aluminum films in ultra-

high vacuum indicates that evaporation is a good method[38]. However, as a more precise measurement, the subsequent use of AFM to observe roughness would be a good approach.

In this project, wet etching or waveguide cover cap are chosen. We could further optimize this wet etching process. However, there are also other options such as lift-off or wafer scale shadow mask for Al layer patterning. The ideas are described a bit more in detail in Appendix B.

Acknowledgements

As I approach the end of my report, I can't calm down for a long time. As my master at UTwente draws to a close, all the experiences I have had during this period come back to me. I would like to thank the university for the training I have received and for the fact that this is the last time in my life as a student before I enter the real world of work.

The project was completed under the careful guidance of UT supervisor prof.dr.ir. H.L. Offerhaus (Herman)and Daily supervisor dr. L. Chang (Lantian). The weekly process meetings kept the professors informed and interested in the progress of my project, discussing the possibilities of each step of the experiment and building the experimental platform together to get the data. Their love and seriousness for

scientific research has set an example for me to strive for in my future life. I would therefore like to express my deepest gratitude to them.

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At the same time, all the OS members, especially Meindert and Frans, have given me a lot of advice and help with my experiments. I also received a lot of help from the MESA+ staffs, whether it was training courses on the instrumentation or discussing and finding better solutions when I encountered problems, they were all very helpful and interested in the progress of my project. I am very impressed and wish them all the best in their future endeavors.

Finally, I would like to thank my family and friends who have given me so much encouragement and relief for staying Netherland and studying alone, which has motivated me to continue my studies.

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Appendix A

In Lumerical, waveguide and simulation zone is set

Change the width (150 µm, 250µm, 400 µm)of the waveguide taper in turn to simulate different beam mode and shape. Simulation structure is shown in Figure A.1.

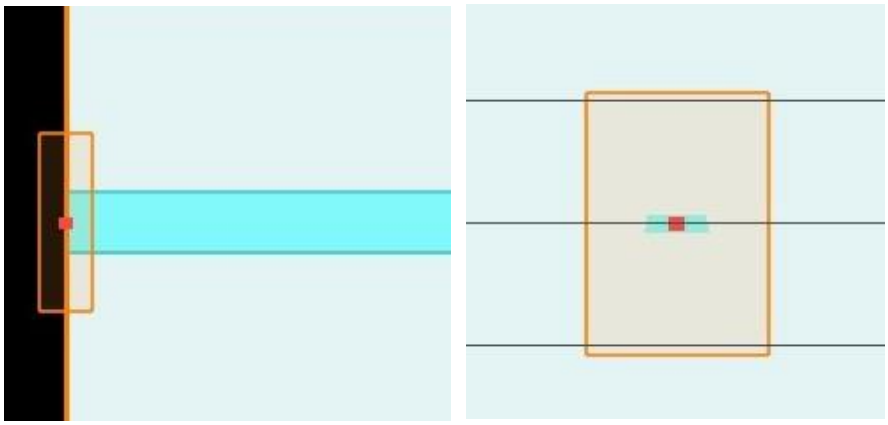


Figure A.1 Si_3N_4 Waveguide with SiO2 cladding

Then, come to **Modal analysis→ Far field settings→ projection method(planar)→ projection distance(50, 75, 100) µm** for recording the beam diameter and mode shape, which is shown in Figure A.2 to A.10.

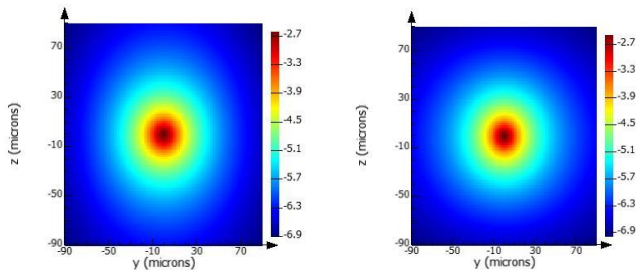


Figure A.2 1/e^2 Mode beam with taper width 150 nm from a distance 50 µm (TE, TM)

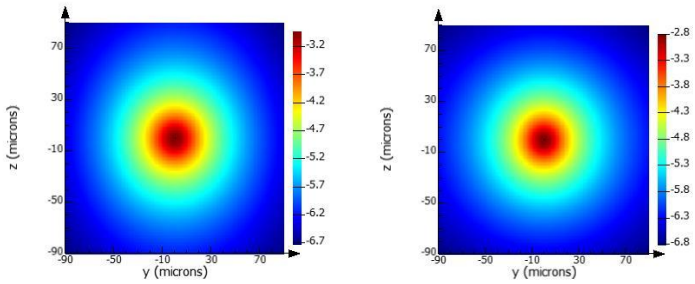


Figure A.3 1/e^2 Mode beam with taper width 150 nm from a distance 75 µm (TE, TM)

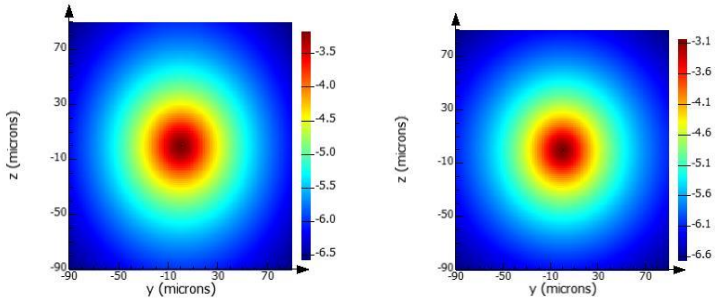


Figure A.4 1/e^2 Mode beam with taper width 150 nm from a distance 100 µm (TE, TM)

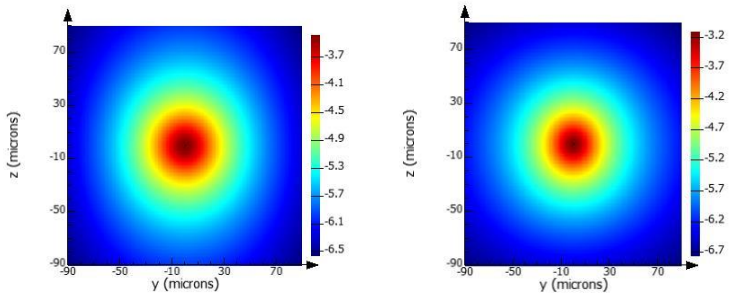


Figure A.5 1/e^2 Mode beam with taper width 250 nm from a distance 50 µm (TE, TM)

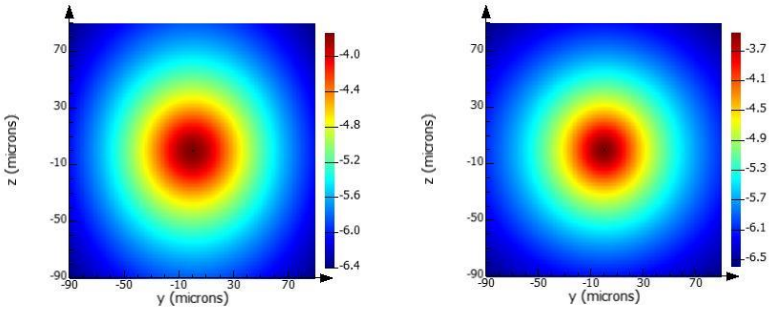


Figure A.6 1/e^2 Mode beam with taper width 250 nm from a distance 75 µm (TE, TM)

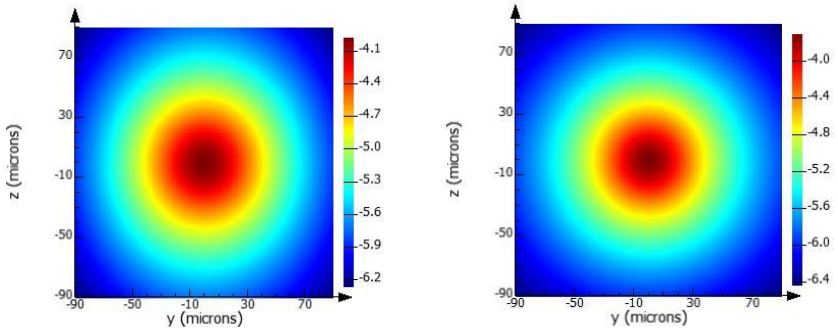


Figure A.7 1/e^2 Mode beam with taper width 250 nm from a distance 100 µm (TE, TM)

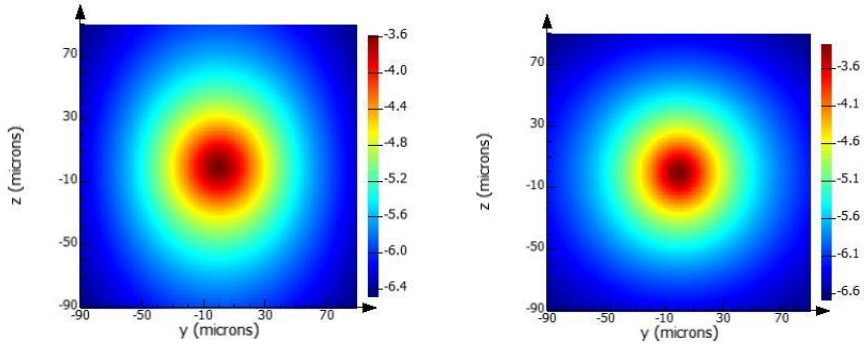


Figure A.8 1/e^2 Mode beam with taper width 400 nm from a distance 50 µm (TE, TM)

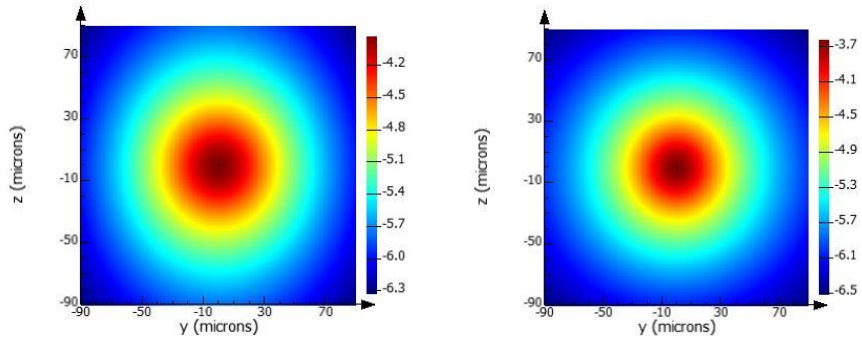


Figure A.9 1/e^2 Mode beam with taper width 400 nm from a distance 75 µm (TE, TM)

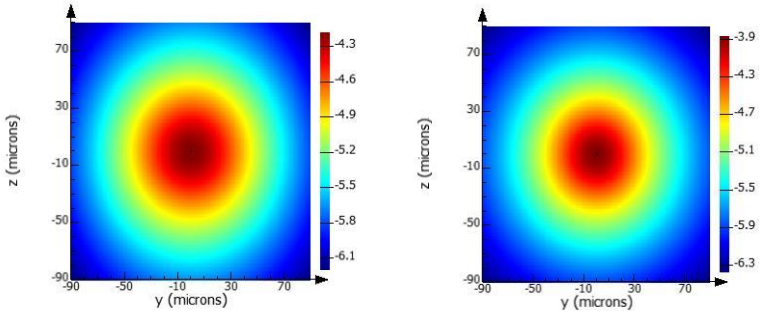


Figure A.10 1/e^2 Mode beam with taper width 400 nm from a distance 100 µm (TE, TM)

Appendix B

B.1 Lift-off

It is a method of creating a target material structure (patterning) on the surface of a substrate (e.g. a wafer) using a sacrificial material (e.g. photoresist). This is shown in Figure B.1. Using this method in this project, as the LOR is isotropic, then it is possible that all of the Al deposited outside the parabolic mirror will be removed, a possibility that will be explored in the future.

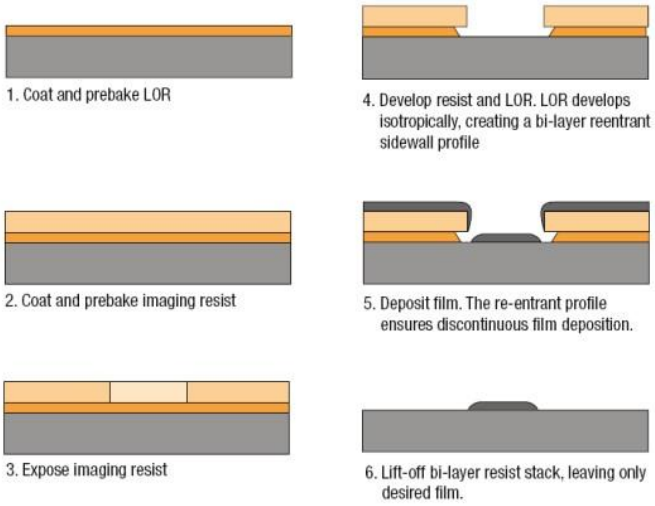


Figure B.1 Metal lift-off process flow

B.2 Shadow mask

It is a common method used in sputtering and evaporation deposition if a particular local area was wanted to be deposited. This is all based on the fact that sputtering and evaporation are directional from the material source and therefore the area covered by the shadow mask will stay away from metal film. Basic idea of shadow mask is shown in Figure B.2.

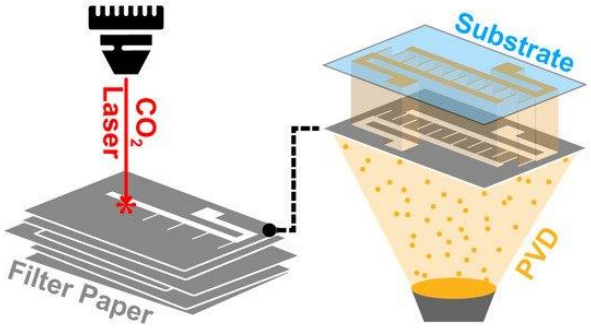


Figure B.2 The laser-cut paper, placed between a PVD materials source and a substrate, functions as a shadow mask for pattern transfer[39].

The basic concepts have been introduced in chapter 4.2. This approach is also a challenge for micron-sized parabolic mirror structures, as we want to ensure that the graphics are aligned precisely in use. It is also difficult to use shadow masks spaced some distance apart because the parabolic mirror is above the waveguide plane.

B.3 Detailed version of fabrication process flow

ILP: In-line Processing	MFP: Metal-free Processing	UCP: Ultra Clean Processing	Removal of Residues

Step	Level	Process/Basic flow	User com

				ments
1		**Substrate silicon with 8µm SiO2** (#subs119)	**NL-CLR-Wafer Storage Cupboard** Orientation: <100> Diameter: 100mm Thickness: 525µm Polished: Single side (OSP) Resistivity: 5-10Ωcm Type: p/Boron Thermal oxide: 8 µm SiO2	
		film1207: LPCVD of Si3N4 (H2)		
2	MFP	**System monitoring** (#spc001)	**NL-CLR-FURNACES** Purpose: monitoring the stability of the furnaces in terms of deposition rate, non-uniformity and optical parameters. Procedure: 1. Take a Silicon wafer from the wafer box with monitor wafers 2. Fill in the digital logbook and write down the last 4 digits of the waferID in the User Comment 3. Write down the run number on the lid of the waferbox	
3	MFP	**Cleaning in 99% HNO3** (#clean001)	**NL-CLR-WB14 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
4	MFP	**Cleaning in 99% HNO3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
5	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
6	MFP	**Cleaning in 69% HNO3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO3 • Temperature: 95°C • Time: 10min	
7	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode	

			Cascade = Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
8	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** **Optional drying step**. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.
9	MFP	**Etching in 1% HF** (#etch127)	**NL-CLR-WB15 Beaker 1** Purpose: remove native SiO2 from Silicon. Chemical: 1% HF • Temperature: room temperature • Time: 1min **This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).**
10	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
11	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.
12	MFP	**Loading of wafers** (#film217)	**NL-CLR-LPCVD FURNACES** Purpose: loading of wafers Program: UN-/LOAD Rules: 1. Start the UN-/LOAD program after cleaning 2. Let the filler wafers cool down for 5 minutes

			3. Load your wafers within 30 minutes 4. Place the monitor wafer in the center of the wafer carrier 5. Always use a full wafer load COMPLY TO THESE RULES FOR MAINTAINING THE LPCVD FURNACE.	
13	MFP	**LPCVD of Si3N4** (#film207)	**NL-CLR-H2 FURNACE** Application: deposition of stoichiometric Silicon Nitride. Program: NITRFLEX **RESTRICTION**: maximum thickness is 300nm. **Settings:** • SiH2Cl2 flow: 25sccm • NH3 flow: 250sccm • N2 flow: 200sccm • Temperature: 745°C (zone 1), 750°C (zone 2-3) • Pressure: 150mTorr Load your wafers within 4 hours after cleaning!	200 nm
14	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
15	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		E-beam lithography		
16	ILP	Dehydration bake (#litho001)	**NL-CLR-WB21/22** Dehydration bake at hotplate • Temp.: 120°C • Time: 5min	

17	ILP	**Priming HMDS (liquid)** (#litho600)	**NL-CLR-WB23** Primer: HexaMethylDiSilazane (HMDS) Use spincoater: • program: 4000 (4000rpm, 45sec)
18	ILP	**Coating of AR-N7520.18**	**NL-CLR-WB23** Coating: Primus spinner • ARN7520.18 (1.5 mL with pipet) • Spin program: 1000 180 (1000rpm, 180sec) (800 nm resist) • Spin program: 1500 180 (1000rpm, 180sec) (650 nm resist) Prebake: hotplate • Time: 60 sec • Temp.: 85 °C
19	ILP	**Coating of AR-PC5091**	**NL-CLR-WB23** Coating: Primus spinner • AR-PC 5090 (1.5 mL with pipet) • Spin program: 2000 45 (2000rpm, 45sec) Prebake: hotplate • Time: 120 sec • Temp.: 50 °C
20	ILP	**Exposure Raith-EBPG5150**	**NL-CLR-RaithEBPG5150** • Dose 1000 µC/cm^2 (for 800 nm resist) • Dose 800 µC/cm^2 (for 650nm resist) • Choose beam current to stay below 100 MHz
21	ILP	**Development of ARN-7520.18**	**NL-CLR-Ebeam wetbench26** Development: AR300-47 • Beaker 1: 30sec (dirty) • Beaker 2: 30sec (clean)
22	ILP	**Quick Dump Rinse (QDR)** (#rinse001)	**NL-CLR-Wetbenches** Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
23	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (no purge) 2. Use the nitrogen gun (fragile wafers or small samples)
etch1775: Directional RIE of Si3N4 by CHF3/O2 Plasma (PT790)			
24	UCP	**Etching of Si3N4** (#etch222)	**NL-CLR-PT790** Settings:

CHF_3 flow: 100 sccm
O_2 flow: 9 sccm
Pressure: 40 mTorr
Power 250W

Etch rate: Si3N4: 60 nm/min - SiO2: 32 nm/min - SiRN: 40nm/min

25 UCP **Chamber clean (PT790)** (#etch199)

NL-CLR-PT790
Application: removal of organic and fluorocarbon residues from the chamber wall.

- Graphite electrode
- O_2 flow: 100sccm
- Pressure: 100mTorr
- Power: 400Watt

Note: always clean the chamber after etching!

26 ILP **Stripping of Resists** (#strip101)

NL-CLR-TePla360
Application: stripping of resist by O2 plasma. **WARNING**: in case of stripping of resist on chromium, then use recipe 041 on the TePla360 (strip1130)!

Step	O2 (sccm)	Ar (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0.6	1000	0:10:00
Stripping of resist	360	160	0.6	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 011: time = 10min
Recipe 012: time = 20min
Recipe 013: time = 30min
Recipe 014: time = 40min
Recipe 016: time = 60min

BACKUP: If the TePla360 is down, contact the administrator on how to continue your processing on the TePla300.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
- continue with UCP processing
- continue with high-temperature processing (MFP)

27 Rem Res **Removal of metal traces in RCA-2** (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

- cleaning in the Pre-Furnace Clean (WB14-MFP)
- processing in the Ultra-Clean Line - Front End (WB12-UCP)
- processing in the Ultra-Clean Line - Back End (WB13-

			UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.
28	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
29	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
		film1208: LPCVD of SiO2 (H3)	
30	MFP	**System monitoring** (#spc001)	**NL-CLR-FURNACES** Purpose: monitoring the stability of the furnaces in terms of deposition rate, non-uniformity and optical parameters. Procedure: 1. Take a Silicon wafer from the wafer box with monitor wafers 2. Fill in the digital logbook and write down the last 4 digits of the waferID in the User Comment 3. Write down the run number on the lid of the waferbox
31	MFP	**Cleaning in 99% HNO3** (#clean001)	**NL-CLR-WB14 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3

			• Time: 5min
32	MFP	**Cleaning in 99% HNO3** (#clean002)	**NL-CLR-WB14 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min
33	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
34	MFP	**Cleaning in 69% HNO3 at 95 °C** (#clean003)	**NL-CR-WB14 BEAKER 3A/3B** Purpose: removal of metallic traces. Chemical: 69% HNO3 • Temperature: 95°C • Time: 10min
35	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
36	MFP	**Substrate drying (WB14)** (#dry022)	**NL-CLR-WB14** **Optional drying step**. After the QDR, you can transfer your substrates directly to a Teflon carrier and strip the native SiO2 in 1% HF (WB15). **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.
37	MFP	**Etching in 1% HF** (#etch127)	**NL-CLR-WB15 Beaker 1** Purpose: remove native SiO2 from Silicon. Chemical: 1% HF • Temperature: room temperature • Time: 1min

			This step is obligatory for the MESA+ monitor wafer (if applicable, see Equipment database).
38	MFP	**Rinsing** (#rinse002)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
39	MFP	**Substrate drying (WB15)** (#dry023)	**NL-CLR-WB15** **Single substrate drying:** 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge). 2. Use the nitrogen gun (fragile wafers or small samples). **Batch drying of substrates:** Use the Semitool for drying up to 25 substrates at once.
40	MFP	**Loading of wafers** (#film217)	**NL-CLR-LPCVD FURNACES** Purpose: loading of wafers Program: UN-/LOAD Rules: 1. Start the UN-/LOAD program after cleaning 2. Let the filler wafers cool down for 5 minutes 3. Load your wafers within 30 minutes 4. Place the monitor wafer in the center of the wafer carrier 5. Always use a full wafer load COMPLY TO THESE RULES FOR MAINTAINING THE LPCVD FURNACE.
41	MFP	**LPCVD of SiO2 (TEOS)** (#film208)	**NL-CLR-H3 FURNACE** Application: deposition of SiO2. Program: TEOS03 **RESTRICTION**: maximum thickness is 1.2µm. Settings: • TEOS flow: 40sccm • N2 flow: 30sccm • Temperature: 725°C (zone 1-2), 730°C (zone 3) • Pressure: 200mTorr Load your wafers within 4 hours after cleaning!
42	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator

			in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.	
43	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.	
		therm1102: Densification of PECVD Oxford 80 capping on Ta/Pt electrodes (B3)		
44	ILP	**Cleaning in 99% HNO3** (#clean005)	**NL-CLR-WB16 BEAKER 1** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
45	ILP	**Cleaning in 99% HNO3** (#clean006)	**NL-CLR-WB16 BEAKER 2** Purpose: removal of organic traces. Chemical: 99% HNO3 • Time: 5min	
46	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	
47	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
48	ILP	**Densification of PECVD coatings** (#therm139)	**NL-CLR-E2 FURNACE** Application: densification of PECVD capping on Ta/Pt electrodes. Program: ANOX950 Settings: • Standby temperature: 400°C • Temperature: 950°C • N2 flow: 4slm* • Ramp: 10°C/min	3 hrs 1100

			Please mention the following setting in the User Comments: • Time: .....min * Check that the time for O2 is set to 0:00:00.
film1405: PECVD of SiO2 for PZT processing (Oxford80)			
49	ILP	**PECVD of SiO_2** (#film401)	NL-CLR-OXFORD Plasmalab 80 + Apply purge sequence before and after use Purge sequence: 1 min N_2, pump down, apply three times Parameters: • Electrode temp. = 300°C • 2% SiH_4/N_2 flow = 200sccm • N_2O flow = 710sccm • pressure = 650mTorr • APC = 33 • power LF = 60W • Deposition rate= xx nm/min
50	ILP	**Chamber clean Oxford 80 PECVD** (#film400)	NL-CLR-Oxford 80 PECVD • Chamber clean
51	ILP	**Layer thickness measurement** (#metro401)	**NL-CLR-WOOLLAM-2000UI ELLIPSOMETER** Consult the user manual to perform a single point or a raster measurement. Use one of the available optical models to determine the layer thickness and optical constants of the coating on your substrate. Provide the following results in the digital logbook: thickness, refractive index (n) at 632.8nm and the nonuniformity of the layer (%range) of a 5-point scan.
52	ILP	**Particle inspection** (#metro201)	**NL-CLR-Cold Light Source (SEM room)** Shine the light onto the surface at an angle in a dark room to check for particles, haze and scratches in the coating(s) on the substrate. Please warn the administrator in case a thermal SiO2 or LPCVD coating contains a lot of particles! Contact Christaan Bruinink for questions.
litho1802: Lithography of Olin Oir 908-35 (positive resist - ILP)			
53	ILP	**HMDS priming** (#litho600)	**OPTION 1 Liquid HMDS priming** **NL-CLR-WB21/22 HOTPLATE** Purpose: dehydration bake Settings: • Temperature: 120°C • Time: 5min After the dehydration bake, perform the liquid priming with minimum delay! **NL-CLR-WB21 Primus SB15 Spinner**

			Primer: HexaMethylDiSilazane (HMDS) Settings: • Spin mode: static • Spin speed: 4000rmp • Spin time: 30s **OPTION 2 Vapor HMDS priming** **NL-CLR-WB28 Lab-line Duo-Vac Oven** Primer: HexaMethylDiSilazane (HMDS) Settings: • Temperature: 150°C • Pressure: 25inHg • Dehydratation bake: 2min • HMDS priming: 5min CAUTION: let the substrates cool down before handling with your tweezer!	
54	ILP	**Coating of Olin OiR 908-35** (#litho102)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 908-35 Spin program: 4000 Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s	
55	ILP	**Prebake of Olin OiR 908-35** (#litho004)	**NL-CLR-WB21 PREBAKE HOTPLATE** Purpose: removal of residual solvent from the resist film after spin coating. Settings: • Temperature: 95°C • Time: 120s	After this the previous step is repeated
56	ILP	**Alignment & exposure of Olin OiR 908-35** (#litho302)	**NL-CLR- EV620 Mask Aligner** Settings: • Hg lamp: 12mW/cm ^{2} • Exposure time: 9sec	Used 50 seconds for exposure
57	ILP	**After exposure bake of Olin OiR resists** (#litho005)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 60s	
58	ILP	**Development of Olin OiR resists** (#litho200)	**NL-CLR-WB21 DEVELOPMENT BEAKERS** Chemical: OPD4262 • Beaker 1: 30sec • Beaker 2: 15-30sec	
59	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents.	

			Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
60	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
61	ILP	**Postbake of Olin OiR resists** (#litho008)	**NL-CLR-WB21 POSTBAKE HOTPLATE** Purpose: Settings: • Temperature: 120°C • Time: 10min
62	ILP	**Inspection by Optical Microscopy** (#metro101)	**NL-CLR-Nikon Microscope** Use the Nikon microscope for inspection.
		etch1600: Directional Etching of SiO2 by C4F8/He/CH4 Plasma (AdixenDE)	
63	ILP	**Plasma Etching of SiO_2** (#etch157)	**NL-CLR-AdixenDE** Application: directional etching of SiO2 at a layer thickness < 5 µm. SH Temp: -10°C - Pos: 120mm - He pres: 10 mbar Flows C4F8: 20sccm - CH4: 15sccm - He: 150 sccm Pressure: 8.5 10^{-3} mbar ICP: 2800 Watt CCP: 350 Watt (RF) Etch rate SiO2: 470-510 nm/min SiRN: variable Olin OiR resists: 150 nm/min
64	ILP	**Chamber clean (AdixenDE)** (#etch201)	**NL-CLR-AdixenDE** Chamber clean to remove fluorcarbon NEEDED after every 20 min processing SH Temp: any- Pos: 150mm - He pres: 10 mbar Flow O2: 200 sccm APC: 100% / Pressure: 1.5 10^{-2} - 6.0*$10^{-6.5}$ mbar ICP: 2000 Watt CCP: 50 Watt (RF) Clean with a plain Si wafer in the etch tool Cleaning time: 30 minutes

65 ILP

Stripping of Resists (#strip100)

NL-CLR-TePla300
Application: stripping of resists by O2 plasma after plasma etching.

PLEASE NOTE

1. RESTRICTION: do not strip resists on chromium in the TePla300, but instead use the TePla360 (choose: recipe 041).
2. BACKUP: TePla300 down? Contact the administrator if you can continue your processing in the TePla360.

Step	O2 (sccm)	N2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	500	1.0	800	0:10:00
Stripping of resist	500	0	1.0	800	*

* Select one of the following recipes to strip the resist, depending on the thickness of the resist, treatment of the resist and the number of wafers. Use the abort option in the last step if you sample requires a shorter stripping time.

Recipe 01: time = 10 min
Recipe 02: time = 30 min
Recipe 04: time = 60 min

66 Rem Res

Removal of metal traces in RCA-2 (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-UCP)
• processing in the Ultra-Clean Line - Back End (WB13-UCP)

Chemicals: HCl:H2O2:H2O (1:1:5 vol.%)

PLEASE NOTE

1. CAUTION: do not process substrates with metal patterns in RCA-2.
2. NO REUSE: reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09.

Procedure:
• Pour 1500ml* of DI water into the beaker
• Turn on the stirrer
• Add 300ml* of Hydrogen Chloride (HCl)
• Heat up the solution to 70°C (setpoint heater = 80°C)
• Slowly add 300ml* of Hydrogen Peroxide (H2O2)
• Submerge your samples as soon as the temperature is above 70°C
• Time = 15min

This process is skipped (after Silcion etch)

			* Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.	
67	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.	This process is skipped (after Silcion etch)
68	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	This process is skipped (after Silcion etch)

etch1652: DRIE of silicon: Bosch HARS (SPTS Pegasus)

69 ILP

DRIE of silicon (HARS)
(#etch218)

NL-CLR-SPTS Pegasus
Application: Bosch HARS standard recipe for micro structures from 3-100 µm.
Scallop size: 350 nm. Use SiO2 as the etch mask (no/less retraction).
Recipe: #B-HARS @20degC #etch218

Settings:
• Platen temp: 20°C
• He pressure 20 Torr

Step (in order)	Deposition	Break	Etch
Time (sec)	0.5		1.75
C4F8 flow (sccm)	150		0
SF6 flow (sccm)	0		275
APC (mTorr/%valve)	20mTorr		26mTorr
ICP (W)	2000		2200
CCP – LF (W)	0		20-30 (ramp)
Duty cycle LF (%)	20		20

Check the process sheet for settings and details: https://mesaplusnanolab.ewi.utwente.nl/mis/generalinfo/downloads/usermanuals/268/Process%20sheet%20-%20SPTS%20-%20Hars%20[etch218]%20sept%202018.pdf

70 ILP

Chamber - Chuck Clean
(#etch219)

NL-CLR-SPTS Pegasus
Application: removal of organic and fluorocarbon residues from the chuck and chamber wall.
Recipe: #A-Clean after use #etch219

Parameters:
O2 flow: 200sccm

Pressure: 5mTorr
ICP: 2500W
CCP: 20W (RF)
Time: 15min

Note: after cleaning the substrate holder temp will be set to 20°C. Perform this recipe at the moment you are done etching.

71 ILP

Stripping of Resists and Fluorocarbon (#strip104)

WARNING - PLEASE READ
This recipe is efficient for stripping of fluorocarbon in microstructures with aspect ratios < 5. Contact the administrator in case you want to strip fluorocarbon in microstructures with aspect ratios > 5 or fluorocarbon in nanostructures. This recipe attacks silicon and nitride coatings on the nanometer scale!

NL-CLR-TePla360
Application: stripping of resists and fluorocarbon after DRIE BOSCH processing by O2/CF4 plasma.

Step	O2 (sccm)	Ar (sccm)	CF4 (sccm)	H2 (sccm)	P (mbar)	Power (W)	Time (h:mm:ss)
Preheating	0	600	0	0	0.6	1000	0:10:00
Resist stripping	250	0	0	0	0.5	800	*
Fluorocarbon stripping	237	0	13	0	0.5	800	0:01:00
Residual Fluorocarbon stripping	250	0	0	0	0.8	800	0:01:00

* Select one of the following recipes depending on the thickness of the resist, treatment of the resist and the number of wafers.

Recipe 035: time = 10min
Recipe 037: time = 20min
Recipe 036: time = 60min

BACKUP: The TePla300 is not a backup for this processing! If the TePla360 is down, contact the administrator.

PLEASE NOTE It is mandatory to remove metal traces originating from plasma tools in RCA-2 (residue1505), e.g. plasma etching or stripping in O2 plasma, in case you:
• continue with UCP processing
• continue with high-temperature processing (MFP)

72 Rem Res

Removal of metal traces in RCA-2 (#residue504)

NL-CLR-WB09
Purpose: removal of metal traces originating from plasma tools in order to protect the cleaning efficiency of the wet benches. For this reason, RCA-2 is compulsory in case you continue:

• cleaning in the Pre-Furnace Clean (WB14-MFP)
• processing in the Ultra-Clean Line - Front End (WB12-

			UCP) • processing in the Ultra-Clean Line - Back End (WB13-UCP) Chemicals: HCl:H2O2:H2O (1:1:5 vol.%) **PLEASE NOTE** **1. CAUTION**: do not process substrates with metal patterns in RCA-2. **2. NO REUSE:** reuse of RCA-2 is forbidden! Contact the administrator in case there is no empty RCA-2 beaker available in WB09. Procedure: • Pour 1500ml* of DI water into the beaker • Turn on the stirrer • Add 300ml* of Hydrogen Chloride (HCl) • Heat up the solution to 70°C (setpoint heater = 80°C) • Slowly add 300ml* of Hydrogen Peroxide (H2O2) • Submerge your samples as soon as the temperature is above 70°C • Time = 15min * Use a glass graduated cylinder of 500ml to measure the volume of the chemicals.
73	ILP	**Rinsing** (#rinse001)	**NL-CLR-WBs QDR** Purpose: removal of traces of chemical agents. Choose one of the two rinsing modes: **QDR =** Quick dump rinsing mode **Cascade =** Overflow rinsing mode for fragile substrates Rinse until message ´End of rinsing process´ is shown on the touchscreen of the QDR, else repeat the rinsing process.
74	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)
		back1102: Dicing for optics (Loadpoint)	
75	ILP	**Coating of Olin OiR 908-35** (#litho102)	**NL-CLR-WB21 PRIMUS SB15 SPINNER** Resist: Olin OiR 908-35 Spin program: 4000 Settings: • Spin mode: static • Spin speed: 4000rpm • Spin time: 30s
76	ILP	**Dicing foil Nitto SWT 10** (#back103)	NL-CLR dicingroom Nitto SWT 10 dicing foil

77	ILP	**UV dicing foil (Adwill D-210)** (#back104)	Nl-CLR- Dicing foil Information: Thickness: 125um Material: 100um PET + 25um Acrylic (adhesive) Adhesion before UV: 2000 mN/25mm Adhesion after UV : 15 mN/25mm UV irradiation : Luminance > 120mW/cm^2 and Quality > 70mJ/cm^2 (wave length: 365nm)
78	ILP	**Dicing of silicon wafer for optics** (#back106)	**Nl-CLR- Loadpoint (only) dicing saw** Applications: Silicon wafers with cross section suitable for optics (max 700µm) Apply wafer on foil **Parameters dicing**: Wafer work size: 110 mm for a standard 100 mm silicon wafer Feed speed: 0.5mm/sec for smooth cut (maximum is 2mm/sec) X, Y values: correspond respectively to Ch1 and Ch2 and those values are determined by mask layout Saw type F1230 **Blade info:** Exposure: 700µm (maximum dicing depth for a new blade) Width: 30um Spindle revolutions: 30. 000rpm **Depth settings:** Maximum cut depth: 700µm Foil thickness: See foil info Minimum blade heigth: 50 µm
79	Rem Res	**Removal of particles (#**residue204)	**NL-CLR-WB06** Purpose: removal of particles after encoding and cleaving by ultrasonication. Use the ultrasonic bath in WB06. • Beaker: DI-water, 10 min. Please use the appropriate carrier
80	ILP	**Substrate drying** (#dry001)	**NL-CLR-WBs (ILP)** Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)

B.4 Measurement of etch part of chip

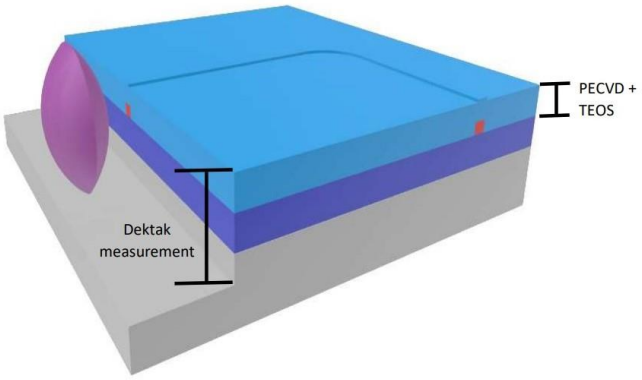


Figure B.2 Description and measurement of the composition of the three layers

Dektak Measurement:
Its known that the silicon etch has non Uniformity. It might needed to measure each etch depth locally. For 3 dies a local measurement is performed using the dektak profilometer. The following depth is measured:
1.3 DIE 1 69.442 nm
1.3 DIE 2 70.120 nm
1.55 DIE 1 69.673 nm
These measurements represents the Dektak measurement in the picture.

PECVD + TEOS:
To get information about the cladding thickness and therefore the location of the waveguide dummy samples where grown in the process together with the device wafer. Elipsometric measurements over the surface gives the thickness of Annealed TEOS and gives the thickness of the PECVD Oxide.

The measurement is done using a standard 25 points surface scan. For The PECVD layer the most outer points measurement failed because the tool could not find the right sample leveling.

The following average thickness has been measured:
TEOS 1.035 ± 25 nm (Woollam surface scan over 25 points)
PECVD 7.718 ± 95 nm (Woollam surface scan over 17 points)

Both layers represent the total cladding over the etched waveguides. Indicated as PECVD + TEOS in the picture.

Appendix C

After Solidworks model is imported into Describe(one software for Nanoscribe to modify printing parameters), it is needed to follow the steps to refine your model as shown in Figure C.1. Then job and data file are automatically generated. As shown in *Code 2*, *Code 3*. At the same time, the estimated print time is also displayed to help with print plan.

Code 2:Job file

```
% File generated by DeScribe 2.6
```

```
% System initialization
InvertZAxis 1

% Writing configuration
GalvoScanMode
ContinuousMode
PiezoSettlingTime 10
GalvoAcceleration 10
StageVelocity 200

% Scan field offsets
XOffset 0
YOffset 0
ZOffset 0

% Writing parameters
PowerScaling 1.0

% Solid hatch lines writing parameters
var $solidLaserPower = 100
var $solidScanSpeed = 100000

% Base writing parameters
var $baseLaserPower = $solidLaserPower
var $baseScanSpeed = $solidScanSpeed

var $interfacePos = 0.5

% Include slicer output
include 0111_3_strcture_data.gwl
```

In job file, ScanSpeed and LaserPower are available to change. All can be modified to suit specific needs.

Code 3: data file Indicates the exact position of the print stage and the depth at which the z-axis begins to print, which plays a decisive role in finding the height of the mirror base to be printed into the substrate recall the Figure 2.9.

```
% File generated by DeScribe 2.6
%
% Creation time
%   2022-01-11T19:26:55+01:00
%
% Source file
%   Type: Mesh
%   Path: C:\Users\s2235617\Desktop\practice\solid\0111_3_strcture.STL
%
% Volume
%   0.00161 mm³
```

```
%
% Bounding box
%   Minimum X: -109.873 Y: -100 Z: 0
%   Maximum X: 109.873 Y: 100 Z: 136.849
%
% Transformation
%   Scaling X: 1 Y: 1 Z: 1
%   Rotation X: 0.5 Y: 0.5 Z: 0.5 W: 0.5
%   Translation X: -115.873 Y: -113.494 Z: 0
%
% Slicing
%   SlicingMode: Adaptive
%   Distance Max: 0.2 Min: 0.1
%   SlopeEvaluation: 1
%   SurfaceNormals: 0
%   VoxelAspectRatio: 6
%   SimplificationTolerance: 0.05
%   FixSelfIntersections: on
%
% Hatching
%   HatchingDistance: 0.3
%   HatchingAngle: auto
%
% Splitting
%   Mode: Rectangular
%   BlockSize X: 285 Y: 285 Z: 137
%   Offset X: 142.5 Y: 142.5 Z: 0
%   Shear: 15
%   Overlap: XY: 2 Z: 1
%   BlockWidth X: 323.977 Y: 323.977 Z: 138
%   BlockOrder: Lexical
%   AvoidFlyingBlocks: on
%   GroupBlocks: on
%   BacklashCorrection: on
%
% Output options
%   HatchLines: OneWay
%   ZAxis: Piezo
%   Exposure: Variable
%   InvertZAxis: on
%   WritingDirection: Up
%   ScanMode: Galvo
%   WritingOrder: ContourFirst
%
```

FindInterfaceAt **$interfacePos**

% BLOCK 0|0|0

include 0111_3_strcture_files\0111_3_strcture_0_0_0.gwl

According to these 2 files, one printing model is shown in Figure C.1. And one short video shows how it works(only works in Word).

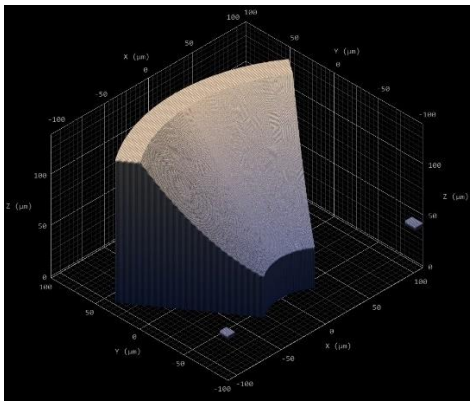
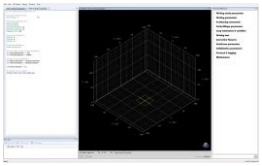


Figure C.1. Parabolic mirror with markers in Describe



Video for printing mirror process

There are 2 methods to explore the shape and size we print through Nanoscribe.

Method 1: Bruker WLI Contour GT-I --- White light interferometry tool. Optical profiler which can create 2D/3D picture of a surface of 2 x 1.7 mm2 (2.5X) down to 10 x 10 um2 (230X). Complementary tool to Dektak stylus profiler.

Figure C.2 White light interferometry in NanoLab

A white light interferometer is an optical instrument that uses the principle of interference to measure the difference in light range to determine the physical quantity in question. Any change in the difference in the optical range between two coherent beams of light causes a very sensitive movement of the interferometric fringe, and the change in the optical range of a coherent beam of light is caused by a change in the

geometric distance it travels or the refractive index of the medium through which it passes, so the movement of the interferometric fringe can be used to measure small changes in the geometric length or refractive index and thus other physical quantities related to it. In this way, it is used for detecting the size of the mirror, which is shown in Figure C.3.

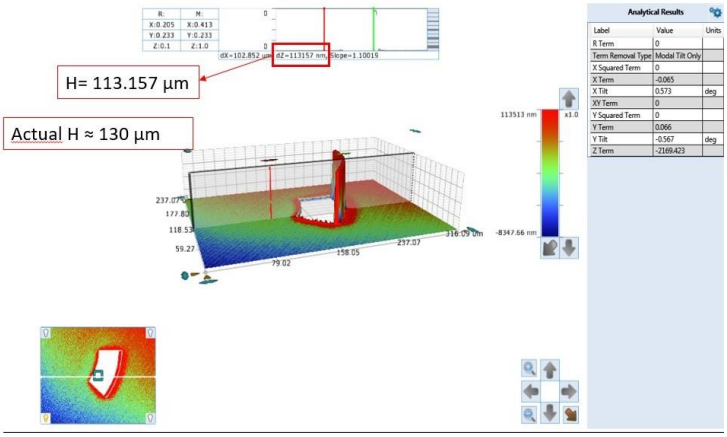


Figure C.3 WLI contour for parabolic mirror

As it can be seen, the 3d contour only shows the distance between the top surface of the mirror and the substrate, while the parabolic part is left blank. Presumably this is because the interference light can only be focused on a flat surface, while the curved part is difficult to focus and is therefore not shown.

Another thing is that measured height is not the same as actual height. It seems there is around 20 µm error. This is probably because the substrate is silicon and the mirror is IP-S: a photolithographic polymer. And they have different refractive index, which causes big error.

Method 2: Dektak 8---- surface profiler is an advanced thin and thick step height measurement tool capable of measuring step down to 10 nm. Substrates up to five inches in dimension can be measured. The Dektak 8 is especially setup up for doing fine measurements, for this purpose it has a 2,5 micrometer stylus.

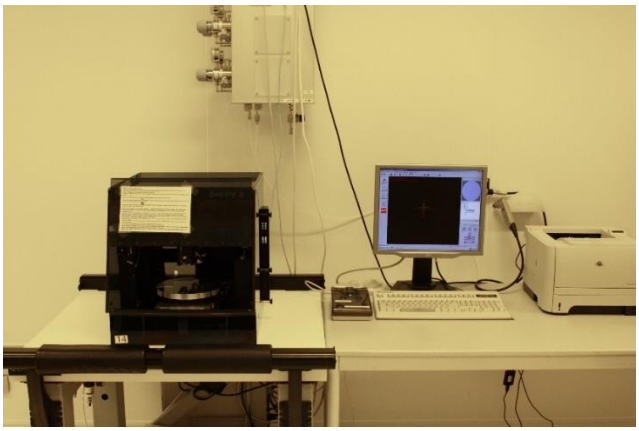


Figure C.4 Dektak 8 in the Nanolab

Scan data can be exported out and input to the Matlab for analysis. Figure C.5 shows the mirror shape line printed. But it is hard to say that the stylus 'route just pasts the central axis of the mirror. Then a small semi-circular ball is printed on the front of the mirror's central axis. If the height of the scanned semicircular sphere is the radius set by the model, it means that the stylus is going on the central axis, then the scanned data is more convincing as shown in Figure C.6. 16 μm is set for the radius and 140 μm is set for the height of mirror. Then, this suggests a dimensional accuracy of approximately 1.42%, but this needs to be backed up by further data.

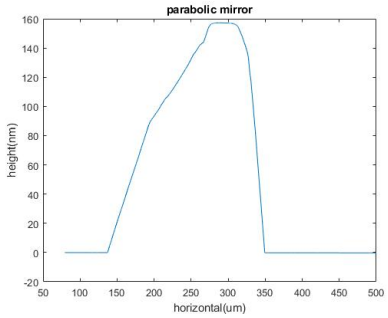


Figure B.6 Scan shape of parabolic mirror

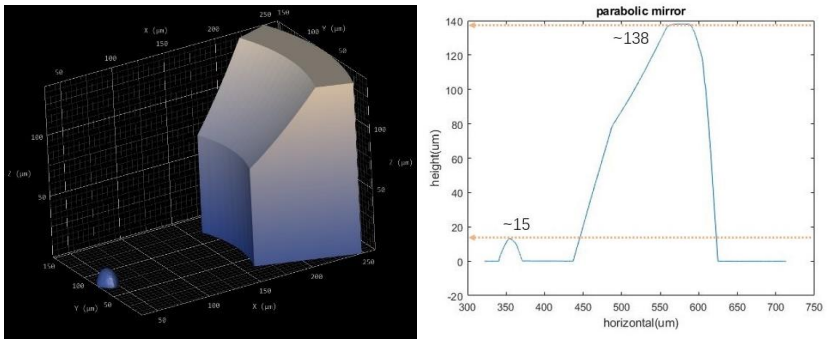


Figure C.6 Scan shape of parabolic mirror with center ball

Appendix D

Since BAK600, as an instrument for high vacuum evaporation, has a particularly large vacuum chamber, as shown in Figure D.1. The upper area where the sample is placed looks like an umbrella and is particularly far from the material source, which is why the maximum deposition thickness is set at 500 nm on the PC.

Figure D.1 Vacuum chamber of BAK600 in Nanolab

With this in mind, the OS group has previously used the device by assembling a special holder, which is fixed to the original sample position with a silicon wafer at one end and vertically close to the material source at the other, so that a thicker material can be deposited on the sample in the same amount of time. Like Figure 3.9 shows. However, as soon as this special holder is used, rotation has to be selected as not used when setting up on the PC. Otherwise, the whole instrument will be damaged.

Another thing is that deposition rate could be added up higher by increasing the current for Al deposition, and basic parameters is set for one time and shown in Table D.1.

Process parameters #Layers 1

Layer#	Material	Thickness [nm]	Em. current [mA]	Rate [nm/s]	Proc. pressure (P4) [mBar]	Info
1	Al	210.0	248.0	0.5	1.0E-7	

Table D.1 Basic parameters set before deposition

About the “Thickness” set, the wanted thickness is 210 nm, which means 30 nm is set on the PC. The reason is explained before. Then it is the process of how to determine the times. As shown in Figure D.2, mirrors are printed around the center and up, down positions are sticked by Kapton tape before deposition. Then, Kapton tape was stripped, giving two areas: an intermediate part with Al deposited, and an upper and lower part with only the Si base.

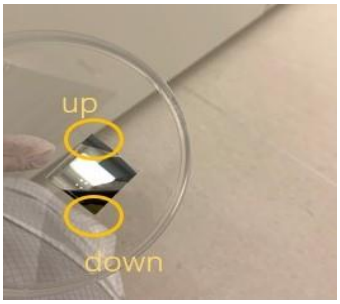


Figure D.2 Use Kapton tape to assist in determining thickness

Put those samples into Dektak 8 for thickness detection. The actual thickness is given by scan data. After collecting several groups of data: a tape is applied to the upper, middle and lower parts and then six points will be selected for scanning. One side is to check the consistency of the deposition, and the other is that the data is relatively reliable with multiple points selected for averaging.

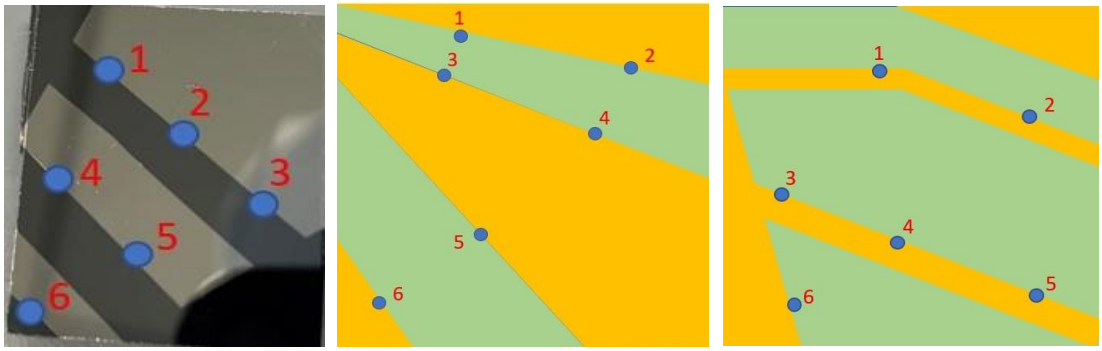


Figure D.3 3 groups of samples for detecting thickness a, b, c (left to right)

Thickness(nm)	A set: 70 nm	B set: 40 nm	C set: 80 nm
1	518	300	610
2	494	296	660
3	510	299	640
4	490	296	600
5	488	302	630
6	480	305	590
Times	7.09	7.10	7.44

Table D.2 Scan data for 3 different set thicknesses

According to the Table D.2, we could say if the special holder was used, the thickness times would be around 7 times.

Appendix E

According to Chapter 3.1, parameters of printing mirror are given. In this chapter, mode of caps is introduced.

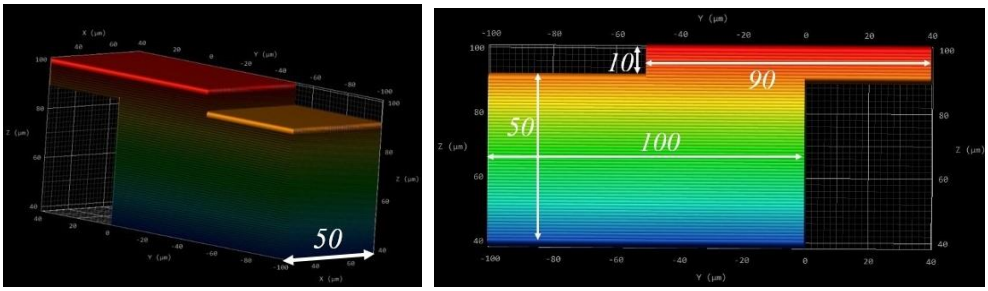


Figure E.1 model for cover caps

After printing mirrors being finished, move center sensor to upper surface and focus on it at the end facet of the waveguide. Through command MoveStageY -100 MoveStageX 25 AddZOffset 40 (unit is µm), make sure that caps cover the end facet of waveguide as shown in Figure E.2.

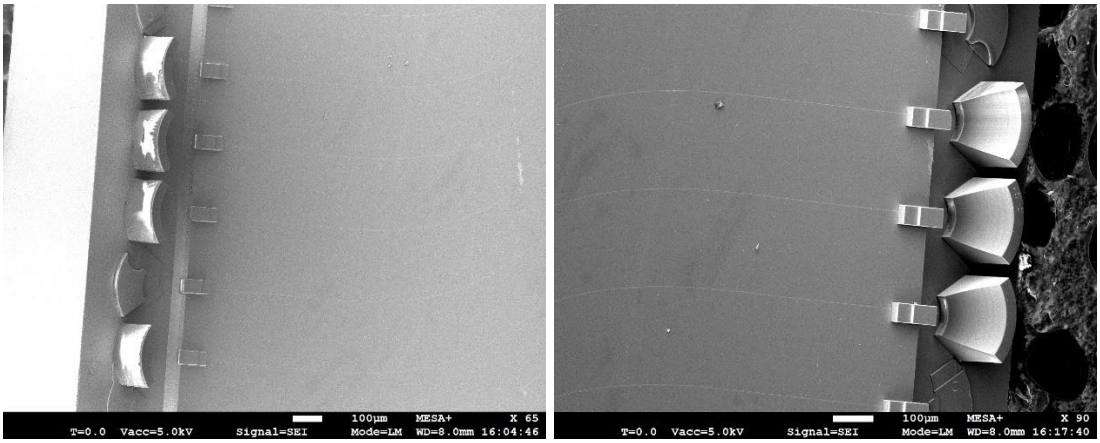


Figure E.2 SEM images for printed caps and mirrors