# Hall effect and field-effect measurements of tin telluride nanowire devices for novel topological quantum computation

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***Abstract*—We electrically characterize tin telluride nanowire devices by employing the Hall effect, where we focus on the determination of the carrier concentration and additionally the mobility. Our interest in electrically characterizing these selective-area grown nanowires is to lay the groundwork for the depletion of tin telluride's highly conductive bulk. Depletion of the bulk is necessary in order to identify unique conducting topological states on the nanowire's surface that could be used as robust, topological qubits. We also extensively investigate the nanowire-to-gate capacitance by modelling our device geometry using the finite-element method, from which we estimate the carrier concentration that can be depleted by the field-effect to be $3 \times 10^{18}$ cm$^{-3}$ for a 10 V gate voltage.**

**We find that the carrier concentration of our newest devices varies between 4.7 and $7.9 \times 10^{20}$ cm$^{-3}$, and the mobility ranges between 60 and 135 $\frac{\text{cm}^2}{\text{Vs}}$.**

**We conclude that our nanowires are indeed not depletable, but we still intend to measure more of these devices for a better picture of their electrical properties. Moving forward, we will electrically characterize lead tin telluride nanowires that are predicted to be less bulk-conductive and attempt depletion in these devices.**

## I. Introduction

Quantum computers are poised to be central in information processing in the near future due to the classical computer's inability to solve problems with increasing complexity[1]. However, a major challenge facing quantum computation is suppressing the effects of noise and decoherence[2]. Though there are extensive approaches to achieve this[3], the existence of topological states of matter could allow for novel, fault-tolerant quantum computation. Topological states are non-local in nature, thereby immunizing the encoded quantum information from any local perturbations[3]. One of such topological materials is tin telluride (SnTe), which has semiconducting bulk properties whilst containing conducting surface states that are symmetry-protected. These properties make it promising for the fabrication of robust, topological qubits. Nanowires are a promising candidate to host these states due to their large surface-to-volume ratio, tunability of device conductance and low disorder[4,5], which is why we decide to investigate tin telluride nanowires.

The problem in identifying these unique surface states arises from tin telluride's heavy p-type doped bulk, which needs to be reduced in order to detect the surface states. Modulation of the carrier concentration can be achieved by applying a gate voltage in a field-effect transistor (FET) configuration, which we juxtapose with Hall effect measurements to electrically characterize the nanowire.

This paper determines the bulk hole concentration and the hole mobility by means of Hall effect measurements at 4.5 K. We compare these results to an estimate of the hole concentration that can be depleted by the field-effect, which is based on a model of the nanowire-to-gate capacitance. Besides the simulations, we also attempt field-effect measurements to determine if the carrier concentration is tunable.

## II. Theory and set-up

### A. Material system

SnTe is classified as a topological crystalline insulator (TCI) with a rock salt crystal structure. Topological crystalline insulators are remarkable due to theoretically being insulating within their bulk whilst they conduct on their surfaces. This means that for the electronic band structure (see Figure 1a), the bands corresponding to the bulk states do not cross the Fermi level (defined at zero energy here), however, the surface states do due to the strong spin-orbit coupling effect that is present there.

The consequence of the spin-orbit coupling is the inversion of the top and bottom of the valence and conduction bands, respectively[6]. Charge carriers can in this way traverse from the valence band to the conduction band without scattering, which makes these materials' surface states very promising for spintronics and quantum computing applications[5].

Investigating SnTe as a quasi-one-dimensional structure such as a nanowire is advantageous due to its high surface-to-volume ratio which enhances the contribution of topological surface states[5] to the conductivity. The reader should be aware that the nanowire itself is nonetheless three-dimensional and still exhibits bulk properties.

Our selective-area grown nanowires are deposited by molecular-beam epitaxy (MBE) in trenches in an amorphous silicon nitride ($\alpha$-SiN$_x$) mask on top of an indium phosphide (InP) substrate. Due to the nature of the growth process, the nanowires overgrow in a mushroom-cap manner out of

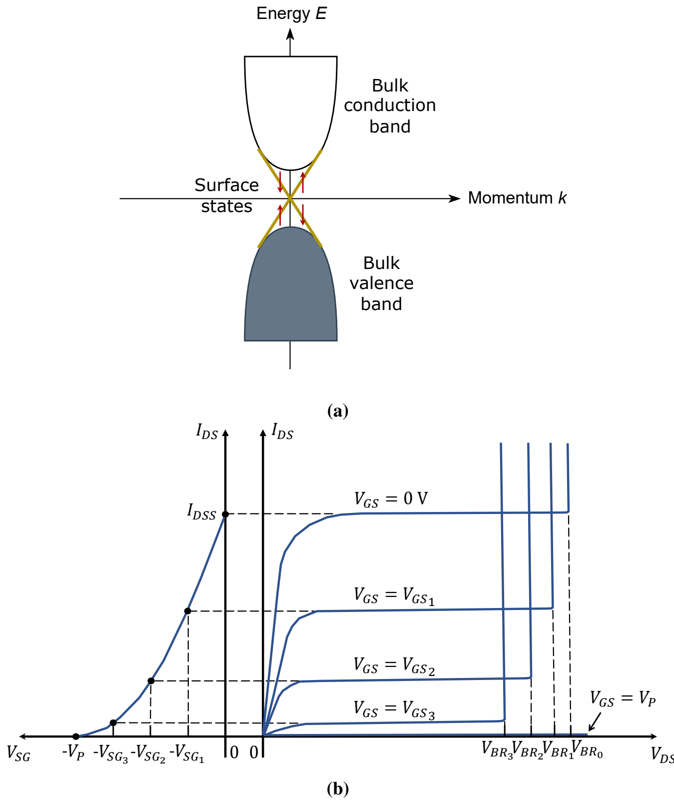


**Fig. 1:** **(a)** Cartoon depiction of electronic band structure of topological insulating materials. The Fermi level $E_F$ is defined at $E = 0$ here, indicating that the bulk is insulating. Note that due to tin telluride's narrow band-gap[7], its bulk properties are semiconducting rather than insulating. Surface states are highlighted in yellow, where the spin-momentum locking is indicated by arrows. Adapted from J. Hoffman[8]. **(b)** P-Channel depletion-mode FET characteristic curve. $V_{BR}$ represents the breakdown voltage, i.e. when the insulating material in the FET becomes conductive, thus leading to a dramatic increase in the drain current. This is an important consideration in the design of top gate devices that may be used in future experiments, as the oxide thickness is very thin (10-50 nm). $I_{DSS}$ is the maximum current that flows through the nanowire FET, i.e. the current in the saturation regime for zero gate voltage. When the pinch-off voltage $V_P$ is reached, no current flows through the channel anymore. The transconductance can be derived from the slope of the graph for $I_{DS}$ vs. $V_{SG}$. Adapted from Dr. Khaldoon N. Abbas[9].

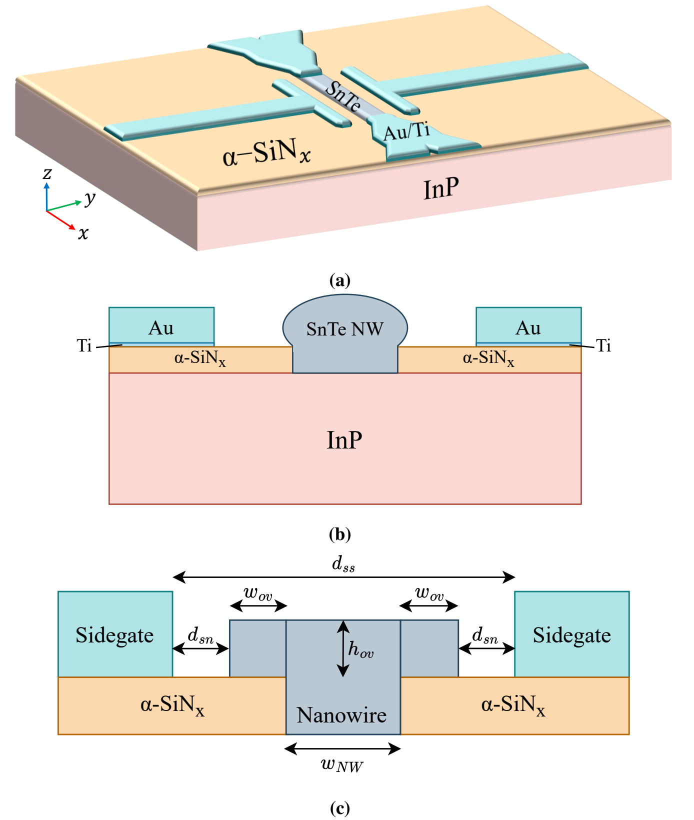


**Fig. 2:** **(a)** Schematic overview of one nanowire device on the substrate in FET configuration. A 5 mm $\times$ 5 mm indium phosphide (InP) substrate is used (360 $\mu$m high) on which a 20 nm high amorphous silicon nitride ($\alpha$-SiN$_x$) layer is deposited. The SnTe nanowires are grown in-plane inside trenches in the $\alpha$-SiN$_x$ mask. The gold (Au) side gates and quasi-four-point source-drain contacts are approximately 30 nm high, with a 2 nm titanium (Ti) adhesion layer to ensure that the metal sticks to the nitride. **(b)** Schematic depicting cross-sectional side view of nanowire device. All layers are approximately to scale except for the 360 $\mu$m InP substrate. **(c)** Schematic of cross-sectional view of device geometry used in COMSOL model and for theoretical calculations of the field-effect carrier concentration. The nanowire diameter or width $w_{NW}$ is varied between 20 and 100 nm, with a 20 nm step-size. Other parameters include the overgrowth width $w_{ov}$, overgrowth height $h_{ov}$, the sidegate-to-nanowire distance $d_{sn}$ and the sidegates separation $d_{ss}$.

the trenches (see Figure 2b). More details about the device geometry and its implications will be discussed in further detail when exploring the field-effect.

A fundamental issue that motivates this paper is that before the TCI states can be demonstrated, the SnTe nanowire's bulk must behave as an insulator. This is not the case due to the presence of Sn vacancies that form acceptor states in the material[10,11], and hence a heavily p-doped bulk. This large background doping hides the presence of the valuable surface states that we want to utilize for quantum computational applications further along in the future. The significant p-type doping is intrinsic to the material and has been shown to have a concentration on the order of $10^{20}$-$10^{21}$ cm$^{-3}$ [12,13] for bulk SnTe and thin-films grown using various methods. Volobuev et al. found that for MBE-grown thin-films, the hole concentration was $2 \times 10^{20}$ cm$^{-3}$ [12]. As our nanowires are also grown using this synthesis technique and in-plane nanowires are essentially one-dimensional thin films, we expect carrier concentrations in this range.

### B. The Field-effect

Nevertheless, in order to tune the background doping in the bulk, the field-effect is used, just as in the operation of a FET. However, rather than using the material for its semiconducting properties in the FET, we use the FET to electrically characterize the SnTe nanowire. A negative bias voltage $V_{DS}$ is necessary to drive a current $I_{DS}$ through the nanowire. In order to control this current, a positive voltage $V_{GS}$ will be applied on both sides of the nanowire channel by two side gates (see Figure 2a). This induces an electric field that repels the p-type carriers, thereby creating a depletion region. With increasing $V_{GS}$, the source-drain current will be reduced due to the growing depletion region, similar to the behaviour in a p-channel depletion-mode device such as a Junction FET (see Figure 1b). The channel current, noting the polarity, can be described by the linear, or ohmic, region of a FET. This is valid for $V_{SD} \leq V_{SG} - |V_P|$, where $V_P$ is the pinch-off voltage, meaning the gate-source voltage for which $I_{SD} = 0$:

$$I_{SD} = \frac{\mu_{FE} C}{L^2} \Big[ (V_{SG} - |V_P|) V_{SD} - \frac{{V_{SD}}^2}{2} \Big], \quad (1)$$

where $C$ is the gate-to-nanowire capacitance [F], $\mu_{FE}$ is the field-effect hole mobility [$\frac{\text{cm}^2}{\text{Vs}}$] and $L$ is the channel length. All presently tested devices have a channel length of 1 $\mu$m, though we also intend to measure 1.3 $\mu$m long devices in future experiments to observe any possible effects on the nanowire's transport properties and gateability. The channel conductance $G$ is given by $\frac{\partial I_{SD}}{\partial V_{SD}}$ for constant $V_{SG}$, whilst the transconductance $g_m$ relates small changes of the channel current to small changes in the source-gate voltage for constant source-drain voltage:

$$g_m = \left( \frac{\partial I_{SD}}{\partial V_{SG}} \right)_{V_{SD}} = \frac{\mu_{FE} C}{L^2} V_{SD}, \quad (2)$$

so that the mobility can be extracted from the slope of the transconductance curve for small $V_{SD}$, i.e. in the linear region. The mobility is an electrical property of interest to us because it relates to the occurrence of scattering events and thereby informs us about the stoichiometry and purity of our nanowires.

The carrier concentration has greater relevance to us than the mobility as tuning the bulk doping is currently our main goal. The field-effect carrier concentration $p_{FE}$ is obtained by dividing the stored charge on the gate at the point of pinch-off $q = CV_P$ by the channel volume $V_{ch}$ and the elementary charge $e$:

$$p_{FE} = \frac{CV_P}{V_{ch}|e|} \quad (3)$$

Though the channel length is essentially equal between all devices, the channel volume is still heavily dependent on the particular device. The devices are not only of various nanowire or trench widths $w_{NW}$ - varying between 20 and 100 nm in steps of 20 nm - but have different amounts of growth out of the trenches as well. In order to approximate the nanowire volume, the aforementioned mushroom-cap growth of the nanowire is assumed to be T-shaped (see Figure 2c). This assumption makes it easier for us to observe the effect of varying certain geometrical parameters. Using the SEM topview images, the overgrowth width $w_{ov}$ is determined, where we assume the overgrowth to be symmetrical with respect to the trench. Furthermore, the overgrowth height $h_{ov}$ is assumed to be 20 nm for all devices, which is also equal to the trench height. For the carrier concentration, we thus not only assume that the doping is uniformly distributed throughout the nanowire, but that the depletion of carriers is uniform as well, which realistically is not the case due to the overgrowth. The estimated field-effect carrier concentration is thus given by:

$$p_{FE} = \frac{CV_P}{|e|(w_{NW} + w_{ov}) 2 h_{ov} L} \quad (4)$$

The advantage of using a nanowire as the channel here is that tuning the significantly large charge carrier density is more achievable due to the nanowire's small size.

However, the nanowire's small size is also the bottleneck in determining the gate-to-channel capacitance necessary to extract the field-effect mobility as given by Equation 2. Conventional C-V profiling is thus not possible here, which is why we performed finite-element method (FEM) modelling of the nanowire devices in COMSOL. Radio-frequency resonator circuits have also shown promise in determining the capacitance of nano-scale FET devices [14], and we intend to use this set-up in the near future. For the purpose of this paper, the FEM-derived capacitances suffice for initial characterizations of the SnTe nanowire devices. This capacitance also takes into account edge and screening effects that simplified models ignore. Note that the gate capacitance only comprises the nanowire-to-gate capacitance, and not the capacitance due to the formed depletion region which is a function of the applied gate voltage. First of all, this is a reasonable approximation because of the channel's and thus depletion layer's nano-scale size. Secondly, it is also appropriate since the nanowire may be assumed to be metallic because the high charge carrier density screens the nanowire by accumulating on its surface. Besides the side gate configuration that we use in current experiments, a top gate model was also simulated for future reference, as devices with top gates are more gateable compared to devices with side gates.

The main results of these simulations are discussed in *Results and Discussion*, but for more details on the determination of the capacitance, we invite the reader to look over *COMSOL Modelling* in the Appendix.

### C. The Hall effect

The carrier concentration and the mobility can also be derived by means of the Hall effect. By applying a magnetic field $\mathbf{B} = (0, 0, B_z)$ perpendicular to the device substrate with a current $I_{DS}$ being driven along the channel in the $x$-direction (see Figure 3c), the charge carriers will experience a magnetic force that is perpendicular to both the current and magnetic field. Once charges begin to deflect from their current path, the carriers also start to feel a force due to the electric field that forms across the nanowire. The force due to the electric field and the magnetic force together constitute the well-known Lorentz force $\mathbf{F}$. The charge carriers are pushed in the $-y$-direction according to Fleming's Left Hand Rule, and accumulate at the wire surface between the Hall contacts that are shown in Figure 3c. For the heavily p-doped nanowire, the holes that accumulate at the side of the nanowire will generate a positive electric field $\mathbf{E} = (0, E_y, 0)$ in the $+y$-direction. As the electric force on the holes increases, the forces eventually reach equilibrium with one another. The result is that a steady-state transverse voltage $V_{xy}$, also called the Hall voltage, forms across the nanowire. We note that the voltage is positive for our nanowires when measuring from the point of carrier accumulation [15]:

$$V_{xy} = \frac{I_{DS} R_H B_z}{t_{NW}} \quad (5)$$

Since the transverse voltage relates linearly to the magnetic field, by sweeping the magnetic field and taking the slope $\frac{\partial V_{xy}}{\partial B_z}$, we can rewrite Equation 5 to determine the Hall coefficient $R_H$ for a known nanowire thickness. We may then compute the Hall carrier concentration $p_H$ as the Hall coefficient relates to $p_H$ by $R_H = \frac{1}{p_H |e|}$.

In order to also extract a mobility value, we conduct measurements of the longitudinal voltage $V_{xx}$ as well. The mobility is given by the ratio of the Hall coefficient to the longitudinal resistivity $\rho_{xx}$, where we take the resistivity at zero magnetic field. The resistivity depends on the sample geometry:

$$\mu_H = \frac{R_H}{\rho_{xx}} = \frac{R_H I_{DS} L}{2t_{NW}(w_{NW} + w_{ov})V_{xx}} \tag{6}$$

We once again approximate the cross-sectional area by the T-shaped overgrowth for fair comparison to the field-effect measurements. One shortcoming resulting from the complexity of the sample geometry is that $t_{NW}$ is non-uniform in the $y$-direction, which could at least cause deviations up to a factor of 2 as we assume here that the thickness is 40 nm.

Since a portion of our nanowire devices are capable of being measured by both the field-effect and Hall effect simultaneously (see Figure 3a), we are also interested in investigating $\mu_H$ and $p_H$ as a function of the gate voltage. Since we do not expect to fully deplete the pure tin telluride nanowires, which is necessary to extract $p_{FE}$, observing trends in $p_H$ versus the gate voltage still gives us valuable information about the extent of carrier depletion that we can achieve.

We expect deviation between the Hall and field-effect derived carrier concentrations due to the field-effect inducing charge that is trapped in interfacial states. The largest influence comes from states between the nanowire and an oxide layer that inevitably grows on top of the nanowire due to air exposure. This means that the field-effect exaggerates the carrier concentration. These states do not contribute to electrical transport within the nanowire [16], which implies that the Hall effect measurements give us a more accurate representation of the bulk carrier concentration, however, both measurements together are still useful as they give us information about how much charge is trapped in these interface states. The field-effect mobility is also limited by adhesion of molecules to the nanowire, which can be minimized by evacuating the sample [4]. Furthermore, the electrodes at source and drain will generally screen the gate voltage in small devices, though this has positive reverberations since this means edge effects are far less influential and the electric field is mainly present directly between the side gates and the nanowire.

### D. Experimental set-up

In order to exclude the line resistance from the voltage measurements, we use quasi-four-point probes as depicted in Figure 3b. This, however, does not eliminate the contact resistance, which can potentially be large if rectifying Schottky contacts are formed instead of ohmic ones. We apply a voltage of 1 V in series with a current-limiting resistor $R_D = 1$ MΩ, which yields a quasi-constant 1 $\mu$A current driven through the nanowire. The current is quasi-constant since the resistance of the nanowire is much smaller in comparison to $R_D$. This assumption is valid as we measured the resistance to be 10 kΩ, i.e. two orders of magnitude less than $R_D$, in basic resistance tests at room temperature. We decided to use a 1 MΩ resistor because we achieved an acceptable signal-to-noise ratio which

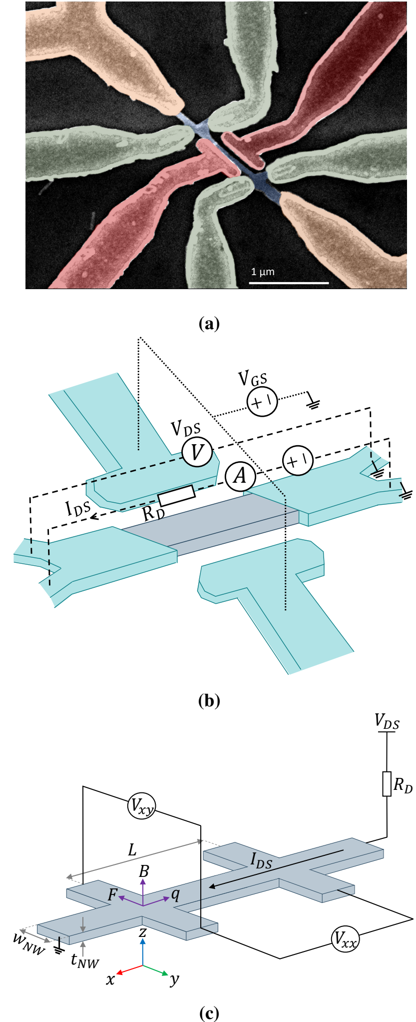


**Fig. 3:** **(a)** False-colored scanning-electron microscope (SEM) image of one complete device, with nanowire (colored in blue), Hall contacts (coloured in green), quasi-four-point source-drain contacts (coloured in yellow) and side gates (coloured in red). **(b)** Overview of experimental set-up for field-effect measurements. A small ($\sim$ 1mV) bias drain-source voltage $V_{DS}$ is applied over the nanowire by a voltage divider circuit, with a gate-source voltage $V_{GS}$ being varied on the side gates. **(c)** Overview of experimental set-up for Hall bar measurements, including relevant geometrical parameters and Hall effect. The reader should be aware that the Hall terminals are not in a 90° angle to the channel, but are instead in a 60° angle. This will also result in a small voltage offset in the data as the centers of two opposite transverse terminals are not completely aligned. A voltage $V_{DS}$ is applied at one of the end contacts, with a current-limiting resistor $R_D = 1$ MΩ in series, leading to a relatively constant current. The six-contact 1-2-2-1 Hall bar geometry is generally useful as we can evaluate sample homogeneity in both the transverse and longitudinal directions if necessary [17]. Note that $q$ denotes an electron, so that a hole flows in the opposite direction. Both set-up's are shown for an idealized nanowire deposition without the formation of mushroom-caps. Adapted from Zurich Instruments [18].

made the voltage measurements more robust, whilst keeping the current in safe limits. The quasi-four-point probes then aid in the field-effect measurements since the voltage probes may be used in parallel to accurately measure $V_{DS}$.

For the Hall measurements, the same principle is used to apply a current, but the voltage probes are placed over the Hall contacts as shown in Figure 3c. In order to minimize noise in both Hall and field-effect measurements, we use pre-amplifiers with an amplification factor of 10, which we attach to lock-in amplifiers. The lock-in amplifiers modulate the 1 V dc input voltage by a 13 Hz reference frequency and mix the output signal frequency with this reference frequency: after applying a low-pass filter, we only measure a dc component. These ac measurements not only generally help with the signal-to-noise ratio, but dc offset voltages can be removed by a capacitor prior to frequency mixing, which gives a more accurate extraction of the electronic properties.

We took careful steps to verify all of the devices through optical microscope imaging to have a general overview of the devices, as well as through scanning-electron microscopy to have a closer look at the metallization around the nanowire. Conclusions based on our first two chips and earlier versions of the metallisation led to our improved third chip: after once again verifying through microscopic techniques and being initially resistance-tested at room temperature, the chip could be measured in our Hall and field-effect set-up's. More information on the fabrication process and our optimization can be found in the Appendix (see *Fabrication and Device Design*) for the interested reader.

All Hall and field-effect measurements are performed at near-liquid helium temperatures ($4.5$ K) to ensure freezing out of electron-phonon scattering as well as the conductivity of the InP substrate. As expected, the resistance decreased with decreasing temperature, which verifies the nanowire's quasi-metallic nature since less collisions occur overall between the carriers. A precautionary measure we take is to make Hall measurements prior to applying any gate voltage in order to lessen the risk of the device succumbing to irreversible damage.

## III. Results and Discussion

The reader should be aware that the simulated capacitances discussed in this section are for a side gate FET geometry. We also tested the Hall bar geometry, which showed overall similar trends so that the capacitances are comparable (see *COMSOL Modelling* in the Appendix). We varied different geometrical parameters like the overgrowth width or the nanowire-to-sidegate distance for various nanowire diameters in order to observe trends in the capacitance.

Figure 4 shows some of the main results of our COMSOL model. Overall, we see that the capacitance between the nanowire and gate is in the range of 100-200 aF. Figure 4a shows that for increasing overgrowth width, the capacitance increases in a similar fashion for each of the nanowire diameters. With increasing overgrowth width, the nanowires are closer in proximity to the side gates, which leads to an increase in capacitance since the electrostatic forces are stronger. Note that the side gate separation is higher for the wider nanowires (for fixed $w_{ov}$), which is the reason why the graphs for smaller diameters show larger capacitances in Figure 4a.

Figure 4c shows the capacitance versus the sidegates separation for various $w_{NW}$ and $w_{ov}$, where once again there are clear trends. One can see that for the same $d_{sn}$, the capacitance is approximately the same which is expected as the distance from the gate terminal to the nanowire is fixed in that case. This showed that the effect of increasing the nanowire diameter is not significant when keeping $d_{sn}$ fixed, and it is more-so the decrease in $d_{sn}$ that dominates. The overgrowth height was also varied, though this showed minimal change in the capacitance (see Figure 8c in the Appendix).

Based on the capacitances, we then estimate the depletable free hole concentration for an applied gate voltage of 10 V, where Equation 4 is made use of. We conclude from Figures 4b and 4d that the thinner 20 nm nanowires are the most gateable: the slight increase in capacitance of the wider nanowires does not compensate for the increase in volume that needs to be depleted. More overgrowth also shows less ability to be depleted (see Figure 4b) even though the capacitance was increased for more overgrowth, which implies that the increase in volume is again too high for the device to remain as gateable.

We see that the depletable carrier concentration at 10 V overall varied between approximately $10^{18}$ and $10^{19}$ cm$^{-3}$, which implies that pinch-off is indeed not realistic to achieve for pure tin telluride nanowires based on bulk carrier concentrations from literature.

Unfortunately, we were not able to perform field-effect measurements to corroborate the results from our COMSOL model and compare to the Hall effect measurements. The primary reason for this was that our side gates were shorting or leaking to either the nanowire, the surrounding contacts, or both. Optical microscopy and especially SEM images showed us the primary causes of these shorts (see Figure 5b). These included an incomplete lift-off of the gold on top of the polymer network, collapse of the side walls from the metal deposition, as well as slight misalignment of the deposited metal. Our current devices have already shown an improved lift-off, and we continue to optimize various fabrication parameters so that field-effect measurements are realizable in the near future. For more details on this optimization, the reader may refer to *Fabrication and Device Design* in the Appendix.

Nevertheless, we performed Hall effect measurements on three devices, one (D1) belonging to our first generation of devices, whereas D2 and D3 belong to our latest third generation of devices: note that the nanowires were grown differently between these two generations. We remark that the current lead on one side of the nanowire was found to be cut-off from the rest of the circuit for both D2 and D3. Instead of applying $I_{DS}$ through these contacts as depicted in Figure 3c, we use one of the Hall probes on the side of the broken lead as the source, i.e. it is grounded. Our transverse voltage measurements thus remained relatively unaffected, though we do see small quadratic components which originate from the magnetoresistance[19] for growing magnetic field strength. Due to the configuration, we also pick up a small Hall component which causes the slight asymmetry in the longitudinal resistance, which by definition should be independent of the direction of

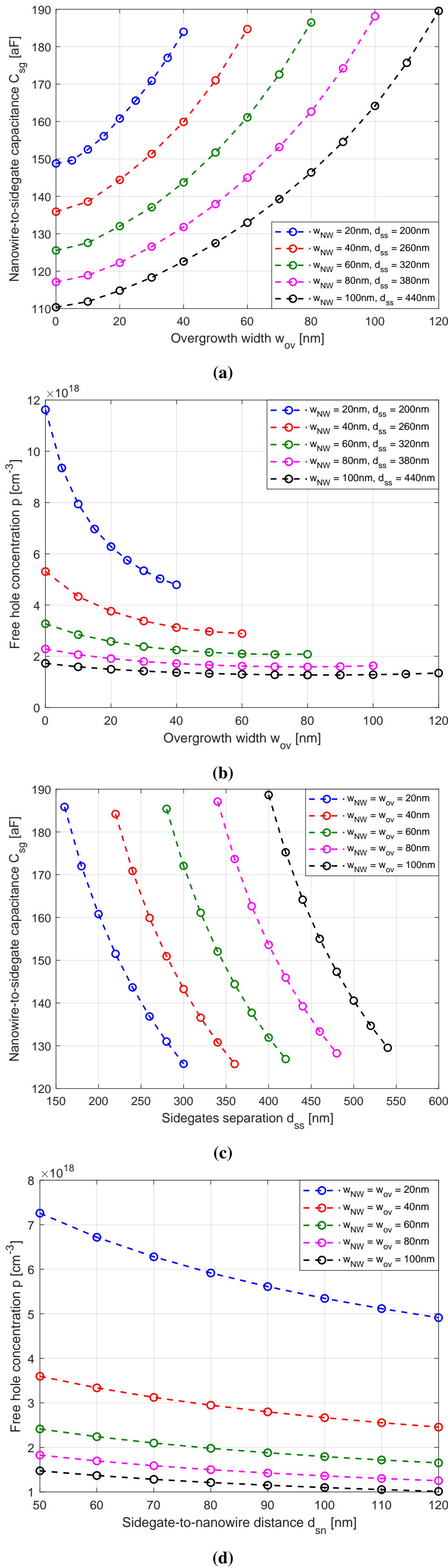


**Fig. 4:** Nanowire-to-sidegate capacitance $C_{sg}$ values computed in COMSOL and estimated depletable free hole concentration $p$ for FET configuration. (a) $C_{sg}$ versus the overgrowth width $w_{ov}$ for fixed $h_{ov} = 20$ nm, different $w_{NW}$ and corresponding fixed $d_{ss}$. **(b)** $p$ versus the overgrowth width $w_{ov}$ for fixed $h_{ov} = 20$ nm, different $w_{NW}$ and corresponding fixed $d_{ss}$. **(c)** $C_{sg}$ versus the sidegates separation $d_{ss}$ for fixed $h_{ov} = 20$ nm, different $w_{NW}$ and corresponding $w_{ov}$. **(d)** $p$ versus the sidegate-to-nanowire distance $d_{sn}$ for fixed $h_{ov} = 20$ nm, different $w_{NW}$ and corresponding fixed $w_{ov}$. $p$ is plotted versus $d_{sn}$ instead of $d_{ss}$ as $d_{sn}$ varies in different ranges for the various nanowire diameters.

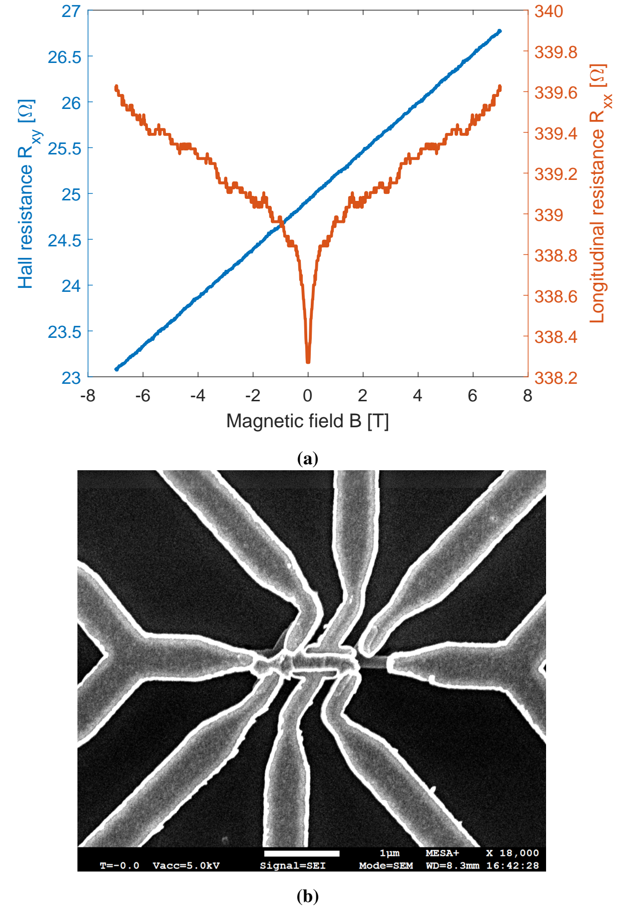


**Fig. 5:** **(a)** Plot of the transverse resistance $R_{xy} = \frac{V_{xy}}{I_{DS}}$ and longitudinal resistance $R_{xx} = \frac{V_{xx}}{I_{DS}}$ versus the magnetic field at 4.5 K, where the magnetic has been swept from $-7$ T to 7 T. $R_{xx}$ and $R_{xy}$ have been symmetrized and anti-symmetrized, respectively, as by definition $R_{xx}$ is independent of the direction of the magnetic field. For $R_{xy}$, the change in resistance should be equal for the same change in magnetic field in either direction. **(b)** SEM image of nanowire with deposited metal. One can immediately notice that contacts and gates are shorting due to either misalignment, incomplete lift-off, or collapse of side walls.

the magnetic field.

We therefore symmetrized and anti-symmetrized the data: the resulting transverse and longitudinal resistances are depicted in Figure 5a. The raw data may be found alongside the (anti-) symmetrization in *Data Processing* in the Appendix.

The Hall resistance coincides with Equation 5 that tells us that $V_{xy}$ relates linearly to the magnetic field. From it, we can extract the carrier concentration, which we do for all tested devices (see Table I). The calculation of the Hall mobility then requires the longitudinal resistivity at zero magnetic field. From Figure 5a, we see a sharp dip in the resistance at zero magnetic field. This is a quantum interference effect known as weak anti-localization which is common in materials with strong spin-orbit interactions like tin telluride at low temperatures[20].

We define error ranges for the extracted Hall mobilities and carrier concentrations based on uncertainty in the nanowire geometry. The errors due to linear fitting and sweep direction are found to be several orders of magnitude lower and are therefore neglected. From analysis of the SEM images, $\pm 5$ nm deviation could be expected in the nanowire overgrowth. On

the other hand, the nanowire thickness could also vary up to 50 nm. Based on these assumptions, a conservative estimate of the error intervals is obtained.

We see that the carrier concentration may vary between $4.7 \times 10^{20}$ and $2.7 \times 10^{21}$ cm$^{-3}$ (see Table I), where we would like to remind the reader that D1 is of a different growth run than D2 and D3. The mobility is also noticeably low for D1, which together with the high value for $p_H$ tells us that the grown nanowires on our first chip are more impure, i.e. at least must contain more Sn vacancies, than those on our third. This gives us direction in the growth of future nanowires: the current parameters that affect the growth are more optimized than those use on our first chip, so we could further optimize from here and realize lower intrinsic carrier concentrations.

Otherwise, comparing D2 and D3 which were on the same chip shows good agreement in the electrical properties. D3 has a $67\%$ wider nanowire than that of D2 and about 8 nm more overgrowth, which altogether means a factor $1.54$ larger cross-sectional area. The lower mobility observed in D2 may be linked to this since a smaller cross-sectional area means that on average more scattering occurs at the nanowire surface. If we would only consider the charge carrier density, a higher mobility should be expected in D2 due to less scattering that occurs off the ionized impurities, though our error margins must be kept in mind.

We also verify that the determined carrier concentrations for our most recent nanowires are on the same order of magnitude when comparing to the MBE-grown thin-films that Volobuev et al. found, albeit circa three times higher. Our results also practically confirm that nanowire depletion will not be possible with the currently grown nanowire. We estimate that for D2 and D3, the tunable carrier concentration based on COMSOL modelling is around $3 \times 10^{18}$ cm$^{-3}$, where we refer to Figure 4d and have used the fact that $d_{ss} = 300$ nm. Therefore, unless we use voltages in the kilovolt range, which far exceeds the breakdown voltage, tuning the nanowires' hole density is simply not possible.

Though the nanowire growth affects the background doping, an effective way to reduce it would be by alloying tin telluride with lead telluride, which is an n-type trivial semiconductor with the same crystal structure[12]. In this way, we can reduce the high p-type background doping, allowing for more gate-able devices and hence depletable nanowires. These alloyed nanowires are not used in our current experiments, but will in fact be implemented in future experiments. We could for example determine the optimal Sn/Pb ratio that significantly diminishes the bulk carrier concentration whilst retaining the TCI property, which would then have to be fine-tuned to our selective-area grown nanowires.

## IV. Conclusion

Our Hall effect measurements showed that the newest generation of devices show almost an order of magnitude higher mobility and a circa four times lower carrier concentration compared to our first tested device. We have also identified trends in the capacitance using our FEM model, which showed that the increased capacitance of the wider nanowires did not compensate for the increase in volume. This means that the thinner nanowires are more optimal for pinch-off, which is our long-term goal. The combined results of the measured Hall carrier concentration and the estimated depletable field-effect concentration confirm our expectations that pure tin telluride nanowires cannot be depleted.

This project has succeeded in yielding an initial electrical characterization of selective-area grown SnTe nanowire devices using the Hall effect, and lays the groundwork for characterization of future improved devices. The remaining devices on our current chip will be measured for a larger collection of data and thus for a more accurate depiction of the nanowires' electrical properties.

Our extensive study of the nanowire-to-gate capacitance is also of great value to this research: the data will serve as a great comparison to future intended high-accuracy RF CV measurements which will be necessary to account for deviations in geometry and assumed material properties. These deviations together cause significant inaccuracies in the capacitance, especially on a nano-scale.

For future devices, the previously mentioned fabrication parameters will be further optimized to ensure well-aligned contacts and complete, uninterrupted lift-off. We also consider furthering our device design with the use of top gates instead of side gates to ensure greater carrier depletability. Alloyed lead tin telluride devices will also be extensively measured in order to pinpoint both an optimal tin/lead ratio and tin- and lead/tellurium ratio for our selective-area grown devices. In this way, both the bulk concentration is minimized and the nanowire is remaining in the TCI phase.

## Acknowledgements

I would like to thank my main supervisor Prof. Dr. ir. Floris Zwanenburg for introducing me to this research project and ir. Maarten Kamphuis for his day-to-day supervision of my BSc thesis project, the fabrication of the nanowire devices and the regular, insightful discussions we had throughout the project. I am also grateful to Dr. ir. Joost Ridderbos for our discussions and especially his insights into COMSOL modelling, to ir. Femke Witmans for her help with measurements, and Dr. ir. Daan Wielens for technical assistance in the lab.

**TABLE I:** Compiled data of tested nanowire devices, including geometrical parameters and experimental results of Hall effect measurements. We also indicate if the device only had Hall contacts and two-point contacts ('Hall'), or if Hall contacts, quasi-four-point contacts and the side gates were present ('Hall + FET'). The overgrowth width $w_{ov}$ is estimated based on SEM images, where we have assumed that the overgrowth is symmetrical with respect to the nanowire trench as only top view images are currently available. Note that D1 not only belongs to a different growth run, but is also fabricated differently: for instance, the metal thickness is 60 nm instead of 30 nm. Also, the lock-in amplifier reference frequency is 137 Hz instead of 13 Hz for the measurements on D1.

| Nanowire device | $w_{NW}$ [nm] | $w_{ov}$ [nm] | $\mu_H$ [$\frac{\text{cm}^2}{\text{Vs}}$] | $p_H$ [$10^{20}\text{cm}^{-3}$] |
|---|---|---|---|---|
| D1 (Hall) | 80 | 39 ± 5 | 1.5 ± 0.46 | 22 ± 4.5 |
| D2 (Hall + FET) | 60 | 28 ± 5 | 89 ± 29 | 5.9 ± 1.2 |
| D3 (Hall + FET) | 100 | 36 ± 5 | 104 ± 31 | 6.6 ± 1.3 |

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## Appendix

### A. Fabrication and Device Design

An overview of some important fabrication steps is given in this section. First of all, the choice to use InP as the substrate is to mismatch the lattice in such a way that a few nanometers from the interface, the nanowire grows in an unstrained manner. In this way, the SnTe grows in-plane on the underlying material and the amount of defects are lessened. Amorphous silicon nitride is used as the mask and has been layered over the InP substrate as illustrated in Figure 2b: we thus selectively grow our nanowires on the substrate as it is not energetically favourable for the tin telluride to nucleate on the $\alpha$-$\text{SiN}_x$ mask. Gold is used as the contact metal, however, to ensure that the contacts stick to the $\alpha$-$\text{SiN}_x$ surface, a 2 nm adhesion layer of Ti is applied below the gold.

Once the samples have been received, SEM imaging of the nanowires is done to determine which are suitable for measurement. We then designed the contacts (see Figures 6a,6b and 6c) which are to be used in both Hall and field-effect measurements.

The fabrication of the contacts involves four important steps:

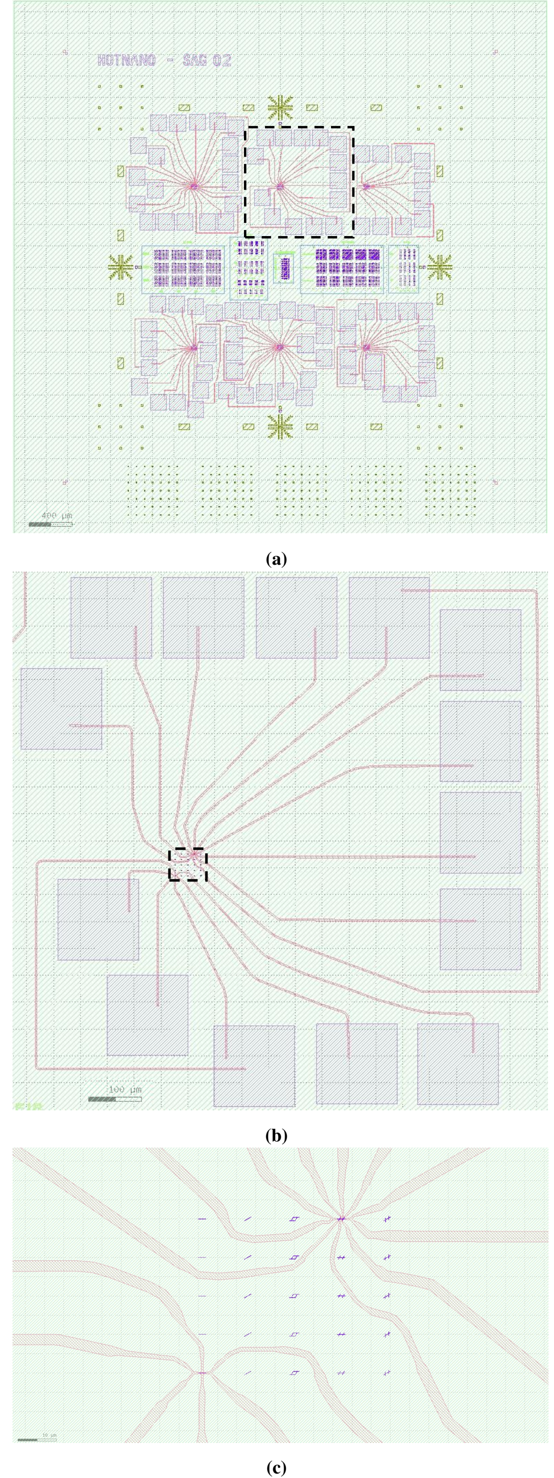
1) Applying the polymethyl methacrylate (PMMA) layer: before this step begins, a pre-cleaning step is done using acetone and isopropanol. A $4\%$ PMMA solution in anisole is spin-coated onto the substrate, after which the sample is put on a hotplate to evaporate this solvent and only leave the polymer network.
2) Electron-beam lithography (EBL) is then used to pattern the pre-defined locations of the metal contacts, as shown in Figure 6a.
3) The samples are then developed: the weakened polymer chains that were shortened by EBL are removed by submerging the sample in methyl isobutyl ketone (MIBK) for a pre-calibrated time period of 30 seconds (Note that for D1 the time was four minutes). Isopropyl alcohol (IPA) is then used to rinse off the MIBK, which halts the development process so that the longer polymer chains remain.

4) The metallization: prior to metallization, in-situ glow discharge is necessary to etch away the native oxide on the nanowire. The Au/Ti contacts are then deposited over the entire chip. Lift-off follows, which dissolves all remaining PMMA with the undesired metal on top using dimethyl sulfoxide (DMSO), and leaves the metal contacts defined by EBL.

Various fabrication parameters like the dose amount during electron-beam exposure, development time, the thickness of both the PMMA and metal layers were optimized since before the start of this project. In this way, devices with sharper features and less side walls, which could collapse following lift-off, were producible. Thicker PMMA layers allow for easier lift-off, however, this also means the side walls that form after metallization will be much higher, thus increasing the chance of shorts in the device. We also saw following tests of the first two chips that the metal leads from the nanowire to the contact pads could have small fissures that led to open circuit measurements. However, since we did not see these closer to the nanowires and the metal was well-defined here, we decided to increase the width of these contact leads with increasing distance from the nanowires for improved lift-off and development. We also noticed that following wire-bonding and de-bonding, contact pads could be almost entirely removed and disconnected from the nanowire contacts, which also leads to open circuit measurements. Though we could pattern a second layer of contacts pads on the first layer to decrease the risk of gold removal, due to possible misalignment which could in turn lead to shorts between contacts, we decide to only bond once on our final set of devices and immediately perform Hall and/or field-effect measurements following resistance testing. To ensure an efficient work pace, in our final run we first verify through both optical and SEM imaging that the devices look functional, after which we wirebond and resistance-test.

### B. COMSOL Modelling

In order to derive the capacitance from the gate to the nanowire, COMSOL is used for its FEM-based modelling capabilities. Assuming that the charges on the gate and nanowire are stationary, i.e. electrostatic, the electric field and device capacitance can be determined. An approximation that is made here is that the nanowire is metallic, when it is in reality a semiconductor: however, considering that the hole concentration is on the order of $10^{20} - 10^{21}$ cm$^{-3}$ for pure tin telluride, this assumption is quite reasonable. The COMSOL modelling is otherwise relatively straightforward as described in the paper, though some details are worth expressing. First of all, as mentioned in the paper, in reality the nanowire grows out of the trench in a mushroom-cap shaped manner. Though this overgrowth could for example be modelled by an ellipse, it is decided to use a T-shaped overgrowth to simplify both the model and the subsequent calculations that make use of the geometry. Moreover, the T-shaped overgrowth more accurately represents the overgrowth, especially for higher overgrowth widths. The sidegate-to-nanowire distance $d_{sn}$ is chosen to be at least 50 nm as in practice lift-off will not be exact, so the sidegate could potentially short to the nanowire. The overgrowth




(a)

(b)

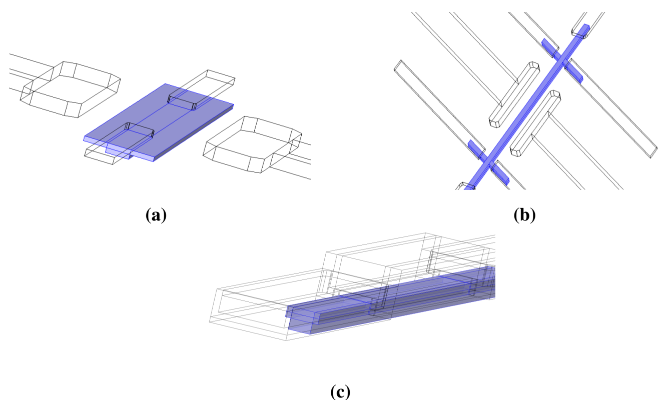
(c)

**Fig. 6:** **(a)** Topview of second selective area grown (SAG) device with contacts design. **(b)** Zoomed-in image of one field on substrate, as marked by dashed lines in Figure 6a, which shows the contact pads and leads. **(c)** Zoomed-in image of field containing nanowires, as marked by dashed lines in Figure 6b. Both an individual FET and a FET in a Hall bar configuration are shown.

height is not exact and consistent as it is relatively variable from the nanowire fabrication. Principally, the overgrowth height $h_{ov}$ is chosen to be 20 nm (note that the trench height is also 20 nm), but different heights are tested to determine the effect on the capacitance.

Figure 2c highlighted another important assumption of the model: the (over)growth is assumed to be uniform in all spatial coordinates, and thus the device is assumed to be mirror-symmetrical from the centre of the nanowire. This also carries on to the theoretical prediction of the depletable carrier concentration, as realistically the nanowire will not be uniformly grown and thus depletion will not occur uniformly either.

An overview of the model used for the nanowire device without Hall contacts is depicted in Figure 7a for $w_{NW} = w_o = 40$ nm. It is worth mentioning that in practice the source-drain contacts will cover the ends of the nanowire, however, the geometry of the contacts is left unchanged for the various parametric sweeps for both simplicity and to solely investigate the effects of changing the parameters shown in Figure 2c. This is expected to have an effect on the capacitance due to the screening effect of the source-drain contacts, but this should not cause significant deviation as the area between the channel and the side gates mostly determines the capacitance.



(a) (b) (c)

**Fig. 7: (a)** Overview of COMSOL model of nanowire FET device geometry with side gates for $w_{NW} = w_o = 40$ nm. Nanowire is shaded in purple. **(b)** Overview of COMSOL model of nanowire six-contact Hall bar device geometry with side gates for $w_{NW} = 40$ nm. **(c)** Overview of COMSOL model of nanowire FET device geometry with top gate for $w_{NW} = 40$ nm.

The six-contact 1-2-2-1 Hall bar geometry is also modelled (see Figure 7b). For simplicity, this geometry is only simulated for $w_{ov} = 0$ nm in order to easily compare between the FET and Hall bar geometry.

A model that uses a top gate instead of side gates is also made as top gate configurations allow for more gateability and thus pinch-off is more likely to be achieved with this configuration. Relevant parameters here are once again $w_{NW}$ and $w_{ov}$, but now with the aluminium oxide ($Al_2O_3$) thickness $t_{ox}$ instead of the sidegates separation. The oxide thickness is varied between 10 and 50 nm as $t_{ox}$ should not be too small to prevent breakdown of the dielectric (and thinner oxides of higher quality are harder to fabricate), but also should not exceed 50nm as the field-effect will not be sufficient to attain pinch-off. It is assumed that the oxide that surrounds the adjacent facets is 10 nm wide for all runs for consistency, whereas the top gate metal facets on the sides are 30 nm wide.

For the material settings, the relative permittivities $\varepsilon_r$ of silicon nitride and aluminium oxide are given as 9.7 and 5.7, respectively, though to make the model more accurate these could be edited to 7 and $9 - 10$, respectively, which are values often found in literature[21]. The dielectric constant is varied to observe the effect on the capacitance; we find that for the side gate model, choosing the literature value for amorphous silicon nitride versus the given values in COMSOL yields capacitances that are 25% lower, which is significant. The simulated capacitances for the side gate model will use $\varepsilon_r = 9.7$ for $SiN_x$ as the main purpose is to identify trends in the capacitance. For the top gate model, $\varepsilon_r = 7$ is used for $SiN_x$ for more accurate values since the deviation was only 3% between 7 and 9.7. This was also important to not overestimate the capacitance, which is more relevant for the top gate model as it is expected to be the best in terms of gateability.

As for the aluminium oxide used in the top gate model, it should be noted that the dielectric constant is thickness-dependent, especially for smaller values of $t_{ox}$ which are used in both the model and to be used in future fabrication. However, the relative permittivity is kept constant regardless of thickness for the model simulations. Based on minimum and maximum values that have been found in literature[22], it is found that for $t_{ox} = 10$ nm and $w_{ov} = 15$ nm, the capacitance varies from 494.78 aF to 881.04 aF for $\varepsilon = 5.7$ to $\varepsilon = 11.1$, which is overall a 75% deviation. For the model simulations, a common value found in literature of $\varepsilon = 9$[23] is used, which is also on the lower end of the expected range so that the capacitance is not overestimated. The indium phosphide material has a relative permittivity of 12.5, and the remaining domains, i.e. the ambient, the nanowire and the gates, are simply attributed to vacuum conditions, which is not problematic for the domains that are assumed to be metallic as they have fixed potentials on their surfaces.

This brings us to the electrostatics settings: 1 V is applied to either both side gates or the top gate, a 1 mV potential is applied to the drain and the source is grounded, which accounts for a 1 mV voltage drop across the nanowire. These values are chosen based on the actual orders of magnitude of the potentials that are applied to the gate and the contacts. On the other hand, one could also simply assume the contacts and nanowires to be grounded based on this difference in potential: this is confirmed during the simulations, where the change in the capacitance is only on the order of 0.1 aF. The Hall probes are given zero potential based on similar grounds: the measured potential across the probes is expected to be several orders of magnitude below the gate potential. Another important assumption of the model is that the nanowire is metallic, meaning that the nanowire is covered in a surface sheet of charge, when in reality the bulk contains the majority of the charge: this is very reasonable because an applied field will pull the charges to the surface and screen the nanowire.

The meshing of the model is also worth discussing, as this is central to the finite-element method. Mesh settings were varied to observe the difference in computed capacitance. The settings were varied until the change in meshing led to

significant deviations in the capacitance, whilst minimizing the computation time for each run. User-defined domains were created in order to vary the mesh settings depending on the location in the model, e.g. the nanowire and contacts in the vicinity were made to be extremely fine, which did not lead to a significantly long computation time due to the size of these objects. The minimum and maximum element sizes used for both the side-gate and top-gate models are compiled in Table II.

**TABLE II:** Mesh settings used in COMSOL.

| Object | Min. element size [nm] | Max. element size [nm] |
|---|---|---|
| Nanowire | 2 | 200 |
| Source-drain | 15 | 350 |
| $\alpha$-SiN$_x$ insulator | 40 | 550 |
| InP substrate | 40 | 550 |
| Ambient | 40 | 550 |
| Sidegates | 15 | 350 |
| Sidegates (wire) | 180 | 1000 |
| Hall contacts | 40 | 230 |
| Topgate | 15 | 350 |
| $Al_2O_3$ insulator (around NW) | 1 | 200 |
| $Al_2O_3$ insulator (rest) | 100 | 800 |
| Ambient (upper layer)[a] | 180 | 1000 |

[a] Used in topgate model to decrease computation time

Parametric sweeps were performed, where care was taken that the electrostatics remained as unaffected as possible. The remaining results of the computations for the side gate model are illustrated in Figure 8. The overgrowth height was changed to observe the effect on the capacitance (see Figure 8c), which showed that for more vertical overgrowth (and fixed $d_{ss}$, $w_{NW}$), the capacitance is higher, which is straightforward since there is more 'direct' area where the electric field lines meet. Also, with increasing overgrowth width, the difference between $h_{ov} = 10$ and 20 nm increases due to the relative change in volume. Figure 8a shows the same parameter variation as in Figure 4c, where the Hall bar geometry has now been simulated and $w_{ov} = 0$ nm for simplicity. The capacitances are in the same range and also follow a very similar trend, but generally the capacitance is higher due to the additional Hall contacts that capacitively couple to the side gates, where we must remark that practically the capacitance will be slightly higher due to the overgrowth that is ignored here.

Based on these capacitances, estimates of the depletable free carrier concentrations are made, in this case the hole concentrations for the pure tin telluride nanowires. A gate voltage of 10 V is applied as this is the maximum order of magnitude of the electric potential that can be applied to the gate in these devices; the charge stored on the gate $q$ is proportional to the applied gate voltage, with the capacitance being the proportionality factor. The depletable hole concentration for a certain gate voltage then follows from Equation 4.

The channel length and channel height are 1 $\mu$m (1.095 $\mu$m for the Hall bar geometry) and 40 nm, respectively, for the graphs of the carrier concentration depicted in Figures 8 and 9, whilst the channel width of course varies with the nanowire diameter. Here we consider the channel length to be the distance between the source-drain contacts for the pure FET configuration, whereas for the Hall bar configuration it is the distance between the Hall contacts. It is important to mention here that for the overgrown nanowires, the volumes of the sideways overgrowth are simply added to the channel volumes without sideways overgrowth. An important assumption here is that the nanowire is depleted uniformly across the nanowire, where in reality the overgrown parts will be depleted more easily than the nanowire in the trench.

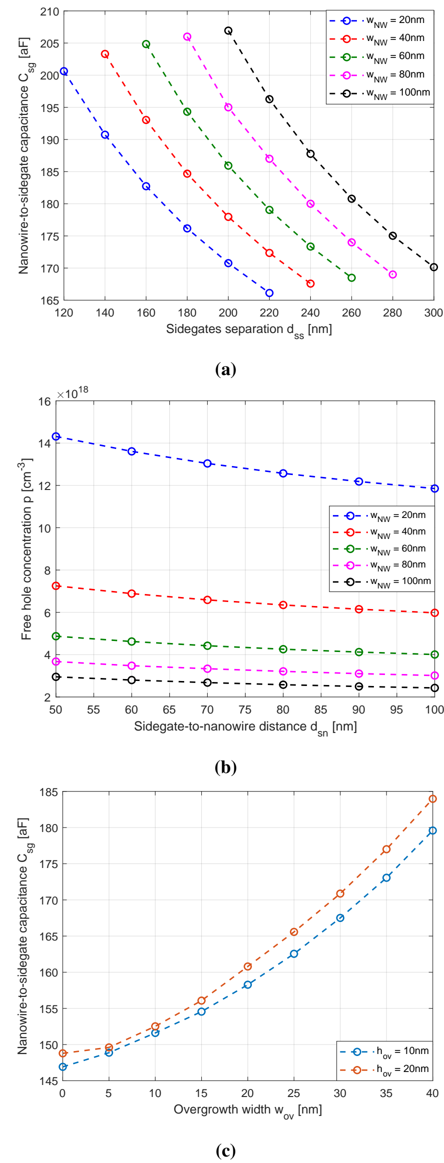



**Fig. 8:** Nanowire-to-sidegate capacitance $C_{sg}$ values computed in COMSOL and estimated depletable free hole concentration $p$. **(a)** $C_{sg}$ versus the sidegates separation $d_{ss}$ for Hall geometry and for fixed $h_{ov} = 20$ nm, different $w_{NW}$ and $w_{ov} = 0$ nm. **(b)** $p$ versus the sidegate-to-nanowire distance $d_{sn}$ for Hall geometry and for fixed $h_{ov} = 20$ nm, different $w_{NW}$ and $w_{ov} = 0$ nm. **(c)** $C_{sg}$ versus the overgrowth width $w_{ov}$ for different $h_{ov}$, $d_{ss} = 200$ nm, $w_{NW} = 20$ nm and for pure FET geometry.

Note that Figure 8b, like Figure 4d, shows the carrier concentration plotted versus $d_{sn}$ instead of $d_{ss}$ as the sidegate-to-nanowire distances that are varied are the same for all nanowire diameters. Both the FET and Hall geometries showed similar trends; note that for the Hall bar model, $w_{ov} = 0$ nm

is assumed and thus there is less volume to deplete which is why the depletable carrier concentration is relatively higher. Comparing the geometries for zero sideways overgrowth and $w_{NW} = 20$ nm shows that both carrier concentrations lie at circa $1.2 \times 10^{19}$ cm$^{-3}$, with the depletable carrier concentration being slightly higher for the Hall bar geometry due to the increased capacitance. It it thus reasonable to assume that the gateability of both devices is the same during experimentation.

The topgate model is also simulated in COMSOL for fixed oxide thickness and varying overgrowth width, and vice-versa, for various nanowire diameters (see Figure 9). For these simulations, when fixing either $t_{ox}$ or $w_{ov}$, the same value was chosen for every nanowire diameter to clearly observe how the depletable carrier concentration varies for the different diameters. For example, Figure 9a shows us that the relation between the capacitance and the overgrowth width is relatively linear, with the larger diameters showing greater capacitances due to more overlapping area on which charge can be stored. However, when computing the depletable carrier concentrations (see Figure 9b), we find that the increase in capacitance clearly does not compensate for the increased volume. Similar behaviour is observed when varying the oxide thickness for the same overgrowth width (see Figures 9c, 9d). Both results show that the 20 nm thick nanowires are $1.5 - 2\times$ more gateable than the 100 nm thick nanowires. This data is of great value in not only observing trends in parameters that are controlled during growth and fabrication from which we can establish trade-offs, but it is also helpful in establishing the optimal Sn/Pb ratio in lead tin telluride nanowires that can still yield gateable devices.

### C. Data Processing

The Statistics Toolbox in MATLAB is used to fit the transverse resistance, i.e. the Hall resistance. Since only the slope is necessary to compute the carrier concentration, the error in the first order coefficient is computed in the linear regression model for a 95% confidence interval. The $R^2$ values are also computed to highlight the very strong correlation (> 99.5% for all three measured devices) between the transverse resistance and the magnetic field. An example of the linear fit, including the errors, is illustrated in Figure 10 for the first tested device.

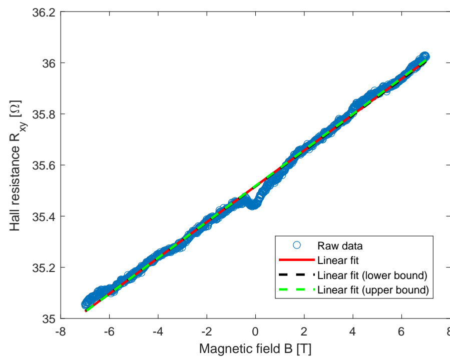



**Fig. 10:** Linear fitting of D1 for upwards sweep of magnetic field, including deviation in coefficients for 95% confidence. Note that the dip at zero magnetic field is a quantum interference effect known as weak anti-localization.

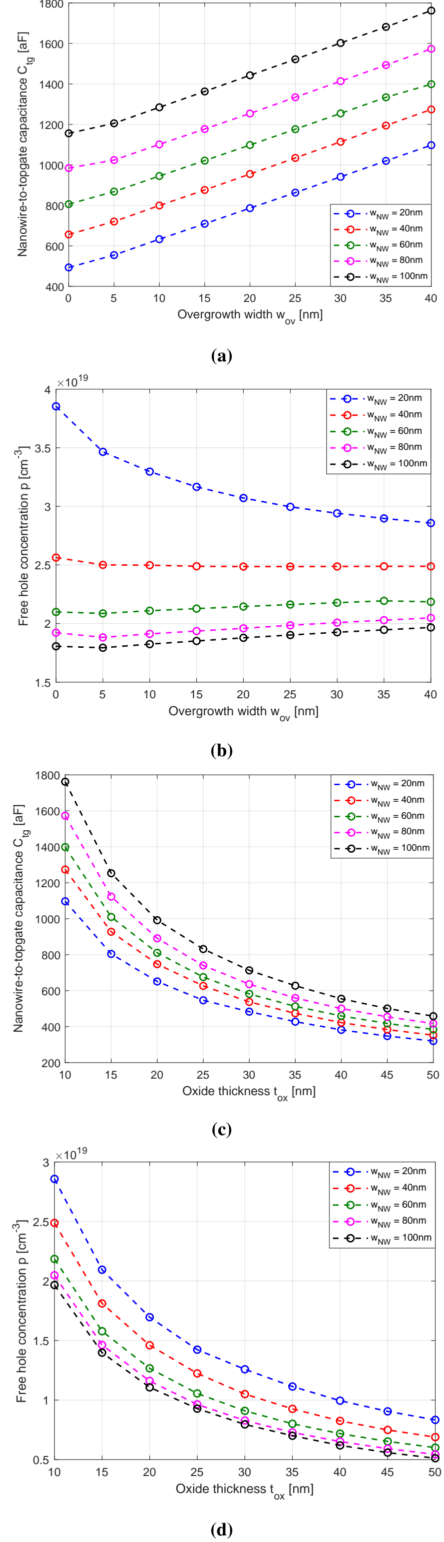
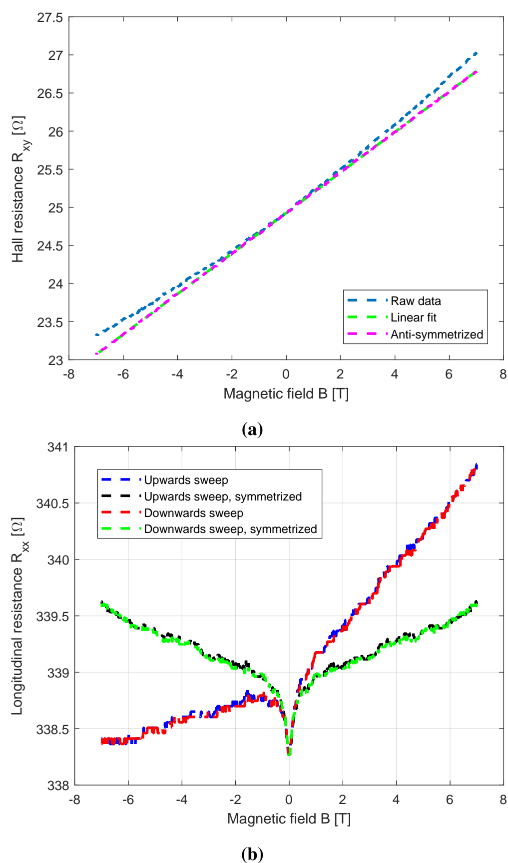



**Fig. 9:** Nanowire-to-topgate capacitance $C_{tg}$ and corresponding free hole concentration $p$ values computed in COMSOL. **(a)** $C_{tg}$ versus the overgrowth width $w_{ov}$ for fixed $h_{ov} = 20$ nm, $t_{ox} = 10$ nm, and different $w_{NW}$. **(b)** $p$ versus the overgrowth width $w_{ov}$ for fixed $h_{ov} = 20$ nm, $t_{ox} = 10$ nm, and different $w_{NW}$. **(c)** $C_{tg}$ versus the oxide thickness $t_{ox}$ for fixed $h_{ov} = 20$ nm, $w_{ov} = 40$ nm, and different $w_{NW}$. **(d)** $p$ versus the oxide thickness $t_{ox}$ for fixed $h_{ov} = 20$ nm, $w_{ov} = 40$ nm, and different $w_{NW}$.




**(a)**

**(b)**

**Fig. 11:** Measurements are shown for D2 of the third generation of devices. **(a)** Measured Hall resistance versus the upwards swept magnetic field, including the raw data, as well as the linear fit and anti-symmetrized slope. Notice that the linear fit and anti-symmetrization are completely aligned. **(b)** Measured longitudinal resistance versus the magnetic field, shown for both sweep directions. Symmetrization is performed on the data to average out unwanted components.

The absolute errors in the slopes are also propagated accordingly when computing the error in both the carrier concentration and Hall mobility.

We also anti-symmetrize the transverse measurements about zero magnetic field so that only a Hall component remained, which showed exact alignment with our linear fitting procedures (see Figure 11a). Similarly, we symmetrize the longitudinal data about zero magnetic field as by definition the direction of the magnetic field does not affect the measured voltage: other components can mix in with the measurements, especially when there is an asymmetrical current distribution. Figure 11b shows both the raw longitudinal measurements, as well as the symmetrized data.