A Dual Active Bridge Based Battery Controller with Zero Voltage Switching for a Grid-Tied Small Wind Turbine

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***Abstract*—In this paper, a design is presented for a battery charge and discharge controller, for a grid-tied small wind turbine (SWT). For this, a dual active bridge (DAB) is used, which is an isolated bidirectional DC/DC converter which has variable power flow. Zero voltage switching (ZVS) is used for high efficiencies and a power splitting algorithm is designed to keep the SWT operating at maximum power point. Previous research has presented a DAB as a battery controller, but it has not used ZVS for increased efficiency. The previous systems could also not safely be connected to the grid. An example system was designed, which reached a theoretical maximum efficiency of 98.9% and a minimum efficiency of 90%. The working of ZVS was verified through simulations, where it was shown that ZVS cannot be used over the whole input voltage range, in these regions efficiency was decreased significantly.**

I. Introduction

In the current energy transition, the shift is towards clean energy sources like wind and solar, as well as towards clean energy storage devices like batteries and flywheels. Wind energy offers a great potential to areas that have a large average wind speed. Large wind turbines can be placed both on and offshore, however they are restricted where they can be placed both due to their size and regulation. When only powering a local grid, a small wind turbine (SWT) is a good option, as they can range between 200W to 300kW as defined by the Canadian Wind Energy Association [1]. Since the wind is not always blowing, the power generation is not reliable. This concern can be addressed with an energy storage device, like a battery, that can store power when an excess is produces and deliver power whenever needed. As the energy needs to go in and out of the battery, the battery controller needs to be as efficient as possible.

At the moment there are no so-called hybrid inverters for SWTs, these inverters connect the output of a SWT to both a battery and the grid. Currently, there is a system visible in Fig. 1 left, that can connect a SWT to a string inverter. It uses a rectifier, to convert the AC output of the SWT to DC. After which a boost converter is used to boost the voltage, so that the voltage is in the operating range of the inverter. However, if battery storage is desirable, the current solution is to connect it at the grid side. This requires more energy conversion steps, making it less efficient in theory.

Some progress has been made towards hybrid inverters for SWTs, a dual active bridge (DAB) has been proposed as a battery charge and discharge circuit [2]-[4]. A DAB is an isolated bidirectional DC/DC converter with variable power flow. These papers have already verified that a DAB can work as a charge and discharge circuit for SWTs. However, these systems do not use zero volt switching (ZVS), leading to high switching losses and/or large component sizes. The previous systems can also not be safely connected to the grid, but only to an AC load.

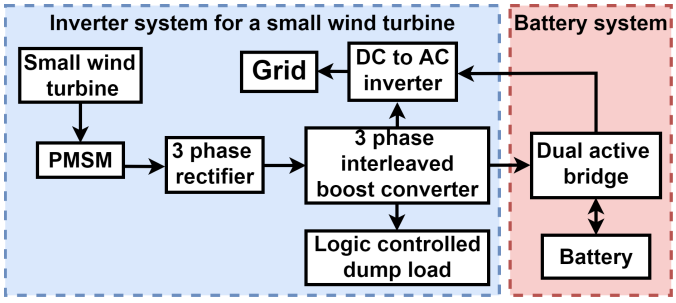


Fig. 1: A complete system overview. Left: the current inverter setup for a SWT. Right: the proposed battery system

This paper presents a novel approach for connecting a battery to a grid-tied SWT, using a DAB based battery controller with ZVS for improved efficiencies. An overview of the proposed system can be seen in Fig. 1. An analysis of the DAB has been performed, which outlined the working principles and a component selection approach. For the DAB the working principle and theoretical analysis of ZVS has been worked out. Using the analysis of the DAB and ZVS, an example is worked out and simulated to verify the design and the working of the ZVS. The design example had a maximum theoretical efficiency of 98.9% and a minimum of 90%.

The paper is arranged as follows: section II analyses the DAB as a charge and discharge circuit; its subsections describe in more detail how it works and how it is operated so that it can use ZVS. Section III discusses a complete system design example using the Nautila 3.5kW SWT: each subsection discusses a different part of the system, where the last discusses theoretical performance. Section IV describes the simulation results in order to validate the design example. Section V discusses the results, future research and error sources. Section VI outlines conclusive remarks.

II. Dual Active bridge as a charge and discharge circuit

A DAB was chosen because it can handle two-way power flow, is isolated, ZVS is possible, can handle highly variable input and output voltages, acts like a current source and can reach high efficiencies [5]. There is also a DAB with a capacitor before the transformer (resonant tank), called a resonant DAB converter. However, a resonant DAB requires a very tight converter gain for ZVS [6]. This is not possible

due to the SWT voltage fluctuating greatly, leading to a large fluctuation in converter gain.

A. Analysis of the dual active bridge

A DAB converter can be seen in Fig. 2, it has an H-bridge on the primary and secondary side of a high frequency (planer) transformer with a leakage inductor L_L and turn ratio n. If the leakage inductor is too small it can be enlarged with a regular inductor, where it does not matter on which side the inductor is, as long as the equivalent inductance is correct. An output capacitor C_{out} at the battery side of the DAB is placed in order to decrease the output voltage and current ripple. An input capacitor C_{in}, can also be added to reduce the ripple at the input when discharging. The switches used can be (SiC) MOSFETs or IGBTs, depending on system requirements. In Fig. 2 MOSFETs are drawn with their body diodes (D_1-D_8) and internal capacitors (C_1-C_8).

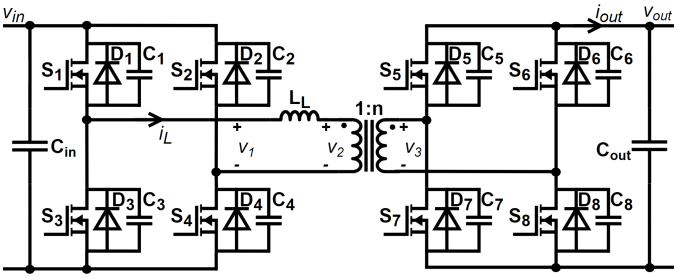


Fig. 2: DAB converter schematic, left four MOSFETs form the primary bridge and the right four MOSFETs form the secondary bridge.

Both H-bridges will create a square wave with a 50% duty cycle, neglecting the dead-time. This is done for the primary bridge by alternatingly driving the pair S_1, S_4 and the pair S_2, S_3. Similarly, in the secondary bridge the pair S_5, S_8 and the pair S_6, S_7 are driven alternatingly. But the alternation happens at a time shift φ of the primary bridge. This operating scheme is called single-phase-shift control [5], where the transmission power is determined by the time shift. The voltage waveform created by the primary bridge (v_1) and secondary bridge compensated for the turn ratio (v_2=$\frac{v_3}{n}$) can be seen in Fig. 3, where the waveform is plotted for one period. The voltage drop over L_L is the voltage difference between the primary and turn ratio compensated secondary bridge ($v_L = v_1 - v_2$). This voltage can also be seen in Fig. 3, where it is visible that the voltage over the L_L goes through four intervals as defined in the figure. The time an interval takes is dependent on the time shift.

The current waveform through L_L can be seen in Fig. 3. Where the slope of the current is dependent on the inductor value and input and output voltage. Due to half-wave symmetry, if the current is known for the first two intervals, the other two intervals are also known. The current i_1 and i_2 as defined in Fig. 3 define the currents at which the MOSFETs switch. When $v_{in} > \frac{v_{out}}{n}$ (as in Fig. 3), i_1 is the switching current of the secondary bridge and i_2 is the switching current of the primary bridge. Vise versa when $v_{in} < \frac{v_{out}}{n}$.

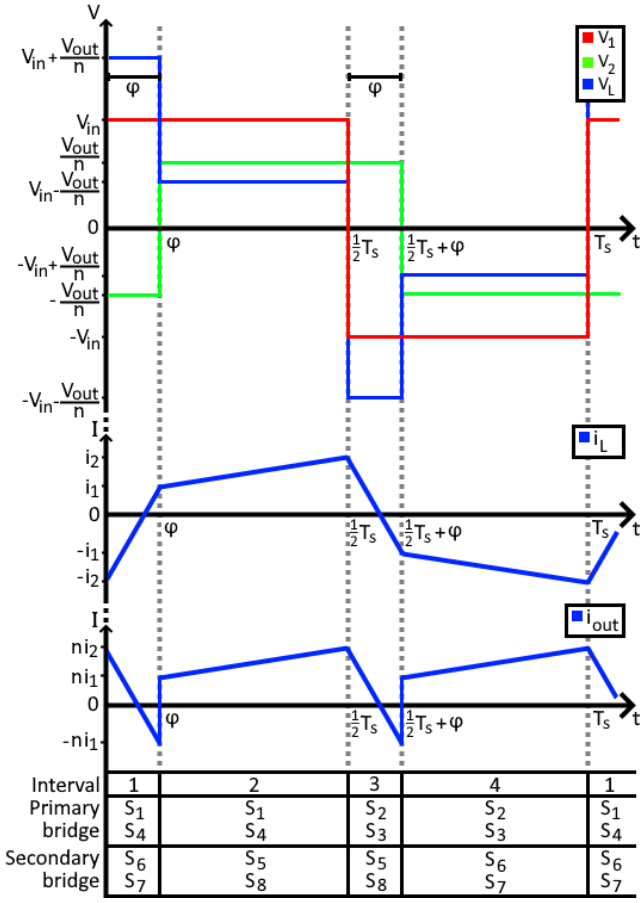


Fig. 3: Waveforms of the charging mode of the circuit of Fig. 2. Top: voltages of the primary (V_1) and secondary (V_2) bridge and leakage inductor (V_L), with time shift φ. Middle: leakage inductor current (i_L). Bottom: output current (I_{out}). Table: switches turned on at each interval.

i_1 and i_2 can be calculated with eq. 2 and eq. 3. Where v_{in} is the input voltage, n is the turn ratio, L_L is the leakage inductor value, f_s is the switching frequency and D_φ is the phase shift ratio defined by eq. 1. Substituting these two equations yields eq. 4 and eq. 5. Where eq. 5 is also the maximum inductor current and at the secondary side the current is $\frac{1}{n}$ higher.

$$D_\varphi = 2\varphi f_s = \frac{2\varphi}{T_s} \tag{1}$$

$$i_1 = -i_2 + \frac{1}{L_L}\int_0^{\varphi} v_{in} + \frac{v_{out}}{n} dt = -i_2 + \frac{v_{in} + \frac{v_{out}}{n}}{L_L} \cdot \frac{D_\varphi}{2f_s} \tag{2}$$

$$i_2 = i_1 + \frac{1}{L_L}\int_{\varphi}^{\frac{T_s}{2}} v_{in} - \frac{v_{out}}{n} dt = i_1 + \frac{v_{in} - \frac{v_{out}}{n}}{L_L} \cdot \frac{1 - D_\varphi}{2f_s} \tag{3}$$

$$i_1 = \frac{v_{in} + \frac{v_{out}}{n}\left(2D_\varphi - 1\right)}{4L_L f_s} \tag{4}$$

$$i_2 = \frac{\left(2D_\varphi - 1\right)v_{in} + \frac{v_{out}}{n}}{4L_L f_s} \tag{5}$$

For the battery and MOSFETs it is optimal that the peak current is as small as possible. The smallest voltage difference occurs when the turn ratio (n) of the transformer equals:

$$n = \frac{v_{out}}{v_{in}} \tag{6}$$

If the input/output voltage varies, the optimal turn ratio can still be chosen to minimize the peak current. This can be done by choosing the median for the input/output voltage, or nominal value if the average peak current needs to be reduced. If the peak current is still too high, a filter can be placed before the battery to reduce the peak current. However, when using ZVS it is better to choose the turn ratio to optimize the range wherein ZVS can occur (see in section II.B).

The output current (i_{out}) is the rectified version of i_L divided by the turn ratio, where if S_5, S_8 are on $i_{out} = \frac{i_L}{n}$ and when S_6, S_7 are on $i_{out} = -\frac{i_L}{n}$. In Fig. 3 the output current waveform is shown, where it is already visible that the average output current is positive in the charging state as expected. Source [7] gives a full derivation of the average output current, the final formula is given in equation 7.

In eq. 8 the average output power is calculated using eq. 7. Fig. 4 shows the average output power versus the phase shift ratio (D_φ), from which it is visible that the power flow can indeed be regulated by the value of D_φ. When D_φ is zero the power is zero, increasing D_φ until 0.5, will increase the power (charging) and decreasing D_φ up to -0.5, will increase the negative power flow (discharging). The maximum/minimum value of D_φ should be chosen smaller than 0.5, to leave a little room for transients and because the control action flips at $D_\varphi = \pm 0.5$, which should be avoided for more stable/simpler controllers [8]. Therefore, the range should be limited to $-0.45 \leq D_\varphi \geq 0.45$.

$$i_{out,av} = \frac{v_{in} D_\varphi (1 - |D_\varphi|)}{2 n L_L f_s} \tag{7}$$

$$P_{out,av} = i_{out,av} \cdot v_{out} = \frac{v_{in} v_{out} D_\varphi (1 - |D_\varphi|)}{2 n L_L f_s} \tag{8}$$

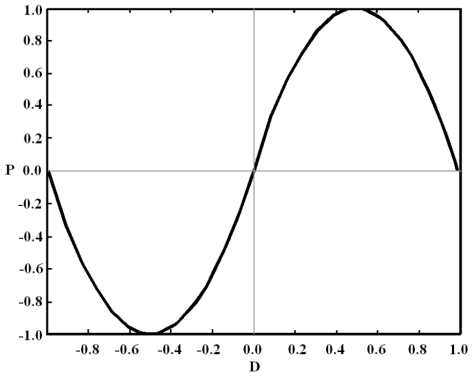


Fig. 4: Average output power characterization of a DAB using a single-phase-shift control [4].

To reduce the ripple at the output, an output capacitor (C_{out}) is used. Using eq. 9 [8], the size of the capacitor can be calculated so that it satisfies for the largest ripple voltage (Δv_{out}) allowed. Where the maximum input voltage and D_φ should be used. The input capacitor can also be calculated with eq. 9, but v_{in} should become v_{out} and vice versa.

$$C_{out} = \frac{v_{in,max} D_{\varphi,max}^2}{8 f_s^2 L_L n \Delta v_{out}} \left(\frac{D_{\varphi,max}^2}{4} - D_{\varphi,max} + 1 \right) \tag{9}$$

B. Soft switching

To reduce the amount of switching loss, soft switching can be used. There are two options, zero current switching (ZCS) and zero voltage switching (ZVS). As the name implies, the MOSFETs are switched at zero voltage or current. The switching loss is zero when either the current (i_{out}) or voltage (v_{ds}) is zero. ZCS will not be considered, because when using single-phase-shift with ZCS, the power would be no longer variable [9].

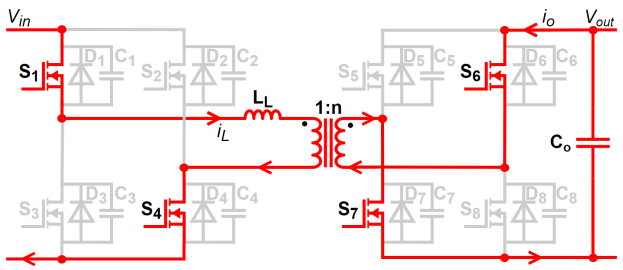
The chosen ZVS method, uses the inductor current to discharge the internal MOSFET capacitors until the internal diodes turn on at the transition between intervals. When the diodes turn on, the voltage over the MOSFETs is equal to the forward bias voltage drop of the internal diodes, which is close to zero volt.

In Fig. 5 this principle is shown for the transition from interval 1 to 2. In Fig. 5a the equivalent circuit at the end of interval 1 is shown, which ends when S_6 and S_7 are turned off. After which the current will discharge the capacitors of S_5 and S_8, as shown in Fig. 5b. When the capacitors are discharged to the forward bias voltage of the internal diodes, the diodes turn on, as shown in Fig. 5c. The diodes conduct until their corresponding switch is turned on as shown in Fig. 5d, at which point the circuit has transitioned to interval 2 with ZVS. The same happens for the other transition periods, where the internal diodes conduct before the MOSFET is switched on. ZVS can both work in charging and discharging mode, as the design is symmetrical.

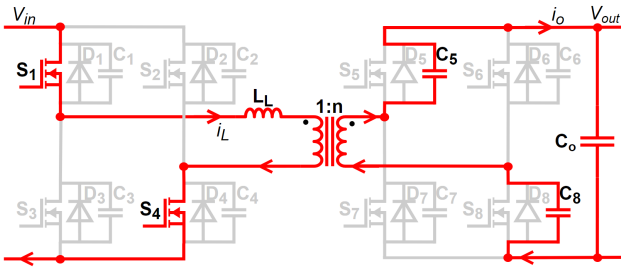
For this operating scheme, the dead time (t_d) is important. If the dead time is too short, the MOSFET will turn on before the diodes conduct, meaning that there will be switching loss. If the dead time is too long, the diodes conduct for a long time and the diodes have a greater conduction loss than MOSFETs, so this will also lead to more loss. However, the conduction losses caused by the diodes are smaller than that of the switching loss in most cases. So a longer dead time is more favorable than a too short dead time, so a margin is preferable, this margin can be chosen equal to the maximum possible deviation in dead time. This maximum deviation is unkown, so the author will arbitrary use 20%. The dead time is different for both bridges and is load dependent, it can be calculated with eq. 10. i_{switch} is the current at the switching instance, it can be found with i_1 and i_2, where the current on the secondary side is $\frac{1}{n}$ higher. v_{ds} is the voltage over the drain and source of the switch, this is v_{in} for the primary side and v_{out} for the secondary side. C_{oss} is the output capacitance that can be found in the datasheet of the MOSFETs.

$$t_d = \frac{2 v_{ds} C_{oss}}{i_{switch}} \tag{10}$$

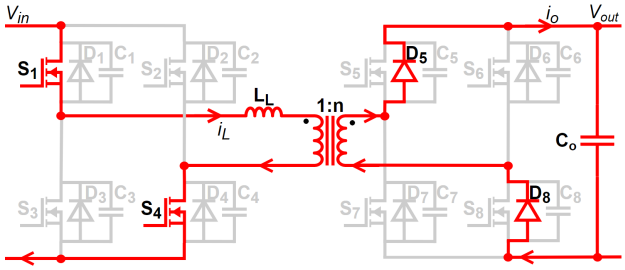
The dead time cannot be too large as this will disrupt the power flow too greatly, the actual maximum dead time is



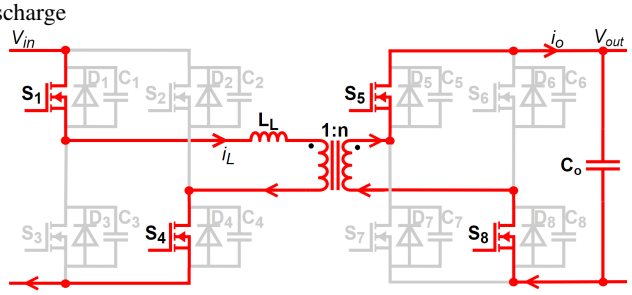
(a) Equivalent circuit at end interval 1



(b) Equivalent circuit between interval 1 and 2, where C_5 and C_8 discharge



(c) Equivalent circuit between interval 1 and 2, where 2 diodes conduct



(d) Equivalent circuit at interval 2

Fig. 5: Equivalant circuit for switching from time interval 1 to 2 in charging mode, where the intervals are defined in Fig.3

highly dependent on the system requirements. A minimum dead time should also be implemented in order to prevent a shoot through (short circuit) from occurring.

ZVS is not possible under all operating conditions. The range in which ZVS can be applied with this method, can be found by determining the minimum current needed to charge/discharge the capacitors. The minimum energy needed to charge two and discharge the other two capacitor can be calculated with eq. 11. This energy is provided by the inductor, this energy can be calculated with eq. 12. Combining eq. 11 and 12 results in a minimum inductor current defined by eq. 13. Where the value is different for the primary and secondary bridge, as C_{oss} is different for the primary and secondary MOSFETs. This equation holds for interval 1 and 2, for interval 3 and 4 the current should be negative $i_{L,min}$.

$$E_{min} = 4 \cdot \frac{1}{2} C_{oss} v_{ds}^2 \tag{11}$$

$$E_{min} = \frac{1}{2} L_L i_{L,min}^2 \tag{12}$$

$$i_{L,min} = \sqrt{\frac{4C_{oss}}{L_L} v_{ds}^2} \tag{13}$$

Rewriting eq. 4 and 5 for D_φ, results in eq. 14 and 15, which indicate the minimum D_φ for ZVS of the primary and secondary bridge. In the situation that no ZVS is possible, hard switching (HS) is used. Where the MOSFETs are switched as fast as possible to reduce losses. There is still a dead time in order to prevent shoot through and the value should be as small as possible and is dependent on MOSFETs and their drivers.

$$D_{\varphi,pri} > \frac{v_{out} - v_{in} n + 4 f_s L_L i_{L,min} n}{2 v_{out}} \tag{14}$$

$$D_{\varphi,sec} > \frac{v_{in} - \frac{v_{out}}{n} + 4 f_s L_L i_{L,min}}{2 v_{in}} \tag{15}$$

Eq. 14 and 15 are equal when $v_{out} = v_{in} n$. This point is the center point of the ZVS region, where both sides can use ZVS. The width of this region is dependent on the D_φ setting. In section III.D it is found that the primary side has significantly more switching losses than the secondary side, so that it is beneficial to have the primary bridge using ZVS at nearly all input voltages. Using eq. 6 the center point can be chosen to be at the minimum input voltage, for a specific battery voltage. This battery voltage can be set to the maximum voltage to ensure primary bridge ZVS under all conditions. Or the battery voltage can be chosen at a lower level to reduce peak currents, this results in no ZVS in the primary bridge for low power levels with a higher than chosen battery voltage.

III. Design Example

The SWT used for this example is the Nautila 3.5kW horizontal-axis SWT. It has a maximum output of 3.5kW at a wind speed of $15.5\mathrm{m\,s^{-1}}$, with a known optimal power curve for generator speed and turbine power [10]. The current system can be seen in blue in Fig. 1 left, where the permanent magnet synchronous motor (PMSM) of the SWT is connected to a full-bridge rectifier, to convert the AC to DC. A three-phase interleaved boost converter is connected thereafter, to boost the signal to at least 130V, in order to meet the minimum input voltage of DC to AC inverter. The ”Fimer UNO DM 3.3” is used as the DC to AC inverter, which is a string inverter commonly used for PV arrays. If the input is higher than 130V, the boost converter will not boost, and the voltage can reach up to 450V. The output power of the inverter can be adjusted from 0W until 3kW with increments of 3W. A power signal feedback (PSF) controller is used for maximum power point tracking (mppt). A dump load circuit is present to burn unwanted energy, there is both an active and relay diversion mechanism.

Using the approach of section II and the system requirements of table I, the inverter system for a SWT will be modified into a $3kW$ hybrid inverter.

A. Battery

The battery cells used are the "WINSTON WB-LYP90AHA $\mathrm{LiFeYPO_4}$ 3.3V 90Ah". The reason for a $\mathrm{LiFeYPO_4}$ battery is that it can operate in temperatures between -25 until 75 °C [11]. This is needed as the battery will operate in the Netherlands, where the temperature can fluctuate between -20 and 37 °C [12]. For comparison, lithium-ion and lead-acid batteries have an operating range of 0 to 45 °C and 20 to 25 °C respectively [13]. When these batteries are used, active cooling/heating should be used, which adds unwanted complexity and power consumption. Other benefits of the $\mathrm{LiFeYPO_4}$ are that the cycle life is more than 3000 with a 70% depth of charge, and good fire safety [11].

In combination with a battery management system (BMS) the cells can be connected in series to increase the capacity of the battery system. The author will use the "tiny BMS s516 $150-700$A", as it can handle 4-16 $\mathrm{LiFeYPO_4}$ cells and is easy to prototype with. This BMS has as downside that the minimum current in or out the battery pack should be $\pm 800\mathrm{mA}$ [14].

It was chosen that at the maximum discharge rate of $3\mathrm{kW}$, the battery should last at least one hour. The capacity of the battery therefore also needs to be $3\mathrm{kW}$ and each cell has $300\mathrm{Wh}$ of power [11], so 10 cells will be used in series. This gives a voltage range between $25\mathrm{V}$ and $42.5\mathrm{V}$, and offers a maximum charge/discharge current of $180\mathrm{A}$ [11].

B. Power splitting

It is important to keep the SWT operating at maximum power point (mpp), the current system uses a power signal feedback (PSF) controller at the inverter to do this. If no alterations were made, charging or discharging the battery would result in the SWT not operating at mpp. A solution to this is to have the inverter deliver the power requirement by the local grid and have the battery system charge/discharge to draw the optimal amount of power from the SWT. The optimal power is determined by a PI controller. This controller tries to keep the total power of the SWT at mpp as determined by the PSF by operating the DAB.

There are seven exceptions when this does not hold. The first is when charging the battery and it is fully charged, and the second when discharging and the battery is empty. In these cases, the mppt will be fully regulated by operating the inverter. The third exception is when the maximum charging/discharging current of the battery state is reached (as determined by the BMS), in that case it will maintain the maximum current and the inverter will regulate the mppt until the battery current can be below the maximum. The fourth exception is when the efficiency would be below 90%, as at that point it would be more efficient to use an AC powerwall [15]. The fifth exception is when the requested charge/discharge current is between $-800\mathrm{mA}$ and $800\mathrm{mA}$, under which the BMS will remain in sleep mode [14]. For the fourth and fifth exception, the inverter will regulate the mppt. The sixth exception is when the inverter is not coupled to the grid, in this case the mppt will be regulated only by the battery system and/or dump load. The exception is when the BMS outputs a fault, in that case the inverter will take over the mppt until the fault is cleared.

C. DAB component calculation

Using the analysis of section II and Table I, the components will be calculated. The turn ratio can still be found by using eq. 6, where it is optimized for ZVS as described in section II.B. The input voltage is taken as $130\mathrm{V}$, because this provides the best primary ZVS range. The nominal battery voltage as determined by its manufacture is $33\mathrm{V}$ [11], this value is used as it will ensure that the peak currents do not get too large. In eq. 16 the turn ratio is calculated to be 4:1. Power planar transformers are not available 4:1 with $3\mathrm{kWh}$, however they can be designed [16].

$$n = \frac{v_{out}}{v_{in}} = \frac{33}{130} \approx 0.25 \tag{16}$$

TABLE I: Circuit requirements for the DAB.

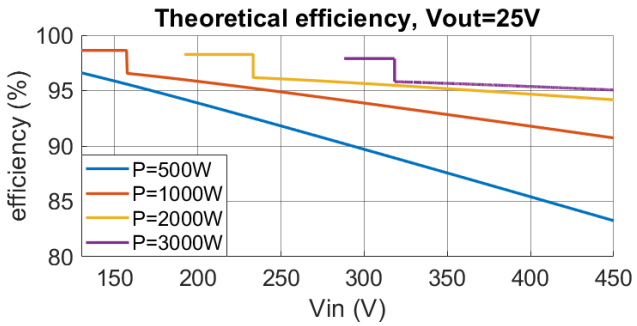
Item	Symbol	Value
DC link voltage	v_{in}	130V - 450V
Battery voltage	v_{out}	25V - 42.5V
Power range	$P_{out,av}$	-3kW - 3kW
Maximum output voltage ripple	$\Delta v_{out,av-pk}$	$0.01 v_{out}$= 250mV

For the switching components in the primary bridge, IGBTs and SiC MOSFETs are both possible due to the high maximum voltage. SiC MOSFETs are chosen as they can switch faster, have lower switching loss than IGBTS [17] and have a low on-resistance. Normal MOSFETs can be used in the secondary bride due to the lower voltage requirements. For the primary bridge the SiHG70N60AEF MOSFETs are chosen and for the secondary bridge the IRFP3206PbF.

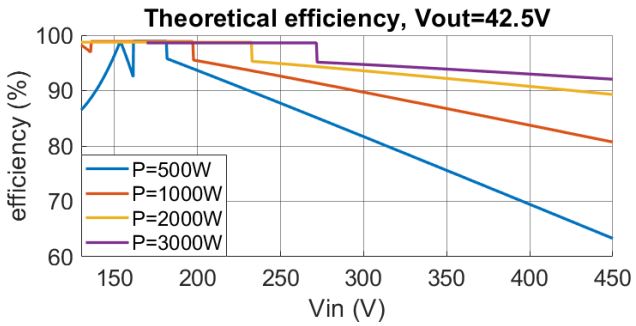
The switching loss is linear with the switching frequency (f_s), however a high switching frequency means smaller components. ZVS is used in order to minimize the switching losses, but the range does not extend to the smaller power levels. $100\mathrm{kHz}$ was found to be a reasonable value where component size was not too large and switching loss at medium power was acceptable (see section III.D). Rewriting eq. 7 for L_L, gives the eq. 18. In this equation, all the values should be chosen such that the inductor value is maximized, to ensure the circuit working under all conditions. The maximum output current is calculated in eq. 17 and $D_{max} = 0.45$. With this in eq. 18 the maximum leakage inductor size is calculated to be $12\mu\mathrm{H}$.

$$i_{out,av,max} = \frac{P_{max}}{v_{out,min}} = \frac{3000}{25} = 120\mathrm{A} \tag{17}$$

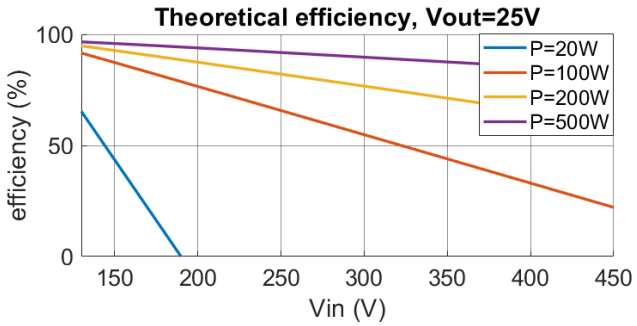
$$\begin{aligned} L_L &= \frac{v_{in,min} D_{\varphi,max}(1 - D_{\varphi,max})}{2 f_s i_{out,av,max} n} \\ &= \frac{130 \cdot 0.45(1-0.45)}{2 \cdot 100000 \cdot 120 \cdot 0.25} \approx 12\mu\mathrm{H} \end{aligned} \tag{18}$$



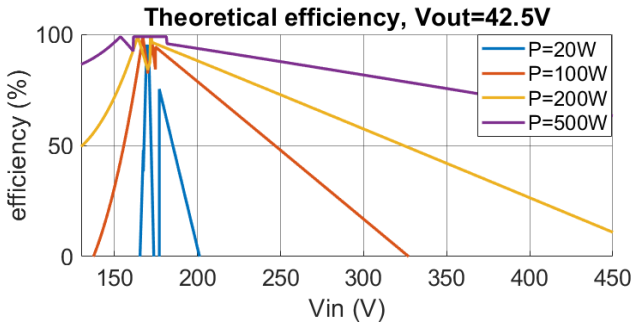
(a) Theoretical efficiency at minimum battery voltage ($25V$), high power.



(b) Theoretical efficiency at maximum battery voltage ($42.5V$), high power.



(c) Theoretical efficiency at minimum battery voltage ($25V$), low power.



(d) Theoretical efficiency at maximum battery voltage ($42.5V$), low power.

Fig. 6: Theoretical efficiency at minimum ($25V$) and maximum ($42.5V$) battery voltage, for different power settings. Taking into account transformer loss, switching loss and conduction loss.

The minimum output capacitor value can be calculated using eq. 9 and the before determined components. In eq. 19 the minimum output capacitor has been calculated, the capacitors used has a 10% tolerance, so when taking this into account the final output capacitor is chosen to be 1000µF. The same can be done for the input capacitor, which results in $C_{in} = 5.3$µF.

$$C_{out} = \frac{450 \cdot 0.45^2}{8(10^5)^2(12 \cdot 10^{-6}) \cdot 0.25 \cdot 0.25}\left(\frac{0.45^2}{4} - 0.45 + 1\right) = 912\text{µF} \tag{19}$$

D. Theoretical performance

There are multiple sources of losses: switching loss, conduction loss and transformer loss (including leakage inductor). There are also, gate driver losses, shunt losses and other smaller losses, but these will be neglected. The efficiency of the transformer, when looking at similar transformers will be roughly 99% [18]. The switching loss can be calculated using eq. 20-22 [19] and the conduction loss can be calculated with eq. 23 [19], where the i_{ds} is the current through the MOSFETs.

$$t_{on} = R_G C_{iss} \ln\left(\frac{v_{gs} - v_{th}}{v_{gs} - v_{gp}}\right) + \frac{R_G Q_{gd}}{v_{gs} - v_{gp}} \tag{20}$$

$$t_{off} = R_G Q_{gd} \frac{v_{ds}}{v_{gp}} + R_G C_{iss} \ln\left(\frac{v_{gp}}{v_{th}}\right) \tag{21}$$

$$P_{sw} = \frac{1}{2} v_{ds} i_{out} (t_{on} + t_{off}) f_s \tag{22}$$

$$P_{con} = i_{ds}^2 R_{ds} D_{duty} \tag{23}$$

The values and symbol meaning, can be found in the data sheet of the MOSFETs [20] [21]. The theoretical driving will follow the setup used by [22], which has a total gate resistance (R_G) of 1Ω and the gate source voltage (v_{gs}) of $15V$ for all MOSFETs. The gate source voltage (v_{gs}) is equal to the input voltage (v_{in}) for the primary bridge and output voltage (v_{out}) for the secondary bridge, if there is no ZVS. It is equal to the diode forward voltage, if there is ZVS. Using eq. 4, 5, 7, 8, 13-15 and 20-23, the efficiency is plotted in Fig. 6 for the total input voltage range and different power levels, at minimum and maximum battery voltage.

In Fig. 6a, it can be seen that not all power levels extend the whole input voltage range. This is in line with the design which was made so that at $V_{in} = 300$V, the system could deliver 3000W. Meaning that if the input voltage is lower, the maximum power is reduced. It can be seen that the efficiency of 1000W, 2000W and 3000W have a drop in efficiency of 2%. This is the point where the secondary bridge no longer can use ZVS and the added switching losses reduce the efficiency. The power level of 500W already starts outside the ZVS range of the secondary bridge, but all power levels start inside the ZVS of the primary bridge. The efficiency when the battery is at its minimum value and when both bridges can use ZVS is between 98.6% and 97.9% dependent on the power. When no ZVS can be used at the secondary bridge, the efficiency is lower than 96.6%. In Fig. 6c, the efficiency of the lower

power levels is shown. In which it is visible that due to ZVS not being possible in the secondary bridge, the efficiency can reach 0% for power levels below 80W. As stated before, when the efficiency is below 90%, the DAB will turn off. In Fig. 6a and 6c it can be seen that at minimum battery voltage the efficiency can be below 90% at high input voltages for power levels below 1000W and for all input voltages below 100W. This efficiency gets so low at high input voltages, due to the currents at the switching instances increasing when the voltage difference between v_1 and v_2 is increases. The switching loss increases when the current trough the MOSFETs at the switching instance increases, leading to lower efficiencies at higher input voltages.

In Fig. 6b and 6d the battery is at maximum voltage, where the behaviour is similar as for Fig. 6a and 6c. The main difference is that the efficiency is lower and that the primary bridge can fall outside its ZVS range for low power levels. This can be seen for the power level of 500W and lower, where the efficiency increases as the current goes from negative to zero. When the current hits zero there is actually ZCS, after the ZCS there is a decrease in efficiency until ZVS is possible (negative spikes before plateau). The primary ZVS range was chosen so that it was possible under all conditions up to a battery voltage of 33V, at maximum battery voltage and low power this is indeed no longer possible for low input voltages as seen in Fig. 6b and 6d.

In Fig. 6d, it is also visible that the slope of the efficiency increase before the secondary ZVS region is greater than the efficiency decrease after the secondary ZVS region. Meaning that it is indeed better to have a wider primary bridge ZVS than secondary ZVS range. This makes it clear that the primary bridge, has higher losses than the secondary bridge, when not in ZVS range. The lower efficiency at maximum battery voltage is due to higher peak currents and these peak currents happen at the switching instances, thus increasing switching loss.

The efficiency when both bridges can use ZVS is between 98.9% and 95% (when the power is above 100W). Outside the ZVS range, the efficiency is at most 96%, but can reach 0% for close to maximum or minimum input voltages at a power below 150W. In Fig. 6d for 20W it can be seen that there are two peaks, the first peak is from ZCS. This peak reaches an efficiency of 95%, after which the efficiency drops until the ZVS region is reached. This only resulted in a efficiency of 75%, compared to more than 95% for the higher power levels. This is because, when switching at the diode voltage there is still switching loss, this is small compared to the large power levels. However, compared to the 20W this switching loss is significant.

IV. Simulation Results

The simulations have been performed with MATLAB Simulink to confirm that ZVS can indeed be used for the in section III designed battery system for a SWT. The model uses ideal MOSFET drivers, current sensors and voltage sensors. The model does not use a SWT, but a variable voltage source. The dead time is calculated using a current sensor at L_L, instead of using eq. 4 and 5.

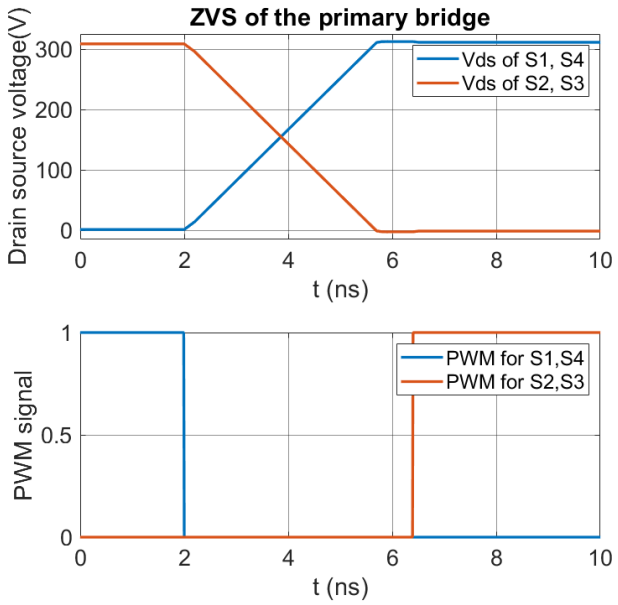


Fig. 7: Drain source voltage and PWM simulation results. With $V_{in} = 310$V, $V_{out} = 30.0$V, charging at 1000W and time steps of 0.1ns.

The simulation conditions are $V_{in} = 310$V, $V_{out} = 33.0$V and the system is charging at 1000W. Using the eq. 1, it can be predicted that only the primary bridge can use ZVS and the secondary bridge needs to use HS. Fig. 7 shows the simulated source drain voltage and the pulse-width modulation (PWM) signal of the MOSFETs of the primary bridge. It can be seen that the voltage over S_2 and S_3 decreases from V_{in} to negative diode forward voltage, when the PWM of S_1 and S_4 is turned to low. That the voltage goes to the negative diode forward voltage, means that the diodes D_2 and D_3 conducts. When the PWM of S_2 and S_3 is turned high, the voltage increases to nearly zero. Meaning, what we see is ZVS.

The results for the next cycle where the PWM of S_1 and S_4 goes high and PWM S_2 and S_3 goes low are identical, except the voltage over S_1 and S_4 decreases and over S_2 and S_3 increases. This indeed verifies that the primary bridge can use ZVS and that the dead time is sufficiently large.

The total time taken to go from V_{in} to zero is 3.7ns and the total dead time is 4.4ns. This means that the dead time is 19% larger, which is close to the 20% margin used. The PI controller outputs a value of $D_\varphi = 0.061$. The simulated inductor current for switching the primary bridge is 40.4A, eq. 4 predicts that this would be 40.4A. The current is estimated correctly, so the dead time could also have been determined by using eq. 4 instead of using a current sensor.

Fig. 8 shows the simulated source drain voltage of the secondary bridge and the PWM signal. The conditions remain the same, except the time axis has been shifted with $\varphi = 303$ns. It can be seen that the voltage does not drop close to zero volt before the PWM signal changes. The voltage instead rises with an extra diode voltage, due to D_6 and D_7 conducting, instead of D_5, D_8 as for ZVS. This is due to the fact that the current is in the opposite direction as would be needed for ZVS. This

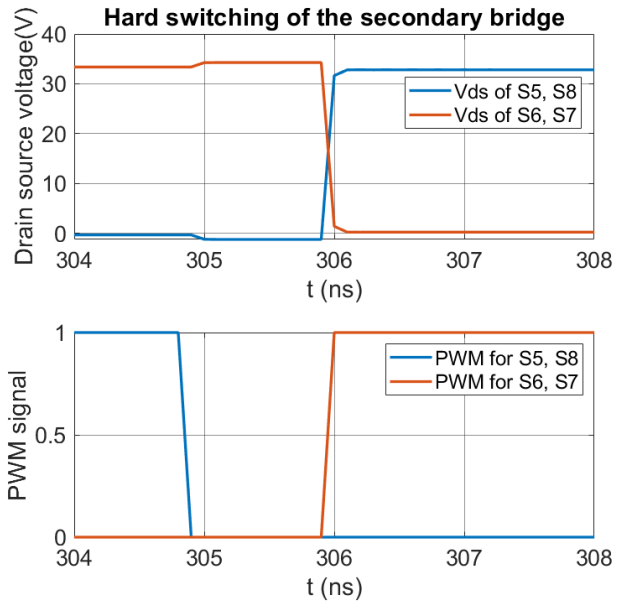


Fig. 8: Drain source voltage and PWM simulation results. With $V_{in} = 310\text{V}$, $V_{out} = 30.0\text{V}$, charging at 1000W and time steps of 0.1ns.

also verifies that the secondary bridge cannot use ZVS under these conditions, which was also expected by eq. 15.

The measured inductor current i_1 is -28.9A, eq. 4 would have estimated the current to be -29.2A. The current has a small error. When using HS, this is not a big problem. However, for ZVS a small error could lead to a different dead time, this is not a problem as long as it stays withing the 20% margin.

The output voltage has a ripple of $\pm 81\text{mV}$ at 33.0V, which is within the maximum ripple of $250mV$. The output current into the capacitor has a range from -117A to 160A. The current range into the battery is from 29.8A to 33.0A, which means that the capacitor also acts like a low pass filter for both the voltage and current. The power can go from 0W to 1000W in 0.2ms. It should be noted that these parameters change, for a change in power flow, temperature, input voltage and battery state of charge. From the above, it can be stated that the DAB can work with ZVS and HS for operation as a battery charger and discharger.

V. Discussion

Previous work [2], [3] have already verified the working of a DAB for a SWT, as a battery charger and discharger. Using a similar design, the simulations verified the working of ZVS at the primary bridge and that ZVS was not possible at the secondary bridge, for $V_{in} = 310\text{V}$, $V_{out} = 33.0\text{V}$ and the system is charging at 1000W. Due to the close match of the theory with the simulation, it is assumed that this trend will extend to the whole range. On these bases, it is stated that the current design can work with ZVS at other operating conditions as well, as long as it is withing the ZVS range. However, the simulation does not prove that the dead time is sufficiently large over the whole ZVS region and if the ZVS region is correctly defined.

A higher error is expected for the theoretical model, due to the assumption that $v_1 = \pm v_{in}$, $v_2 = \pm \frac{v_{out}}{n}$ and $v_L = v_1 + v_2$. As there is a non-constant voltage drop over the MOSFETs (conductance or body diodes) and transformer resistance, dependent on the square of the current. This voltage drop should be subtracted from v_1 and v_2 in order to get a closer approximation of what the voltage over the leakage inductor is. Therefore, the leakage inductor voltage changes if the current changes. The steps in eq. 2 and 3 are therefore not true, resulting in an error between theory and practice at larger currents. This has can be observed in the results, as i_1 is lower than expected due to the before named voltage drops.

The theoretical efficiency plot of Fig. 6 is a maximum efficiency as a wide variety of other power losses are neglected. The boundaries of the ZVS that are visible are also ideal, the expected boundaries will be a bit smaller. The range where both the primary and secondary bridge can use ZVS is small, but this small region has high efficiencies. [23] has found that this ZVS range can be extended by adding a buck boost converter at the input of the DAB, i.e. to create a narrow input voltage range and thus increasing the ZVS range. This would reduce peak efficiency, but increase the average efficiency significantly more. Further research is needed to look into the feasibility of using the buck-boost DAB with a SWT and the effects on the efficiency.

VI. Conclusion

In this paper a design is presented of a DAB as a charge and discharge circuit for a grid-tied SWT, using ZVS. This pointed out that there are specific operating regions where ZVS cannot be used in the primary and/or secondary bridge. In addition, the author has worked out a design example and a simulation to verify the working of ZVS and how the SWT can be kept at mpp. Simulation results demonstrated that ZVS can be used to decrease switching loss and improve efficiency, as well as that the theoretical model provided an accurate dead time estimation. The theoretical performance of the design example was found to be between 98.9% and 90%, dependent on operating conditions. Where if both bridges could use ZVS, the efficiency would not drop below 95% for the power levels above 100W. Further research is needed to point out if the overall efficiency could be increased by adding a buck-boost circuit before the DAB.

References

[1] Canadian wind energy association. (n.d.). Small Wind Turbine Purchasing Guide. From web.archive.org/web/20130302211547/www.ontario-sea.org/Storage/39/3065_Small_Wind_Turbine_Purchasing_Guide_-_Off-grid%2C_Residential%2C_Farm_%26_Small_Business_Applications.pdf

[2] Y. Takayama and H. Yamada, "Dual Active Bridge Converter Based Battery Charger in Stand-Alone Wind Power Generation System With High-Inertia Wind Turbine," 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), 2019, pp. 1-5, doi: 10.1109/ICEMS.2019.8921791.

[3] Y. Takayama and H. Yamada, "Experimental Verification of Dual Active Bridge Converter Based Battery Charger in a Stand-Alone Wind Power Generation System," 2020 23rd International Conference on Electrical Machines and Systems (ICEMS), 2020, pp. 1022-1026, doi: 10.23919/ICEMS50442.2020.9290867.

[4] G. Barone et al., ”A dual active bridge dc-dc converter for application in a smart user network,” 2014 Australasian Universities Power Engineering Conference (AUPEC), 2014, pp. 1-5, doi: 10.1109/AUPEC.2014.6966538.

[5] B. M. Kumar, A. Kumar, A. H. Bhat and P. Agarwal, ”Comparative study of dual active bridge isolated DC to DC converter with single phase shift and dual phase shift control techniques,” 2017 Recent Developments in Control, Automation Power Engineering (RDCAPE), 2017, pp. 453-458, doi: 10.1109/RDCAPE.2017.8358314.

[6] H. Chen, ”High-Frequency Isolated Dual-Bridge Series Resonant DC-to DC Converters for Capacitor Semi-Active Hybrid Energy Storage System,” M.A.Sc. thesis, Dept. of ECE, Univ. of Victoria, Canada, 2015.

[7] McRae, T. (2021, May 28). Lecture 8.8: The Dual Active Bridge. YouTube. From youtu.be/FSGQEqNU588

[8] McRae, T. (2021b, July 6). Tutorial 5: DAB Design. YouTube. From youtu.be/w5SGHoz5zPE

[9] A. Amin, ”A Transformerless Dual Active Bridge DC-DC Converter for Point-of-Load Power Supplies,” M.A.Sc. thesis, Dept. of ECEm Univ. of Toronto, Canada, 2015. from tspace.library.utoronto.ca/bitstream/1807/70201/1/Amin_Amr_201511_MAS_thesis.pdf

[10] Nautilus Power. (n.d.). NAUTILA 3.5 technical specs. From https://www.nautilus-power.com/nautila-3-5

[11] Thunder Sky. (n.d.) Instruction Manual for LFP/LCP/LMP Lithium Power Battery. From https://www.thunderstruck-ev.com/Manuals/Thundersky%20Product%20Manual.pdf https://faktor.de/out/media/TinyBMS_Use_Manual.pdf

[12] Compendium voor de Leefomgeving. (2020, June 4). Temperatuurextremen in Nederland, 1907–2019. From https://www.clo.nl/indicatoren/nl0589-temperatuur-extremen

[13] D. D. Agwu, F. Opara, N. Chukwuchekwa, D. Dike, and L. O. Uzoechi, ”Review Of Comparative Battery Energy Storage Systems (Bess) For Energy Storage Applications In Tropical Enviroments,” IEEE 3rd International Conference on Electro-Technology for National Development (NIGERCON), 2017, pp. 1000–1005. from www.researchgate.net/publication/327966044

[14] Energus Power Solutions Ltd. (2018, July 30). User Manual Tiny BMS s516 – 30A / 150A / 750A. From https://faktor.de/out/media/TinyBMS_User_Manual.pdf

[15] Tesla (2022). Tesla Powerwall. From www.tesla.com/powerwall

[16] Texas Instruments. (n.d.). Designing Planar Magnetics. From https://www.ti.com/download/trng/docs/seminar/Topic4LD.pdf

[17] Comparison of SiC MOSFET and Si IGBT. (2020, August 17). TOSHIBA. From https://toshiba.semicon-storage.com/info/docget.jsp?did=69799

[18] SIZE 500 Power Capacity 500W to 5kW. (n.d.). PAYTON PLANAR. From https://www.paytongroup.com/webfiles/files/6af8f070703006d72457a0278e6a8ccb.pdf

[19] Power Electronics - Switching Losses in a MOSFET. (2020, April 6). From https://www.youtube.com/watch?v=RViwOc4g-gw

[20] SiHG70N60AEF. (2017, August 21). VISHAY. From https://www.farnell.com/datasheets/2370019.pdf

[21] IRFP3206PbF. (n.d.). Infineon. From https://www.infineon.com/dgdl/irfp3206pbf.pdf?fileId=5546d462533600a401535628d64a1ff0

[22] Ramakrishnan, H., Kumar, N. N., Bhardwaj, M., Song, L. (2021, October). Bidirectional, Dual Active Bridge Reference Design for Level 3 Electric Vehicle Charging Stations. Verwijder. From https://www.ti.com/lit/ug/tidues0b/tidues0b.pdf

[23] M. Soleimanifard and A. Y. Varjani, ”A Bidirectional Buck-Boost Converter in Cascade with a Dual Active Bridge Converter to Increase the Maximum Input and Output Currents and Extend Zero Voltage Switching Range,” 2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), 2020, pp. 1-6, doi: 10.1109/PEDSTC49159.2020.9088491.