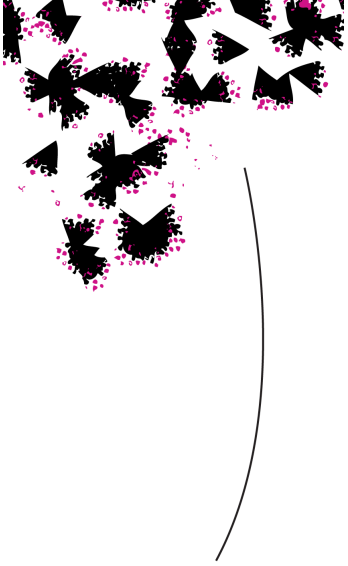

Optimization of a single-electron transistor for charge sensing

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Date:
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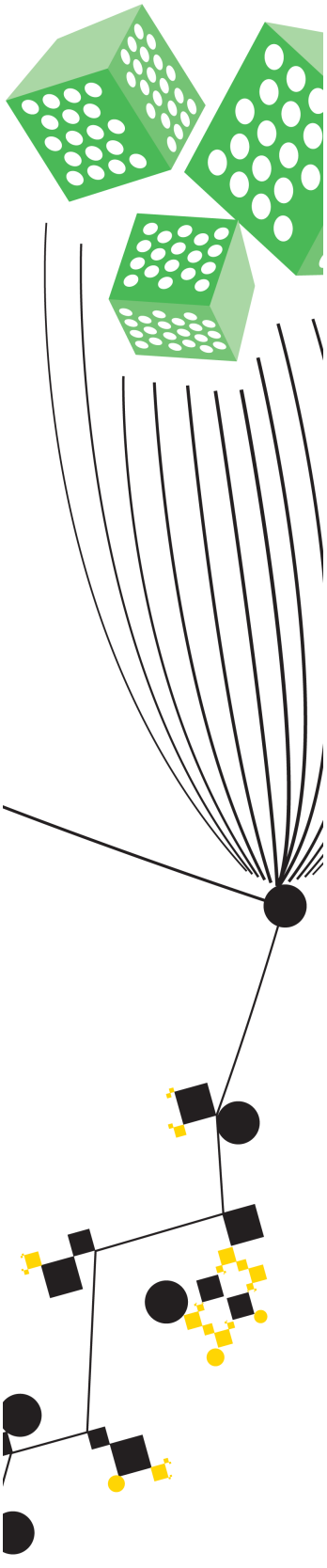

UNIVERSITY OF TWENTE.

Abstract

Quantum computers are a promising tool for computations of nanostructures and interactions between atoms. Quantum computers rely on qubits. Spin qubits are qubits that are based on the spin state of for instance an electron. The read-out of the spin state of these electrons can be done using single-electron transistors. These single-electron transistors can detect when an electron has tunneled from a donor atom, for instance bismuth. In this research, single-electron transistors are optimized for charge sensing. This is done by investigating the influence of various gate electrodes and the influence of the combination of bismuth implantation and Rapid Thermal Annealing. The source-drain voltage results in higher currents, but has no effect on the turn-on and pinch-off voltage. The plunger gate voltage shifts the turn-on voltage and the pinch-off voltages. The lead gate voltage can be used to make an intentional quantum dot more distinguishable from an unintentional quantum dot. Rapid thermal annealing did not have the intended influence, as charge traps were still present and even an offset was introduced in a device. The offset could be caused by an overlap between the implantation area and the SET. For future research, the implantation method needs to be adjusted so the implantation window is known not to lay beneath the architecture of the single-electron transistor. To get a better indication of the exact influence of rapid thermal annealing, I would recommend measuring more devices and measuring the electrical activation yield of the bismuth atoms before and after rapid thermal annealing.

Acknowledgements 1

When I started studying at the University of Twente, I never would have thought that I would be conducting my own research on the topic of quantum physics. I would like to show my gratitude to the people who made this possible.

First of all, I would like to thank my daily supervisor Antonio Sousa de Almeida for helping me during this project. Without him, the project would have been a lot tougher, since he knows his way through the lab as no one else does. I would also like to thank Floris Zwanenburg for giving me this opportunity to conduct my own small little research at the Nano-Electronics group. His insights and continuous search for extra things to do have motivated me to get as much out of this project as possible. I would also like to show my gratitude towards Rik Seelen, with whom I have worked intensely. I enjoyed this collaboration very much, as he was always available for quick questions. The chips that have been measured in this report were also fabricated by Rik. I wish to thank Amber Heskes as well, as she was always open to discussions and questions. She was open to helping me with practical issues at any time, which enabled me to get a lot more work done. My thanks go to Ray Hueting for accepting to be the external member. Last but not least, I wish to thank the whole Nano-Electronics group, I learned a lot about research in general. Such an active group with a lot of activities is an ideal group to be working in.

Contents

Introduction 2

Technologies developed by humans have always had the goal to make our lives easier or more fun. This description fits computers and their components. In order to make computers faster and more efficient, the size of transistors has been decreasing for decades. This is as predicted by Moore's law, which states that every two years, the amount of transistors on a dense integrated circuit multiplies by a factor of two [1]. However, the downscaling has come to a point where physical limits at room temperature are disturbing this trend [2]. Quantum effects were always present in these devices, but now they can be exploited to keep decreasing the size of transistors.

The prediction is that regular computers and laptops will remain the standard option for daily usage for the upcoming decades. However, the focus of large organizations is now on quantum computers as well, since the potential of these quantum computers is outstanding. Quantum computers make calculations based on probabilities, potentially making it possible to make calculations where a lot of probabilities are involved [3]. It is predicted that quantum computers will be able to solve complex computations like simulations of nanostructures [4]. Instead of classical bits, such quantum computers use quantum bits. Quantum bits, or qubits in short, are crucial in the working of a quantum computer and can be regarded as analogous to classical bits. They can be based on a couple of techniques. One that is investigated heavily is a qubit based on spin states. In order to be able to control and read-out the spin states, quantum dots can be used since they have discrete energy levels [5]. There are several ways to form these quantum dots [6]. In this report, the focus is on gate-induced quantum dots in silicon. These devices can also be called single-electron transistors if the gates are configured correctly. Single-electron transistors can be used to make a read-out of the spin states [7]. However, before a single-electron is able to do so, the device should be able to do charge sensing. Charge sensing is the process where the tunneling of an electron is detected.

2.1 | Aims of the research

In this research, the goal is to optimize single-electron transistors for charge sensing. The influence of different gate voltages is investigated, as well as the effect of the combination of bismuth implantation and rapid thermal annealing on the characteristics of the single-electron transistor. The focus is on the influence of the combination of bismuth implantation and rapid thermal annealing.

2.2 | Outline

This report starts with section 3, which is about the theory necessary to understand the characteristics of the single-electron transistor. Topics like the Coulomb blockade, stability diagrams, and defects are treated. After a general theoretical part, section 4 treats the design that is used in this research. Important characteristics are highlighted and discussed. Section 5 covers the measurement set-up used and the systematic approach used to measure the devices. The results are displayed and discussed in section 6. The conclusion of the research conducted is given in section 7. Finally, section 8 makes note of follow-up research and future improvements.

Theory 3

3.1 | Quantum Computing

Quantum computing is based on quantum bits. In these quantum bits, there are states that are analogous to a 1 or a 0 in classical bits. That means that when measured, there are two possible states of the quantum bit. Quantum bits that use spin-up and spin-down as states are called spin qubits. When the spin state is measured, there is a chance that the electron has spin-up and a chance that the electron has spin-down. When the spin state is not measured, the electron is in a state that is a combination of both spin-up and spin-down. In classical computation, this would mean that a bit is both a 0 and 1 at the same time, something that is not possible in classical bits. This principle is called superposition. This can be put in an equation like equation 1 [8]

$$|\Psi\rangle = \alpha|1\rangle + \beta|0\rangle \tag{1}$$

where:

$$1 = |\alpha|^2 + |\beta|^2 \tag{2}$$

Here, the states 1 and 0 can be appointed to spin-up and spin-down, and α and β are the chances that the qubit is in either state 1 or 0, respectively. Ψ is the wavefunction of the electron inside the qubit. When multiple quantum bits are combined, the amount of states increases exponentially as there are 2^N states, where N is the number of qubits. Notice that quantum bits and qubits mean the same thing. This exponentially increasing amount of states combined with the superposition principle is where a quantum computer has the advantage over classical computers. In one computation, a quantum computer could potentially calculate all outcomes for each bit sequence whereas a classical computer needs to calculate the answer for each bit sequence one by one. For longer bit sequences, this saves time exponentially. [8]

3.2 | Quantum Dots

Quantum dots are "man-made structures in a solid, typically with sizes ranging from nanometres to a few microns"[6]. They consist of between thousands and billions of atoms and a number of electrons in the same order. In silicon, these electrons are all but a few bound to the nuclei of the silicon atoms [9]. These few free electrons are the interesting ones and can range from a single electron to hundreds of electrons. When these electrons are confined, there are different terms based on their confinement. If the free electrons can move freely in 2 dimensions it is called a quantum well, if they can move freely in 1 dimension and is confined in two dimensions, it is called a quantum wire. When the electron is confined in three dimensions we speak of a quantum dot[10].

The three-dimensional confinement of the electrons results in a quantized energy spectrum, when the size of the quantum dot is close to the deBroglie wavelength of these electrons [9]. This quantized energy spectrum is the reason that quantum dots are also referred to as *artificial atoms*. If we limit ourselves to quantum dots created between the source and the drain (see figure 1), measurements of the electrical transport between

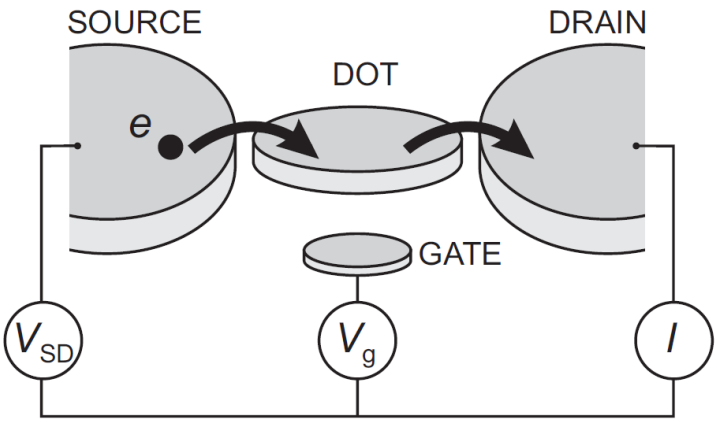

Figure 1: Schematic of a quantum dot in lateral geometry [11]

these two electrodes can be performed. By tuning the gate voltage, we can set the exact amount of electrons present in the quantum dot. With this, artificial atoms and their characteristics can be simulated and measured. Current-voltage measurements give insight to observe the behaviour of these artificial atoms and their atom-like behaviour. [6]

We have limited ourselves to a quantum dot that is created between the source and drain. The quantum dot is capacitively coupled to the drain, source and to the gate. This configuration can be seen in figure 1. If high-potential barriers are created between the quantum dot and the source/drain, tunnel rates between the source/drain and the quantum dot are low. In that case, there is a distinguishable amount of electrons present in the quantum dot(N). In this case, a current can only flow when electrons tunnel one by one from the source to the drain. Therefore, the number of electrons in the quantum dot can differ by one at a time. When one electron has tunneled to the dot, Coulomb repulsion between electrons increases the required energy needed for another electron to tunnel to the dot significantly [6]. At low temperatures, an electron is unable to gain this extra amount of energy unless the voltage is increased and this extra energy is provided. This principle is called *Coulomb blockade* and is the reason for electrons tunneling one by one. The amount of energy needed for an extra electron to tunnel to the dot is called the addition energy E_{add}. [6]

3.3 | Constant Interaction Model

The constant interaction model (figure 2) can be used to describe the energy levels in a quantum dot. It helps to understand the basic principles of a quantum dot. First of all, it assumes that the Coulomb interaction between electrons is independent of the number of electrons N. Secondly, the Coulomb interactions of an electron on the dot with all other electrons (both inside and outside the dot) can be modeled with a single capacitance C. [6]

Using the assumptions made, the total capacitance can be described by $C = C_g + C_s + C_d$. The total energy of the dot then can be described by the sum of the energy due to classical confinement and energy due to quantum-confinement, depending on the number

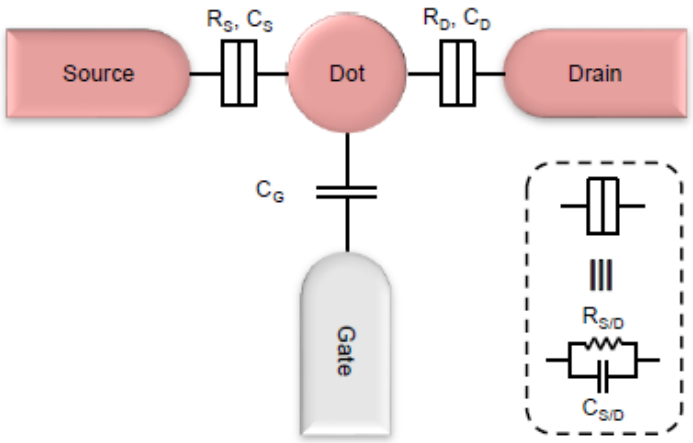

Figure 2: Depiction of the assumptions made in the Constant Interaction Model [7]

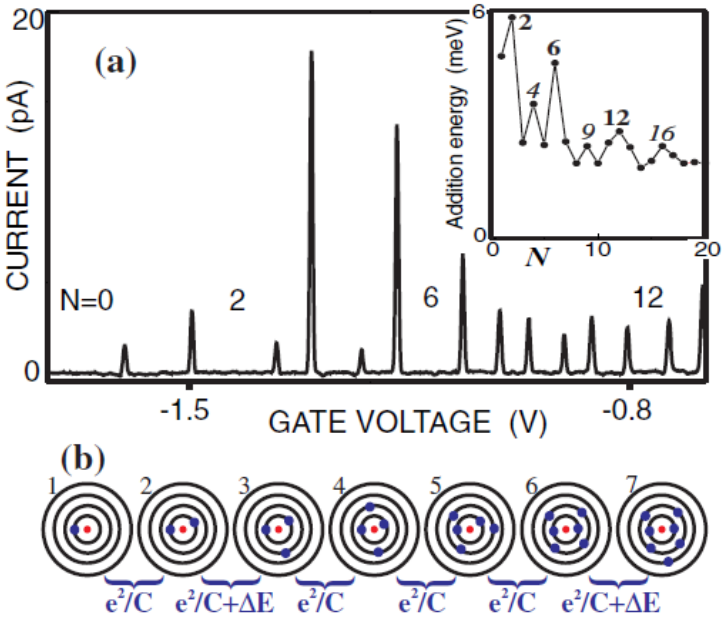

Figure 3: (a) The distance between the peaks is related to the addition energies. There is no current flowing between the peaks, this is called Coulomb blockade. (b) the addition energy varies based on the amount of electrons present in the quantum dot [6]

of electrons on the dot (N) [6]:

$$U(N) = \frac{(|e|(N - N_0) - C_g V_g)^2}{2C} + \sum_{n=1}^{N} E_{n,l}(B) \tag{3}$$

Here, $N = N_0$ when $V_g = 0$ and it is assumed that $V_s \approx V_d \approx 0$ [6][12]. The electrochemical potential of the dot is defined as $\mu_{dot}(N) = U(N) - U(N-1)$, so this is given by

$$\mu_{dot}(N) = (N - N_0 - 1/2)E_C - e(C_g/C)V_g + E_N \tag{4}$$

The addition energy then is defined as $\Delta\mu(N) = \mu_{dot}(N+1) - \mu_{dot}(N)$, so filling this in gives

$$E_{add} = \Delta\mu(N) = U(N+1) - 2U(N) + U(N-1) = E_C + E_{N+1} - E_N = e^2/C + \Delta E \tag{5}$$

In the constant interaction model, the addition energy consists of two parts, as can be seen in equation 5. The first part is the charging energy, which is constant and due to the Coulomb interactions between the electrons and is given by $E_C = e^2/C$. The second part is due to the energy difference between neighbouring quantum states and this is characterized as ΔE. This can be seen in figure 3b. The addition energy varies based on the number of electrons present on the quantum dot. When the electron is added to the same spin-degenerate level, ΔE can be zero. This can be seen in figure 3.[6] [7]

The charging energy E_C should be larger than the thermal energy $k_B T$ to avoid multiple electrons being able to tunnel to the dot at the same time. Also, the charging energy should be larger than the tunnel coupling $h\Gamma$ as this results from the Heisenberg uncertainty principle $dEdt = (e^2/C)RC > h$ as $\Gamma^{-1} = RC$ [13]. This can be summarized by $E_C > k_B T, h\Gamma$. Here k_B is the Boltzmann constant, T the temperature, h the Planck constant, and Γ the tunneling rate. [13]

3.4 | Transport through the quantum dot

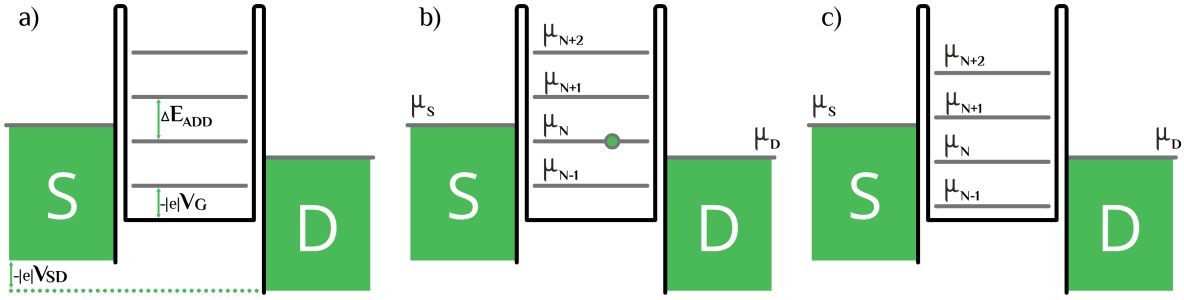

Figure 4: Single-Electron Transistor potential landscape. (a) shows important characteristics(V_{SD}, E_{add} and V_G) and their influence. (b) shows the configuration where conduction is possible, since $\mu_S > \mu_N > \mu_D$. (c) shows the configuration where no conduction is possible(Coulomb blockade), since $\mu_S, \mu_D > \mu_N$ and $\mu_S, \mu_D < \mu_{N+1}$

In figure 4, the potential landscape of a single-electron transistor is depicted, with the electrochemical potential μ on the y-axis and position on the x-axis. The potential landscape is based on the constant interaction model. In figure 4a, the addition energy and the influence of the gate voltage are shown. The addition energy is given by equation 5. Usually, for larger dots, it holds that $E_C >> \Delta E$ and thus that the distance between the electrochemical potentials μ_N and μ_{N+1} is approximately the same [7]. When the gate voltage is varied, these energy levels shift up and down. A more positive gate voltage means that the potential levels go up, and a less positive gate voltage means that the potential levels go down. An important characteristic of electrons is that they can tunnel to a lower potential if available. Only if the electrochemical potential of a certain amount of electrons μ_N lies between the potential of the source and drain ($\mu_S > \mu_N > \mu_D$), current can flow. This situation can be seen in figure 4b. Here, $e|V_{SD}| = \mu_S - \mu_D$. [14] When the electrochemical potential of the current amount of electrons does not lie between the potentials of the source and drain($\mu_S, \mu_D > \mu_N$ or $\mu_S, \mu_D < \mu_N$), electrons cannot tunnel from the source to the quantum dot and then to the drain without gaining or losing energy. This situation can be seen in figure 4c. This is the case when there is Coulomb blockade. [7][12]

All this can be measured by varying the gate voltage and measuring the current or conductance between the source and drain. This result in figures like figure 5a. The width and height of these peaks depend on multiple factors. The temperature has a huge influence on this figure. When the thermal energy of the electrons is high enough, tunnel rates increase as the electrons can shortly gain more energy and go to a potential level higher than the potential level of the source. If then the gap between the potential of the source and for instance μ_{N+1} in figure 4c is small enough, current can flow from source to drain. That is why the thermal energy and thus the temperature needs to be sufficiently small. The peaks visible in 5a are called Coulomb peaks. They happen in-between regions of Coulomb blockade. [12]

3.5 | MOSFET Analogy

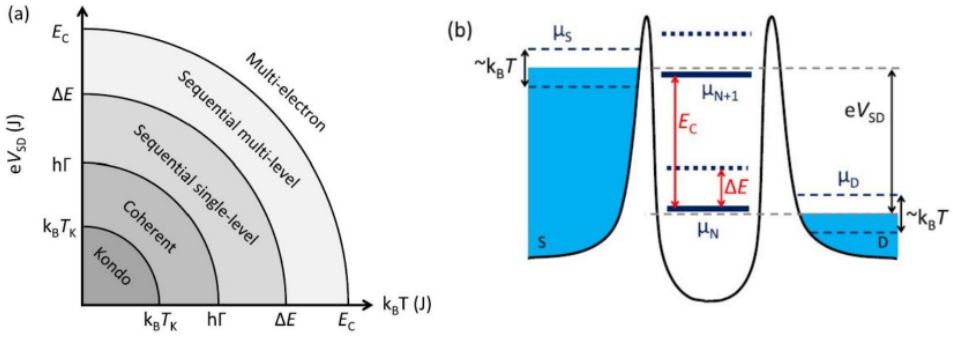

Figure 5: Transport regimes and important characteristics in a three-terminal quantum device. (a) shows five different transport regimes as a function of the external energy scales k_BT and V_{SD}. (b) shows the potential landscape of the three-terminal quantum device [15]

In figure 5a, five transport regions are defined, where eV_{SD} and k_BT influence the transport region. They are the external energy scales and should be compared to the internal energy scales. The internal energy scales are the Kondo temperature T_k, the level broadening $h\Gamma$, the level spacing ΔE and the charging energy E_C. The total tunnel rate to the localized state Γ consists of the tunneling rate to the source Γ_S and the tunneling rate to the drain Γ_D, which can also be put as $\Gamma = \Gamma_S + \Gamma_D$. Usually, it holds that $T_K \ll h\Gamma \ll \Delta E \ll E_C$. Note that the transition between two transport regimes is not as abrupt as figure 5a suggests. The external energy scales, ΔE and E_C are depicted in figure 5b. As both external energy scales have a similar effect on the transport characteristics, it is not necessary to distinguish between these scales when comparing them to the internal energy scales. [15] [16]

A single-electron transistor operates in the sequential single-level regime, while a MOSFET operates in the multi-electron regime. In figure 6a, a schematic cross-section of a MOSFET-based quantum dot device is depicted. The oxide(SiO_2) separates the intrinsic silicon from the metal gates. A positive voltage is applied to the lead gate. This attracts electrons to the Si/SiO_2-interface and also creates a two-dimensional electron gas (2DEG). What happens, is that the positive voltage pulls the conduction band below the Fermi level. This means that electrons can flow from the source to the drain through this gas. The difference between a single-electron transistor is that for the SET, a quantum

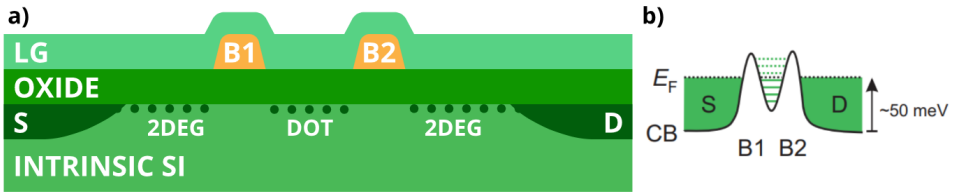

Figure 6: Formation of a quantum dot using a MOSFET-based architecture.(a) shows a schematic cross-section of a quantum dot device based on a MOSFET. (b) shows the electrochemical potential landscape [17]

dot is formed in the middle when a voltage is applied to the barrier gates (B1 and B2). The barrier gate voltage deplete the 2DEG locally, as can be seen in figure 6a and figure 6b. In figure 6b, it can also be seen that the conduction band is higher than the Fermi level, confining electrons between these barrier gates. This creates a quantum dot and the electrochemical potential landscape can be seen in figure 6b. For a MOSFET, there is no quantum dot formed and the gate voltage only controls whether the 2DEG connects the source with the drain or not. Another method to create a quantum dot with the same architecture is by applying a negative voltage on the lead gate. This in turn pulls the valence band above the Fermi level, which creates a two-dimensional hole gas (2DHG). [17]

3.6 | Turn-on & pinch-off voltage

The *turn-on voltage* is defined as the voltage where a two-dimensional electron gas (2DEG) is formed [18]. The turn-on voltage is used as the first step to seeing if a fabricated device works and if a quantum dot can be formed. All gates are swept from 0 to 3 V when a small (a few millivolts) V_{SD} is applied, and the current from source to drain is measured (I_{SD}). Somewhere between 1 and 2V, the current increases like in figure 7 if a 2DEG is successfully created. The exact turn-on voltage can vary due to for example charge traps at the Si/SiO_2-interface and the thickness of the SiO_2 layer.

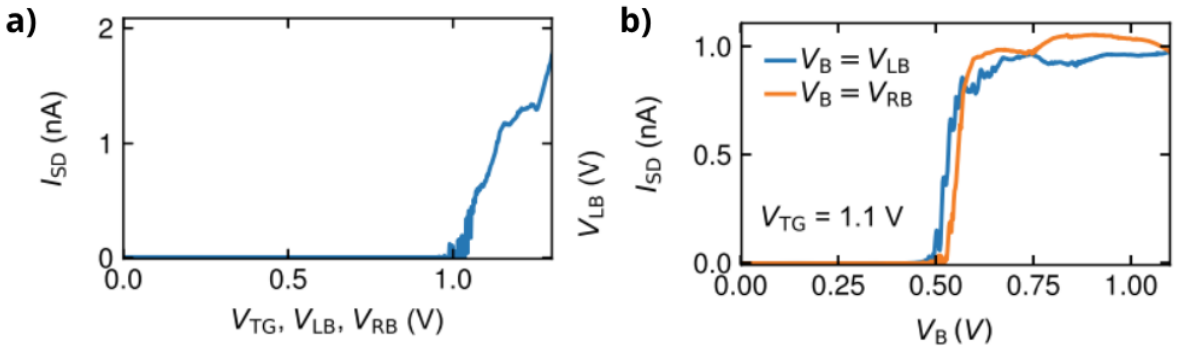

Figure 7: Turn-on & pinch-off voltage (a) Turn-on around 1.0 V (b) Pinch-off around 0.55 V for both barrier gates. [18]

The second step is to see if each barrier is able to deplete the 2DEG. This can be done by keeping all but one barrier gate at a constant voltage. This voltage should be higher than the previously determined turn-on voltage. This one voltage is swept from 0 to 3 V again. The highest voltage where I_{SD} is suppressed is called the *pinch-off voltage*. Physically,

at this voltage the 2DEG is depleted below the barrier gate that is swept. [18]

This also makes it possible to detect defects. For instance, non-ideal behaviour could be a plateau below the pinch-off voltage or peaks in the current (instead of a smooth transition from low to high current). A plateau could indicate that there is another current path between the source and drain, other than the quantum dot.

When the device is configured in such a way that both barrier gate potentials are close to their pinch-off voltages, a 2DEG is formed between the barrier gates that is not connected to the source and drain leads. In figure 6a, it can be seen that in this case, the 2DEG between the barrier gates does not touch the 2DEG at the source or the 2DEG at the drain. When either barrier gate voltage is changed, oscillations in current can be seen.[18]

3.7 | Charge Stability Diagrams

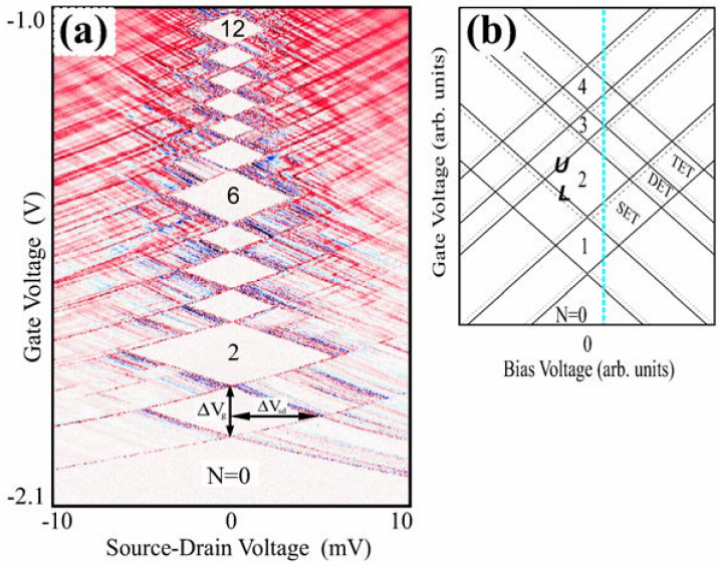

Figure 8: Stability diagram. [6]

Coulomb peaks occur when the gate voltages are swept while the source-drain voltage is kept constant. Examples of Coulomb peaks can be seen in figure 3a and figure 10b. Here, electrons can flow when the electrochemical potential of the gate is spaced between the electrochemical potentials of the source and drain. If this is not the case, this is called Coulomb blockade and no electrons flow from source to drain or vice versa. Such a figure can be obtained when one measures along the blue line in figure 8b. Next to sweeping the gate voltage, sweeping the source-drain voltage can also lift the Coulomb blockade [14]. When the source-drain voltage is varied as well, Coulomb diamonds occur. A figure where two voltages are swept independently from each other and where the conductance or current is measured is called a (charge) stability diagram. An example of this can be seen in figure 8a. Inside these diamonds, no current flows and the quantum dot is in Coulomb blockade. On the edges of the diamond, current can flow. Here, the electrochemical potentials of the source and quantum dot are equal. [5] From these stability diagrams, a lot of information on the quantum dot can be derived. For instance, every diamond belongs to a certain amount of electrons (N). For every diamond, this

number is different ($N + 1$, $N + 2$, etc.). These numbers are also indicated in figure 8. At $N = 0$, no diamond can be seen as one side is open. The diamond next to this has $N = 1$ and the diamond next to that has $N = 2$, etc. This way, one is able to address the exact amount of electrons to a diamond. [6]

There are also characteristics of the quantum dot that can be derived from a stability diagram. For instance, the addition energy can be derived by measuring the width of the diamond. This can be seen in figure 8a and in figure 9. The operation regime at certain voltages can also be derived, as indicated in figures 8 and 9. Here, DET stands for Double-Electron Tunneling and TET stands for Triple-Electron Tunneling. In these operation regimes, there are two and three electrochemical potential levels at the dot between source and drain, respectively. Also, the relative capacitance can be derived, and thus the location of the quantum dot can be derived as well since the location is directly linked to the relative capacitances. These relations between the stability diagram characteristics and the values of the capacitances are indicated in figure 9. [19]

Even though the model described here can be used to understand the basic principles like how quantization of charge and electrons leads to Coulomb blockade and Coulomb oscillations, some things are not considered. First of all, co-tunneling is not taken into account. This happens when the tunneling rate between the dot and source or drain is increased. Then, higher order (higher than first-order) tunneling processes become important. Next to this, the spins of electrons are not taken into account, which for instance excludes exchange effects between electrons with the same spin. [14]

When the values of the capacitances are derived, one can also calculate the theoretical size of the quantum dot. Since we have assumed the quantum dot to be a disk, we can calculate the radius of the quantum dot as follows [20]:

$$C = 8\varepsilon_0\varepsilon_r r \tag{6}$$

where ε_0 is the permitivity of a vacuum, ε_r is the relative permitivity of silicon and r is the radius of the quantum dot.

In the stability diagrams like figure 8 and 9, the source-drain voltage is on the x-axis and the gate voltages are on the y-axis. Stability diagrams where two gate voltages are varied independently from each other also offer insight in the characteristics of the quantum dot. When an intentional quantum dot is measured and no defects or unintended quantum dots are present, such a stability diagram could look like the one in figure 10a [18]. When a line cut is made across the green line in figure 10a, figure 10b emerges. Clear Coulomb peaks can be seen at lower voltages. In figure 10a, the diagonal lines can be referred to as Coulomb oscillations and they mean that the single-electron transistor has been formed successfully. The slope of these Coulomb oscillations corresponds to the ratio of the lever arms[18]. If V_{B1} is on the y-axis and V_{B2} is on the x-axis, the slope is equal to the ratio $\frac{\Delta V_{B1}}{\Delta V_{B2}} = \frac{C_{B1}}{C_{B2}}$, where C_{B1} and C_{B2} are the capacitive couplings between the SET island and B1 and B2, respectively.

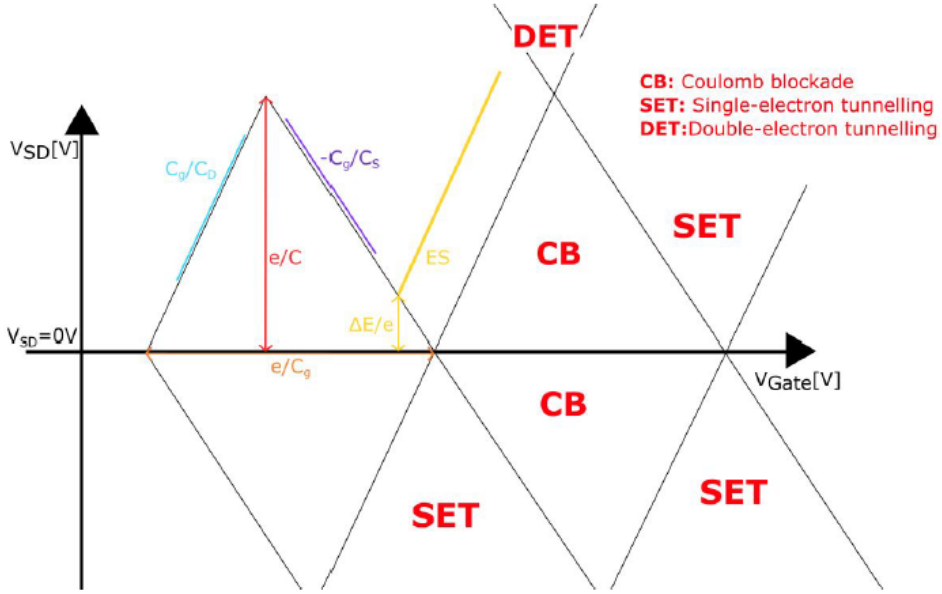

Figure 9: Stability diagram where an indication of characteristics of the quantum dot is present. [19]

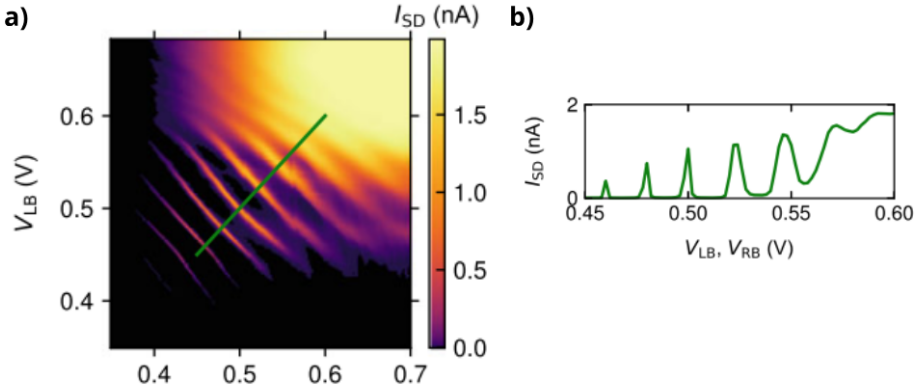

Figure 10: Stability diagram of two barrier gates (a) Stability diagram without unintentional quantum dots or defects present at the voltage window used. (b) Line cut across the green line in (a). [18]

3.8 | Charge Sensing

Charge sensing comes down to measuring the charge state of a donor atom. In the devices used in this research, the donor atoms are bismuth-atoms and the charge state of these atoms could either be ionized(D^+) or neutral(D^0)[18]. The implantation window is the area where the bismuth atoms are implemented. If the bismuth atoms are electrically activated, there is one free electron per bismuth atom. The consequence is that there are more free electrons in this area compared to its surroundings. It is possible that an electron tunnels to an ionized donor atom or an empty charge trap near the SET island. After an electron has tunneled to an ionized donor atom, the donor atom is not ionized anymore and becomes neutral. This donor atom or charge trap can be regarded as a second quantum dot that is capacitively coupled to the SET island. When an electron tunnels to this quantum dot, the electrochemical potential of the SET island changes since there is a coupling between the two quantum dots and since the donor atom is no

longer ionized. This can be seen in figure 11b. The electrochemical potential levels of the SET shift like a change in gate voltage would do (even though the capacitive coupling is lower). Since now the electrochemical potential of the gate is changed, the conduction of the source to drain is also changed. If this new electrochemical potential of the gate again lies between the potential of the source and drain, current can flow. If not, no current flows between the source and drain. [18]

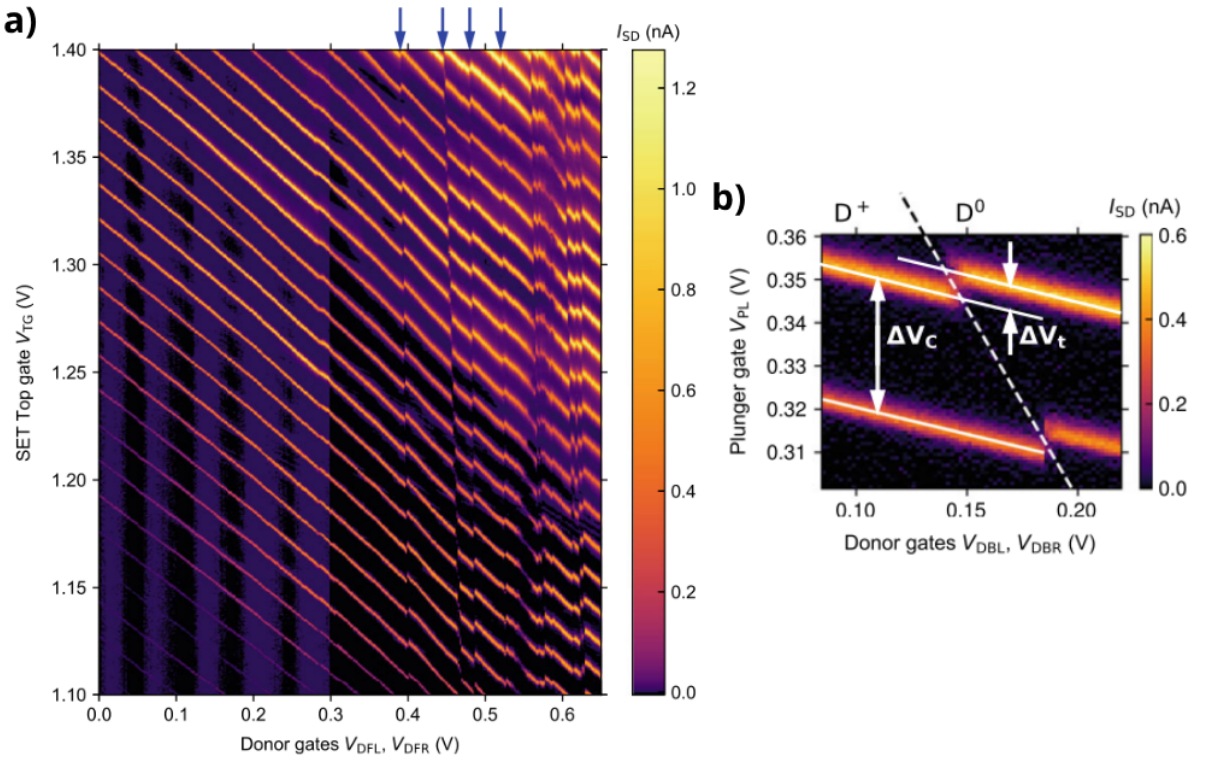

Figure 11: Charge stability diagrams (a) Charge stability diagram where charge transitions are indicated with blue arrows. (b) Characteristics of a charge transition. [18]

Potential donors can be detected with stability diagrams where a barrier that is strongly coupled to the SET is swept, like the lead gates, and where a gate is varied that strongly influences the electrochemical potential of the donor atoms, like the donor gates [7][18]. An example of such a charge stability diagram can be seen in figure 11a. From these charge stability diagrams, one can determine the increase in electrochemical potential of the SET's island due to an electron tunneling to a donor atom or charge trap with equation 7 [18].

$$\Delta\mu(N) = E_C \frac{C_m}{C_d} \tag{7}$$

where E_C is the charging energy, C_m is the mutual capacitance between the donor atoms and the SET island and C_d is the total capacitance of the donor, where C_m is included ($C_m/C_d \leq 1$). The ratio C_m/C_d is equal to the ratio $\Delta V_t/\Delta V_C$ where V_t is the Coulomb peak shift due and V_C is the difference in potential between two Coulomb peaks, as depicted in figure 11b. Note that in figure 11a, the top gate is varied while in figure 11b, the plunger gate is varied. Using the charge stability diagram, the SET can be tuned to the Coulomb peak at the side of the charge transition where the donor is ionized to

detect charges tunneling. This detection is the easiest when the Coulomb peak shift is large. This peak shift depends on the ratio C_m/C_d and thus on the location of the donor atom. [5][18]

3.8.1 Spin-dependency

If a magnetic field is applied, the electrochemical potential of the electrons in the electron reservoir is split into the potential of an electron with spin-up and the one of an electron with spin-down. Then, the sensing of spin can be done if the electrochemical potential of the SET-island(μ_2) lies between these two potentials of the spins ($\mu_{1\uparrow}$ and $\mu_{1\downarrow}$), since now only electrons with spin-up can tunnel to the SET-island. This is depicted in figure 12. This is the basic working principle of spin detection and more research has been conducted on this topic. Pla *et. al.* elaborate more on this topic. [7][21][22]

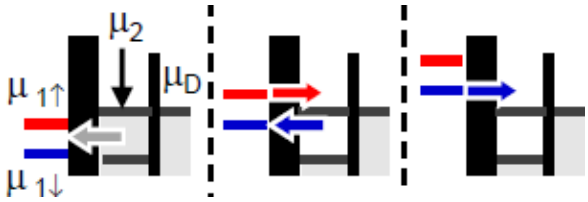

Figure 12: Spin-dependent tunneling. [7]

3.9 | Defects

There are multiple causes for defects. These can be divided into three categories. The first category consists of the material properties used in the device. The second category is about the interfaces between different materials. The third category consists of the defects caused by morphology. Even though all these categories are interesting, this is a study on its own and for instance done by Paul-Christiaan Spruijtenburg [13]. Here, I treat three causes that are relevant for analyzing the behaviour of the devices used in the measurements in this report.

3.9.1 Defects on the Si/$SiOS_2$ interface

At this interface, the crystalline structure of silicon is disrupted. This interface has been studied before, as it also is of interest for MOSFET studies. There are multiple types of defects at this interface and they are separated based on their distance to the interface. This distinction can be seen in figure 13b. P_b-centers occur at the interface and E'-centers are named border traps or oxide traps. Firstly, P_b-centers can be described as a silicon atom at the interface which has a dangling bond. A dangling bond is an unsatisfied valence on an atom that cannot move. There are two types of P_b-centers, as can be seen in figure 13. The first type is P_{b0}-center. This center is bonded to two silicon atoms and one oxygen atom. The P_{b1}-center is bonded to three silicon atoms. [13]

Defects can be categorized based on multiple characteristics. One of those methods is to characterize by charge state. For a defect with three possible charge states, the charge states are the positive D^+, neutral D^0, and negative D^-. At a certain electrochemical potential, the energies of the positively charged defect and neutral defect are equal. This

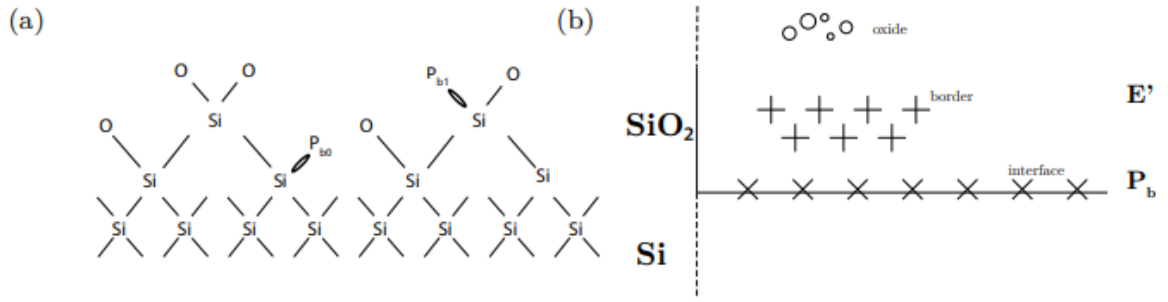

Figure 13: Multiple types of defects at the Si/SiO2-interface. (a) shows the types of P_b-centers. (b) shows the defects distinguished based on the distance to the Si/$SiOS_2$ interface. [13]

level is called the transition level $\mu(+,0)$. When $\mu < \mu(+,0)$, the defect is positively charged in the ground state, and when $\mu > \mu(+,0)$, the defect is neutral in the ground state. Something similar also happens at the interface between the neutral and negative charged defects and this is the transition level $\mu(0,-)$. Now for silicon, the transition levels $\mu(+,0)$ and $\mu(0,-)$ are located at 0.25 eV and 0.85 eV above the valence band maximum, respectively. If the positive charge states approach the valence-band maximum (VBM), this state can be regarded as a donor-like state. For a negative charge state a similar principle is true, as a negative charge state can be interpreted as an acceptor-like state if the state is close to the conduction-state minimum (CBM) [13]. Defects with this kind of behaviour are called *amphoteric* and such behaviour can be seen in figure 14. In figure 14b, the system is positively charged since the Fermi level has the effect that the charge state that behaves like a donor is half-filled. D_{it} is the density of these transition levels [13]. Depending on the annealing bias, the transition level density varies as can be seen in figure 15. This indicates that there are fewer P_b-defects after annealing.

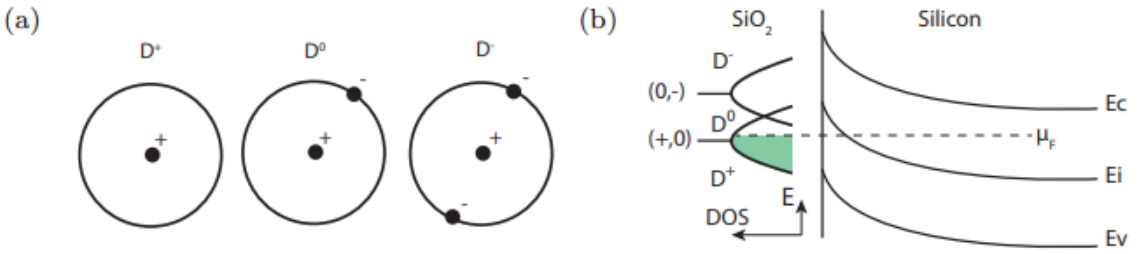

Figure 14: P_b-center defects (a) shows the three charge states. (b) shows the P_b-center charge state distribution depending on the Fermi level. [13]

3.9.2 Defects due to strain

The coefficient of thermal expansion (CTE) of silicon and aluminium are different, $2.6 \cdot 10^{-6}K^{-1}$ and $23 \cdot 10^{-6}K^{-1}$ respectively. Since the electrodes are made of aluminium and these electrodes are touching the SiO_2-interface, there is a local mismatch in CTE. Such a mismatch will cause strain when the device is cooled down and can setup strains in the order of 0.6% when the temperature is changed by 300 K. Since no device is solely made of silicon and electrodes usually are made of metals, the interface between silicon

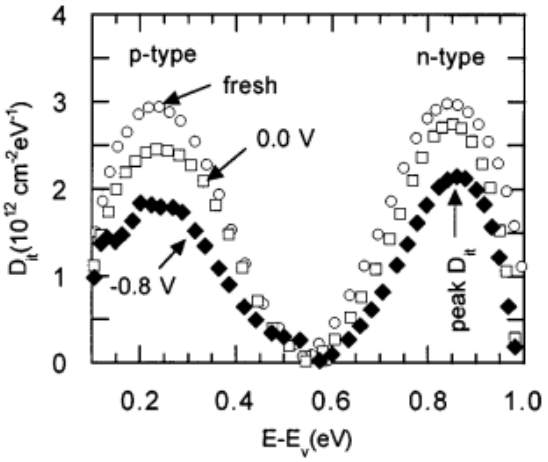

Figure 15: Density of transition levels versus potential. The density is also shown as a function of the bias voltage during annealing. [23]

and metal will always be there. Metals usually have a higher CTE and thus will contract more than silicon when the temperature is lowered. This can be seen in figure 16. The combination of stresses and strains that are induced by this difference in CTE causes a difference in the conduction band, as can be seen by the red line in figure 16. As discussed in the section about quantum dots, an unintentional dot can be formed when an electron can be trapped between the peaks. That happens when the barrier height is larger than the thermal energy and larger than the charging energy. [24]

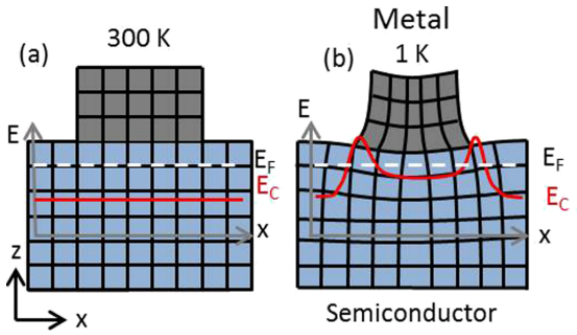

Figure 16: The effect of strain on the electrochemical potential, where E_C is the energy of the conduction band. [24]

3.9.3 Defects due to bismuth-implantation

There are several advantages of using bismuth donors, as the bismuth donor has a large Hilbert space, clock transitions, and also has the potential to couple to superconducting flux qubits due to its large zero-field splitting [25]. However, bismuth atoms have a high atomic mass and there is a large mismatch in covalent radii [26]. When the atoms impact, the crystalline structure of the silicon is distorted heavily. This causes the electrical activation yield to drop. This means that dangling bonds are formed, as the bismuth atoms do not fit in the silicon lattice perfectly. These bismuth atoms that have dangling bonds are not electrically activated and thus do not donate an electron to the conduction band. Rapid Thermal Annealing can repair this damage partially. [26]

3.10 | Rapid Thermal Annealing

Rapid Thermal Annealing (RTA) is the process where a silicon sample is baked at temperatures up to 1000 degrees Celsius for a short time. This short time can be up to 300 seconds. Rapid thermal annealing has the goal of electrically activating bismuth atoms in the implantation area. Rapid thermal annealing can result in electrical activation yields of up to 64% for high fluences and 46% for low fluences for ion implantation of $25keV$ Bi[25]. Electrical activation of a donor means that this donor now has one electron which it can donate to the conduction band. Thus, the electrical activation of more bismuth atoms results in more free electrons. This in turn increases the chance that the electrons from the implantation area can tunnel to a nearby unintentional quantum dot or charge trap. Thus the chance that the tunneling of an electron can be sensed using charge sensing is increased.

The defects due to bismuth implantation are the defects that are targeted to be solved with RTA. However, when diffusion is not limited enough, the uncertainty in donor placement increases [25]. Rapid thermal annealing can also induce leakage currents. When the Bismuth atoms are electrically activated, more electrons are present in the implantation window and the implantation area gets more conductive. [27]

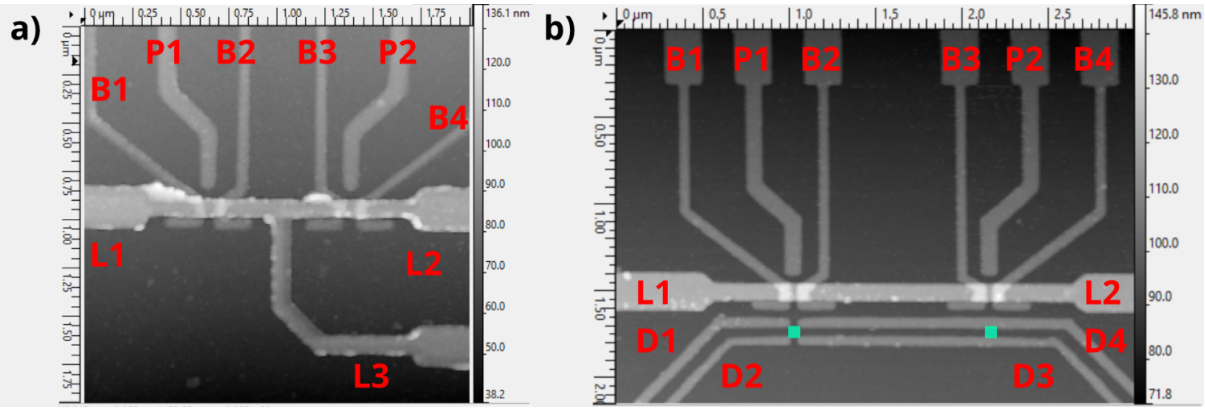

Figure 17: AFM images of two separate devices. (a) shows device GH (not processed by RTA). (b) shows device VC (bismuth implanted and processed by RTA). The green squares indicate the implantation area.

In figure 17 one can see that the devices are on the scale of micrometers in the x- and y-direction and in the order of nanometers in the z-direction. These AFM images were taken by Rik Seelen. In figure 17, the architectures of the devices GH and VC can be seen, as well as the placement of the implantation window in device VC. Rapid Thermal Annealing was part of the fabrication process of device VC, but not of device GH. There are also some minor other changes in device architecture between these two devices. In figure 17a, an extra lead gate L3 can be seen. Below this lead gate, an extra electrode is also present. This made it possible to individually test the left quantum dot and the right quantum dot, as it is now possible to create a current path through one SET at a time. This is beneficial when there was a defect in either of the SET's. Such examples can be seen in the appendix (figure 30). In figure 17b, there are also dopant gates present. These were not used but could have been used to control the number of electrons coming from the dopant. They can also be used to make charge stability diagrams. For the left quantum dot, this amount could be tuned more sensitively as there are four dopant gates that influence the rate of charges tunneling close to the left quantum dot. For the right quantum dot, only two gates are able to influence the rate of charges that tunnel close to it. [18]

The devices are fabricated on top of the implantation area. This is due to the inaccuracy of the fabrication set-up used. This is done to make sure that electrons from this implantation window can tunnel to the quantum dot. Rapid thermal annealing electrically activates the Bismuth atoms, resulting in more electrically active Bismuth atoms near the single-electron transistor in the devices that have been processed by RTA (RTA'd devices).

Measurement Set-up 5

The characterization of single-electron transistors is a large part of this project. Therefore, it is important to write down how this is done. Using a step-by-step plan, this characterization is done in a systematic manner.

5.1 | Optical inspection

The first step is to inspect the devices visually. This is done by looking at the chip through a microscope and by looking at individual devices using an Atomic Force Microscope (AFM). Figures like figure 17 are taken using AFM. In the appendix, figures can be found of faulty devices. Using this inspection method, a first selection of devices is made. Using a regular microscope, the bond pads are also checked for damage and if they are even on the chip.

5.2 | Wirebonding

On the chips, several bonding pads are present per device (one for each electrode). These need to be connected to the PCB, since only the PCB can be connected to the dipping stick that goes in liquid helium. This can be seen in figure 18a. The method to connect the device with the PCB is called wire bonding. Here, an aluminium wire is connected to the bond pads of the PCB and device using the wire bonding device depicted in figure 18b.

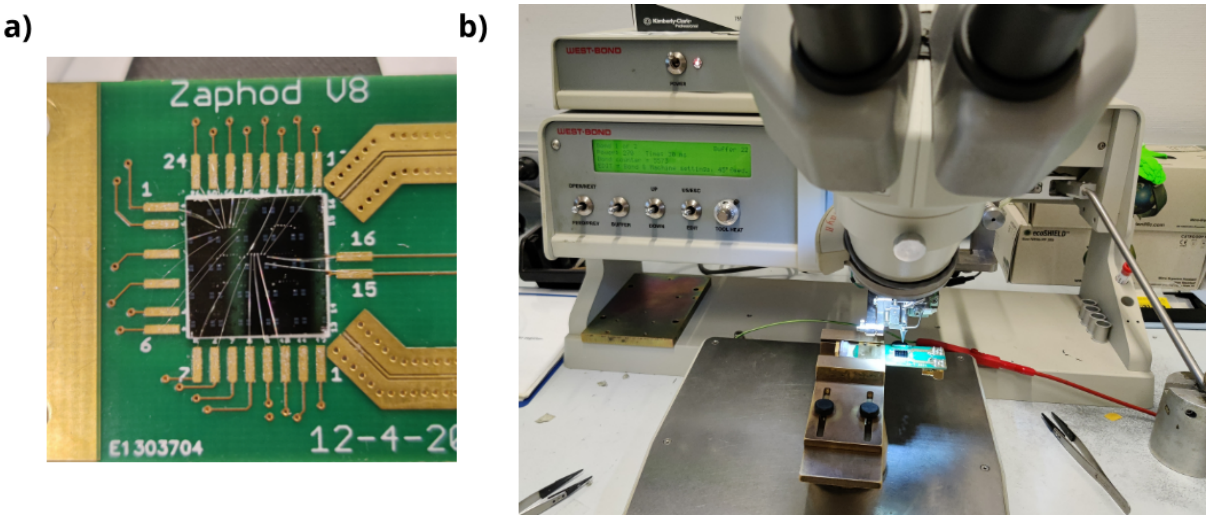

Figure 18: Wirebonding set-up and its result (a) shows the chip where two devices are wirebonded to the PCB. (b) shows the wirebonding device and a microscope

5.3 | Leakage tests

Now that the PCB is connected to the device, the PCB can be connected to the measurement system that allows measurements at 4.2 K. This measurement system is depicted in figure 19, 29 and 28. Its main parts are an isolated barrel filled with liquid helium, the Matrix Module (MM), the IV-VI rack, and a dipping stick. The PCB is connected to the matrix module via the dipping stick. The dipping stick is constructed in such a way that the PCB and chip are protected when entering the liquid helium. If the chip is cooled down, leakage tests can be performed by using a device called the BEEP-R. This device measures the resistance of an electrode. One electrode is measured while all others are grounded, and the resistance between that one electrode and the ground is measured. If this resistance is very high, there is no conduction path between this electrode and other electrodes. If there is a resistance that is not close to infinity, one needs to find out to what electrode there is leakage. When there is a conduction path between two electrodes that is not supposed to be there, this could be due to multiple causes. For instance, two wires used to connect the PCB with the device could touch, shorting two electrodes. Another reason could be that the temperature is too high or that there is a conduction path via the implantation area between two gates. In our case, there should only be a path between the lead gates as they are the only electrodes that are connected by an aluminium piece.

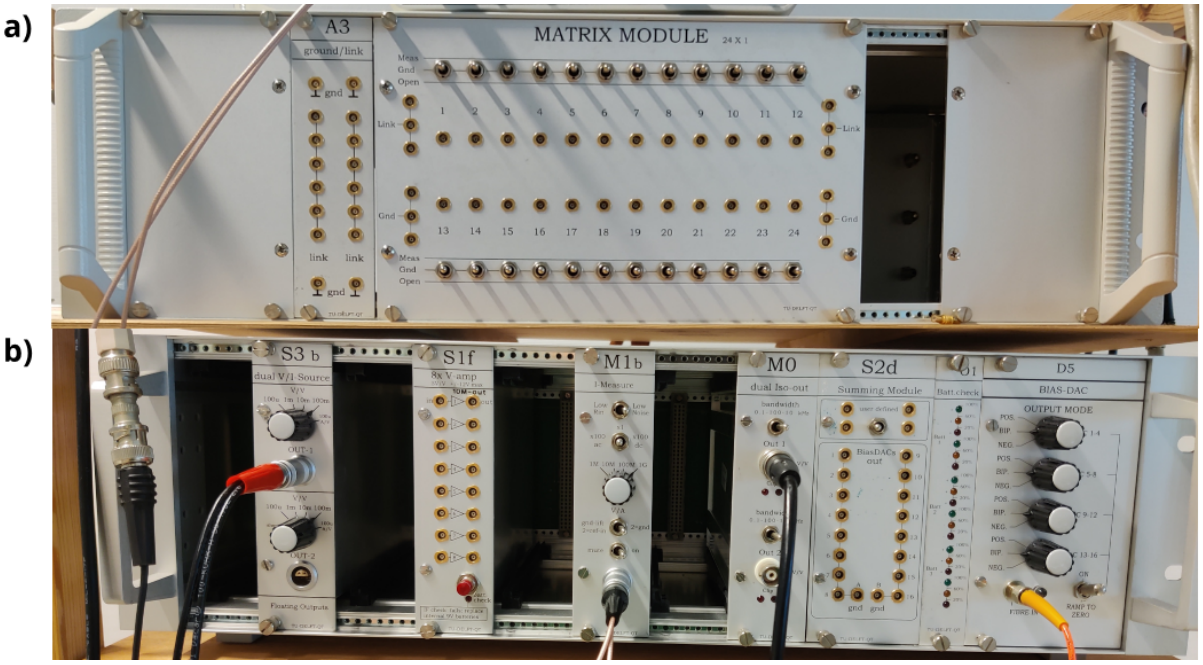

Figure 19: (a) shows the Matrix Module. (b) shows the IV-VI rack.

5.4 | Turn-on & pinch-off

After the leakage test, the dipped device needs to be connected to the computer. This is done via the MM and the IV-VI rack. The gates of the MM that correspond to the correct gates are connected with the IV-VI rack. A 5x times amplifier is used, as the DACs of the IV-VI rack have a range of -2V to 2V. This enables us to set negative voltages on certain gates while sweeping another gate from 0 to 3V. For measuring the turn-on voltage and pinch-off voltages, this is not yet necessary. The barrier, plunger and lead gates are swept from 0 to 3V, while a small (0.5mV or 1mV) bias voltage is applied to the source and drain. Using this test, one can filter out some devices that are not able to form a quantum dot between the barrier gates that can be used for charge sensing.

5.5 | Stability Diagrams

The next step is to make stability diagrams to get an insight into the characteristics of the quantum dot formed. It is still possible that a quantum dot is not successfully formed, or one is formed that is coupled to a certain gate very heavily. Coulomb oscillations (diagonal lines) like the ones in figure 10 indicate that a quantum dot has been successfully formed between the barrier gates. The angle of the Coulomb oscillations is around 45 degrees, indicating that the formed quantum dot is evenly coupled to both barrier gates. If these Coulomb oscillations are visible, one can make Coulomb diamonds to determine the charging energy.

Results & Discussion 6

This section describes the results of the measurements that have been done. In total, devices from three different chips were measured and tested using the measurement method described in the previous section. To understand the behaviour of the devices, the influence of the gate electrodes is investigated. Next to this, devices that could create a quantum dot are compared and evaluated. Thirdly, the performance of all devices is evaluated.

6.1 | Influence of electrodes

In order to understand the behaviour of the quantum dots, it is crucial to understand the influence of each electrode. It is better to measure than to calculated this influence, as theory is different from reality. Therefore, an analysis of the influence of each gate electrode is given in this section.

6.1.1 Influence source-drain voltage

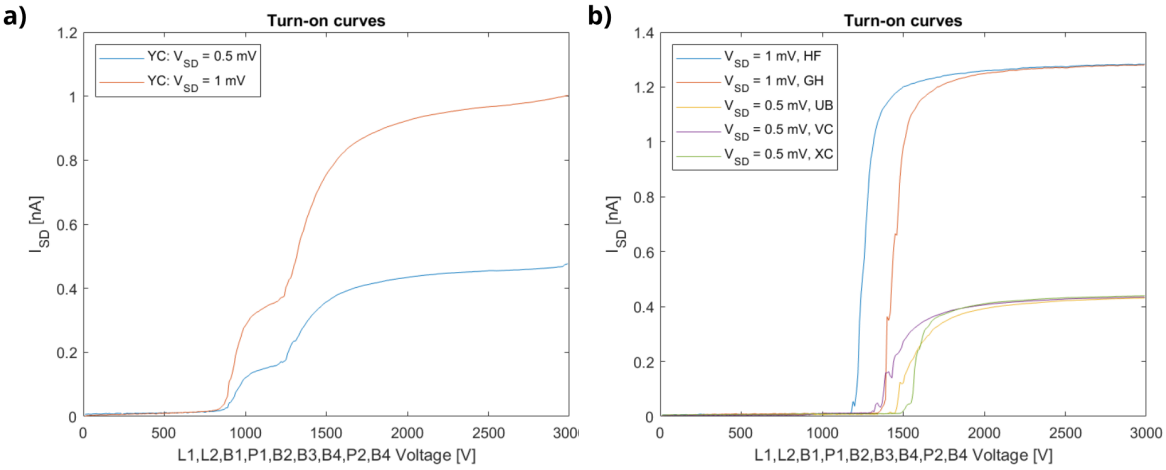

Figure 20: Turn-on voltage of devices XC,HF and YC

Device HF and are GH not RTA'd, but device XC,UB and YC are RTA'd. In figure 20a, the influence of the bias voltage between the source and drain is plotted. Overall, the current is greater for a higher bias voltage, approximately twice as large (but not exact). The main characteristics like the turn-on voltage seem unaffected. In figure 20b, multiple turn-on curves are plotted, for both RTA'd devices and non-RTA'd devices. For both RTA'd devices and non-RTA'd devices the turn-on voltage vary around 200 mV. The current in non-RTA'd devices is approximately three times as large as the current in RTA'd devices at a large gate voltage. In figure 21, the influence of the source-drain voltage on the pinch-off curve of device YC can be seen. In this device, there was a current path next to the current path through the intentional quantum dot. It can be seen that for a higher source-drain voltage, this leakage current increases. In general it holds that for a higher source-drain voltage, the current increases (again with an approximate factor of 2). The pinch-off voltage does not change for barrier gate B1 of device YC when the source-drain voltage is changed.

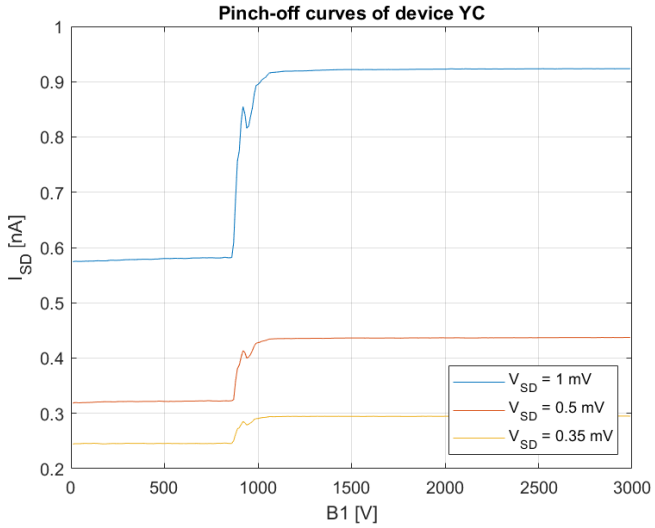

Figure 21: Pinch-off voltages of devices YC where the source-drain voltage is varied. The plunger gate voltage was equal to 0V and the lead gate voltages were equal to 2V ($V_{P1} = 0V$, $V_{L1} = V_{L2} = 2.0V$)

6.1.2 Influence plunger gate voltage

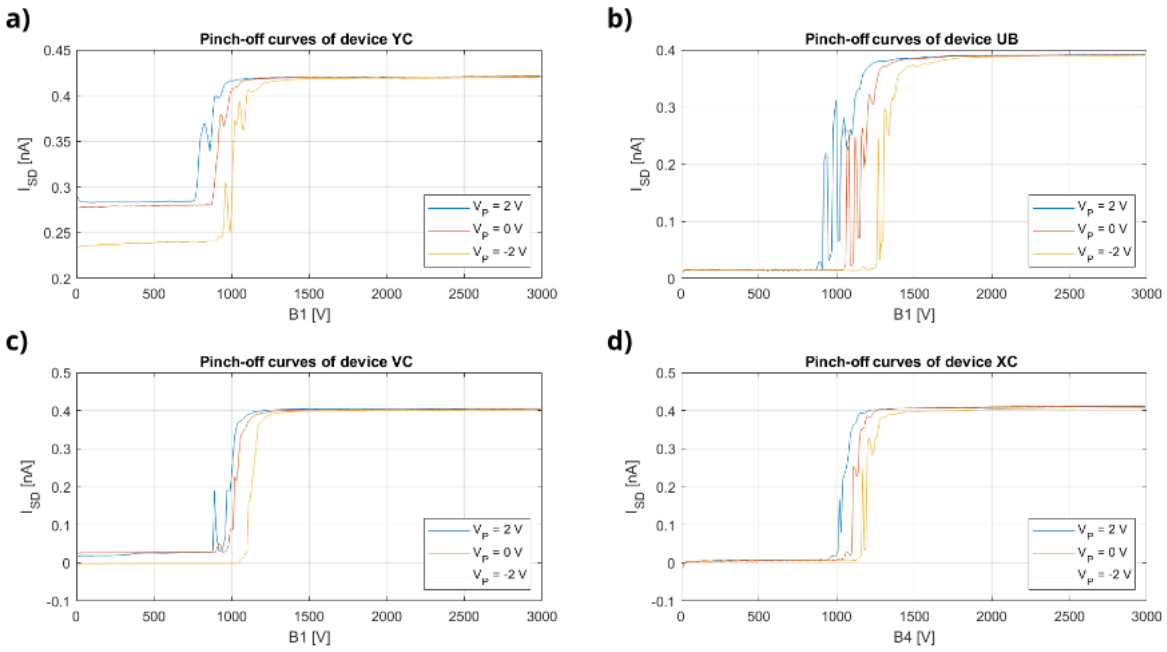

Figure 22: Pinch-off voltages of devices YC(a), UB(b), VC(c) and XC(d) where the plunger gate voltage is varied. The source-drain voltage was equal to 0.5mV and all other gate voltages were 2V.

In figure 22, the pinch-off curves of one barrier gate is plotted per subplot for different plunger gate voltages and of different devices. All other gate voltages were set to 2V. That means that when for instance the pinch-off curve of B1 is measured, $V_{L1} = V_{L2} = V_{B2} = V_{B3} = V_{P2} = V_{B4} = 2V$. Changing the plunger gate shifts the pinch-off curve across the x-axis. For a higher plunger gate voltage, the pinch-off voltage is lower. Also, a change

in plunger gate influences the smoothness of the pinch-off curve. This smoothness can be disturbed by sharp peaks, which could be caused by charge traps or dangling bonds [5]. This is visualized in figure 23. In figure 22c, a lower plunger gate voltage increases the smoothness of the curve, as there are less sharp peaks visible in the curve. This means that, at this plunger gate voltage, electrons have no other way to go from the source to the drain than via the quantum dot. However, in figure 22d, it does not hold that a lower plunger gate voltage means that there are less sharp peaks. This suggests that the smoothness of the pinch-off curves depends on the location of the charge traps and can be tuned by changing the plunger gate voltage. In figure 23, this can be thought of as the plunger gate voltage changing the electrochemical potential level of the area between the two peaks caused by the barrier gate voltage. Since the unintentional quantum dots are very small, only a few electrons can occupy it [19]. A change in the potential of the middle could rearrange the electrochemical potential levels inside the unintentional QD, resulting in this level changing from being between the electrochemical potential levels of the source and SET island to not being inbetween these levels. This change results in a change in current.

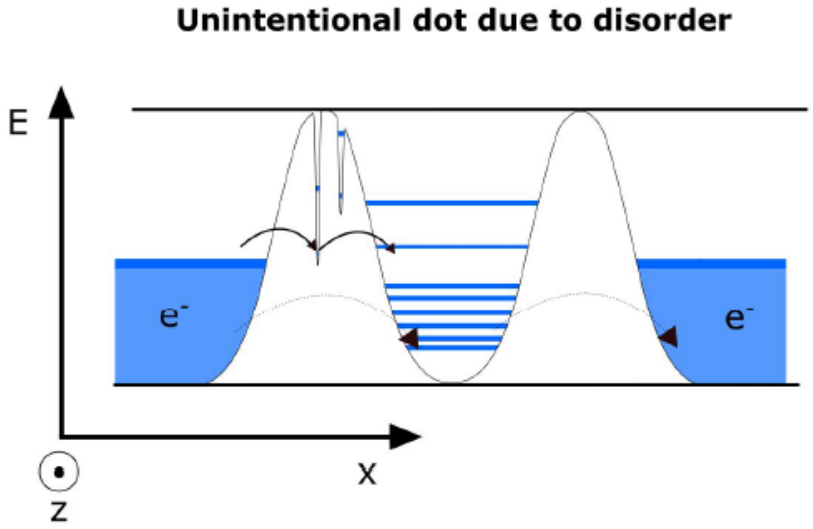

Figure 23: Charge traps create unintentional quantum dot under the barrier gate, disturbing the ideal electrochemical potential landscape [19]

6.1.3 Influence lead gate voltage

In figure 24 it can be seen that with a higher lead gate voltage, the intentional quantum dot is more highlighted and the unintentional quantum dot's influence becomes less, as the Coulomb oscillations are clearer. The repetitive vertical and horizontal lines suggest that there is a unintentional quantum dot. The consistency can best be seen in figure 24a. When the lead gate voltage is made more positive, more electrons are attracted to the lead gate. Since it can be seen that the current through the intentional QD (IQD) is increased with respect to the unintentional QD(UQD) when the lead gate voltage is increased, it could be the case that the electrons that flowed through the UQD, now flow through the IQD. That could be the case when the UQD is placed somewhere close to the IQD.

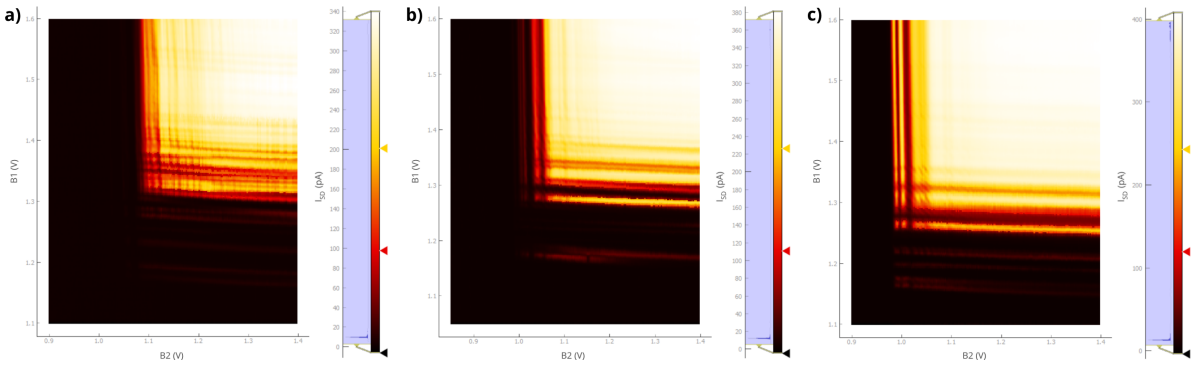

Figure 24: Stability plots of device UB where $V_{SD} = 0.5mV$ and $V_{P1} = -2V$. The barrier gate voltages B1 and B2 are varied, while $V_{B3} = V_{P2} = V_{B4} = 2V$(a) shows the stability diagram where $V_{L1} = V_{L2} = 1.8V$. (b) shows the stability diagram where $V_{L1} = V_{L2} = 2.0V$. (c) shows the stability diagram where $V_{L1} = V_{L2} = 2.2V$.

6.2 | Stability diagrams RTA vs non-RTA

Both devices in figure 25 are tuned so that the Coulomb oscillations are as distinguishable as possible. Here, figure 25a was measured by Rik Seelen. An offset is visible in figure 25b, as the black area corresponds to a current of around 300 pA. In both figures, defects can be spotted. In figure 25a, there is current flowing around $V_{B2} = 670$ mV, independently of V_{B1}. This indicates that there is a defect beneath the second barrier gate. This is non-ideal, but there are clear diagonal lines visible between $V_{B2} = 680$ mV and $V_{B2} = 710$ mV when V_{B1} >560 mV. This indicates that there is an intentional quantum dot formed. These lines have a slope of $\frac{\Delta V_{B1}}{\Delta V_{B2}} = -1.02$, corresponding to 45.58°. This means that the intentional quantum dot created in device FH is slightly more capacitively coupled to B1. In figure 25b, something similar happens. Here, a current flows around V_{B1}= 900 mV, this time independently of V_{B2}. This in turn indicates that there is a defect beneath the first barrier gate. There are clear diagonal lines visible between $V_{B1} = 930$ mV and $V_{B1} = 970$ mV when V_{B2} >1100 mV. These lines have a slope of $\frac{\Delta V_{B1}}{\Delta V_{B2}} = -0.82$, corresponding to 39.51°. This means that the intentional quantum dot created in device YC is more capacitively coupled to B2. Generating a line cut at the regions where Coulomb oscillations can be observed creates figure 26.

In figure 26 Coulomb peaks can be observed. When comparing figure 26a with 26b, it can be seen that in the left plot the maximum current is lower, but that for voltages below 520 mV the current is close to zero. The peaks are also more repetitive for device FH; the peaks have approximately the same peak height. For device YC, the peak height varies. Also, the relative change in current is higher at the peaks in 26a, as for a peak the current increases from 80 pA to 120 pA. In 26b, the current increases not only increases by just a maximum of 30 pA, this increase is also relatively smaller (from 340 pA to 370 pA). This makes device FH more sensitive to a change in voltage and thus more fit for charge sensing.

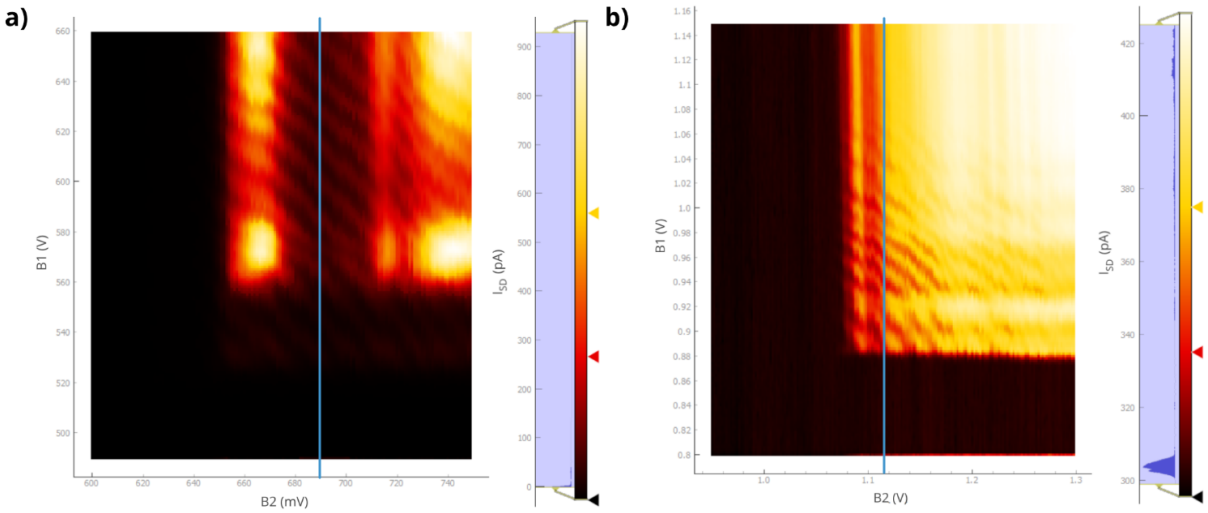

Figure 25: Stability plots where Coulomb oscillations are visible.(a) shows the stability diagram of device FH (not processed by RTA) where V_{SD} = 0.1 mV and V_{P1} = -1 V. (b) shows the stability diagram of device YC (processed by RTA) where V_{SD}= 0.5 mV and V_{P1}= 0 V. The barrier gate voltages V_{B1} and V_{B2} are varied, while $V_{B3} = V_{P2} = V_{B4}$ =2 V

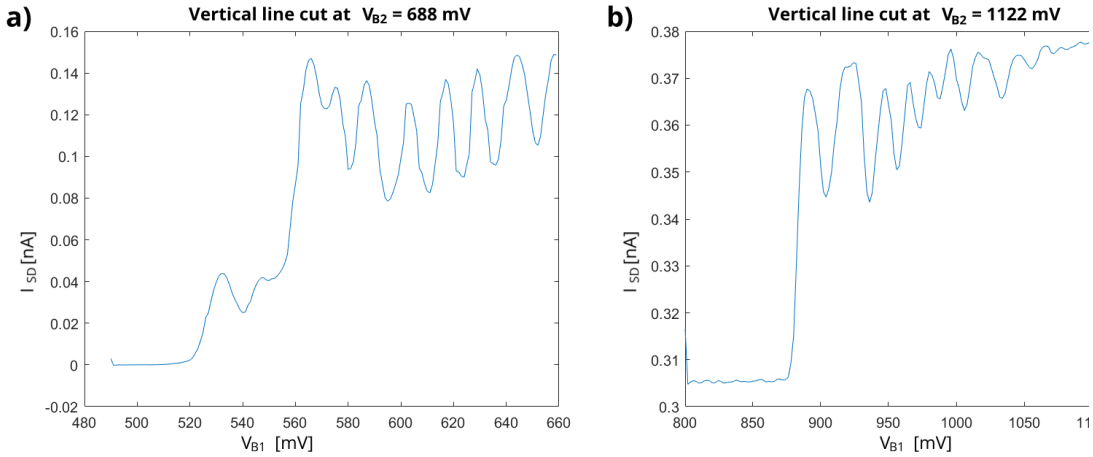

Figure 26: Line cuts of figure 25.(a) shows the line cut at V_{B2} = 688 mV in figure 25a.(b) shows the line cut at V_{B2} = 1122 mV in figure 25b

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6.3 | Device performances

In total, 35 devices have been measured. There were also AFM images taken of 8 more devices. These devices were not wire-bonded, as the AFM images taken indicated that it was unlikely that they would form quantum dots. These are devices GG,GJ,HH,HJ,HK,IH,IJ and JH and their AFM images can be seen in figure 30. Of these devices, GG and HH show some potential while they have not been measured. If all but these devices are taken in consideration, 41 devices have been measured. Of these devices, 6 devices showed quantum dot behaviour in their stability diagrams. 11 devices had no connection between the lead gates, 3 devices had leakage between the lead gate and a barrier gate, and 1 device had leakage between two barrier gates (B1 and B4). Another device had leakage between P1,P2,B3 and B4. This is mapped out and can be seen in figure 27.

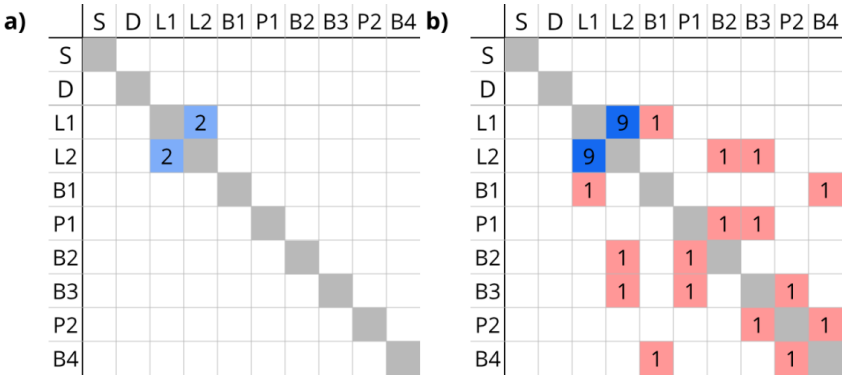

Figure 27: Leakage map where the amount of times a leakage occurs is indicated. Blue means that there is no connection where a connection is expected. Red means that there is a connection where a connection is not expected. (a) shows the leakage map of devices that are not bismuth implanted and not RTA'd.(b) shows the leakage map of devices that are bismuth implanted and RTA'd.

When comparing these figures, it should be noted that 5 non-RTA'd devices have been measured, while there are 30 RTA'd devices measured. Next to this, the devices depicted in 30 are not taken into account, since a leakage test is not done for these devices. With an optical inspection however, it is visible that some of these devices have no connection between the lead gates. In total, 13 devices did not pass the leakage test which means that 22 devices did not show leakage using the BEEP-R. Of these 22 devices, 6 were able to form a quantum dot and 16 devices were not able to do so.

In figure 31, the turn-on curves of devices MX and NY can be seen. All devices from chip KZ that passed the leakage test showed similar curves. All devices were not able to form a quantum dot and showed no sudden increase in current. During fabrication, there was a three week pause between the last steps. During this pause, interactions with the surroundings could have influenced the behaviour of the devices. 5 devices that could not form a quantum dot but had no leakage in the test with the BEEP-R are on the KZ-chip.

The turn-on curves and pinch-off curves of the other devices that passed the leakage test but were not able to form a quantum dot can be found in the appendix, in figure 32-39. Devices VA and YD (figure 32 and figure 39) have a very high current when the devices are turned on. In both devices, only one barrier gate was able to pinch off the 2DEG. Therefore, quantum dots could not be created by these devices. For device VB, the current was also in the order of 3 nA after turn-on and for this device, no barrier gate was measured that could deplete the 2DEG. Device VD has a current in the order of 80 pA after turn-on and the turn-on voltage is not well-defined. Both the turn-on and pinch-off curves have multiple steps. In device WA, multiple plateaus are present in the turn-on curve and all barrier gates have pinch-off curves similar to figure 35b.

Conclusion 7

In this research, the goal was to optimize single-electron transistors for charge sensing. The influence of gate voltages was investigated, as well as the effect of the combination of bismuth implantation and rapid thermal annealing. The theory suggests that rapid thermal annealing has potential to electrically activate more bismuth atoms and thus decrease the number of charge traps. The performance comparison of the RTA'd devices versus the non-RTA'd devices can be regarded as unreliable, as the sample size is not large enough. Not enough non-RTA'd devices have been measured. Since not enough devices have been measured, it is also impossible to draw hard conclusions regarding the direct influence of the combination of bismuth implantation and rapid thermal annealing. However, based on the data collected, some indications and notes can still be made. The data obtained in this report suggest that the sensitivity for charge sensing of the single-electron transistor is not greater when they are bismuth implanted and have been processed by rapid thermal annealing (RTA'd). The Coulomb peaks are relatively greater for non-RTA'd devices than for RTA'd devices (40 pA with respect to 120 pA compared to 30 pA with respect to 370 pA). This is due to the offset in the current of the RTA'd device. This current could be caused by the creation of a conduction path via electrically activation of bismuth atoms. Besides this phenomenon, there are still charge traps and dangling bonds that disturb the behaviour of the quantum dot. This can be seen as sharp peaks in figure 22 and as vertical and horizontal lines in figure 24. In all RTA'd devices that were able to form a quantum dot, there were also unintentional quantum dots present. The amount of influence that they have can be tuned, and thus the single-electron transistors can be tuned. However, the presence of unintentional quantum dots and charge traps suggests that the rapid thermal annealing procedure can still be tuned towards a higher electrical activation yield and thus potentially fewer charge traps.

For future research, I would recommend improving the Rapid Thermal Annealing process and evaluating that process. In this research, the implantation area was overlapping the area where the single-electron transistor was fabricated. A fabrication set-up that allows for more precise implantation can both prevent leakage currents that cause offsets and prevent charge traps due to non-electrically activated bismuth atoms disturbing the single-electron transistor behaviour. The electrical activation yield of the bismuth atoms of these devices has not been measured yet. Measurements of this activation yield can provide helpful insight into the process. Also, a greater sample size could help create even better insights into the influence of the electrodes. When a quantum dot is created where fewer defects are present, Coulomb diamonds can provide more insight into the characteristics of the quantum dot. Measurements of those diamonds were done for the non-RTA'd devices at temperatures below 1 K by Rik Seelen, but are not shown in this report since they are not processed yet. These measurements can also be done for the RTA'd devices that showed the formation of quantum dots, but were not done as the RTA'd devices that could form a quantum dot could not do so when they were measured a second time. This was due to electrostatic discharge or due to measuring the device while the battery used by the IV-VI rack was empty.

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Appendix 8

8.1 | Measurement devices

Figure 28: Barrel filled with helium where the dipstick is loaded

Figure 29: Close-up of the dipstick

8.2 | AFM Images

During the lift-off step of the fabrication process, there are things than can go wrong. For instance, if the metal electrodes are connected to the metal on top of the PMMA, the metal electrodes might also come off. This could explain why in figure 30a,b,d,e,f and j there are parts of the lead gate that are missing. The white areas are parts of the lead gate that are pointing upwards and these parts might be the missing lead gate. In figure

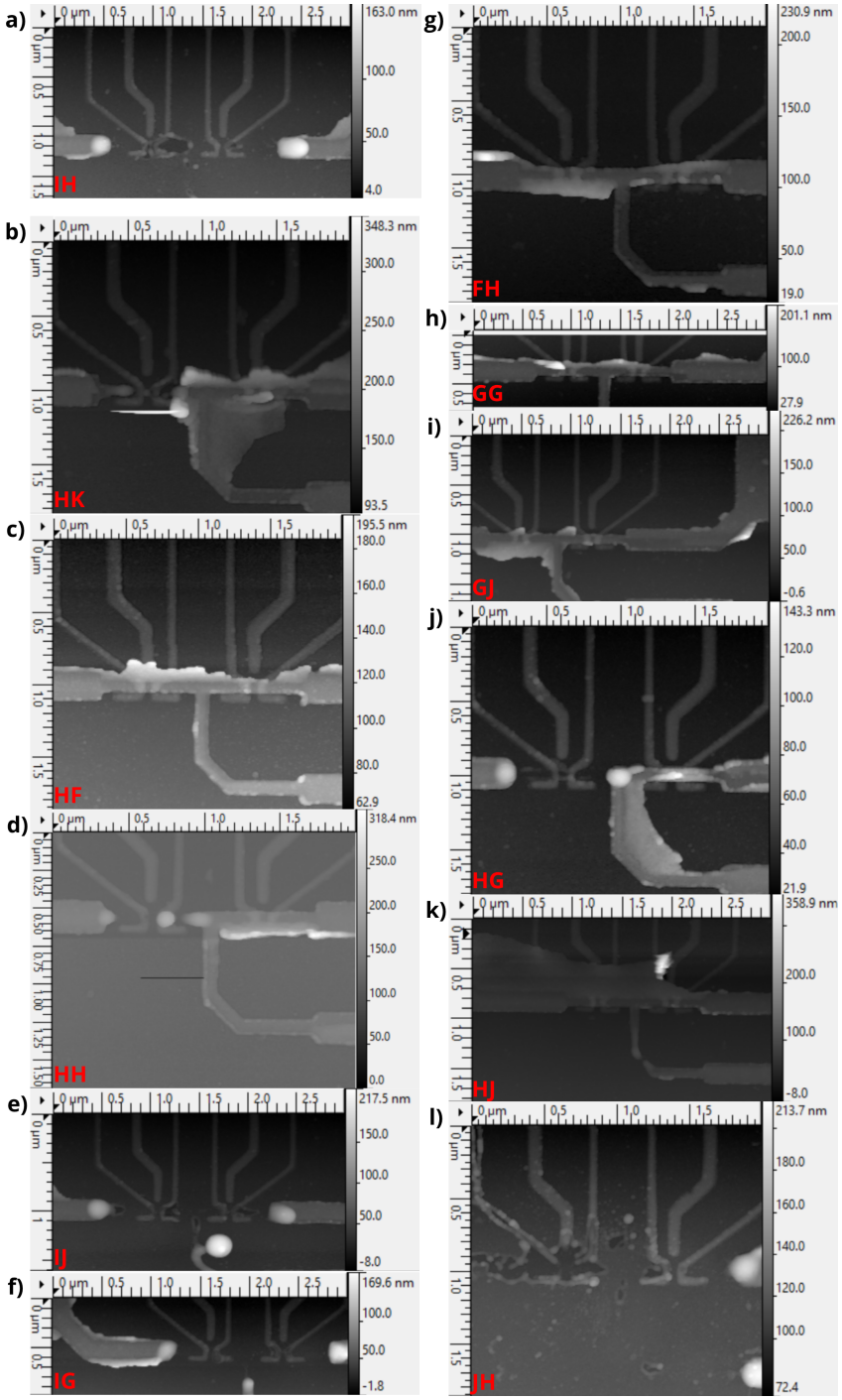

Figure 30: AFM images of devices on chip FK (non-RTA)

30l, some explosion has occurred. This could have happened due to a person not being grounded when touching the device. All these images are taken pre-annealing.

8.3 | Turn-on & Pinch-off curves

Figures 33,34,36,38 and 34 are measured by Rik Seelen.

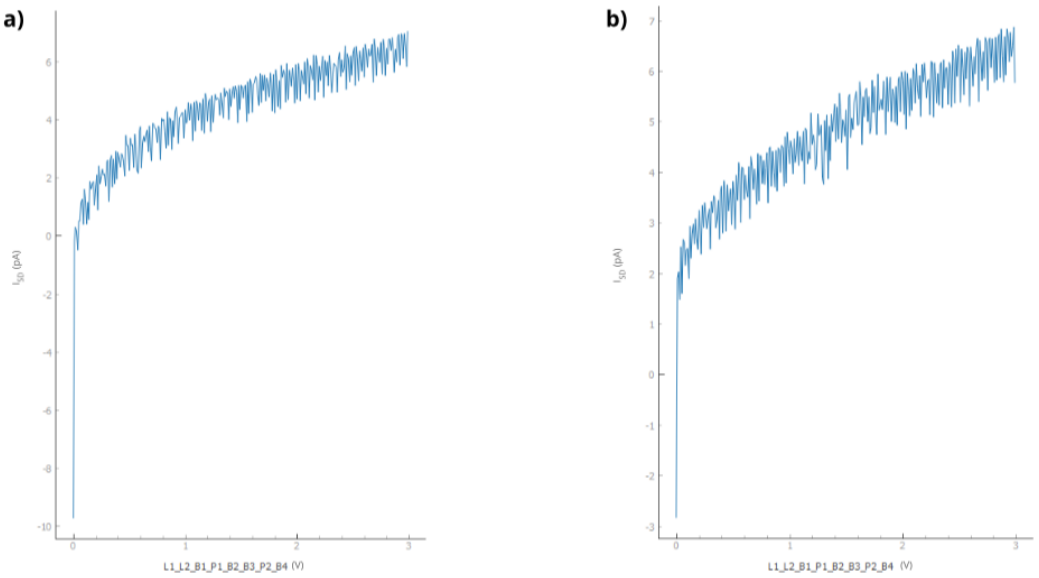

Figure 31: Turn-on curves. (a) shows the turn-on curve of MX (RTA'd). (b) shows the turn-on curve of NY (RTA'd).

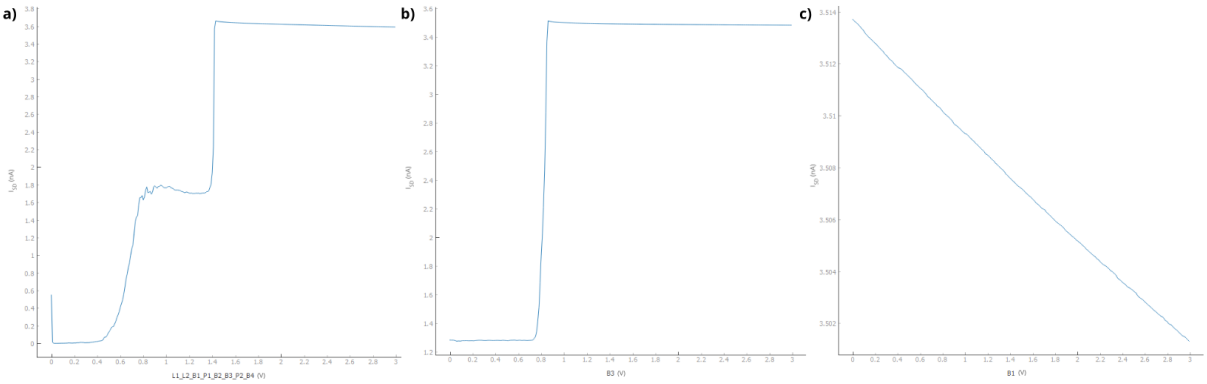

Figure 32: Turn-on curve and pinch-off curves of device VA (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2.

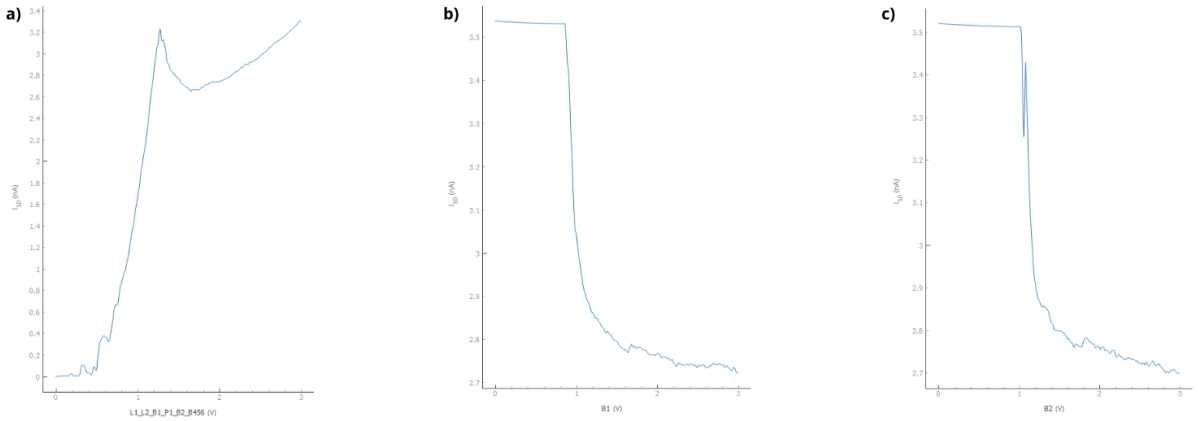

Figure 33: Turn-on curve and pinch-off curves of device VB (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2.

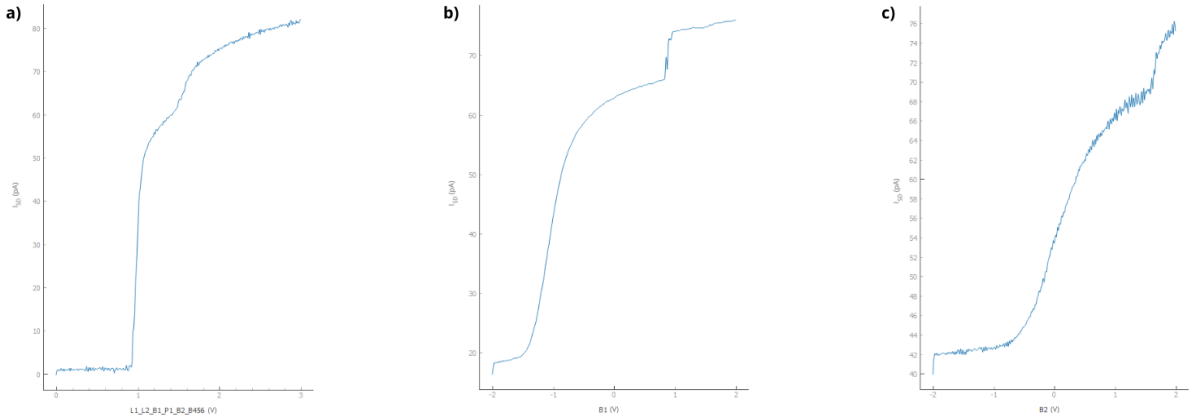

Figure 34: Turn-on curve and pinch-off curves of device VD (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2

8.4 | Process Flow Fabrication RTA

In the figures below, the fabrication method used for the RTA'd chips(KZ and UE) is depicted. This process flow is made by Rik Seelen, as the chips are also fabricated by Rik. Note that there are no bismuth atoms implanted.

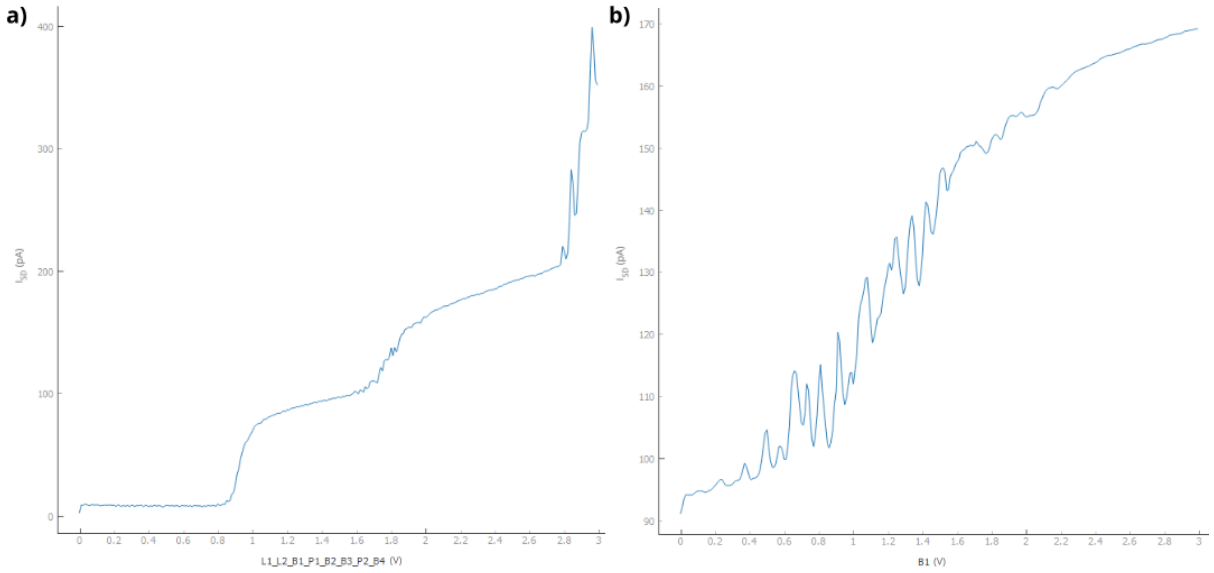

Figure 35: Turn-on curve and pinch-off curve of device WA (RTA'd). (a) shows the turn-on curve of B1.

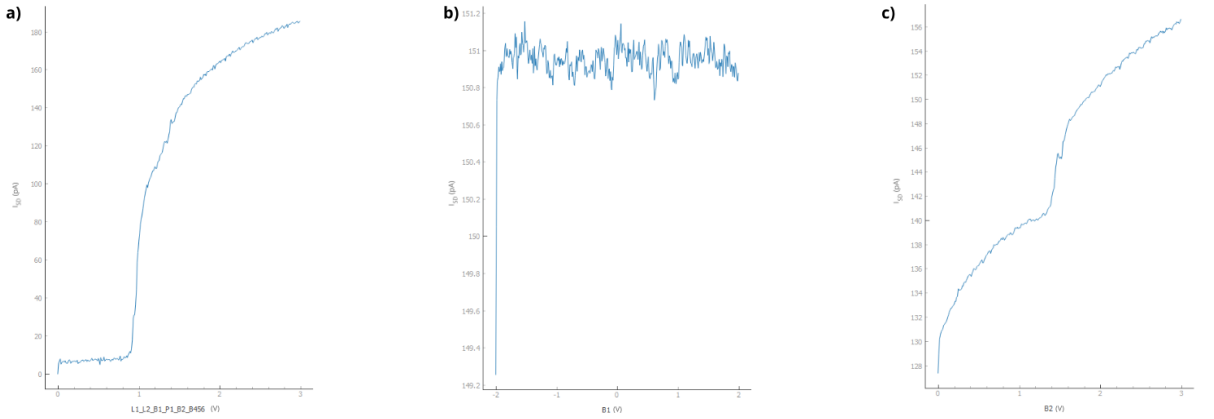

Figure 36: Turn-on curve and pinch-off curves of device WD (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2.

8.5 | Process Flow Fabrication non-RTA

In the figures below, the fabrication method used for the non-RTA'd chip(FK) is depicted. This process flow is made by Rik Seelen, as the chips are also fabricated by Rik. Note that there are no bismuth atoms implanted.

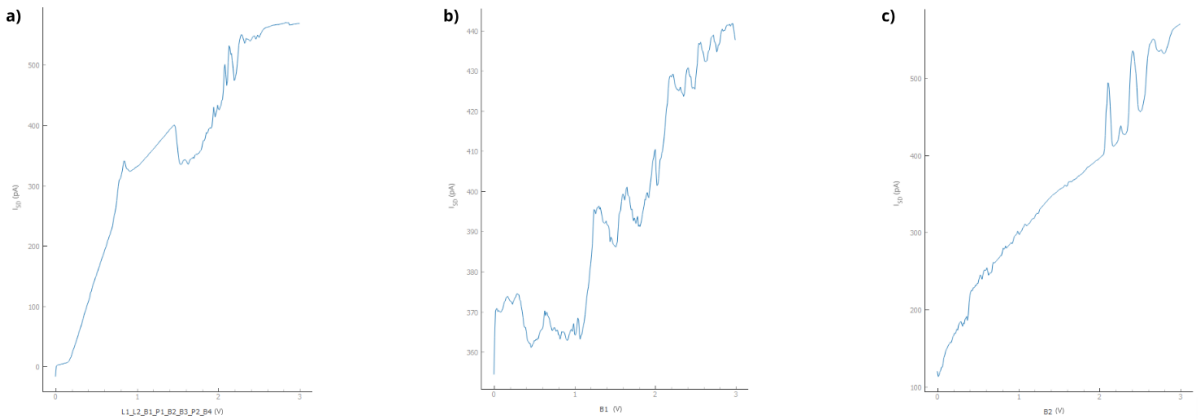

Figure 37: Turn-on curve and pinch-off curves of device XA (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2.

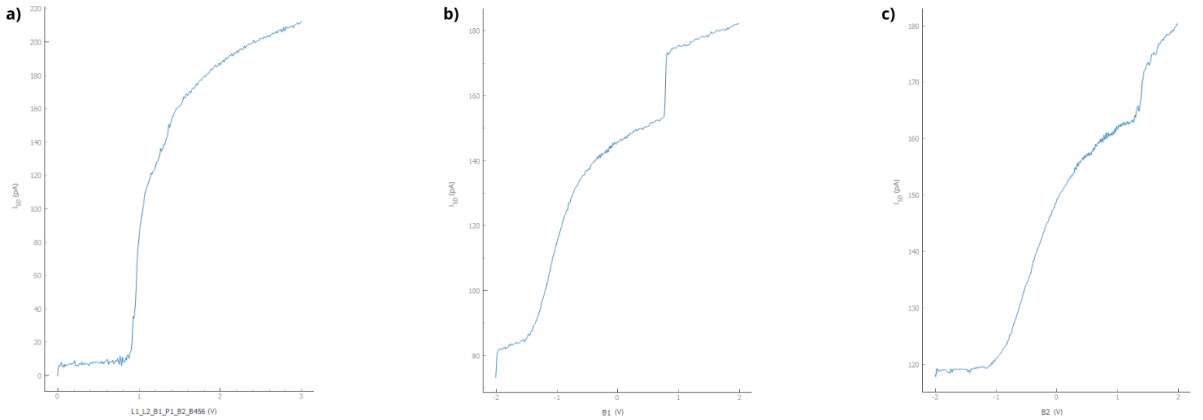

Figure 38: Turn-on curve and pinch-off curves of device XB (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2.

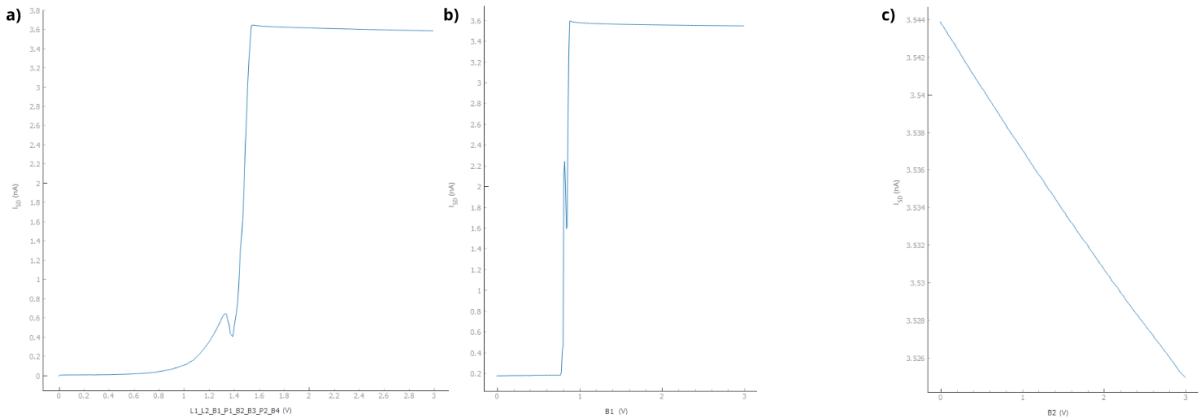

Figure 39: Turn-on curve and pinch-off curves of device YD (RTA'd). (a) shows the turn-on curve of B1. (b) shows the pinch-off curve of B1. (c) shows the pinch-off curve of B2.

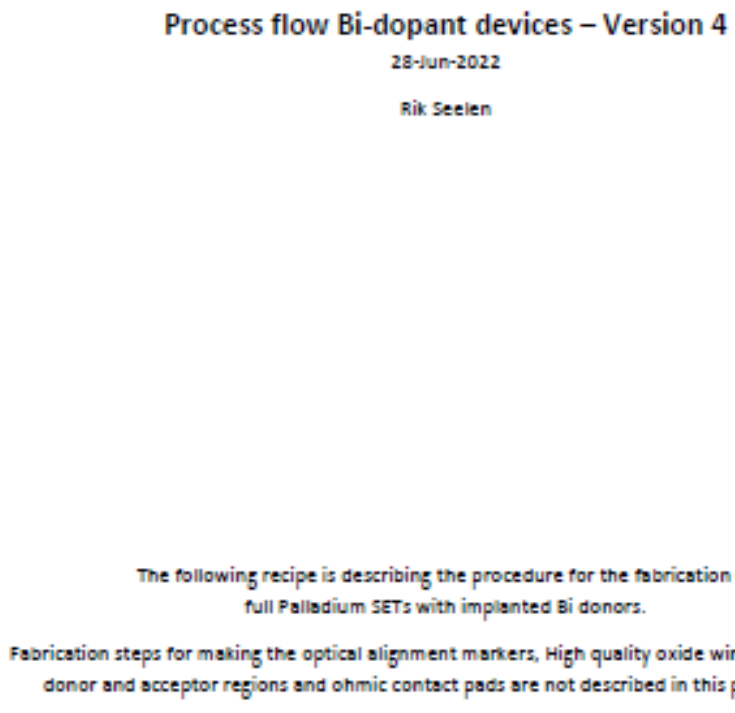

Figure 40: Titlepage

Implantation and Preparation	
EBL preparation	
WB23: PMMA spinning (thickness = 200 nm) A4, at 4000 RPM for 45 s Hotplate softbake 160°C, 3 min.	
EBL Patterning (see end of document)	
PMMA development	
WB 26: 55 sec. in MIBK:IPA (1:3) solution Flush with IPA for 30 sec. Dry	
Implantation of Bismuth (ion implantation)	
Implanted at IBS at 8 keV and 15 keV doses of 1e11, 2.5e11 and 5e11 cm^{-1}	
Optical alignment	
Optical (dark field) inspection of implantation windows, check position with respect to HQO and ohmics. Adapt design to ensure correct alignment.	
Cleaning	
Clean chip in Acetone, soak for 5 minutes IPA rinsing Dry	Optical check: All PMMA should be removed.
Rapid Thermal Annealing (RTA) (optional)	
Annealing in N2 atmosphere 800°C 10 minutes	

Figure 41: Page 2

Metal Markers	
Cleaning of the chip	
If coming from diced wafer: Acetone bath to dissolve PMMA Otherwise: Acetone rinsing IPA rinsing Dry	Optical check – Chip should be free of visible particles.
EBL preparation	
WB23: PMMA spinning (thickness = 200 nm) A4, at 4000 RPM for 45 s Hotplate softbake 160°C, 5 min.	
EBL Patterning (see end of document)	
PMMA development	
WB 26: 55 sec. in MIBK:IPA (1:3) solution Flush with IPA for 30 sec. Dry	
Sputtering of markers	
T'COathy sputter coater: Starting pressure $6x10^{-7}$ mbar Ti = 2 nm Pt = 50 nm	Check deposition rates in log
Lift off	
WB 11: Heat up DMSO to 80°C in ultrasonic bath WB 6: Heat up DMSO to 90°C on Hotplate Place chips 5 min. in heated DMSO Move DMSO & chips into ultrasonic bath WB 11, Ultrasonic Bath: 37 Hz, power = 30, 15 s 90 Hz, power = 30, 10 s 37 Hz, power = 30, 5 s 90 Hz, power = 30, 5 s Remove chip from DMSO Flush with IPA Dry	Heating of DMSO can be done beforehand to save time. Optical Check: Check for metal flaking and falling off.

Figure 42: Page 3

First Metal Layer – Barrier and plunger Gates	
Cleaning of the chip	
Acetone rinsing IPA rinsing and Dry	
EBL preparation	
WB 23: PMMA A4 spinning (thickness = 200 nm) at 4000 RPM for 45 s Hotplate Bake: 160°C, 5 min.	
EBL Design alignment (optional)	
Adapt the design (KLayout) of the Lead gate to align to the implanted regions	
EBL Patterning (see end of document)	
PMMA development	
WB 26: 55 sec. in MIBK:IPA (1:3) solution Flush with IPA for 30 sec. and Dry	
Electron beam Evaporation	
TOPdamper 2 nm Ti 15 nm Pd Pd Depostion rate 0.5 Å/s	Check log for deposition rates.
Lift off	
WB 11: Heat up DMSO to 80°C in ultrasonic bath WB 4: Heat up DMSO to 90°C on Hotplate Place chips 5 min. in heated DMSO Move DMSO & chips into ultrasonic bath WB 11, Ultrasonic Bath: 37 Hz, 30% power, 15 s 90 Hz, 30% power, 10 s Remove chip from DMSO Flush with IPA and Dry	Optical Check: Check for metal flaking and falling off.
Thermal ALD	
Picosun reactor 4: Al2O3, 250 °C 55 cycles, ~5 nm TMA and H2O	

Figure 43: Page 4

Process flow for small chips Second Metal Layer – Lead Gate	
The process for the second layer is very similar to that of the first layer. Differences are highlighted below, including Evaporation, Lift-off and Annealing.	
Electron beam Evaporation	
TOPdamper 2 nm Ti 35 nm Pd Pd deposition rate: 0.5 Å/s	
Lift-Off	
WB 11: Heat up DMSO to 80°C in ultrasonic bath WB 4: Heat up DMSO to 90°C on Hotplate Place chips 5 min. in heated DMSO Move DMSO & chips into ultrasonic bath WB 11, Ultrasonic Bath: 37 Hz, 30% power, 15 s 90 Hz, 30% power, 10 s 37 Hz, 40% power, 10 s 90 Hz, 40% power, 10 s Maybe more. Remove chip from DMSO Flush with IPA Dry	Lift-off is rougher, due to the fusing of PMMA and Pd during evaporation. This makes it quite a bit tougher to remove.
Thermal ALD	
Picosun reactor 4: Al2O3, 250 °C 55 cycles, ~5 nm TMA and H2O	
Thermal Annealing	
Picosun reactor 2: H2, 400 °C 30 min.	H2 flow settings: 40 ml/min, 1 mbar Ar flow: 50 ml/min Cool down should be done veeeery carefully.

Figure 44: Page 5

Electron Beam Lithography (EBL)

Machine used - RAITH EBPG5150
Write field = 500x500 µm

Patterning on PMMA layer of 200 nm.
PEC is applied.

Implantation windows	
Current	50 nA
Dose	1100 µC/cm²
Markers	
Current	50 nA
Dose	1100 µC/cm²
Fine structures -- First and Second layer	
Current	1 nA
Dose	800 µC/cm²
Course structures – First and Second layer	
Current	50 nA
Dose	800 µC/cm²

Figure 45: Page 6

Process flow Bi-dopant devices – Version 3

09-Mar-2022

Rik Seelen

The following recipe is describing the procedure for the fabrication of
full Palladium SETs. For the full Bi-dopant device, the process flow will have to be extended.

Figure 46: Titlepage

Process flow for small chips Metal Markers	
Cleaning of the chip	
If coming from diced wafer: Acetone bath to dissolve PMMA Otherwise: Acetone rinsing IPA rinsing Dry	Optical check – Chip should be free of visible particles.
EBL preparation	
WB23: PMMA spinning (thickness = 200 nm) A4, at 4000 RPM for 45 s Hotplate softbake 160°C, 5 min.	
EBL Patterning (see end of document)	
PMMA development	
WB 26: 55 sec. in MIBK:IPA (1:3) solution Flush with IPA for 30 sec. Dry	
Sputtering of markers	
T'COathy sputter coater: Starting pressure $6x10^{-7}$ mbar Ti = 2 nm Pt = 50 nm	Check deposition rates in log
Lift off	
WB 11: Heat up DMSO to 80°C in ultrasonic bath WB 6: Heat up DMSO to 90°C on Hotplate Place chips 5 min. in heated DMSO Move DMSO & chips into ultrasonic bath WB 11, Ultrasonic Bath: 37 Hz, power = 30, 15 s 90 Hz, power = 30, 10 s 37 Hz, power = 30, 5 s 90 Hz, power = 30, 5 s Remove chip from DMSO Flush with IPA Dry	Heating of DMSO can be done beforehand to save time. Optical Check: Check for metal flaking and falling off.

Figure 47: Page 2

First Metal Layer – Barrier and plunger Gates	
Cleaning of the chip	
Acetone rinsing IPA rinsing and Dry	
EBL preparation	
WB 23: PMMA A4 spinning (thickness = 200 nm) at 4000 RPM for 45 s Hotplate Bake: 160˚C, 5 min.	
EBL Design alignment (optional)	
Adapt the design (KLayout) of the Lead gate to align to the implanted regions	
EBL Patterning (see end of document)	
PMMA development	
WB 26: 55 sec. in MIBK:IPA (1:3) solution Flush with IPA for 30 sec. and Dry	
Electron beam Evaporation	
Tantallum/BIOS evaporator 2 nm Ti 20 nm Pd Pd Depostion rate 0.5 Å/s	Check log for deposition rates.
Lift off	
WB 11: Heat up DMSO to 80˚C in ultrasonic bath WB 4: Heat up DMSO to 90˚C on Hotplate Place chips 5 min. in heated DMSO Move DMSO & chips into ultrasonic bath WB 11, Ultrasonic Bath: 37 Hz, 30% power, 15 s 90 Hz, 30% power, 10 s Remove chip from DMSO Flush with IPA and Dry	Optical Check: Check for metal flaking and falling off.
Thermal ALD	
Picosun reactor 4: Al2O3, 250 ˚C 55 cycles, ~5 nm TMA and H2O	

Figure 48: Page 3

Process flow for small chips Second Metal Layer – Lead Gate	
The process for the second layer is very similar to that of the first layer. Differences are highlighted below, including Evaporation, Lift-off and Annealing.	
Electron beam Evaporation	
Tantallum/BIOS evaporator: 2 nm Ti 40 nm Pd Pd deposition rate: 0.3 Å/s	
Lift-Off	
WB 11: Heat up DMSO to 80˚C in ultrasonic bath WB 4: Heat up DMSO to 90˚C on Hotplate Place chips 5 min. in heated DMSO Move DMSO & chips into ultrasonic bath WB 11, Ultrasonic Bath: 37 Hz, 30% power, 15 s 90 Hz, 30% power, 10 s 37 Hz, 40% power, 10 s 90 Hz, 40% power, 10 s Maybe more. Remove chip from DMSO Flush with IPA Dry	Lift-off is rougher, due to the fusing of PMMA and Pd during evaporation. This makes it quite a bit tougher to remove.
Thermal ALD	
Picosun reactor 4: Al2O3, 250 ˚C 55 cycles, ~5 nm TMA and H2O	
Thermal Annealing	
Picosun reactor 2: H2, 400 ˚C 30 min.	H2 flow settings: 40 ml/min, 1 mbar Ar flow: 50 ml/min Cool down should be done veeeery carefully.

Figure 49: Page 4

Electron Beam Lithography (EBL)

Machine used - RAITH EBPG5150
Write field = 500x500 µm

Patterning on PMMA layer of 200 nm.
PEC is applied.

Markers	
Current	50 nA
Dose	1100 µC/cm³
Fine structures -- First and Second layer	
Current	1 nA
Dose	800 µC/cm³
Course structures -- First and Second layer	
Current	50 nA
Dose	800 µC/cm³

Figure 50: Page 5