# A comparison of the performance limitations of RC-, Shift Register- and Delay-locked loop- based multiphase clock generation schemes

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***Abstract*—Multi-phase clock generators (MPCGs) are often used in wireless communication systems, high-speed serial links and other applications where high frequency clock signals are advantageous to system performance. As a result of their increasing importance in modern systems, various generation schemes exist. This paper analyses three generation schemes: Shift register-based MPCG (SR-MPCG), RC-based MPCG (RC-MPCG) and Delay-locked loop-based MPCG (DLL-MPCG).**
**The paper begins by outlining the principles behind the operation of each scheme and proceeds to convey the observations and results from generating an 8-phase, 500MHz output signal using each scheme. All circuits are realised using $0.12\mu m$ MOSFET technology and 1.2V supply voltage. Finally, using phase accuracy and power usage as criteria, a cross-scheme comparison is made. The result of this comparison is that the SR-MPCG offers the highest level of phase accuracy and lowest power consumption. The DLL-MPCG had the lowest phase accuracy and the highest power consumption.**

***Index Terms*—Multi-phase clock generator, delay-locked loop, shift register, RC clock generator**

## I. Introduction

MULTI-PHASE clock generators (MPCG) are a subset of clock generators characterised by their ability to generate clock signals of varying phase from a single input signal. The ability to generate clock signals of varying phase finds utility in a number of fields, one of which is high-speed serial links. In this field, multi-phase clock signals are used to attain gate-speeds that surpass the speed limitations that exist when multiplexing and demultiplexing serial data [1]. Another use is in analog-to-digital converters (ADCs), where they are used in order to achieve data rates higher than the local clock signal [2]. This report will study and compare the performance of three multi-phase clock generation schemes in terms of phase accuracy and power. The systems to be evaluated are an RC-based MPCG, a shift-register based MPCG and a delay-locked loop MPCG. The primary motivation behind this research is to carry out a fair comparison of the three MPCG topologies by implementing the circuits using a single technology. Through implementing each topology in the same technology and driving the same load, a better understanding of the respective differences can be established. In order to achieve this goal, the research was structured around tackling the following questions:

- Which clock generation scheme offers the highest phase accuracy while generating an 8-phase, 500MHz output clock signal?
- Which of the three schemes offers the best power usage for a 500MHz output clock signal, while using $0.12\mu$m MOSFET technology?
- What factors limit the phase accuracy of the individual generation schemes when driving a standard load modeled to represent the typical load of an MPCG?

In terms of structure, the architecture section will explore the underlying principles behind each scheme's operation. Following this, the simulations and results for each scheme will be described and the discussion section will make a comparison based on these results. Furthermore, limitations in the generation schemes shall be explored. Finally, the conclusion will answer the research questions introduced above and provide recommendations for future research.

## II. Architecture

This section of the report will outline the principles behind the operation of each generation scheme.

### A. Shift register-based MPCG

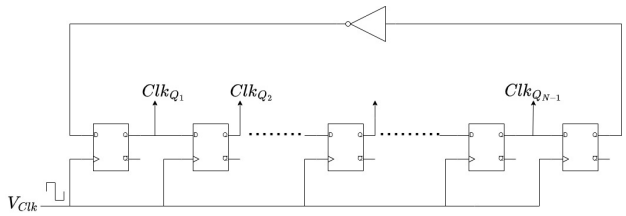


Fig. 1. Block schematic of SR-MPCG

The Shift Register-based Multi-phase Clock Generator (SR-MPCG) is based on the MPCG proposed in [3]. D flip-flops are designed to store data input provided at the rising edge of the clock signal (through the D port) and output this at the Q port during the other parts of the clock signal. Since the output of the D flip-flop can only change at rising edges of the clock signal, two D flip-flops connected in series, and operating on the same clock signal, will have output signals with a difference of one clock period.

The simple reason for this is that the difference between two consecutive rising edges of a clock signal is one clock period. The SR-MPCG leverages this characteristic of D flip-flops in order to produce multiple phases from a single clock signal. It is worth noting, however, simply connecting N consecutive D

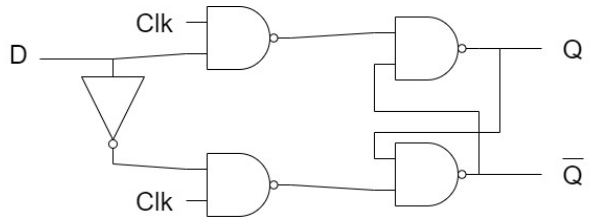


Fig. 2. Block diagram of implemented D flip-flop

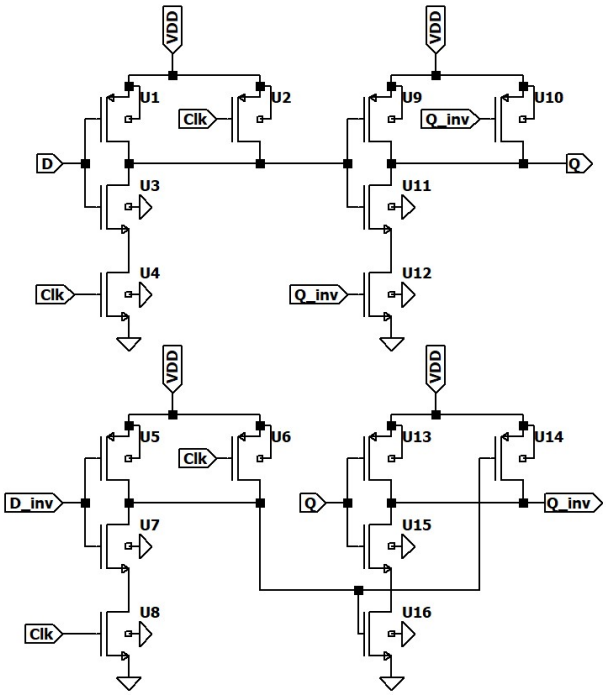


Fig. 3. Schematic of implemented D flip-flop

flip-flops is not sufficient to produce the desired clock signals. It is also necessary to connect the flip-flops in a feedback loop with an inverter, as seen in fig.1. By connecting the D input of the first flip-flop to the output of the last flip-flop, all stages of the system are connected in a feedback loop; however, it is necessary to include an inverter within this loop in order to produce a complete clock signal. In other words, the inverter changes the input to the first flip-flop such that the logical high and low part of a clock signal are generated at the output of each flip-flop. In this way, the SR-MPCG acts as a divide-by-2N circuit, where N is the number of flip-flop stages.

### *B. RC-based MPCG*

The MPCG analysed in this section is based on the multi-phase generator proposed in [4]. It consists of a chain of capacitors connected in series, followed by a chain of resistors connected in series. Between each pair of components, a phase shifted version of the input signal may be retrieved, as shown in fig. 4. The buffers are then used to create square waves from the sinusoid input.

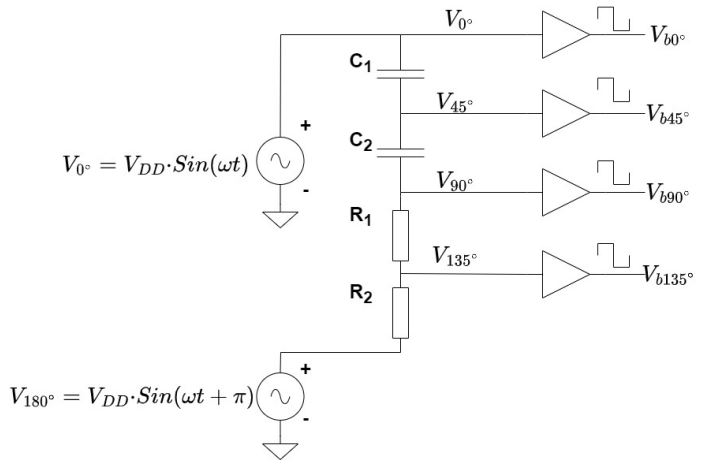


Fig. 4. RC-MPCG Circuit

For an input frequency, $f$, the resistor and capacitor values may be calculated as follows:

$$C_\phi = \frac{C_1 C_2}{C_1 + C_2} \tag{1}$$

$$R_\phi = R_1 + R_2 \tag{2}$$

$$\omega = 2\pi f \tag{3}$$

Then,

$$V_{45^\circ} = V_{0^\circ} \cdot \frac{\frac{1}{j\omega C_1}}{\frac{1}{j\omega C_2} + \frac{1}{j\omega C_1} + R_\phi} - \frac{R_\phi + \frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2} + \frac{1}{j\omega C_1} + R_\phi} \cdot V_{0^\circ} \tag{4}$$

$$\frac{V_{45^\circ}}{V_{0^\circ}} = \frac{C_2 - C_1 - j\omega R_\phi C_1 C_2}{C_2 + C_1 + j\omega R_\phi C_1 C_2} \tag{5}$$

Therefore,

$$Arg(V_{45^\circ}) = tan^{-1}\Big(\frac{\omega R_\phi C_1 C_2)}{C_1 - C_2}\Big) - tan^{-1}\Big(\frac{\omega R_\phi C_1 C_2}{C_1 + C_2}\Big) \tag{6}$$

Since,

$$tan^{-1}(x) - tan^{-1}(y) = tan^{-1}\left(\frac{x-y}{1+xy}\right) \tag{7}$$

$$tan(45^\circ) = \frac{\omega R_\phi C_1 C_2 (2C_2)}{(C_1 - C_2)(C_1 + C_2)} \cdot \frac{(C_1 - C_2)(C_1 + C_2)}{(\omega R_\phi C_1 C_2)^2}$$

$$1 = \frac{2C_2}{\omega R_\phi C_1 C_2}$$

$$C_1 = \frac{2}{\omega R_\phi} \tag{8}$$

The designer will then choose what value of $R_\phi$ or $C_\phi$ is acceptable for their system. A general rule when deciding is that $R_\phi C_\phi = \frac{1}{2\pi f}$, where f is the frequency being applied. The reason for this rule is as follows:

$$V_{90^\circ} = V_{0^\circ} \cdot \frac{R_\phi}{R_\phi + \frac{1}{j\omega C_\phi}} + V_{180^\circ} \cdot \frac{\frac{1}{j\omega C_\phi}}{R_\phi + \frac{1}{j\omega C_\phi}} \tag{9}$$

Since $V_{180^\circ} = -V_{0^\circ}$,

$$V_{90^\circ} = V_{0^\circ}\left(-\frac{1 - j\omega C_\phi R_\phi}{1 + j\omega C_\phi R_\phi}\right) \tag{10}$$

Then,

$$H(j\omega) = \frac{V_{90^\circ}}{V_{0^\circ}} = -\frac{1 - j\omega C_\phi R_\phi}{1 + j\omega C_\phi R_\phi} \tag{11}$$

Since at cut-off frequency, the phase shift is at half of its range, the next step is then to find the cut-off frequency. From eq.11, the cut-off freq is given by

$$H(j\omega) = (1 - j\omega C_\phi R_\phi) \cdot \frac{1}{1 + j\omega C_\phi R_\phi} \tag{12}$$

At cut-off freq,

$$|H(j\omega)| = \frac{1}{\sqrt{2}} \tag{13}$$

To simplify calculations, $(1 - j\omega C_\phi R_\phi)$ will be ignored since these are the zeros of the system and may therefore be viewed as the gain. In order to satisfy eq.13,

$$\omega = \frac{1}{C_\phi R_\phi} \tag{14}$$

Then, it holds that

$$C_\phi R_\phi = \frac{1}{\omega} \tag{15}$$

Once the values of $R_\phi$ and $C_\phi$ are chosen, similar steps along with simultaneous equations can be used to find the optimum values for $C_1$, $C_2$, $R_1$ and $R_2$.

### C. Delay-Locked Loop-based MPCG

The Delay-Locked Loop-based MPCG (DLL-MPCG) can be divided into 3 blocks: phase frequency detector (PFD), charge pump (CP) and the voltage-controlled delay line (VCDL). Fig. 5 shows how these blocks are connected within the system. The VCDL is used to delay the clock signal and thereby produce multiple phases from one clock signal. The CP produces a voltage that regulates the delay of the various stages of the VCDL such that $V_{VCDL}$ will be in phase with $V_{Clk}$. In order to produce this control voltage from the CP, the PFD is used to compare the phase of $V_{VCDL}$ with that of $V_{Clk}$. The output of this comparison are the signals $V_{UP}$ and $V_{DWN}$, which correspond to whether the phase of $V_{VCDL}$ must be increased or decreased. The loop filter is a low-pass filter used to smoothen $V_{Ctrl^*}$.

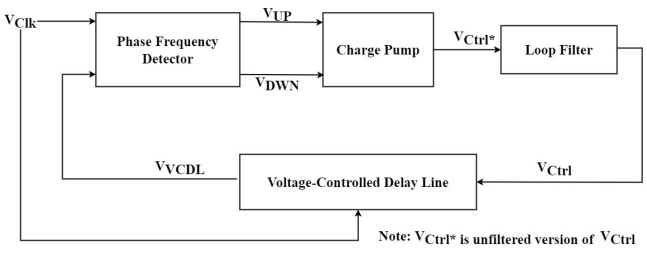


Fig. 5. DLL-MPCG block diagram

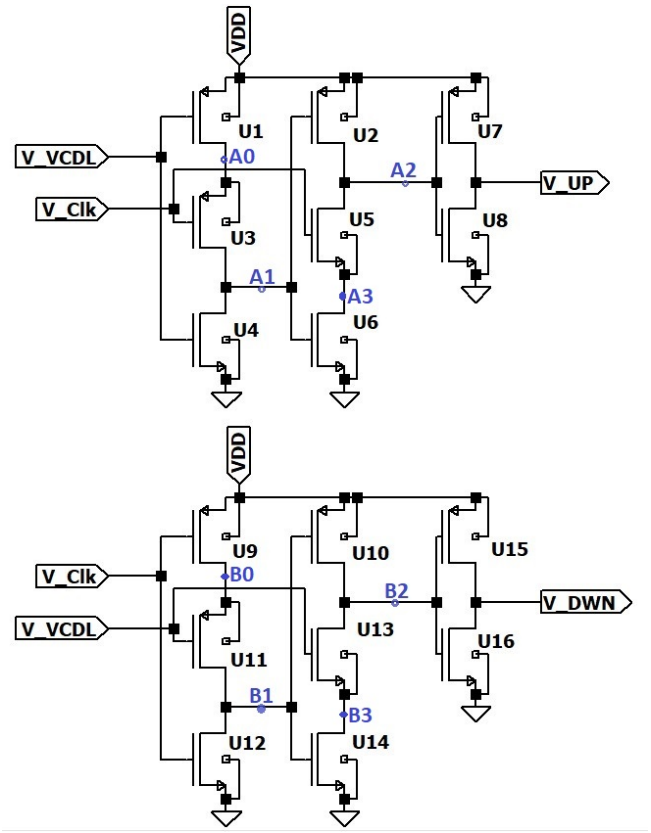


Fig. 6. Circuit of PFD

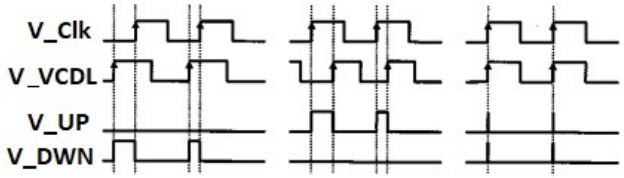


Fig. 7. Operation of PFD [5]

*1) Phase Frequency Detector:* The function of this block is to detect the difference in phase between the reference clock signal ($V_{Clk}$) and the output from the VCDL ($V_{VCDL}$). Fig. 6 shows the PFD implemented in this research [5].

The output of the PFD are the signals $V_{UP}$ and $V_{DWN}$ which correspond to an "up" and "down" signal, respectively. A logic high for $V_{UP}$ occurs when $V_{Clk}$ is leading in phase, relative to $V_{VCDL}$. Similarly, $V_{DWN}$ has a logic high when $V_{VCDL}$ is leading in phase, relative to $V_{Clk}$. Table I and table II show truth tables that describe the operation of the PFD. More specifically, the tables outline the expected behaviour of the PFD in the current state, given a specific previous state. It is necessary to note the previous state in two of the four possible input combinations, due to the PFD using the parasitic capacitance of MOSFETS to produce a memory effect within the system. The effect can be observed when a node is floating and keeps the state it was previously in for at least 1 clock period.

It is worth noting that the circuitry responsible for

generating $V_{UP}$ and $V_{DWN}$ are generally the same, with the exception that the input values are swapped as shown in fig. 6. An analysis of the circuitry for $V_{UP}$ is therefore sufficient to understand the operation of the PFD.

When $V_{VCDL}$ is at a logic high, then the PMOS (U1) will be switched off while the NMOS (U4) will be switched on. This is due to PMOS transistors being in the cut-off region when the magnitude of gate voltage is higher than the magnitude of threshold voltage, whereas NMOS transistors will be switched on under the same conditions. Since the MOSFET U4 is on, it may be treated as a closed switch to the ground terminal. The node A1 to the next stage will therefore be at a logic low. As a result, the PMOS (U2) connected to the power supply ($V_{DD}$), will be switched on and cause node A2 to be at logic high. $V_{UP}$ will therefore be at logic low. The output $V_{UP}$ will be in this state whether $V_{Clk}$ is at a logic high or at a logic low.

When $V_{Clk}$ is at a logic high while $V_{VCDL}$ is at a logic high then PMOS U3 will be switched off while NMOS U4 is on. Node A1 will then be at a logic low due to U4 being connected to ground. Since A1 is at a low state then U2 will be switched on. U5 will also be switched on due to $V_{Clk}$ but since U6 is switched off, U5 will have no effect on the state of node A2. A2 will therefore be at a logic high due to U2 being switched on and having a connection to $V_{DD}$.

In the case that $V_{Clk}$ is at a logic low while $V_{VCDL}$ is at a logic high, then U1 will be switched off while U3 and U4 will be switched on. The node A1 will then be a logic low since U4 connects to ground while U3 connects to the switched off MOSFET U1. $V_{Clk}$ being at a low state causes U5 to be switched off while U2 is switched on. A2 will therefore be at logic high and cause $V_{UP}$ to be at a logic low.

When $V_{VCDL}$ is at a logic low and $V_{Clk}$ is at a logic low, then node A1 will have a connection to $V_{DD}$ since U1 and U3 will be switched on. A1 will therefore be at a logic high. A1 being at a logic high will cause U6 to be switched on, whereas U2 will be switched off. $V_{Clk}$ being at a logic low causes U5 to be switched off. As a result, node A2 will have no connection to both ground and $V_{DD}$. In this situation, the node is said to be floating and will retain its previous state.

- If the previous state was $V_{VCDL}$ being at logic low while $V_{Clk}$ is at logic high, then the current state is ill-defined and will depend on the last well-defined state. The reason for this is that $V_{VCDL}$ being at a logic low causes U1 to be switched on while U4 is switched off. $V_{Clk}$ being at logic high will cause U3 to be switched off while U5 is switched on. Since there is no connection to the ground or supply, then A1 will be defined by its' previous state. Node A1 will then cause A2 to be defined by its' previous state.
- If the previous state was $V_{VCDL}$ being at logic high while $V_{Clk}$ is at either logic high or logic low, then node A2 will be at logic high. As previously mentioned, when $V_{VCDL}$ is at logic high then node A1 will be at logic low and switch on U2, which will cause node A2 to be at logic high. In terms of the current state this will result in $V_{UP}$ being at logic low.

For the scenario where the current state of $V_{VCDL}$ is at logic low and $V_{Clk}$ is at logic high, then node A1 will be ill-defined because U3 and U4 will both be switched off. A1 therefore keeps the value of its' previous state. In this instance, the previous state will be one of two options:

- if both $V_{VCDL}$ and $V_{Clk}$ were at logic low, then A1 will be at logic high since U1 and U3 are switched on while U4 is switched off. Since the current state will define A1 as a logic high due to the previous state, U6 will be switched on while U2 is switched off. $V_{Clk}$ having a logic high in the current state will cause U5 to be switched on, resulting in A2 being at logic low due to the connection to ground. $V_{UP}$ shall therefore be at logic high in the current state.
- if the previous state had both $V_{VCDL}$ and $V_{Clk}$ at logic high, then the current state of A1 will be defined as logic low. This will cause U2 to be switched on along with U5. As a result of the connection, A2 will be at logic high, causing $V_{UP}$ to be at logic low.

*2) Charge Pump:* The function of the charge pump is to convert the signals $V_{UP}$ and $V_{DWN}$ from the PFD into a control signal ($V_{Ctrl}$). This control signal is used to modulate the delay within the VCDL, such that $V_{VCDL}$ is in-phase with $V_{Clk}$. A single-ended drain-switched charge pump was chosen to implement this function in the system. In addition to having a low level of complexity, this topology has the advantage of offering low rates of power consumption during operation [6]. It is made up of two current mirrors, a pair of MOSFETs that operate as switches, and an inverter and loop filter that are connected to the input and output, respectively.

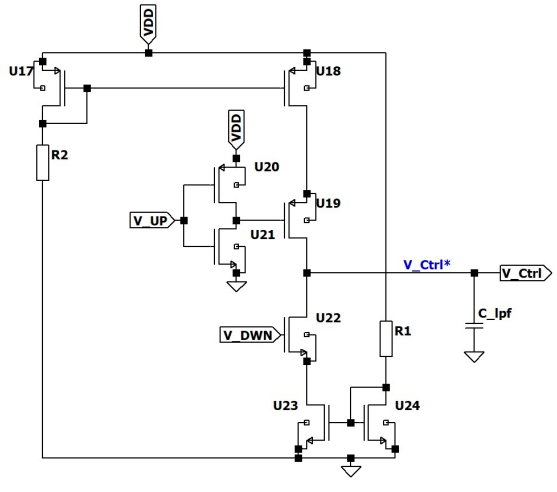


Fig. 8. Circuit of charge Pump

In terms of operation, the PMOS U19 and NMOS U22 operate as switches that are controlled by the output from the PFD. When $V_{UP}$ is at a logic high, U19 switches on due to the logic high being inverted by the transistors U20 and U21. Transistors U18 and U17 together form the current

TABLE I
TRUTH TABLE SHOWING OPERATION OF PFD'S $V_{UP}$ CIRCUITRY

| $V_{VCDL}$ | $V_{Clk}$ | **A0** | **A1** | **A2** | **A3** | $V_{UP}$ |
|---|---|---|---|---|---|---|
| Case: $V_{VCDL}$ lagging $V_{Clk}$ | | | | | | |
| 0 | 0 | 1 | 1 | (previous state) | 0 | (previous state) |
| 0 | 1 | 1 | 1 (previous state) | 0 | 0 | 1 |
| 1 | 1 | 1 (previous state) | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 (previous state) | 0 |
| 0 | 0 | 1 | 1 | 1 (previous state) | 0 | 0 |
| 0 | 1 | 1 | 1 (previous state) | 0 | 0 | 1 |
| 1 | 1 | 1 (previous state) | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 (previous state) | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| Case: $V_{VCDL}$ leading $V_{Clk}$ | | | | | | |
| 0 | 0 | 1 | 1 | (previous state) | 0 | (previous state) |
| 1 | 0 | 0 | 0 | 1 | 0 (previous state) | 0 |
| 1 | 1 | 0 (previous state) | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 (previous state) | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 (previous state) | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 (previous state) | 0 |
| 1 | 1 | 0 (previous state) | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 (previous state) | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 (previous state) | 0 | 0 |

TABLE II
TRUTH TABLE SHOWING OPERATION OF PFD'S $V_{DWN}$ CIRCUITRY

| $V_{VCDL}$ | $V_{Clk}$ | **A0** | **A1** | **A2** | **A3** | $V_{UP}$ |
|---|---|---|---|---|---|---|
| Case: $V_{VCDL}$ lagging $V_{Clk}$ | | | | | | |
| 0 | 0 | 1 | 1 | (previous state) | 0 | (previous state) |
| 0 | 1 | 1 | 1 (previous state) | 0 | 0 | 1 |
| 1 | 1 | 1 (previous state) | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 (previous state) | 0 |
| 0 | 0 | 1 | 1 | 1 (previous state) | 0 | 0 |
| 0 | 1 | 1 | 1 (previous state) | 0 | 0 | 1 |
| 1 | 1 | 1 (previous state) | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 (previous state) | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| Case: $V_{VCDL}$ leading $V_{Clk}$ | | | | | | |
| 0 | 0 | 1 | 1 | (previous state) | 0 | (previous state) |
| 1 | 0 | 0 | 0 | 1 | 0 (previous state) | 0 |
| 1 | 1 | 0 (previous state) | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 (previous state) | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 (previous state) | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 (previous state) | 0 |
| 1 | 1 | 0 (previous state) | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 (previous state) | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 (previous state) | 0 | 0 |

mirror which acts as a current source to U19. At the moment that U19 is switched on due to $V_{UP}$, a current pulse occurs and increases the value of $V_{Ctrl}$. Similarly, when $V_{DWN}$ is at logic high, U22 switches on and due to the connection it has to the current mirror formed by U23 and U24, current is sunk to ground thereby decreasing the value of $V_{Ctrl}$.

It is worth noting that due to current pulses within the CP, as well as non-idealities associated with the switching of the MOSFETs in the charge pump, the control voltage from the CP generally contains ripples. In order to obtain a control voltage that is relatively constant as current pulses occur, a loop filter is connected between the output of the charge pump and the input of the VCDL, as shown in fig. 5.

When designing a loop filter, it is necessary to consider the effect this filter will have on closed-loop stability of the overall system. In general, higher order low-pass loop filters provide better output due to filter attenuation above the bandwidth being proportional to the number of poles [7]. On the other hand, closed-loop stability decreases as the number of poles in a system is increased. For this reason, the capacitor $C_lpf$ is used to implement a first order low-pass filter. The advantage of implementing the loop filter in this way, is that the capacitance of $C_lpf$ can be added to the parasitic capacitance of the charge pump to form an equivalent capacitance that will not increase the number of poles within the system.

*3) Voltage-Controlled Delay Line:* The VCDL is primarily made of a chain of delay units which provide an equidistant phase shift of the reference clock signal $V_{Clk}$. Each delay unit has two inputs: $V_{DU}$ and $V_{Ctrl}$. $V_{DU}$ is generally the output of the previous stage, with the exception of the first delay unit that takes $V_{Clk}$ as an input. As shown in fig. 9, the second input is the filtered control voltage ($V_{Ctrl}$).

In general, the VCDL block aims to match the output of its final stage ($V_{VCDL}$) with the reference clock signal $V_{Clk}$. It achieves this by implementing an overall delay equal to a period of $V_{Clk}$. In other words, the number of delay units determines how much phase shift is attained at the output of each stage since the final stage will be in phase with $V_{Clk}$.

The individual delay units are able to achieve the required delay as follows. As shown in fig. 10, the MOSFETs in the delay unit add parasitic capacitance to the circuit [8].

$C_{pn_{gd}}$ is the combined gate-drain capacitance of P1 and N1. $C_{p_{db1}}$ and $C_{n_{db1}}$ are the drain-bulk capacitance of P1 and N1, respectively. The drain-bulk capacitance are a result of having a reverse-biased pn junction within the MOSFETs. Similarly, $C_{n_{db2}}$ is the drain-bulk capacitance of N2. $C_w$ is the wire capacitance. This becomes increasingly important as the MOSFETs gets smaller in size. Finally, $C_{p_g}$ and $C_{n_g}$ are the gate capacitance of P2 and N3.

In order to understand the propagation delay introduced by this circuit, the parasitic capacitance indicated in fig. 10 are combined into a single parasitic capacitance $C_{eq} = C_{pn_{gd}} + C_{p_{db1}} + C_{n_{db1}} + C_{n_{db2}} + C_w + C_{p_g} + C_{n_g}$ .

When $V_{DU}$ instantaneously changes from a logic high to logic low state, N1 will operate in the cut-off region while P1 will operate from the saturation region. Additionally, if $V_{Ctrl} = 0V$ then N2 will also be in the cut-off region. A simplified model to represent this situation would then have P1 represented by a resistor and N1 represented by an open switch with $C_{eq}$ in parallel (fig. 11a). This setup is equivalent to a basic RC circuit and it can therefore be said that the time it will take for the output of the inverter to reach 70% of the maximum value is $\tau = RC$, where R and C are given by:

$$C = C_{eq} + C_1 \tag{16}$$

$$R = R_{P1_{DS}} + R_{N2_{DS}} \tag{17}$$

for $R_{P1_{DS}}$ the drain-source resistance of P1 and $R_{N2_{DS}}$ the drain-source resistance of N2. Note that $C_1$ is an external capacitor placed in the circuit to increase the delay range of each delay unit.

A similar model can be made for the situation when $V_{DU}$ instantaneously changes from a logic low to logic high state, while $V_{Ctrl} = 0V$. The difference being that P1 and N2 will operate in the cut-off region while N1 is in saturation.

When N2 and $V_{Ctrl}$ are taken into account, the model of fig. 11 slightly changes to have a current source in parallel with $C_{eq}$ and $C_1$, as shown in fig. 12. The current source (N2) changes the time constant $\tau = RC$.

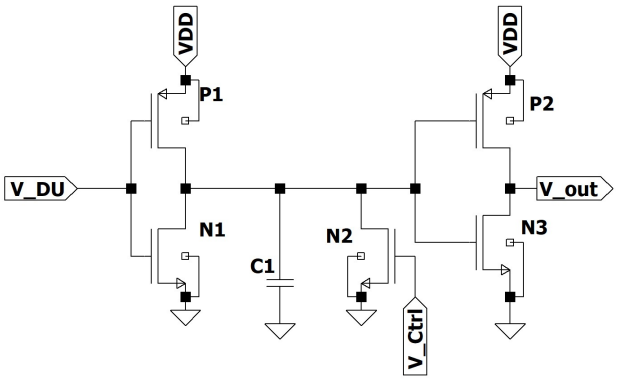


Fig. 9. Circuit of delay unit

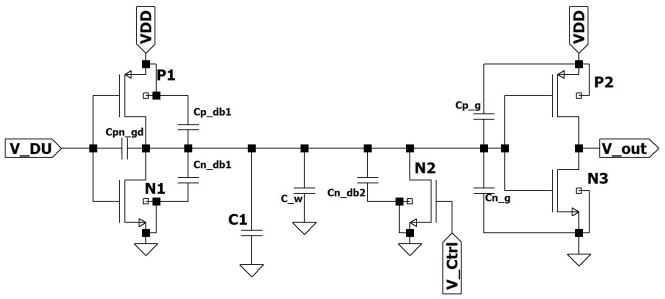


Fig. 10. Equivalent circuit modelling the parasitic capacitance of a delay unit

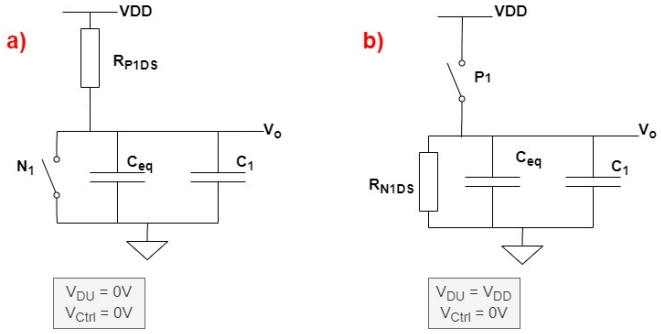


Fig. 11. Simplified model of delay unit when **a)**$V_{DU} = 0V$ **b)** $V_{DU} = V_{DD}$

When gate voltage of N2 increases due to rising $V_{Ctrl}$, then more current is pulled to ground. When more current is pulled to ground, then the time taken to charge $C_{eq}$ and $C_1$ increases. Similarly, reducing $V_{Ctrl}$ decreases the delay because less current is pulled to ground resulting in a shorter charging time. It is necessary to scale N2 such that the delay of a unit is $-20\%t_{delay}$ when $V_{Ctrl} = 0V$ and $+20\%t_{delay}$ when $V_{Ctrl} = \frac{V_{DD}}{2}$, where $t_{delay}$ is the desired time delay.

## III. Methodology

The aim of this research was to tackle the following research questions:

- Which clock generation scheme offers the highest phase accuracy while generating an 8-phase, 500MHz output clock signal?
- Which of the three schemes offers the best power usage for a 500MHz output clock signal, while using 0.12$\mu$m MOSFET technology?

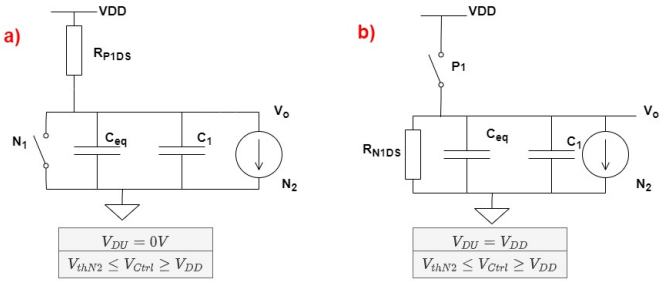


Fig. 12. Simplified model of delay unit when N2 is not in cut-off region and **a)**$V_{DU} = 0V$ **b)** $V_{DU} = V_{DD}$

- What factors limit the phase accuracy of the individual generation schemes when driving a standard load modeled to represent the typical load of an MPCG?

In order to achieve this goal while maintaining a fair evaluation between the different generation schemes, boundary conditions were set. The first condition is that a standard load will be applied to each topology since MPCGs are typically connected in a system where they drive a certain load. In this way, the research can provide more realistic results. Bearing this in mind, the load was arbitrarily chosen to be a magnitude four times larger than the CMOS inverters being implemented in the topologies. As such, the load had $W_{NMOS} = 0.64\mu m$, $W_{PMOS} = 1.6\mu m$ and $L_{NMOS} = L_{PMOS} = 0.48\mu m$, where $W_{NMOS}$ and $W_{PMOS}$ are the NMOS and PMOS width, while $L_{NMOS}$ and $L_{PMOS}$ are the channel length of the NMOS and PMOS.

The second condition is that the output of each circuit must be a 500MHz clock signal. This condition will increase fairness in the research since the SR-MPCG produces an output signal with a frequency inversely proportional to the number of delay stages i.e. an input of 4GHz to a 4-stage SR-MPCG will result in a 4-phase 500MHz output, whereas the same input to the RC-MPCG will give a 4GHz output. Implementing a condition based on the output signal rather than the input signal will enable this research to gain a better understanding on the quality of output signal a scheme can produce inspite of the differences in implementation.

The final condition is that the supply voltage, $V_{DD}$, will be limited to 1.2V for all schemes. This condition will ensure the power evaluation is an accurate reflection of the system's ability. Additionally, 1.2V is the value of supply voltage in many CMOS applications which will make the results more relevant to current work.

### A. Simulations & Results

*1) SR-MPCG:* The clock signal ($V_{Clk}$) for this circuit was an 8GHz square wave. As mentioned in earlier sections, this scheme produces an output with frequency $F_{out} = \frac{F_{Clk}}{2N}$, where N= number of D flip-flop stages. In this case, a 500MHz output from eight stages will require an 8GHz clock signal.

The D flip-flops of the SR-MPCG each operate on a rising edge of the clock signal, which means that the generated phases should be $22.5^\circ$ apart since the D flip-flops operate at intervals of 1 clock period apart. Per stage phase difference is calculated as follows:

$$\phi_{diff} = \frac{\tau_{Clk}}{\tau_{phase}} \cdot 360^\circ = \frac{0.125 * 10^{-9}}{2 * 10^{-9}} \cdot 360^\circ = 22.5^\circ$$

where $\tau_{Clk}$ = period of the reference clock; $\tau_{phase}$ = period of the generated phase.

Table III shows the measured and expected phase difference between the first phase and the seven other phases generated by the SR-MPCG. Note that the measured values had a phase error of $\approx 8^\circ$ which was considered to be due to clock skew. As such, it was neglected from the measured values.

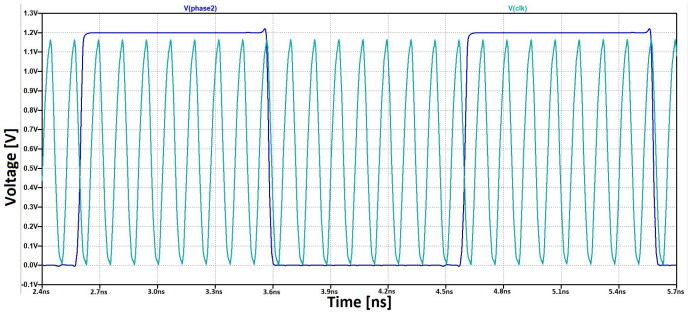


Fig. 13. showing waveform of $V_{Clk}$ and second phase of SR-MPCG ($V_{phase2}$)

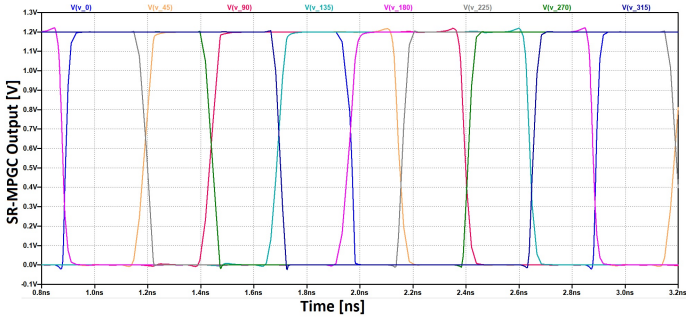


Fig. 14. showing 8-phase Output of SR-MPCG

TABLE III
SR-MPCG PER STAGE PHASE DIFFERENCE RELATIVE TO FIRST PHASE

| Compared Phases | Expected Phase Difference | Measured Phase Difference |
|---|---|---|
| Phase 1 & Phase 2 | 45.0° | 45.0° |
| Phase 1 & Phase 3 | 90.0° | 90.0° |
| Phase 1 & Phase 4 | 135.0° | 135.0° |
| Phase 1 & Phase 5 | 180.0° | 180.0° |
| Phase 1 & Phase 6 | 225.0° | 225.0° |
| Phase 1 & Phase 7 | 270.0° | 270.1° |
| Phase 1 & Phase 8 | 315.0° | 315.2° |

The average power to the circuit from the power supply was measured to be $P_{V_{DD}} = 191\mu W$, whereas the absolute power from the reference clock signal was $P_{Clk} = 2\mu W$, with an average current of $6nA$.

*2) RC-MPCG:* In order to find the capacitor and resistor values required, the steps of Section II-B were implemented. Using the approximation that $R_\phi C_\phi = \frac{1}{2\pi f}$, it was chosen that $R_\phi = 1100\Omega$. As a result, $C_\phi \approx 289fF$.

Using eq.8 and the value of $R_\phi$, $C_1$ could be calculated. In order to simplify computation, it was assumed that the capacitors have the same magnitude. This is to say, $C_1 = C_2 = 578fF$. Once the values of $C_1$ and $C_2$ were verified to give the required angle, similar steps were taken to find the value of the resistors $R_1$ and $R_2$. The difference between the calculations, however is that in this case $R_\phi = R_1 + R_2$. Therefore, setting $R_1 = R_2$ results in $R_1 = R_2 = 0.5R_\phi$. The final values of resistors and capacitors were as shown in fig.15.

TABLE IV
RC-MPCG PER STAGE PHASE DIFFERENCE RELATIVE TO FIRST PHASE

| Compared Phases | Expected Phase Difference | Measured Phase Difference |
|---|---|---|
| $V_{0^\circ}$ & $V_{45^\circ}$ | 45.0° | 44.0° |
| $V_{0^\circ}$ & $V_{90^\circ}$ | 90.0° | 90.1° |
| $V_{0^\circ}$ & $V_{135^\circ}$ | 135.0° | 136.2° |
| $V_{0^\circ}$ & $V_{180^\circ}$ | 180.0° | 178.6° |
| $V_{0^\circ}$ & $V_{225^\circ}$ | 225.0° | 222.1° |
| $V_0^\circ$ & $V_{270^\circ}$ | 270.0° | 268.2° |
| $V_{0^\circ}$ & $V_{315^\circ}$ | 315.0° | 314.0° |

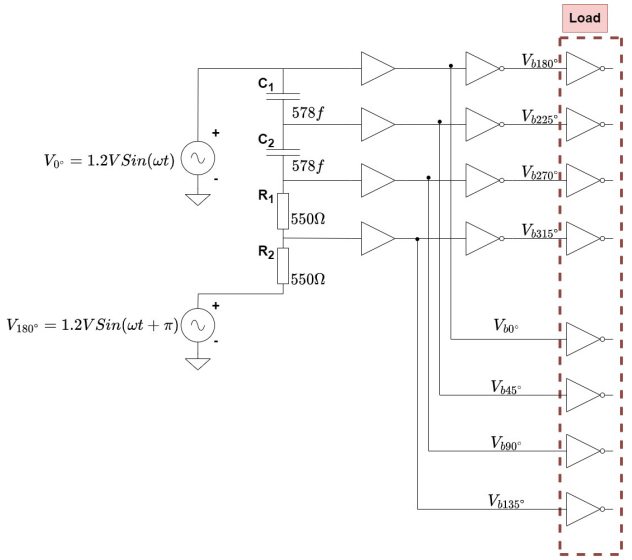


Fig. 15. Implemented 8-phase RC-MPCG Circuit

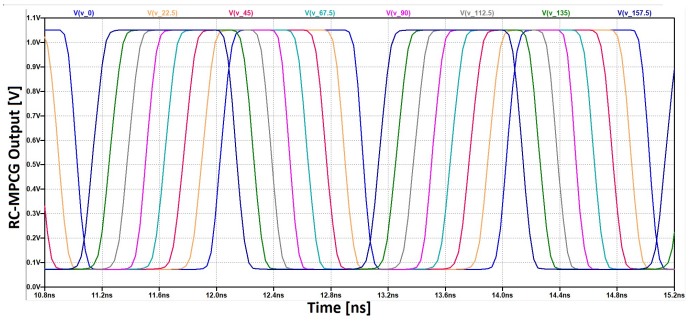


Fig. 16. 8-phase square wave output of RC-MPCG

A 1.2V, 500MHz sinewave with 0° phase shift and another 1.2V, 500MHz sine wave with a 180° phase shift, were applied to the system as shown in fig. 15. It is worth noting that the first 4 phases, between 0° and 180°, can be generated directly from the output of the corresponding buffer stage. On the other hand, to generate the phases between 180° and 360°, the first 4 phases must be inverted to produce a 180° phase shift in each signal. Table IV shows a summary of the measured phase accuracy for each of the expected phase shift values. The average power from the power supply to the circuit, was measured to be $P_{V_{DD}} = 291\mu W$. The power from the reference clock was $P_{Clk} = 17\mu W$.

*3) DLL-MPCG:* A 1.2V, 500MHz square wave was used as the $V_{CLK}$ input. The operation of the PFD was verified by plotting the output wavforms for $V_{VCDL}$ lagging and leading $V_{CLK}$ (fig.17 and fig.18 respectively).

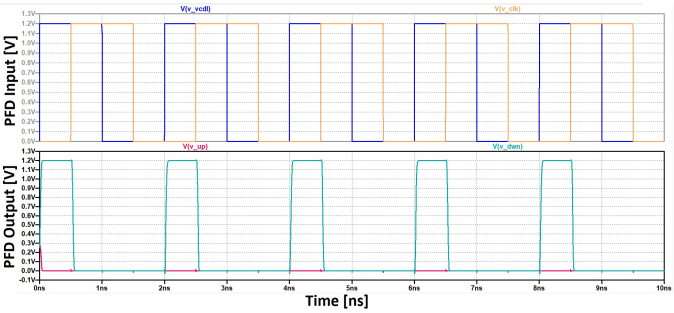


Fig. 17. PFD output when $V_{VCDL}$ is leading $V_{Clk}$

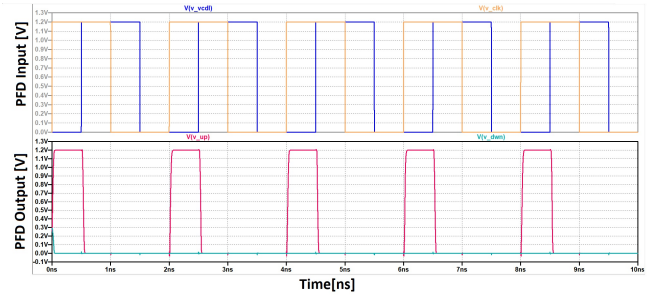


Fig. 18. PFD output when $V_{VCDL}$ is lagging $V_{Clk}$

The capacitor used in the loop filter ($C_{lpf}$) as shown in fig.8 was selected such that $\tau = 50ns$. Therefore, $C_{lpf} = 0.5pF$. The calculations were as follows:
For a capacitor it holds that,

$$I_C = \frac{dV_C}{dt}C \tag{18}$$

where, $I_C$ = current through the capacitor; $V_C$ = voltage of the capacitor; C = capacitance
In order to find the time taken to charge to $V_C = \frac{V_{DD}}{2} = 0.6V$, eq.18 becomes

$$V_C = \frac{I_C}{C} \cdot t \tag{19}$$

Eq.19 shows the relation between charge time and capacitance.

In terms of the delay unit, transistor N2 (from fig.19) was scaled such that each delay unit has a delay range of $202ps - 304ps$ for $V_{ctrl} = 0V$ and $V_{ctrl} = 0.6V$, respectively.

In terms of implementation, eight stages were implemented with an inverter as the load.

As with other topologies simulated in this research, the simulation was taken with time steps of 55.6fs to represent a phase accuracy of $+/-0.1^\circ$ for 500MHz signals. The delay

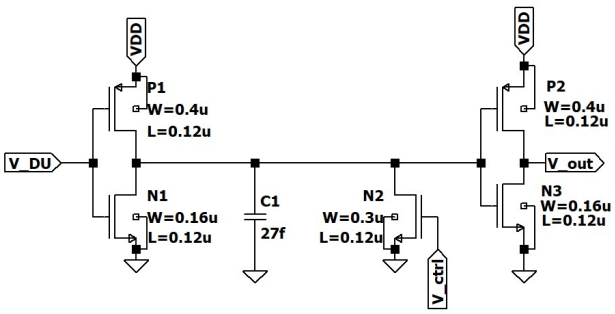


Fig. 19. Implemented delay unit

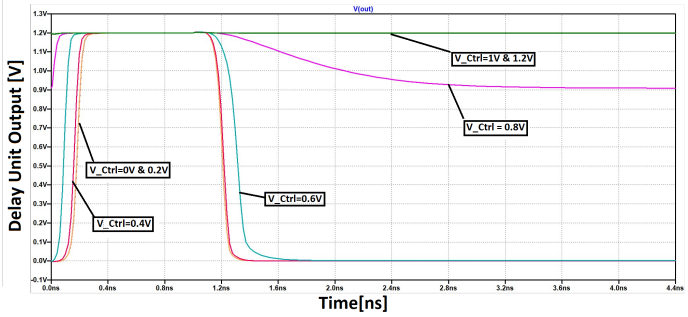


Fig. 20. Graph of delay unit output as a function of $V_{Ctrl}$ when the input is a 1ns pulse of 1.2V

measured from the first to the last stage of the VCDL was 1782ps. In addition to the 238ps delay between the clock signal and first stage, the total delay of the VCDL block was 2020ps. For this result, the charge pump settled at a value of $V_{Ctrl} = 350mV$. Compared to the delays shown in table V, the delays measured in table VII are larger than expected by at least 40ps. Part of this increase is due to the gate-drain

TABLE V
MEASURED DELAY PER DELAY UNIT FOR $0V \leq V_{Ctrl} \geq 1.2V$

| V_Ctrl[V] | Delay[ps] |
|---|---|
| 0 | 202.1 |
| 0.2 | 202.2 |
| 0.4 | 210.5 |
| 0.6 | 304.1 |
| 0.8 | _ |
| 1 | _ |
| 1.2 | _ |

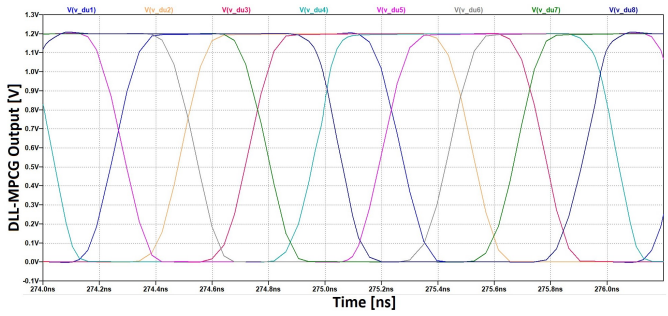


Fig. 21. DLL output showing 8 phases, where $V_{du1}$ is the output of the first delay unit and $V_{du8}$ is the output of the last delay unit.

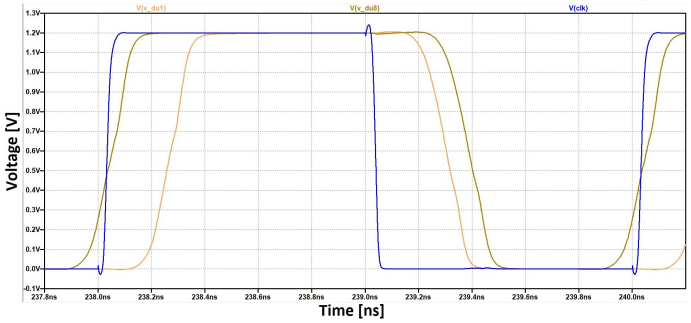


Fig. 22. showing the output of the first stage of the VCDL ($V_{DU1}$), the last stage of the VCDL ($V_{DU8}$) and the clock signal ($V_{Clk}$)

TABLE VI
PHASE DIFFERENCE OF DLL-MPCG STAGES RELATIVE TO THE FIRST PHASE

| Compared Phases | Expected Phase Difference | Measured Phase Difference |
|---|---|---|
| Phase 1 & Phase 2 | 45.0° | 46.3° |
| Phase 1 & Phase 3 | 90.0° | 92.3° |
| Phase 1 & Phase 4 | 135.0° | 138.2° |
| Phase 1 & Phase 5 | 180.0° | 184.0° |
| Phase 1 & Phase 6 | 225.0° | 229.5° |
| Phase 1 & Phase 7 | 270.0° | 274.7° |
| Phase 1 & Phase 8 | 315.0° | 320.8° |

TABLE VII
DELAY PER STAGE OF VCDL

| Delay Stage | Output Delay [ps] |
|---|---|
| 1 | 238 |
| 2 | 257 |
| 3 | 256 |
| 4 | 255 |
| 5 | 254 |
| 6 | 253 |
| 7 | 251 |
| 8 | 256 |

capacitance of the inverters of the next stage and the drain-bulk capacitance from the previous stage. This effect, however, accounts for at most 20ps of the added delay. It is uncertain at this point, the other reason(s) behind the increased delay in each stage.

The average power from the power supply to the DLL-MPCG was measured to be $P_{V_{DD}} = 538\mu W$ and the reference clock had an average power of $P_{V_{Clk}} = 145nW$ and an average current of $288pA$.

## IV. DISCUSSION

### A. Phase Accuracy & Power Usage

In order to compare the phase accuracy across topologies, the average error margin($EM_{avg}$) will be evaluated. This is calculated as follows,

$$EM_{avg} = \frac{\sum_{N=2}^{8} |\phi_{meas} - \phi_{exp}|}{k} \tag{20}$$

where $\phi_{meas}$ = measured phase; $\phi_{exp}$ = expected phase; N = phase number; k = total number of phases compared

The SR-MPCG generates equidistant phases that are $45°$ apart. In terms of the average error margin, this topology had

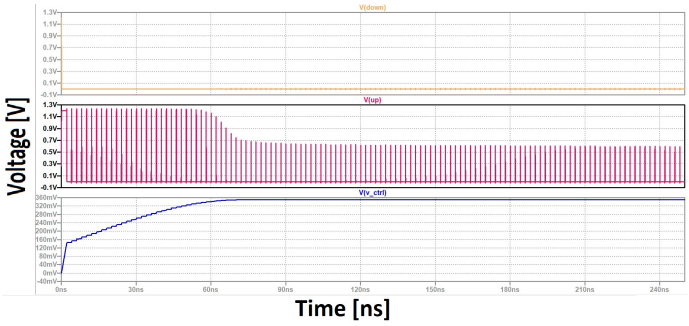


Fig. 23. **Top:** Charge pump input $V_{DWN}$; **Middle:** Charge pump input $V_{UP}$; **Bottom:** Charge pump output $V_{Ctrl}$

the lowest phase error ($EM_{avg} = 0.03°$) which makes it the topology with the highest phase accuracy.
In the case of the RC-MPCG, consecutive phases are separated by $45°$. In terms of phase accuracy, it had $EM_{avg} = 1.34°$. This value made it the topology with the second-highest phase accuracy when compared with the other topologies.
For the DLL-MPCG, similar to the RC-MPCG, phases are separated by $45°$. This topology, however, had the lowest phase accuracy with $EM_{avg} = 3.69°$.

In terms of power usage, the main area of focus was the power generated from the power supply to each topology ($P_{V_{DD}}$). The power supplied by the reference clock ($P_{Clk}$) in each topology was also measured, however, it was considered to have less weight in the comparison due to being magnitudes smaller and therefore not a true reflection of the power required to operate each topology.
SR-MPCG had the lowest power requirement with $P_{V_{DD}} = 191\mu W$ and $P_{Clk} = 2\mu W$. The RC-MPCG has the next lowest power requirements with $P_{V_{DD}} = 291\mu W$ and $P_{Clk} = 17\mu W$. Finally, the DLL-MPCG has the highest power requirements with $P_{V_{DD}} = 538\mu W$ and $P_{Clk} = 145nW$.

TABLE VIII
TOPOLOGY COMPARISON BY CRITERIA

| Criteria | SR-MPCG | RC-MPCG | DLL-MPCG |
|---|---|---|---|
| Phase Error [$EM_{avg}$] | $0.03°$ | $1.34°$ | $3.69°$ |
| Supply Power [$P_{V_{DD}}$] | $191\mu W$ | $291\mu W$ | $538\mu W$ |
| Clock-input Power [$P_{Clk}$] | $2\mu W$ | $17\mu W$ | $145nW$ |

In future,the fairness of the comparison could be improved by taking into account the optimisation of implemented circuits. In the current research, the DLL-MPCG was not fully optimised which means that some blocks may demand more power than necessarily required. Bearing this in mind, future research can improve on this work by making a comparison with fully optimised topologies.
Secondly, the difference in input signals between the RC-MPCG and the other topologies, made the research less fair as the clock signal in the DLL-MPCG and SR-MPCG were a square wave that was driving a buffer. On the other hand, the input to the RC-MPCG came from 2 sine waves.
Lastly, the SR-MPCG requires a much higher input clock frequency to operate, compared to the other topologies. Fairness can be improved if this difference is accounted for within the power usage comparison of future work.

### B. Limitations

The first consideration is the switching speed of the D flip-flops used in the SR-MPCG. Due to the MPCG being made of a chain of D flip-flops, if using a reference clock signal that has a period close to the flip-flop switching speed, the flip-flops struggle to switch as quickly as the clock signal. As a result of the setup and hold times being violated by the continuous switching, the generated phases produce distorted square waves.
The second limitation is the number of phases being extracted from the RC-MPCG and the circuit's loading. Due to the RC-MPCG inducing a phase shift via capacitors and resistors, the complexity of determining component values increases with the number of components in the RC block. The reason for this is that for a given frequency, a specific impedance value is necessary to achieve the desired phase shift. When that impedance is made of other impedances with their own requirements, changing component values greatly affects the output of other phases since the impedance for other phases will be affected. Similarly, the loading of the circuit adds impedance to the overall circuit. As such, the impedance at each phase fluctuates.
Lastly, it was noted that the DLL-MPCG had a total delay of 2020ps rather than 2000ps which may be attributed to a "deadband" in the PFD. When the phase difference between the inputs of the PFD gets small enough, the PFD is unable to distinguish this difference and temporarily malfunctions. It is fair to say that this 20ps difference from the expected total delay can be attributed to this effect. As such, the presence of a deadband in the PFD is a limitation to the phase accuracy of the DLL-MPCG.

## V. CONCLUSION

In this paper, an 8-phase, 500MHz output clock signal was generated from three clock generation schemes. Following an outline of the operation of each generation scheme, circuit performance was compared in terms of phase accuracy and power usage. It was determined that SR-MPCGs offer the highest phase accuracy among the three schemes.The RC-MPCG then had the second-highest phase accuracy. This was on the basis of having an error margin of $1.34°$ compared to the DLL-MPCG that had an error margin of $3.69°$. Furthermore, the evaluation of power usage showed that the SR-MPCG has the lowest power requirements with an input power of $P_{V_{DD}} = 191\mu W$. The highest power consumption was from the DLL-MPCG that had $P_{V_{DD}} = 538\mu W$. Lastly, it was noted that phase accuracy of the SR-MPCG is limited by the switching speed of implemented D flip-flops. On the other hand, the phase accuracy of the RC-MPCG is affected by the circuit's loading and the number of phases to be generated.
Based on the conducted research, a recommendation for future research would be to compare the quality of output signals generated by each topology over a set range of frequencies,

while being implemented in the same technology and having a load. By exploring this recommendation, the difference in frequency range per topology and the resistance of each system to noise, can be compared and evaluated.

## REFERENCES


[1] C.-K. K. Yang and M. Horowitz, "A 0.8-/spl mu/m cmos 2.5 gb/s oversampling receiver and transmitter for serial links," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 2015–2023, 1996.

[2] Z. Wang, Y. Zhang, Y. Onizuka, and P. R. Kinget, "Multi-phase clock generation for phase interpolation with a multi-phase, injection-locked ring oscillator and a quadrature dll," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1776–1787, 2022.

[3] X. Gao, E. A. M. Klumperink, and B. Nauta, "Advantages of shift registers over dlls for flexible low jitter multiphase clock generation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 3, pp. 244–248, 2008.

[4] A. Khashaba, A. Elkholy, K. M. Megawer, M. G. Ahmed, and P. K. Hanumolu, "A low-noise frequency synthesizer using multiphase generation and combining techniques," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 592–601, 2020.

[5] Y. Moon, J. Choi, K. Lee, D.-K. Jeong, and M.-K. Kim, "An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 377–384, 2000.

[6] P. Mane and S. Pawar, "An ultra low current mismatch charge pump and loop filter in 0.18um cmos process for low spur pll applications," *International Journal of Engineering Trends and Technology*, vol. 69, pp. 14–24, 06 2021.

[7] G. Ellis, "Chapter 9 - filters in control systems," in *Control System Design Guide (Fourth Edition)*, fourth edition ed., G. Ellis, Ed. Boston: Butterworth-Heinemann, 2012, pp. 165–183. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780123859204000096

[8] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Chapter 5: The CMOS Inverter*, second edition ed. Upper Saddle River, N.J: Pearson Education, 2003. [Online]. Available: https://books.google.nl/books?id=_7daAAAAYAAJ