A Method for Modeling the Dominant Parasitic Behaviour of a Chip Interface as a RLC-Network by Fitting onto Simulated s-Parameters

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***Abstract*—This paper presents a method for modelling the dominant parasitic behaviour of a package interface for an n-path filter/mixer chip, as a lumped element equivalent circuit. 3D electromagnetic (EM) simulation software is used to model the interface geometry and extract the parasitic s-parameters. These parameters are used to fit a lumped element equivalent circuit, such that the difference between the s-parameters of the RLC-network and the EM simulation is minimised. The RLC-model enables estimation of the package performance and gives insight into the dominant parasitic behaviour of the package parasitics. The method can be generalized to model a wide variety of IC interfaces.**

I. Introduction

The growth in usage of wireless communication has resulted in an increasingly high demand on the frequency spectrum. In the quest of designing faster, more linear and more efficient front-ends for software-defined radios (SDR), n-path filters have received a lot of attention over the past decade [1, 2]. By postponing the gain stages until after the mixer stage, these passive mixer-first topologies differentiate themselves from their active counterparts and improve their overall linearity and power consumption.

N-path filters use a switch capacitor network to create a band-pass filter around the switching frequency. Although the RC structure looks simple, the time-variant characteristics of the switches make mathematical analysis difficult without simplifications. In [3], a performance analysis is given. Figure 1 shows the topology and the frequency response of the filter, which is a periodic function.

Due to the ever-increasing demand on the frequency spectrum, N-Path filters are designed for increasingly high operating frequencies. Although the package around the integrated circuit and other sources of parasitics are small enough to be neglectable for frequencies beneath 1 GHz, they start to play a prominent role for higher frequencies, when their size is within an order of magnitude of the wavelength [4]. These parasitics are especially problematic for the performance of N-path filters/mixers. In [5], Darvishi *et al.* explain that the addition of parasitic capacitance will not only lower the centre frequency, but will also reduce the filter's gain. This can be intuitively explained by the fact that adding parasitic capacitance, there exists charge sharing by the base-band capacitors and the parasitic capacitance.

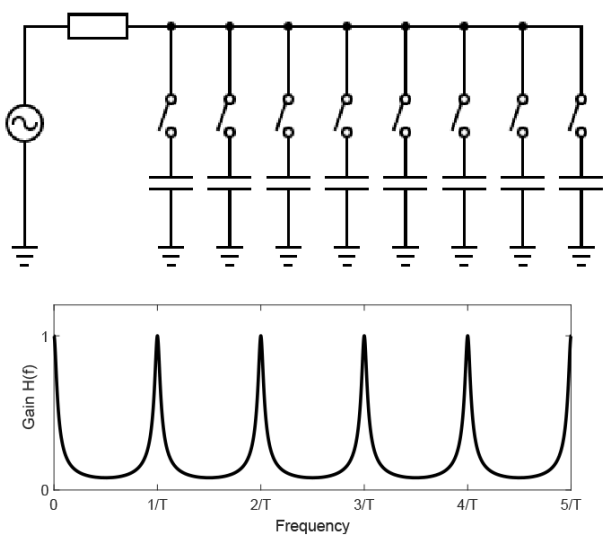

Fig. 1. Simplified Schematic of N-Path filter and frequency response [3, 6]

Methods are explored to mitigate the effects of these parasitics. However, to test the filter's performance, the integrated circuit (IC) needs to be connected to measurement equipment through an interface that introduces parasitics. Such an interface may consist out of the package and internals with among others the bond pads, bond wires and lead frames and the printed circuit board (PCB) with among others transmission lines, connectors and soldering pads.

A good model of the parasitics introduced by the interface is required to get a measure of the performance of the N-path filter/mixer. Only using three dimensional electromagnetic (3D EM) simulations, which result in s-parameters, can be useful enough to determine to what extent the interface degrades the filter's performance. Furthermore, to use the s-parameters when doing transient simulations, Broad Band SPICE (BB-SPICE) interpolation can be applied. This method uses a very large amount of ideal controlled voltage and current sources to accurately depict the s-parameters [7]. However, mapping the model to a passive RLC-circuit gives more insight into the parasitics themselves. Additionally, using simple RLC-networks over large BBSPICE networks will decrease the

computation time per simulation.

In this paper, a method is proposed to get an estimate of these parasitics over a wide frequency range and model the worst-case scenario as lumped elements. Ideally, due to the folding-back of signals every $Nf_{switching}$ onto the desired signal [8], the estimate should cover at least this band. So a 4-path filter ($N = 4$), with a switching frequency of $f_{switching} = 6$GHz should accurately model the parasitics until 24GHz.

The proposed method uses 3D EM simulation to determine the s-parameters of the interface. These EM simulated s-parameters are then used as a reference to extract the parasitic lumped elements. This is done by using a predetermined RLC-network of which the lumped elements are optimized with a global optimization tool, such that the circuit s-parameters are fitted onto the EM simulated s-parameters. The circuit as shown in Figure 5 is used in this paper to fit the parameters, but this circuit can be extended to achieve more accuracy.

In this paper the method is demonstrated by using the geometry model introduced in section II to retrieve the EM simulated s-parameters, using the in section III proposed circuit model and the in section IV method for parameter extraction. In section V, the s-parameters from the EM simulation are compared to the s-parameters from the proposed circuit model. Finally, in section VI, a conclusion is provided.

II. Interface Geometry

To get an idea of the parasitics in the interface between the measurement equipment and chip-die, 3D EM simulations are performed. For these simulations, a 3D model is made that approximates the geometry of the interface. The interface for an n-path filter will consist of at least the following components:

1) an RF-input, for in incoming RF-signal;
2) a Clock input, or LO-input;
3) some DC-inputs for power;
4) and the base-band output, for the downconverted and filtered signal output.

In Figure 2, an overview is given of the interface. Ideally, since the EM-simulations will be used as a reference, the geometry of the model should be as close to reality as possible. However, adding complexity to the model will result in more complexity in the s-parameter results. For simplicity, the decision was made to exclude the DC inputs and the base-band output from the 3D model, as well as the SMA Connectors and the 50Ω transmission lines. These factors are expected to have minimal impact on the s-parameters results, since they are either small and far away from the signal traces on the PCB, or can be assumed to be perfectly 50Ω. As result, a system with a package and a PCB with two transmission lines is modelled: one for the RF-in and one for LO-in.

The 3D model is made using Cadence Clarity 3D Solver. This software package is able to perform 3D electromagnetic simulations that result in s-parameters. Since bond wires play a key role in the interface parasitics, 2.5D planar EM solvers like sonnet are not used. In Cadence Clarity, there is an integrated tool to model bond wires.

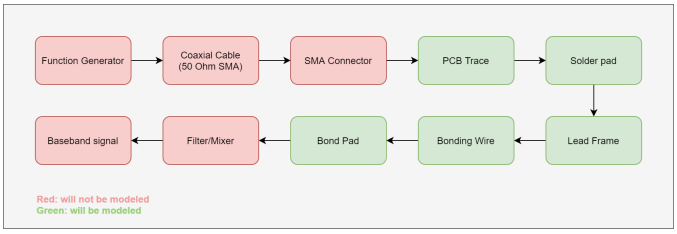

Fig. 2. Overview of the sub-components in the interface

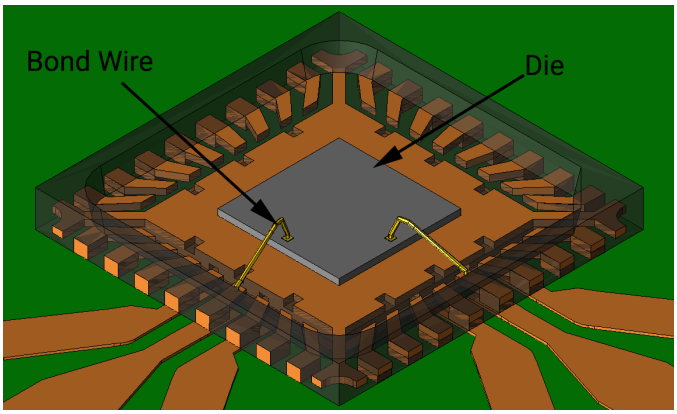

Fig. 3. 3D model of the Package with internals. Copper is displayed as brown, gold as yellow, package moulding material is black and silicon grey.

A. Modeling the Package

In [9], SEMPAC provides 3D drawings of their packages. A 32 lead 5mm x 5mm quad-flat no-leads (QFN) package is used in the model. In Figure 3, the 3D model of the package with its internals are shown. The golden bond wires were made with the build-in bond wire tool, whereby the standard values for length and height are used. For the bond pads, $100\mu m \times 100\mu m \times 10\mu m$ golden slabs are used.

For the die in the middle of the package, a $2mm \times 2mm \times 0.1mm$ silicon slab is used as a model. The slab is made of solid, intrinsic silicon. In reality, this slab is not solid silicon and not intrinsic, but for the purpose of modelling the RF behaviour outside of the die, this model will be sufficient.

B. Modeling the PCB

In Figure 4, part of the PCB model is shown. The model is based on the PCB designed by Purushothaman for [2] but heavily simplified. In [2], balanced signal traces are used. For simplicity, the model used here consists of two single-ended signal traces, which are microstrips with co-planar waveguides. Additionally, all extra traces for DC inputs and base-band outputs are left out of the model.

III. Proposed Circuit Model

In Figure 5, the proposed circuit model with electrical parameters (RLC) is shown. The model is based upon the

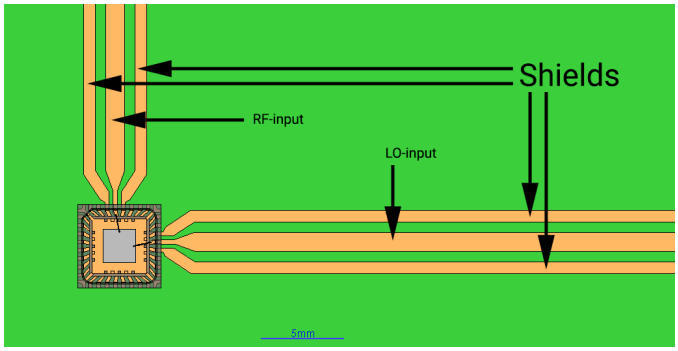

Fig. 4. 3D model of the PCB. The RF4 material is displayed in green, copper traces in brown.

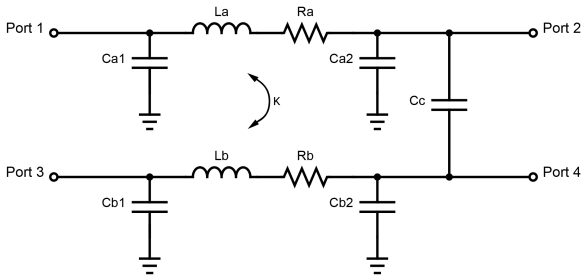

Fig. 5. Proposed circuit model

model used in [10], where H. Xue *et al.* propose a numerical method for extracting the electrical parameters for a similar RLC-model of a bond wire. The model is based on the widely-used π-model. If one ignores the capacitor C_c, it is easy to see that the network consists out of two separate transmission lines, one between port 1 and port 2 and one between port 3 and 4. These two lines represent the two transmission lines for RF-in and LO-in.

The capacitor C_c is used to model the coupled capacitance between the two input lines of the interface. Furthermore, k is the mutual inductance between L_a and L_b. The model may be extended with extra elements to provide for more accuracy in the end.

IV. Fitting the RLC-model onto the EM simulated S-parameters

To extract the parameter values from the EM simulated s-parameters, an optimization algorithm is used. The EM simulated s-parameters are simplified and used as a reference to optimize the circuit, such that it has approximately similar behaviour.

A. Approximating the Dominant Parasitic Behaviour

Due to multiple reflections of the signal around high-Q resonant structures within the geometry of the transmission line, the simulated s-parameters have ripple formation [11, 12]. These ripples are hard to include in an RLC-circuit since this would require a high degree of freedom and thus a large

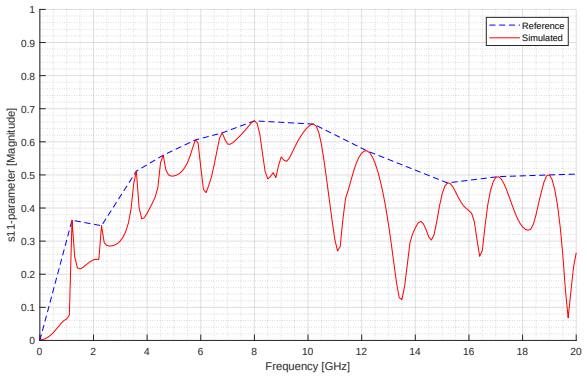

Fig. 6. Comparison between the S_{11}-parameters of the EM-simulation and the approximation over the top of the curves.

number of components. Since the goal is to have a simple and clear approximation of the parasitics, it was chosen to approximate the s-parameters with the worst-case scenario, i.e. the tops of the s-parameters.

In order to get a usable continuous curve from the peaks, straight line segments are plotted between the maxima of the s-parameters. Cadence Virtuoso ADE Assembler has a built-in function that can detect the peaks from an input waveform and return the X and Y coordinates of these peak points in the form of a waveform [13]. In Figure 6, the approximation compared to the s-parameter is plotted. With this approximation, it is important to correctly set up the tolerances, to filter out the intermediate peaks such as the one around 14GHz. The resulting curve will be referred to as 'reference curve' or 'reference' in further discussions.

B. Fitting Circuit Parameters to Approximate S-Parameters

To fit the circuit parameters the RLC-circuit shown in Figure 5, such that the computed s-parameters fit the reference curve, an optimization algorithm is used. This was done by minimizing the difference between the reference s-parameters and the computed s-parameter result from the circuit using the least-squares method. Therefore, the function that needs to be minimized is as follows:

$$S_{xy\_error} = \sum_n \left| S_{xy\_CIR}[n] - \texttt{peak}\left(S_{xy\_EM}[n]\right) \right|^2 \quad (1)$$

where S_{xy_CIR} is an s-parameter computed from the circuit diagram, S_{xy_EM} is an imported s-parameter from the EM simulation and `peak[f(x)]` results in a waveform consisting of straight line segments between the peaks of the magnitude of function `f(x)`.

S_{xy_error} in Equation 1 is a function of the circuit component values. By using the global optimization toolbox in Cadence Virtuoso ADE Assembler, the values can be tweaked such that the error given by the equation is minimized. This optimization method can be used with any RLC circuit. If more accuracy is desired, the circuit model can be extended with extra components.

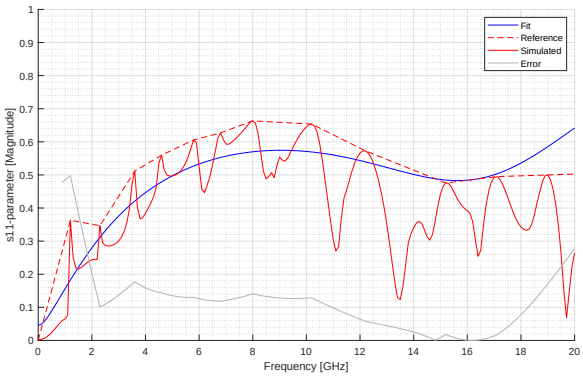

Fig. 7. A plot of s-parameters S_{11} of the EM simulation compared to the RLC-Model

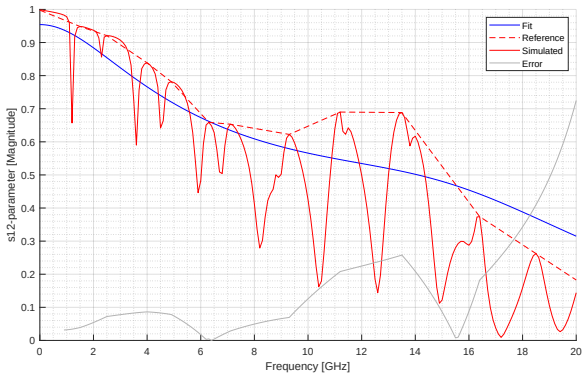

Fig. 9. A plot of s-parameters S_{12} and S_{21} of the EM simulation compared to the RLC-Model

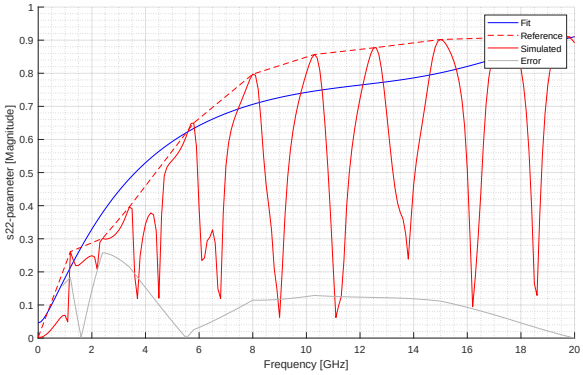

Fig. 8. A plot of s-parameters S_{22} of the EM simulation compared to the RLC-Model

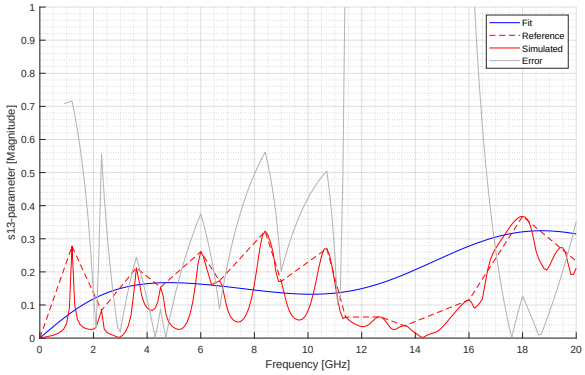

Fig. 10. A plot of s-parameters S_{13} of the EM simulation compared to the RLC-Model

V. Results

A 3D EM simulation of an interface between an integrated circuit and measurement equipment result in the s-parameters as shown in Figure 6. The proposed method in combination with a global optimisation algorithm, using the reference s-parameters (as discussed in subsection IV-A) and the circuit schematic as shown in Figure 5, result in the circuit parameters as shown in Table I. The circuit is then simulated using the resulting parameters and the scatter parameters are computed.

Looking at the network with the values in Table I, it seems that the dominant parasitic capacitance is at the package side of the network, i.e. C_{a2}, C_{b2} and the coupled capacitance C_c in Figure 5. The self-capacitances C_{a2} and C_{b2} are around 0.6pF. The coupled capacitance is around 0.45pF. Furthermore, there are parasitic inductances L_a and L_b. These inductances are both around 0.4nH. Additionally, there is a coupled inductance between the transmission lines, with a coupling factor of 0.23. However, in the case of the n-path filter, as discussed in the introduction and [5], the capacitances will be the most problematic for the performance of the filter.

TABLE I
Circuit Model Values

Parameters	Optimised Value	Parameter	Optimised Value
C_{a1}	220fF	L_a	410pH
C_{a2}	620fF	L_b	420pH
C_{b1}	220fF	k	0.23
C_{b2}	630fF	R_a	4.8Ω
C_c	450fF	R_b	4.6Ω

In Figure 7, the S_{11} parameters are plotted. The dashed line represents the computed s-parameters from the RLC-Model and the solid line the EM simulated one. It is evident that the proposed method is able to produce the S_{11} parameter with reasonable accuracy. When comparing the reference s-parameters to the RLC-Model, the error stays within 20% for frequencies larger than 2GHz. Similarly, in Figure 8, the S_{22} parameters are plotted. Again, comparing them to the reference function gives an error of 30% or less.

The transmission coefficients S_{12} and S_{21} are plotted. Since the networks only contain reciprocal elements, those parameters are equal. Although the peak around 14GHz is not completely covered, there is a smaller peak visible. The error between the reference and the RLC-Model stays within 30% until 18GHz.

The coupling between the transmission lines, i.e. S_{13}, is plotted in Figure 10. This parameter also follows the trend of the EM simulated reasonably well. However, there are large errors between approximately 8 and 17GHz. However,

although these errors are big, the overall trend is followed.

Overall, within the 20GHz range, the method is able to model the dominant parasitic behaviour of the interface with reasonable accuracy. However, for the purpose of modelling an interface for an n-path filter, this range is a bit too small. Nonetheless, adding components to the RLC-network can increase the degree of freedom and thus the overall accuracy.

VI. Conclusion

In this paper, a method for modelling the dominant parasitics behaviour of an interface between an integrated circuit and measurement equipment is presented. Such an interface may consist out of PCB with traces and ground pads and a package with lead frames, bond wires and bond pads. The proposed method uses 3D EM simulation to determine the s-parameters of the interface. These EM simulated s-parameters are then used as a reference to extract the parasitic lumped elements. This is done by using a predetermined RLC-network of which the lumped elements are optimized with a global optimization tool, such that the circuit s-parameters are fitted onto the EM simulated s-parameters.

The method results in an RLC circuit of which the electronic parameters are determined, such that the s-parameters computed from the circuit approximate the dominant parasitic behaviour of the chip interface. The circuit, consisting out of ten components as given in Figure 5, results in a model of which the S_{11}, S_{12}, S_{21}, S_{22} and S_{13} parameters are shown to track the envelope of the EM simulated s-parameters up to 20GHz with reasonable accuracy. For the purpose of modelling an interface for an n-path filter, this range is a bit too small. However, expanding the RLC-network can increase the overall accuracy.

The model can be implemented with SPICE networks in simulations of, for example, the integrated circuit model. Although the s-parameters from the EM simulation can often be implemented too, using for example BBSPICE, the RLC model might give more insight into the parasitics of the interface. For the geometry of the interface used in this paper, the method resulted in a dominant parasitic of approximately 0.6pF and a self-inductance of 0.4nH.

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