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Faculty of Electrical Engineering, Mathematics & Computer Science

Influence of Control and Output-Quality Constraints on the Scalability and Optimization of Multi-branch Multi-level Flying Capacitor Converters

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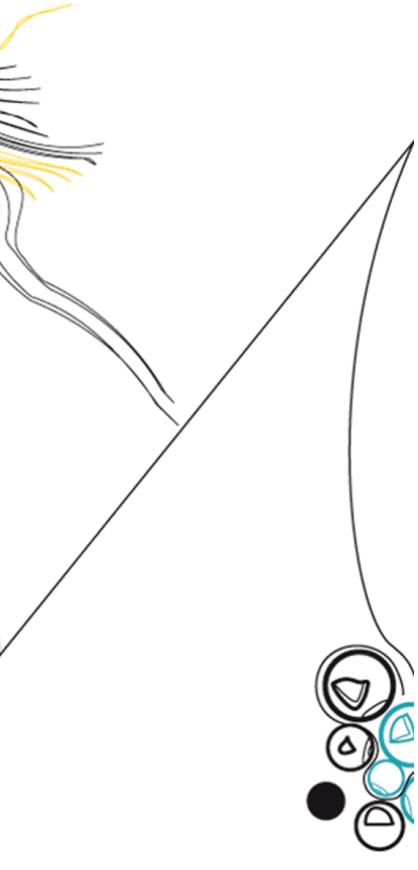
M.Sc. Thesis

August 2022



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Influence of Control and Output-Quality Constraints on the Scalability and Optimization of Multi-branch Multi-level Flying Capacitor Converters

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***Abstract*—The usage of multi-branch multi-level Flying Capacitor Converters (FCCs) is increasing, driving the need for fundamental scaling laws relating constraints (i.e. output quality, control bandwidth, and lifetime) to design variable limits in the context of system optimization. In contrast to other multi-objective design papers, not just the design variables (number of levels, branches, and parallel FETs, switching frequency, and output filter), but also the constraints are varied to identify these relations. The basis for the analysis is a gradient amplifier for Magnetic Resonance Imaging (MRI) systems, an application that can benefit from the advantages the FCC topology brings (i.e. low noise, and easily scalable power output). It is shown how the output quality and control bandwidth constraints provide design limits for the FCC designs through the effective switching frequency, a combination of the switching frequency, number of levels, and the number of branches, but not through these design variables directly. The relations between the three constraints and costs are also discussed, furthermore, it is shown that the most cost-effective designs (for MRI) have a 40% to 50% margin on the rated semiconductor voltage and current, which is largely driven by the lifetime constraint.**

I. Introduction

The usage of multi-branch multi-level Flying Capacitor Converters (FCCs) is increasing, with more publications implementing such converters [1]–[4]. The applications range from inverters for electric aircraft [1] to PV inverters and PFC rectifiers [4]. This is to little surprise as this multi-level topology features advantages such as reduced switching losses (snubberless) and low harmonic content on the generated output voltage, while only requiring a single DC source [5]. Nonetheless, an overview of how different FCC design parameters (**Fig. 1**) such as the number of levels M, the number of branches N, the number of parallel FETs k, or the switching frequency f_{sw}, are limited by design constraints is not yet covered. This work focuses on the relationship between these design parameters and constraints related to output quality, control bandwidth, and lifetime, filling in this gap. These relations lead to design space limits, bounding the design variables in the context of system optimization. Furthermore, their effect on cost-based optimization is also covered.

This work on FCCs specifically focuses on the application of Magnetic Resonant Imaging (MRI) gradient amplifiers. Three such amplifiers drive the three large gradient coils ($R_{\mathrm{load}} \approx 100\,\mathrm{m\Omega}$ and $L_{\mathrm{load}} \approx 400\,\mu\mathrm{H}$ each) for the X-, Y-, and Z-axis with large peak currents $>1000\,\mathrm{A}$ with a high change rate $>4000\,\mathrm{A/ms}$. The latter requires a large output voltage $>2000\,\mathrm{V}$. Which combined with the peak current, results in a very high peak output power of $>2\,\mathrm{MW}$ for such amplifiers. In addition, to achieve clear images, the output voltage and current need to be generated with high precision and low harmonic content. This makes the FCC topology a great fit for this application, benefiting from the modularity of the multi-level and multi-branch design for the high power output, combined with its low noise.

For the application in MRI, the considered design constraints are output quality in the form of RMS output voltage ripple, control bandwidth, defined as a function of output filter cut-off frequency, and amplifier lifetime, for which the semiconductors are the limiting factor. What separates this work from other multi-objective design papers is that not just the design variables, but also the constraints are varied to identify relations and fundamental scaling laws for the FCC topology. Besides the already mentioned design variables, M, N, k, and f_{sw}, the output capacitors $C_{\mathrm{DM,[A,B]}}$ (**Fig. 1**) are also variable. However, the filter inductors $L_{\mathrm{DM},i\mathrm{[A,B]}}$, and flying capacitors $C_{\mathrm{FC}i}$ are fixed based on a maximum allowed ripple current and voltage respectively. To achieve an equal voltage load across all the switches, the flying capacitor voltages are defined following,

$$V_{\mathrm{FC}i} = \frac{i}{M-1} \cdot V_{\mathrm{bus}} \quad \text{with } i \in [1, \ldots, M-2]. \tag{1}$$

The choice of semiconductor switches is limited to three Silicon Carbide (SiC) MOSFETs with low on-resistances and a varying blocking voltage capability of $650\,\mathrm{V}$, $900\,\mathrm{V}$, and $1200\,\mathrm{V}$. Each amplifier consists of an A and B side, generating opposite voltages across the load. Each side can contain multiple parallel multi-level FCC cells with filter inductors, all connected to a single set of output capacitors, as shown in **Fig. 1**.

First, the general operation of FCC converters and the design variables are explained for both a $M = 3$-level FCC cell with a single branch, and one with $N = 3$ branches as examples in **Section II**. Finishing this section off is a summary of all design variables and constants in **Section II-E**. Next, the loss models, worst-case operating conditions, and costs, for each of the components; semiconductors, inductors, and capacitors, are discussed in **Section III**. The constraints related to output quality, control bandwidth, and lifetime

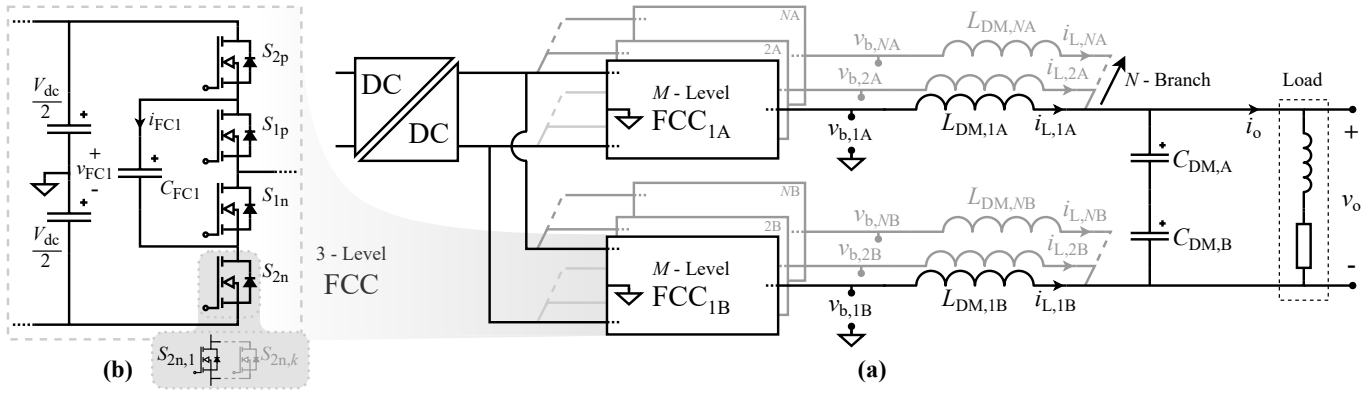


Fig. 1. a) FCC-based gradient amplifier topology with N parallel branches that each contain an M-level FCC cell. b) Example of a $M = 3$ level FCC cell where 'k' indicates the number of parallel FETs per switching element.

are explained in relevant subsections throughout **Section II** and **Section III** but are also summarized for clarity in **Section III-A**. Following this, the found relations, scaling laws, and cost optimization are covered in **Section IV**. Finally, the validation of the semiconductor loss and thermal model using an experimental prototype 4-Level 1-Branch FCC operating at $2400\,\mathrm{V}$ is detailed in **Section V**.

II. Operating Principle of FCCs

This section outlines the operating principle of FCCs considering constant output current $i_\mathrm{o}{}^*$ and using the switching states and waveforms depicted in **Fig. 2**. Understanding these waveforms is required to be able to consider the output quality and control-related constraints of the amplifier, discussed in **Section II-A** and **Section II-B** respectively. The shown waveforms in **Fig. 2** are modelled using a Fourier-series representation in the frequency-domain in MATLAB [6]. The time-domain representation that is shown here is the result of an inverse Fourier transform. A smoothing filter is applied to eliminate the Gibbs phenomenon from the waveforms to aid the visual representation.

The operating principle of an FCC is explained for a 1-branch 3-level FCC in **Section II-A** and for a 3-branch 3-level FCC in **Section II-B**, with a constant output current $i_\mathrm{o}{}^*$ and constant output voltage $v_\mathrm{o}{}^*$. Afterwards, in **Section II-C**, the relationship between the filter cut-off frequency and control bandwidth is defined. Based on this, the output quality and control-related constraints are summarized in **Section II-D**. Finally, in **Section II-E**, an overview of all the design variables, design constants and their value (ranges) is presented.

A. 3-Level 1-Branch FCC

Fig. 2(a) shows the different switching states of a 1-branch (single cell) 3-level FCC during positive output current i_o over a single switching period of T_sw. Two, $(M-1)$, complementary switching pairs S_2p-S_2n and S_1p-S_1n are shown, each driven by a PWM signal with a duty-cycle D calculated using:

$$\begin{aligned} D &= \frac{{v_\mathrm{o}}^*}{V_\mathrm{dc}\cdot 2} + 0.5 \\ D &= \frac{v_\mathrm{b,mean}}{V_\mathrm{dc}} + 0.5. \end{aligned} \tag{2}$$

The PWM signals of the two pairs are phase shifted by $T_\mathrm{sw}/(M-1)$ with respect to each other, where $T_\mathrm{sw} = 1/f_\mathrm{sw}$ is the switching period of each of the switching elements and f_sw the switching frequency. Combined the switch pairs generate a v_b voltage at a frequency of

$$f_\mathrm{sw,branch} = f_\mathrm{sw}\cdot(M-1) = \frac{1}{T_\mathrm{sw}/(M-1)}, \tag{3}$$

with three $(M = 3)$ possible voltage levels dependent on the dutycycle D following:

$$v_\mathrm{b} = \begin{cases} -V_\mathrm{dc}/2 & \text{if } D = 0 \\ [-V_\mathrm{dc}/2, 0] & \text{if } 0 < D < 0.5 \\ 0 & \text{if } D = 0.5 \\ [0, V_\mathrm{dc}/2] & \text{if } 0.5 < D < 1 \\ V_\mathrm{dc}/2 & \text{if } D = 1 \end{cases} \tag{4}$$

Considering constant positive output current $i_\mathrm{o}{}^*$ and branch voltage $v_\mathrm{b,mean} = (D-0.5)\cdot V_\mathrm{dc}$ at $D = 0.6$, **Fig. 2(b)** illustrates the corresponding time intervals and waveforms of inductor current $i_\mathrm{L,1A}$, branch voltage $v_\mathrm{b,1A}$, flying capacitor current $i_\mathrm{FC,1A}$ and voltage ripple $\widetilde{v}_\mathrm{FC,1A}$, and the semiconductor states.

In the first time interval $[0,\ t_0]$, S_2p and S_1n are conducting. As v_FC1 is approximately equal to $V_\mathrm{dc}/2$ (following (1)), this results in a net branch voltage $v_\mathrm{b,1A} \approx 0\,\mathrm{V}$ resulting in the declining inductor current $i_\mathrm{L,1A}$ (as v_o is positive). Simultaneously, the positive current through the flying capacitor C_FC leads to the increase of $\widetilde{v}_\mathrm{FC1,1A}$. Next, the conduction state of S_1p and S_1n flip at t_0, causing $i_\mathrm{L,1A}$ to increase due to $v_\mathrm{b,1A}$ rising to $V_\mathrm{dc}/2$. As a result, the inductor current has a ripple with a peak-to-peak amplitude of $i_\mathrm{L,pp}$. Between t_0 and t_1, the flying capacitor voltage v_FC1

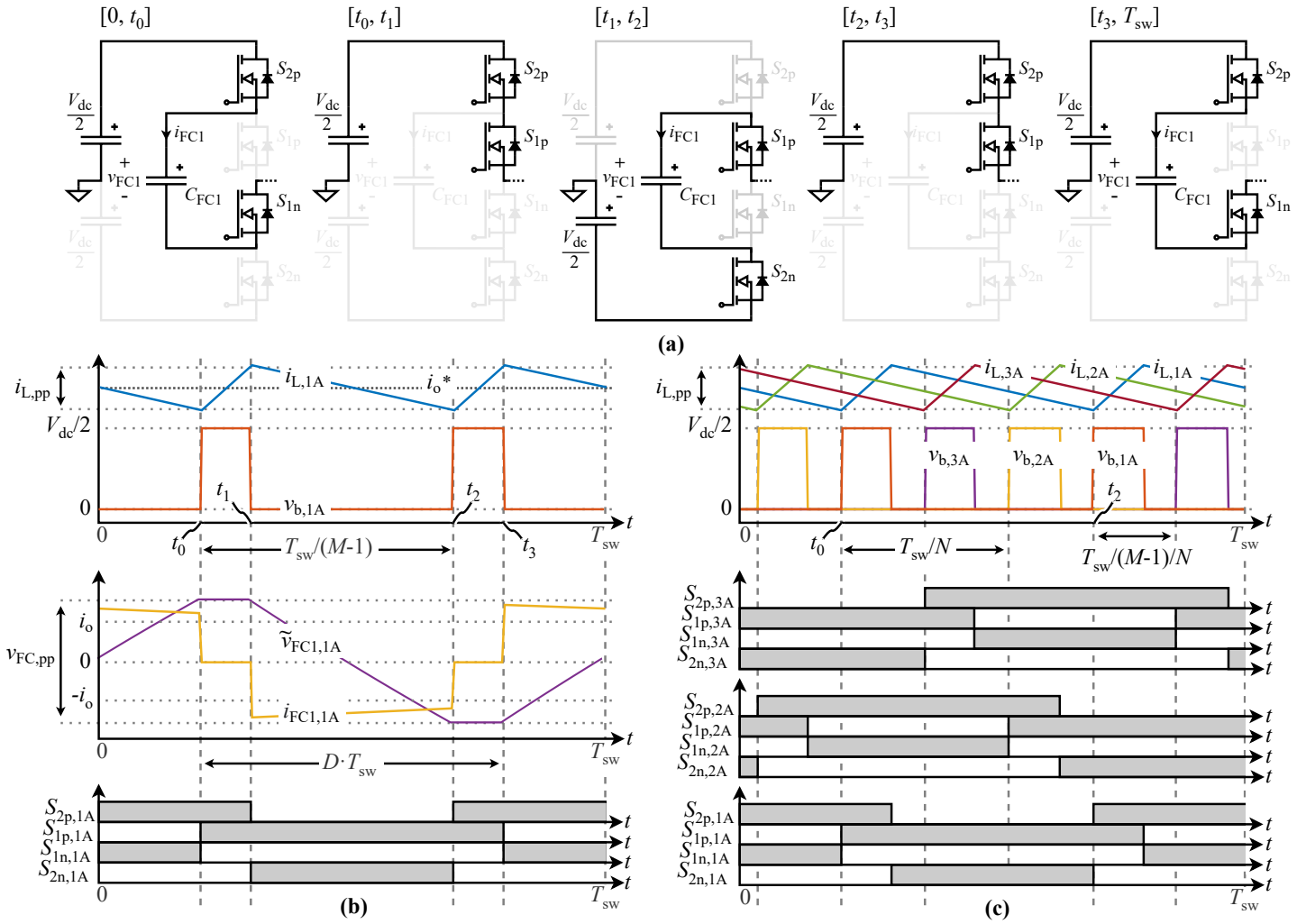


Fig. 2. **(a)** Switching states of a 1-branch (single cell) 3-level FCC considering constant positive output current $i_o{}^*$ at $D = 0.6$. **(b)** Corresponding time intervals and waveforms of inductor current $i_{L,1A}$, branch voltage $v_{b,1A}$, flying capacitor current $i_{FC,1A}$ and voltage ripple $\widetilde{v}_{FC,1A}$, and semiconductor conductor states. **(c)** Waveforms of inductor currents, branch voltages, and semiconductor conductor states for similar conditions as in **(a,b)** but now considering a 3-branch 3-level FCC, also illustrating the interleaving principle.

is constant following that C_{FC1} is not conducting. It only starts discharging again during the next time step from t_1 to t_2. Here the conduction state of S_{2p} and S_{2n} are flipped, once again resulting in a approximately 0 V branch voltage $v_{b,1A}$. The next time step, $[t_2,\ t_3]$, is almost identical to $[t_0,\ t_1]$ with the only difference being the flying capacitor voltage, which has a peak to peak value of $v_{FC,pp}$. Finally, the time step $[t_3,\ T_{sw}]$ is identical to the first, making the sequence a loop.

There are two important things to note. Firstly, as previously noted, the branch voltage and current have double the switching frequency compared to the semiconductors according to (3). And secondly, v_{FC1} is only approximately equal to $V_{dc}/2$ and has a ripple of $v_{FC,pp}$ around this value. This directly affects the branch voltage $v_{b,1A}$ and can propagate to the output voltage v_o of the amplifier. The impact of this flying capacitor ripple $v_{FC,pp}$ is inversely proportional to C_{FC}, which is shown in **Figs. 3(a,b)**. First the output voltage ripple $\widetilde{v}_o$ is displayed for three different flying capacitances over a single period with dutycycle $D = 0.5$ in **Fig. 3(a)**. This dutycycle was carefully chosen as here the inductor ripple of the two amplifiers (FCC_{1A} and FCC_{1B}) cancel each other out, leaving only the FC-related ripple. This is most clearly shown in **Fig. 3(b)** where the RMS output voltage ripple $\widetilde{v}_{o,RMS}$ is presented as a function of dutycycle D for the same three flying capacitances. Implying that for this $M = 3$-Level FCC, the ripple of the summed inductor currents dominates $\widetilde{v}_{o,RMS}$ at $D \neq 0.5$. **Fig. 3(c)** will be discussed in **Section II-B**.

The RMS output voltage ripple is used as a measure of output quality and acts as a design constraint. For example, a given FCC amplifier design is required to have a ripple below $\widetilde{v}_{o,RMS,max}$ throughout all its possible operating conditions. It is important to note that bus voltage ripple, and its effect on the output voltage ripple, is not considered.

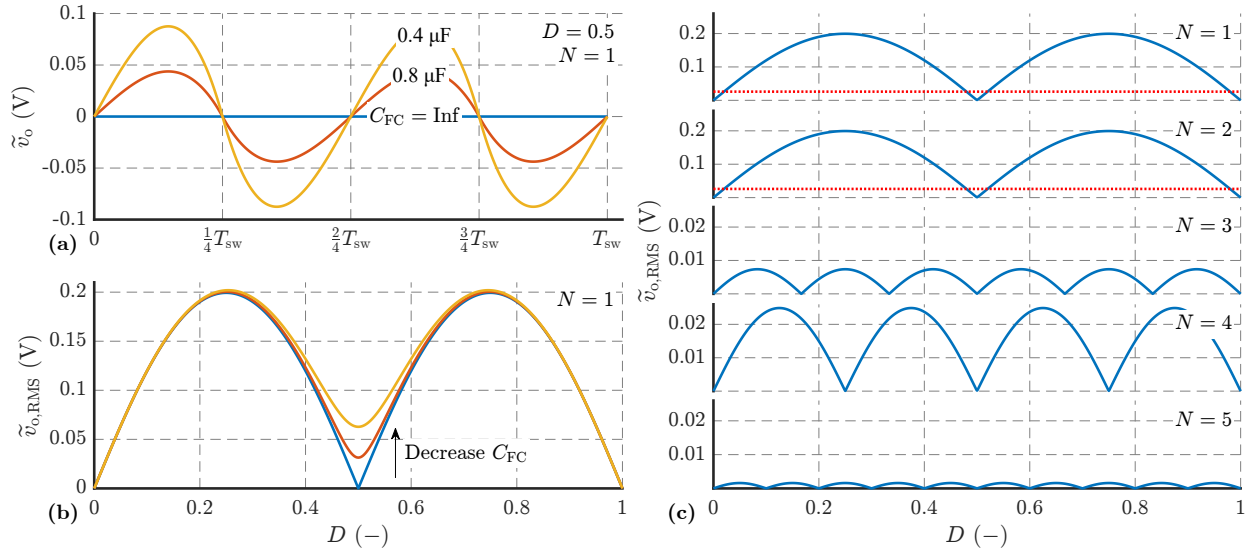


Fig. 3. Simulation results for a 3L1B FCC: **(a)** output voltage ripple $\widetilde{v}_o$ at $D = 0.5$ for three values of C_{FC} and **(b)** RMS output voltage ripple $\widetilde{v}_{o,RMS}$ as a function of dutycycle D for the same three values of C_{FC}. **(c)** RMS output voltage ripple $\widetilde{v}_{o,RMS}$ as a function of dutycycle D for an $M = 3$-Level, $N = [1, \ldots, 5]$-Branch FCC. The output filter is identical in all cases. Note the change in scale of the Y-axis for the bottom three plots, they are zoomed in by a factor of 10 for visibility. The red dotted line is equal to the top of the bottom three plots.

B. 3-Level 3-Branch FCC and Interleaving Principle

Fig. 2(c) illustrates waveforms of inductor currents $i_{L,[1,2,3]A}$, branch voltages $v_{b,[1,2,3]A}$, and semiconductor conductor states for similar conditions as in **Figs. 2(a,b)**, i.e. considering constant positive output current $i_o{}^*$ and output voltage $v_{b,mean}$ at $D = 0.6$, but now for an FCC with $N = 3$ parallel connected 3-level branches. Note that the waveforms and conduction states belonging to the first branch 1A are identical to the ones shown in **Fig. 2(b)**. From the semiconductor conduction states, it is visible how the three different branches are phase-shifted by $T_{sw}/3$ with respect to each other, which, when expressed in general terms, represents a phase shift of T_{sw}/N. Combining this with the frequency doubling effect from (3), an effective (switching) frequency of the summed branch current ($\sum (i_{L,[1,2,3]A})$) equal to

$$f_{sw,eff} = f_{sw} \cdot (M-1) \cdot N = \frac{1}{T_{sw}/(M-1)/N} \tag{5}$$

is obtained for any case where

$$(M-1) \bmod N \neq 0 \ \wedge \ N \bmod (M-1) \neq 0 \tag{6}$$

holds. (6) states that the number of levels minus 1, $(M-1)$, and the number of branches, N, can not be integer multiples of each other for (5) to be valid. In cases where (6) does not hold, the frequency doubling effects of the levels and branches will (partially) cancel each other out. Therefore, such cases will rarely result in optimal designs. This effect is shown in **Fig. 3(c)**. Here the RMS output voltage ripple $\widetilde{v}_{o,RMS}$ is again shown as a function of dutycycle D, just like in **Fig. 3(b)**. But now the number of branches N is varied between $N = 1$ and $N = 5$ to show the effect of (6). In general, the number of peaks in the harmonics plot is equal to $(M-1) \cdot N$, and as N increments, the ripple reduces. This reduction is to be expected given an increase in effective switching frequency while the filter remains constant. However, as can be seen, here both $N = 2$ and $N = 4$ show unexpected behavior. Incidentally these are two cases where (6) does not hold.

There is a potential solution to the frequency doubling cancellation, however, it comes with its own downside. Currently, each level is phase shifted by $T_{sw}/(M-1)$ and every branch by T_{sw}/N. If instead the branches are shifted by $T_{sw}/(M-1)/N$, this cancellation would no longer occur. The downside to this approach is that the voltage ripples introduced on the bus voltage by each of the branch input currents no longer cancel each other out. It is therefore not considered any further.

C. Filter Cut-Off Frequency and Control Bandwidth

The effective switching frequency $f_{sw,eff}$ is particularly relevant for the output filter of the amplifier. The filter inductance L_{DM} is defined by the maximum voltage across the inductor $V_L = V_{bus}/(2 \cdot (M-1))$, the conduction time at 50% dutycycle to achieve maximum ripple, $t_{on,50\%} = 1/(2 \cdot (M-1) \cdot f_{sw})$, and the maximum allowed inductor current ripple $I_{L,pp,max}$ as

$$L_{DM} = V_L \cdot \frac{t_{on,50\%}}{I_{L,pp,max}} = \frac{V_{bus}}{4 \cdot (M-1)^2 \cdot f_{sw} \cdot I_{L,pp,max}}. \tag{7}$$

The filter capacitors C_{DM} are left as design variables. Combined L_{DM} and C_{DM} define the cut-off frequency of the filter as

$$f_c = \frac{1}{2\pi\sqrt{\frac{L_{DM}}{N} \cdot C_{DM}}}, \tag{8}$$

assuming $L_{DM,[1,\ldots,N][A,B]} = L_{DM}$ and $C_{DM,A} = C_{DM,B} = C_{DM}$. It should be noted however that in any practical design, the filter inductances are never precisely equal and if not corrected for, are another source of output voltage ripple.

Both the effective switching frequency $f_{\mathrm{sw,eff}}$ and the filter cut-off frequency f_{c} affect the possible control bandwidth B_{control} of the amplifier. The control bandwidth threshold is known as the control constraint and is discussed next.

The conventional way to define bandwidth is to analyze the transfer function from the input of the controller to the output of the amplifier. But given the sheer number of possible amplifier designs within the optimization, it is simply infeasible to design (a set of) controllers that cover every option. Nevertheless, it is assumed that the control bandwidth threshold, $B_{\mathrm{control\ threshold}}$, the maximum attainable control bandwidth of a design, is linearly dependent on the minimum filter cut-off frequency $f_{\mathrm{c,min}}$:

$$B_{\mathrm{control\ threshold}} = \frac{f_{\mathrm{c,min}}}{r_{\mathrm{control\ ratio}}}. \tag{9}$$

This holds for positive values of $r_{\mathrm{control\ ratio}}$ and only in cases where $f_{\mathrm{sw,eff}} \gg f_{\mathrm{c}}$. The constant $r_{\mathrm{control\ ratio}}$ is based on an actual FCC controller design.

D. Output Quality and Control Constraint

Until now, the output quality and the control constraint have only been discussed separately, however, they are related. The output quality is defined by the maximum RMS ripple on the output voltage of the amplifier, $\widetilde{v}_{\mathrm{o,RMS,max}}$, which can be reduced by, among others, increasing the output filter capacitance. This has the side effect of lowering the cut-off frequency f_{c}. The control bandwidth threshold, $B_{\mathrm{control\ threshold}}$, which is known as the control constraint, is directly related to the cut-off frequency through (9). In other words, increasing the filter capacitance not only lowers the output voltage ripple (improving the output quality), it also lowers the cut-off frequency and with it the control bandwidth threshold. The trade-off between the output quality and the control bandwidth will limit the number of valid designs.

E. Design Variables and Constants

To summarize, the FCC amplifier has 5 design variables: M, N, k, f_{sw}, and C_{DM}. These variables have all been limited to a discrete set of options, the range of which is listed in **Table I(a)**. Besides these design variables, there are also two design constants related to the peak to peak flying capacitor voltage ripple $v_{\mathrm{FC}i,\mathrm{pp}}$, and the peak to peak filter inductor current ripple $i_{\mathrm{L,pp}}$ (see **Fig. 2(b)**).

An ideal 3-Level FCC with infinitely sized $C_{\mathrm{FC}i}$ operating at $D = 0.5$ has no ripple on the branch voltage (like shown in orange, **Fig. 4(a)**). However, in realistic scenarios, the FC voltage ripple will be visible on the branch voltage v_{b}. This FC related ripple $\widetilde{v}_{\mathrm{b,FC\text{-}related}}$ is presented for $M = [3, 5, 7]$-Level FCCs in **Fig. 4**. Due to how the different FCs, with each a different capacitance, are interleaved into the conduction path to charge and discharge, the ripple waveform becomes more complex for $M > 3$ FCCs. To keep the comparison between various numbers of levels fair, a maximum FC related ripple is defined $V_{\mathrm{b,FC\text{-}related,pp,max}}$ at $D = 0.5$ (a common dutycycle for MRI load profiles, **Section III-B**) to dimension the individual $C_{\mathrm{FC}i}$. The result of this is visible in **Fig. 4** where the maximum peak-to-peak ripple is independent of the number of levels. Finally, this reduces the differences in effect on $\widetilde{v}_{\mathrm{o,RMS}}$.

TABLE I
FCC AMPLIFIER DESIGN VARIABLES AND CONSTANTS

(a) Design Variables

Symbol	Range	#	Design variable
M	$[3, 4, \ldots, 8]$	6	Number of levels
N	$[1, 2, \ldots, 20]$	20	Number of branches
k	$[1, 2, 3]$	3	Number of parallel FETs
f_{sw}	$[1\,\mathrm{kHz}, 3.9\,\mathrm{kHz}, \ldots, 100\,\mathrm{kHz}]$	35	Switching frequency
C_{DM}	$[1\,\mathrm{nF}, 1.3\,\mathrm{nF}, \ldots, 1\,\mu\mathrm{F}]$[a]	30	Filter capacitance

[a] Contrary to the other variables, this range is on a logarithmic scale

(b) Design Constants

Symbol	Value	Design constant
$V_{\mathrm{b,FC\text{-}related,pp,max}}$	10 V	Maximum FC related voltage ripple @ $D = 0.5$
$r_{\mathrm{L,pp,max}}$	25%	Relative maximum inductor current ripple

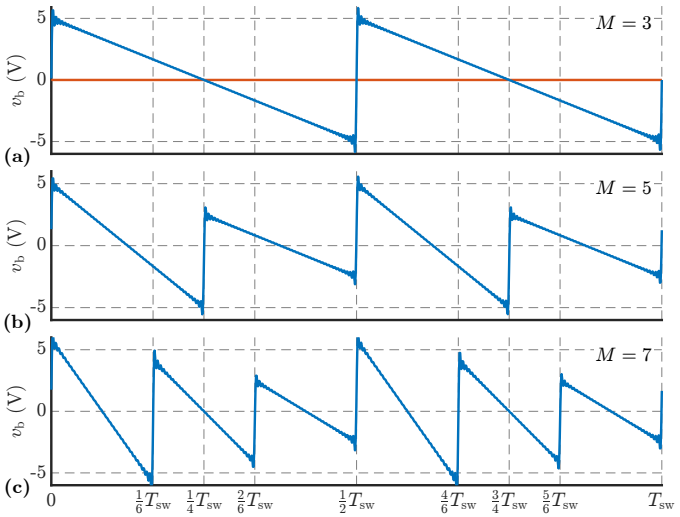


Fig. 4. Branch voltage v_{b} over time of a $M = [3, 5, 7]$-level FCC operating at $D = 0.5$ to show only the FC related ripple $\widetilde{v}_{\mathrm{b,FC\text{-}related}}$: **(a)** $C_{\mathrm{FC1}} = \mathrm{Inf}$ (orange) and **(a,b,c)** properly dimensioned $C_{\mathrm{FC}i}$ (blue) such that $V_{\mathrm{b,FC\text{-}related,pp,max}} = 10\,\mathrm{V}$. Gibbs phenomenon is not smoothed out.

For the inductor ripple, the peak to peak ripple current $I_{\mathrm{L,pp,max}}$ is designed to scale with the peak current through the inductor. Consequently $I_{\mathrm{L,pp,max}}$ is defined as

$$I_{\mathrm{L,pp,max}} = r_{\mathrm{L,pp,max}} \cdot \frac{I_{\mathrm{o,max}}}{N} \tag{10}$$

where $I_{\mathrm{o,max}}$ is one of the power constraints and $r_{\mathrm{L,pp,max}}$ is the relative ripple ratio. This definition is important in the view of the filter cut-off frequency f_{c}, which becomes apparent when (7) and (10) are substituted in (8),

$$f_{\mathrm{c}} = \frac{(M-1) \cdot \sqrt{f_{\mathrm{sw}} \cdot r_{\mathrm{L,pp,max}} \cdot I_{\mathrm{o,max}}}}{\pi \sqrt{V_{\mathrm{bus}} \cdot C_{\mathrm{DM}}}}. \tag{11}$$

The cut-off frequency, and thus the control bandwidth threshold, $B_{\mathrm{control\ threshold}}$ (9), are independent of the number of branches N. Both design constants are laid-out in **Table I(b)**.

III. Loss Models and Optimization

This section covers the loss models of the main components in the amplifier: semiconductors, filter inductors, and both the flying and filter capacitors. Throughout the subsections for the different components, the remaining optimization constraints will be discussed. **Section III-A** provides a clear overview of all the constraints and what is discussed where for later reference. Next, the operating conditions for which the components are dimensioned are discussed in **Section III-B**. The loss models are explained and the component selection methods are defined in **Sections III-C**, **III-D**, and **III-E**. And finally, the cost of the components and the amplifier as a whole is covered in **Section III-F**.

A. Optimization Constraints

This section serves to create an overview of all constraints that bound the optimization and either have been mentioned in the earlier sections already or will be discussed in this section. There are four main constraints: output quality, control bandwidth, amplifier lifetime, and power output. However, the power constraint is divided into a peak voltage and current, and an RMS current that can be sustained indefinitely. **Table II** serves as a summary where each of the constraints is listed with a short explanation and the relevant section(s) in which they are mentioned.

As mentioned before, these constraints will be varied to bring perspective into how they bound the possible and optimal amplifier designs. Where the effects of the output voltage and current can be predicted, the balance between the output voltage ripple and the control bandwidth threshold, discussed in **Section II-D**, is less straightforward. Additionally, the cost of for example increased lifetime can easily be investigated in this way.

TABLE II
FCC Amplifier Optimization Constraints

Symbol	Explanation	Section
$\widetilde{v}_{\mathrm{o,RMS,max}}$	Maximum RMS output voltage ripple	II-A
$B_{\text{control threshold}}$	Maximum attainable control bandwidth	II-B
$t_{\mathrm{lifetime,min}}$	Minimum attainable amplifier lifetime	III-C
$V_{\mathrm{o,max}} = V_{\mathrm{bus}}$	Maximum output voltage, equal to the bus voltage	III-C, III-E
$I_{\mathrm{o,peak}}$	Peak output current	III-E
$I_{\mathrm{o,RMS,max}}$	Maximum sustained RMS output current	III-D

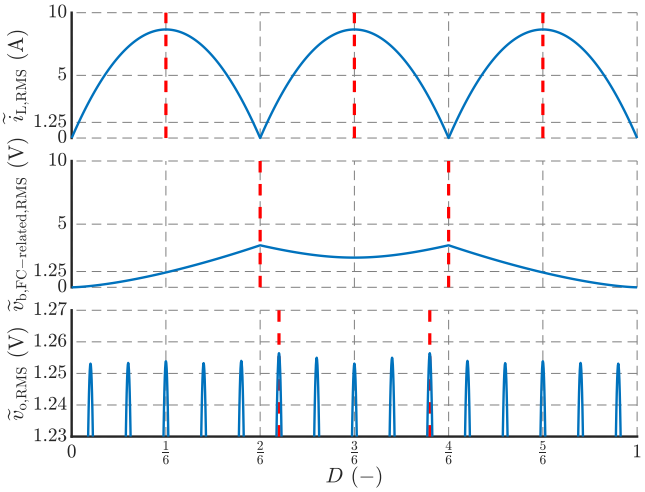


Fig. 5. Inductor current ripple (top), FC-related branch voltage ripple (middle), and output voltage ripple (bottom) as functions of duty-cycle of a 4-Level 5-Branch FCC. The red dashed lines indicate the worst-case operating points for each of the components. Note that the Y-axis is zoomed in for the bottom plot to make the difference in peak height visible.

B. Worst-Case Operating Points

All components are dimensioned for their worst-case operating condition. This is not a single operating point, but rather a worst-case point specific to every component. To better convey this, the inductor current ripple $\widetilde{i}_{\mathrm{L,RMS}}$, FC related branch voltage ripple $\widetilde{v}_{\mathrm{b,FC\text{-}related,RMS}}$ and the output voltage ripple $\widetilde{v}_{\mathrm{o,RMS}}$ are plotted versus the duty-cycle for a 4-Level 5-Branch FCC in **Fig. 5**. The worst-case operating point is different for all three, as indicated by the locations of peaks in the ripple. Also note that the location of these peaks is dependent on the number of levels M and branches N (as discussed in **Section II-B**), meaning that the worst-case operating point is different for every component and every amplifier design. The points with the highest inductor current ripple define the filter inductor design discussed in **Section III-D**, the flying capacitor design is defined by the operating points with the highest flying capacitor voltage ripple, and similarly, the output filter C_{DM} is characterized by the maximum output voltage ripple. Both (i.e. flying- and output-) capacitor designs are discussed in **Section III-E**.

In addition to the static operating points (i.e. duty-cycle, and thus output voltage, dependent) in **Fig. 5**, there is also a dynamic worst-case current profile (i.e. varying output current, voltage, and duty-cycle, **Fig. 6**) which is used to determine the lifetime of the semiconductors (**Section III-C**). This profile is based on two types of MRI imaging techniques: diffusion-weighted imaging (DWI), and echo planar imaging (EPI). DWI pulses are slow with a large peak current while EPI pulses are much faster with about half the peak current. The DWI pulses result in the largest junction temperature swing and are therefore defining for the semiconductor lifetime. Generally, such pulses are bipolar with frequencies between 100 Hz and 800 Hz [7]. But, to maximize the load on a single set of semiconductors ($S_{[1,\ldots,M-1]\mathrm{p}}$) a unipolar DWI was used instead, leading to $f_{\mathrm{DWI}} \approx 50\,\mathrm{Hz}$. The worst-case profile is designed such that the total length of the EPI pulses is equal to that of a single DWI pulse ($t_{\mathrm{on}} + t_{\mathrm{off}}$). All specifications of the designed profile can be found in **Table III**. It is important to state that while this profile resembles profiles used in MRI applications, it sacrifices correctness to be an absolute worst-case.

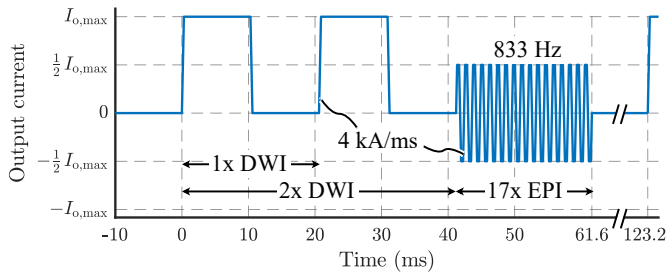
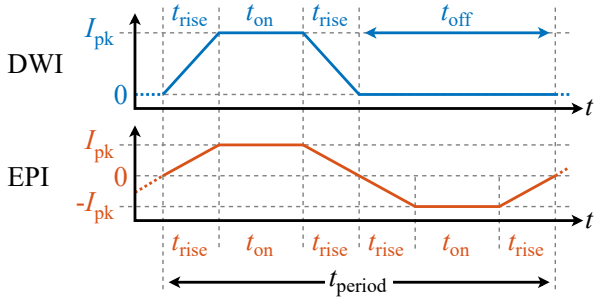


Fig. 6. Worst-case output current load profile consisting of 2 unipolar DWI pulses followed by 17 bipolar EPI pulses. 1 DWI pulse is approximately equal in length to the 17 EPI pulses. Following this 61.6 ms sequence is an equally long idle period. The profile repeats every 123.2 ms

TABLE III
WORST-CASE OUTPUT CURRENT PROFILE SPECIFICATIONS

	I_{pk}	t_{rise}	t_{on}	t_{off}	t_{period}	f	#
DWI	$I_{o,max}$	300 µs	10 ms	10 ms	20.6 ms	48.5 Hz	2
EPI	$\frac{1}{2}$ $I_{o,max}$	150 µs	300 µs	–	1.2 ms	833 Hz	17



C. Semiconductors

The lifetime of the semiconductors is one of the optimization constraints. It is dependent on the junction temperature swing and average junction temperature. Calculating the junction temperature over the course of a load profile, like shown in **Fig. 6**, requires a loss model and a thermal model. First, the loss model will be explained, followed by the thermal model. Next, their application in estimating the lifetime constraint is demonstrated. Finally, the method for choosing a semiconductor is described. The thermal model is based on the experimental prototype which is also used in the validation in **Section V**.

Semiconductor losses comprise two parts, conduction losses P_{cond}, dependent on RMS drain current $I_{d,RMS}$, and junction temperature T_j, and switching losses P_{sw}, dependent on drain source voltage V_{ds}, drain current I_d, and junction temperature T_j. Both assume a fixed gate voltage, 2 Ω gate resistors, and gate driver.

The conduction losses have been modeled using the data provided in the datasheets for R_{on} as functions of both current and temperature. A polynomial surface is fitted through this data such that the on-resistance can be approximated at any operating point. One of these fits is presented in **Fig. 7**. The conduction losses can be calculated using:

$$P_{cond} = {I_{d,RMS}}^2 \cdot R_{on}(I_{d,RMS}, T_j). \tag{12}$$

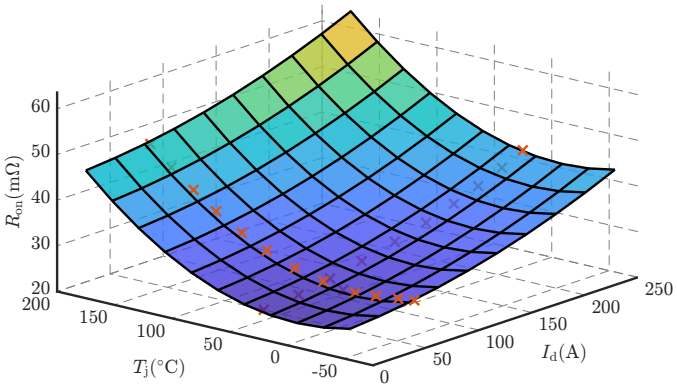


Fig. 7. Fitted on-resistance, R_{on}, as a function of junction temperature T_j and drain current I_d of the selected 1200 V SiC FET. The crosses show the data points that are extracted from the datasheet and through which the surface is fitted.

The switching losses are modeled in a very similar way but now based on manufacturer-provided measurement data. The data lists both turn-on and turn-off switching loss energies at various voltages, currents, gate resistances, and temperatures. A $P_{sw} = f(I_d, T_j)$ surface is fitted for every measured V_{ds}. These fits are linearly interpolated to find the switching losses for any value of V_{ds}, in addition to all possible values of I_d and T_j on the individual fits. The average power loss can then be calculated by dividing the switching energies by the switching period:

$$P_{sw} = \frac{E_{on}(V_{ds}, I_d, T_j) + E_{off}(V_{ds}, I_d, T_j)}{T_{sw}}. \tag{13}$$

In a real amplifier, the bus voltage will drop during a load profile (**Fig. 6**) as a result of the high power draw. However, in the simulations it is assumed that the bus voltage remains constant throughout such a profile, meaning the losses will be overestimated.

In the experimental setup, the semiconductors are soldered onto a metal-core PCB that is attached to a coldplate with water cooling to effectively sink the generated heat. Schematically, the stackup looks like the drawing in **Fig. 8(a)** for a single FET. These individual layers: solder, copper, dielectric, metal core, thermal interface material (TIM) or thermal paste, and the coldplate, are each represented by an RC element in the thermal Cauer model of **Fig. 8(b)**. The values are derived using the area, thickness, density, thermal conductivity, and thermal capacity, of the different materials. To account for the diagonal spreading of heat, each metal layer is modeled to be 50% wider and longer than the layer above it. In addition to these 6 layers, there are 6 RC pairs dedicated to the SiC FET. The value of these 6 RC pairs is determined by fitting a Foster model through the thermal characteristics in the datasheet and converting it to a Cauer model to be in line with the other parameters.

The entire thermal model represents a single FET. No effects from nearby FETs are taken into account. This influences the results in two ways: heat generated by nearby FETs does not spread through the layers, resulting in

lower peak temperatures and, countering this, the thermal capacitance of the dielectric, thermal paste, and most importantly the coldplate, only considers the area (diagonally) beneath the FET. Any extra volume that the heat can spread to, for example, the area below non-conducting FETs, is not taken into account.

Both the thermal swing and average temperature are important because of the semiconductor lifetime constraint. SiC MOSFETs can display various types of wear-out mechanisms [8]. However, only the mechanisms that are influenced by the design variables are of interest. That leaves only the power cycling lifetime. It describes the number of thermal cycles the MOSFET can endure before failure N_f as a function of temperature swing ΔT_j and average junction temperature $T_\mathrm{j,mean}$. This relation can be described by a LESIT model which applies a Coffin-Manson acceleration factor for the temperature swing and an Arrhenius acceleration factor for the mean temperature [8]–[10]:

$$N_\mathrm{f} = A \cdot (\Delta T)^{\alpha} \cdot \exp\left(\frac{E_\mathrm{A}}{k_\mathrm{B} T_\mathrm{j,mean}}\right). \tag{14}$$

The data for Wolfspeed SiC MOSFETs [8] was fitted, resulting in the parameters found in **Table IV**.

By knowing the number of thermal cycles per worst-case profile $N_\mathrm{worst\text{-}case}$, the duration of the profile $t_\mathrm{worst\text{-}case}$, and the percentage that the amplifier is used for this profile r_usage, the lifetime can be estimated by applying (14):

$$t_\mathrm{lifetime} = \frac{N_\mathrm{f}}{N_\mathrm{worst\text{-}case}} \cdot t_\mathrm{worst\text{-}case}/r_\mathrm{usage}. \tag{15}$$

This assumes that all other profiles have a negligible effect on the lifetime, which is a fair assumption given the considered maximum possible load profile and the dominance (power of ≈ -5) of the temperature swing ΔT in (14). Lifetime is one of the optimization constraints and is set to $t_\mathrm{lifetime,min} = 10\,\mathrm{years} = 315\,360\,000\,\mathrm{s}$, being a typical value used in the industry.

For the presented profile in **Fig. 6**, $N_\mathrm{worst\text{-}case} = 2$, one for each of the DWI pulses, $t_\mathrm{worst\text{-}case} = 123.2\,\mathrm{ms}$, and r_usage is assumed 3.33%. For the lifetime estimation, this profile is repeated for up to 15 seconds to reach thermal equilibrium before the thermal swing and mean temperature are extracted, eliminating the start-up transient. The two thermal cycles per profile and the stabilization of the junction temperature are both displayed in **Fig. 9**.

Finally, there are three preselected SiC MOSFETs, all with a low R_dson and a varying voltage blocking capability of 650 V, 900 V, and 1200 V. Choosing one of these three semiconductors is based on their voltage blocking capability. A 33% voltage margin $r_\mathrm{V,FET}$ is used to account for related reliability concerns such as Accelerated Life Test High Temperature Reverse Bias (ALT-HTRB), and the effects of terrestrial neutrons [8]. The voltage across the semiconductors is dependent on the number of levels M, and the power

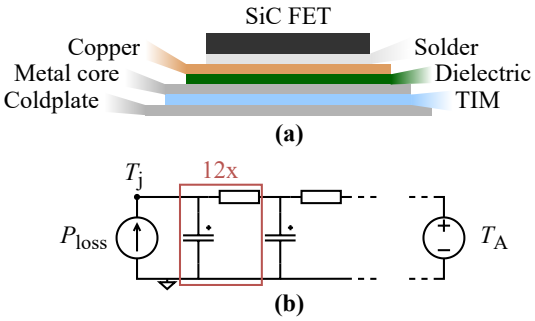


Fig. 8. Thermal semiconductor and heatsink model: **(a)** schematic overview of how the semiconductor is attached to the coldplate in the experimental setup and a **(b)** thermal Cauer network representation of the different layers where T_A is equal to the water temperature in the coldplate. The first 6 RC pairs are dedicated to the SiC FET, followed by 6 RC pairs to model the remaining layers shown in **(a)**. This model would have to be changed in case power modules based on direct bonded copper (DBC) substrates are used.

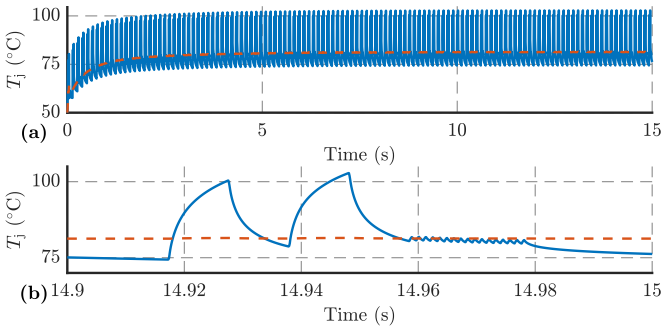


Fig. 9. Thermal response of junction temperature to the worst-case profile from **Fig. 6**: **(a)** Junction temperature in blue and its moving average in dashed orange over the entire 15 s. **(b)** Zoomed-in version showing just the final run of the profile, used for extracting the peak-to-peak and average junction temperatures.

TABLE IV
LESIT MODEL PARAMETERS

Symbol	Value	Unit	Comment
A	$2.2 \cdot 10^{6}$	$\mathrm{K}^{-\alpha}$	Constant
α	-4.923	-	Constant
E_A	$9.892 \cdot 10^{-20}$	J	Activation energy
k_B	$1.380 \cdot 10^{-}23$	$\mathrm{J\,K}^{-1}$	Boltzmann constant

constraint V_bus. The minimum required blocking voltage of a semiconductor is therefore,

$$V_\mathrm{blk,min} = \frac{V_\mathrm{bus}}{(M-1) \cdot 0.667}. \tag{16}$$

And the definitions of the voltage and current margins (which will be covered in **Section IV-B**) are as follows,

$$\begin{aligned} r_\mathrm{V,FET} &= \frac{V_\mathrm{blk} - V_\mathrm{bus}/(M-1)}{V_\mathrm{blk}}, \\ r_\mathrm{I,FET} &= \frac{I_\mathrm{d,max} - I_\mathrm{o,max}/N/k}{I_\mathrm{d,max}}. \end{aligned} \tag{17}$$

From the three preselected semiconductors, the unit with the lowest valid blocking voltage is chosen, this results in **Table V** for $V_\mathrm{bus} = [2400\,\mathrm{V}, 1800\,\mathrm{V}, 1400\,\mathrm{V}]$.

TABLE V
SELECTED SEMICONDUCTOR BLOCKING VOLTAGE FOR VARYING BUS VOLTAGES AND NUMBER OF LEVELS

M	V_{bus}		
	2400 V	1800 V	1400 V
3	-	-	1200 V
4	1200 V	900 V	900 V
5	900 V	900 V	650 V
6	900 V	650 V	650 V
7	650 V	650 V	650 V
8	650 V	650 V	650 V

D. Filter inductors

Designing power inductors comes with many degrees of freedom. Most importantly there is the inductance itself, but there are many inductor design variable combinations that result in the same inductance value. The considered parameters are the type of powder core material (no ferrites are considered), the number of stacked cores, wire type, number of windings, and the number of parallel wires. A separate in-house inductor design tool is used which varies all these parameters in parallel to compute hundreds to thousands of different inductor designs. The inputs to this tool are the desired inductance and a margin, the RMS and peak current, the current as a function of frequency, and the voltage over time.

Processing of the resulting inductor designs is done in two steps. First, the designs are filtered based on design limits such as volume, height, mass, losses, and peak temperature. This leaves just the valid designs. For these, the cost-loss product is calculated and the design with the lowest product, i.e. the best loss-cost ratio, is chosen. Calculating the losses and peak temperature is not straightforward. First, the core losses based on the improved Generalized Steinmetz Equation (iGSE) are explained, followed by the wire losses and the skin effect. Finally, the simplified thermal model is discussed.

The original Steinmetz Equation (SE) is the most used equation for characterizing core losses [11]. It relies on three material parameters k, α, and β, known as the Steinmetz parameters. They can be extracted from, or are listed in, inductor core datasheets. SE describes the time-average power loss per unit volume P_{v} as a function of peak sinusoidal flux density $\hat{B}$ with frequency f.

$$P_{\mathrm{v}} = k f^{\alpha} \hat{B}^{\beta} \tag{18}$$

The major downside of SE is that it only works for sinusoidal flux waveforms. This is one of the improvements that iGSE brings. It can be applied to any arbitrary flux waveform. iGSE still does not consider magnetic relaxation effects, nor does it deal with premagnetization. However, iGSE has been evaluated as the most accurate state-of-the-art loss model based on the original Steinmetz parameters [11]:

$$P_{\mathrm{v}} = \frac{1}{T} \int_0^T k_i \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (\Delta B)^{\beta-\alpha} \mathrm{d}t \tag{19}$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} \, 2^{\beta-\alpha} \mathrm{d}\theta}. \tag{20}$$

Some more elaborate models do take into account these other effects, but they all require additional material parameters that cannot be extracted from the data traditionally provided by core manufacturers. Relaxation effects occur shortly after constant flux, or when a high flux slope is followed by a very slow flux change (which only occurs at high or low dutycycles, $D_{\mathrm{L}} > 0.8$ or $D_{\mathrm{L}} < 0.2$) [12]. During the output current slopes of the worst-case profile **Fig. 6**, semiconductor dutycycles of $D = 0.1$ and $D = 0.9$ are common. However, due to the interleaving of the levels, this does not translate to equally high dutycycles on the inductors D_{L}. Therefore, iGSE was deemed sufficient.

Besides the core losses, the ohmic wire losses also play a big part in the loss model. The resistance of a conductor increases with frequency due to eddy currents that lead to the skin effect. These are self-induced eddy currents. Eddy currents can also be induced by an external magnetic field from for example other nearby conductors. This is called the proximity effect. In this loss model, only the skin effect and DC losses are taken into account. They are calculated using [11]:

$$P_{\mathrm{S}} = R_{\mathrm{DC}} \cdot F_{\mathrm{R}}(f) \cdot \hat{I}^2 \tag{21}$$

where $R_{\mathrm{DC}} = \frac{4}{\sigma \pi d^2}$,

$$F_R = \frac{\xi}{4\sqrt{2}} \left(\frac{\mathrm{ber}_0(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\,\mathrm{ber}_1(\xi) - \mathrm{bei}_0(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right), \tag{22}$$

$\xi = \frac{d}{\sqrt{2}\delta}$, and $\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}}$. Here δ is known as the skin depth, f the frequency, d the conductor diameter, and σ the conductivity of the wire material.

The proximity effect, which is not taken into account, becomes more important the more wires are closely bound together. This is the case when windings consist of multiple layers. Therefore a limit of 2 layers was set as an inductor design constraint.

The thermal model that these combined losses are fed into resembles the inductor in a very simplified way. It is a first-order model where the windings and cores are combined into a single thermal resistance R_{th} and are directly attached to a coldplate through a thermal interface material (TIM) and an electrical isolation sheet. The combined core and winding losses are applied to this model to determine the maximum temperature. The temperature dependence of the resistance of the winding is taken into account, but the temperature dependence of the core material properties is not. It is thus a very simplified model which can therefore not be used to determine the maximum possible load for an inductor. It does give an initial impression of the temperature, that can be used to filter inductor designs that stay clear of any thermal limits.

Losses in the inductor are calculated at the operating point with the largest inductor current ripple, defined by the duty-cyle, and the maximum sustained RMS current of the amplifier. The current ripple causes maximum core losses while the RMS current maximizes winding losses. The maximum RMS current, $I_{\mathrm{o,RMS,max}}$, is one of the power constraints.

E. Flying and Filter Capacitors

Losses in capacitors are typically characterized by the dissipation factor $\tan\delta$ as a function of frequency. It can be split up into a parallel component $\tan\delta_{\mathrm{P}}$ dependent on the insulation resistance, a dielectric component $\tan\delta_{\mathrm{D}}$ associated with the energy used to polarize and repolarize the dielectric, and a series component $\tan\delta_{\mathrm{S}}$ related to the resistance of the leads and the metal layers [13]. These can be summed to ultimately find $\tan\delta$. This dissipation factor can also be expressed as an equivalent series resistance through

$$ESR = \frac{\tan\delta}{2\pi f \cdot C}, \tag{23}$$

which allows for very easy calculation of the losses using $P = I^2 \cdot ESR$. In addition, the selected EPCOS film capacitors all list their ESR as a function of frequency in their datasheet [14], making its usage straightforward.

A dataset of individual EPCOS film capacitors is used, storing the capacitances, voltage ratings, peak RMS currents, volumes, costs, and the previously mentioned ESRs as a function of frequency. Additionally, the peak loss of each capacitor is calculated using the peak RMS current and the ESR at the listed frequency. To further increase the number of options, any combination of multiple parallel and/or series capacitors of the same type is also considered. Designing a capacitor based on this dataset requires the desired capacitance, C_{goal}, the minimum voltage rating, and the worst-case current as a function of frequency. The flying capacitances are defined by their maximum branch voltage related ripple $V_{\mathrm{b,FC\text{-}related,pp,max}}$ (**Section II-E**), their minimum voltage rating is described by (1) and dependent on the power constraint V_{bus} and the number of levels M. The output filter capacitance is a design variable discussed in **Section II-C**. Furthermore, its minimum voltage rating is defined by the maximum output voltage $V_{\mathrm{o,max}}$.

For each of the capacitors in the dataset, the minimum required number in series and parallel is determined. Next, the loss, resulting capacitance, cost, and volume of each potential design is calculated. Following this, the number of series and parallel capacitors are increased in steps until the peak loss is within the limits calculated for each of the dataset capacitors while making sure the capacitance stays above C_{goal}. Finally, the cost and volume of each design are multiplied as a figure of merit and the minimum is selected as the optimal design. This workflow is used for both the flying capacitors and the output filter capacitors, and is visualized in **Fig. 10**.

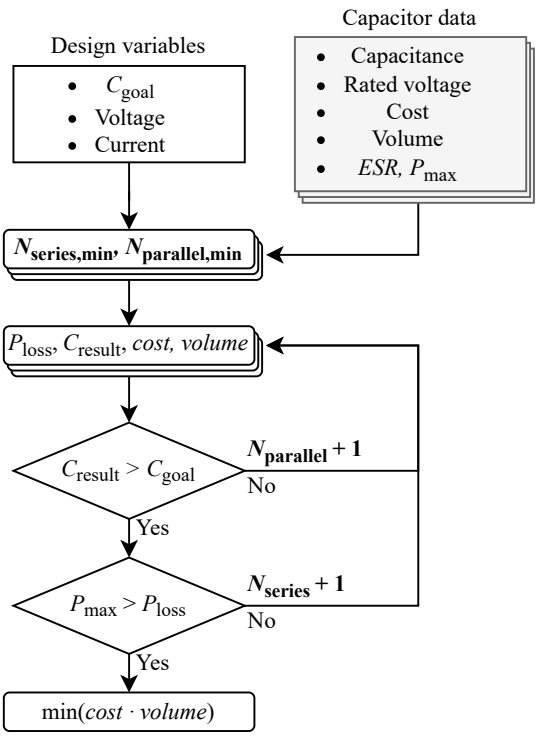


Fig. 10. Implemented capacitor design workflow for flying- and filter capacitors.

As a worst-case design operating point for the flying capacitors, the point with maximum FC ripple is used (**Section III-B**) with maximum output current $I_{\mathrm{o,peak}}$. For the output capacitor the dutycycle with maximum output voltage ripple (**Section III-B**) is chosen. Another relevant design parameter for the output capacitors is their maximum current due to the fast rise and fall times of the output voltage ($\mathrm{d}v_{\mathrm{o}}/\mathrm{d}t$) during the worst-case waveform. This is not accounted for in the presented design workflow but can easily be mitigated by over-dimensioning the output capacitor. The potential effect this has on the cost-related optimization results is minimal due to the dominance of the semiconductors, filter inductors, and flying capacitors in this regard.

F. Costing

The costs of the amplifier can largely be fit into two categories, first, the defined components (semiconductors, inductors, and capacitors), and secondly, parts that are not as clearly defined but scale with the design parameters, such as the coldplate that scales with the number of semiconductors. For this second category, the costs are derived from the prototype FCC its PCBs such that the cost of the smaller auxiliary circuits is not ignored. All considered costs are listed in **Table VI**. Costs that are independent of the design variables such as the DC-DC converters supplying the amplifiers, or the cabinet that the amplifiers are mounted in, are not included. In this work, absolute costs are not discussed, rather the cost relative to the most cost-effective design is used.

TABLE VI
CONSIDERED AMPLIFIER COSTS

Category		Parts
Components		Semiconductors
		Filter inductors
		Flying capacitors
		Filter capacitors
Scale with number of	Semiconductors	Coldplate size
		# Gate drivers
		# Isolated gate drive supplies
	Branches	# PCBs
		# Auxiliary components

IV. SCALING LAWS AND THE EFFECT OF CONSTRAINTS

Through the behaviour of FCCs as discussed in **Section II**, and the component loss models covered in **Section III**, the output quality, control bandwidth, and lifetime are calculated for varying FCC designs following the design variable ranges in **Table I(a)**. Resulting are the scaling laws explored in **Section IV-A** and the optimal designs examined in **Section IV-B**. The shown results are all bound by the default constraints (24) unless stated otherwise.

$$\begin{aligned} \widetilde{v}_{\mathrm{o,RMS}} &< 1.5\,\mathrm{V} \\ B_{\text{control threshold}} &> 50\,\mathrm{kHz} \\ t_{\mathrm{lifetime}} &> 10\,\mathrm{years} \\ V_{\mathrm{o,max}} = V_{\mathrm{bus}} &= 2400\,\mathrm{V} \\ I_{\mathrm{o,peak}} &= 1200\,\mathrm{A} \\ I_{\mathrm{o,RMS,max}} &= 400\,\mathrm{A} \end{aligned} \tag{24}$$

The simulations have been completed using a brute-force method to simulate all possible parameter combinations (378.000 in this case) in parallel in batches of 70. While computationally the most expensive way to approach such a problem, $\approx 40\,\mathrm{h}$ on a server with two Intel Xeon Gold 6230T CPUs at 2.8 GHz (40 cores, 80 threads total) at 100% utilization, it does guarantee a complete solution set. An attempt was made to utilize MATLAB's built-in multi-objective solver *gamultiobj*, but satisfactory results were not achieved within a reasonable time frame. Either the solver would get stuck in local minima and never explore the global optimal points, or not the entire Pareto front would be covered, something also observed in [15], where it is determined that the solver does not handle discrete parameters very well. Therefore, a brute-force method was ultimately used to achieve the presented results.

A. Scaling Laws

Knowing how the design variables should scale in relation to the constraints is of use when designing FCC-based amplifiers. Due to the high number of variables and constraints that are varied, the scope is limited on a plot-by-plot basis to highlight a certain relation. It is therefore important to mind the notes on each of the diagrams.

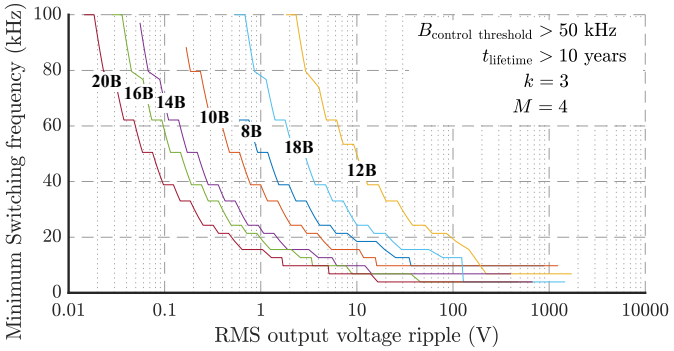
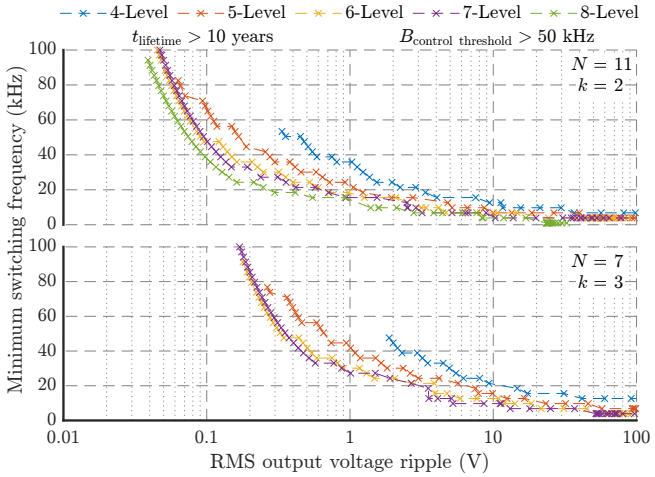


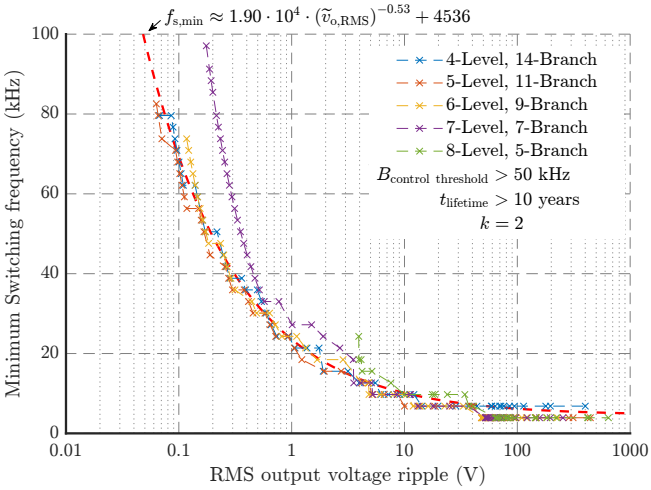
Fig. 11. Minimum switching frequency as a function of RMS output voltage ripple for a $M = 4$-Level FCC with varying amount of branches as indicated by the bold labels on the lines. The 12, and 18-Branch lines appear out of the expected order because the frequency doubling effects partially cancel each other out as discussed in **Section II-B** and following (6). Also the 8, 10, and 14-Branch FCCs lines do not extend all the way to $f_{\mathrm{sw}} = 100\,\mathrm{kHz}$ as the maximum loss is bound through the lifetime constraint $t_{\mathrm{lifetime}} > 10\,\mathrm{years}$.

1) Switching Frequency: Switching frequency f_{sw}, the number of branches N, and with them, the effective switching frequency $f_{\mathrm{sw,eff}}$ (5) affect the output voltage ripple $\widetilde{v}_{\mathrm{o,RMS}}$ (**Fig. 11**). Generally speaking, the output ripple lowers as the number of branches increases. Exceptions to this rule are designs where the frequency doubling effects of the branches and levels cancel each other out when (6) does not hold. As a result, the 12-Branch variant has 10 times more ripple than the 8-Branch variant despite having 50% more semiconductors. Additionally, each design has a maximum switching frequency bound by the semiconductor losses through the lifetime constraint $t_{\mathrm{lifetime}} > 10\,\mathrm{years}$. A similar result is shown for $[4, \ldots, 8]$-Level FCCs in **Fig. 12(a)** where a higher number of levels results in a lower output ripple. In the range $1\,\mathrm{V} < \widetilde{v}_{\mathrm{o,RMS}} < 10\,\mathrm{V}$, doubling the switching frequency reduces the output ripple by approximately a factor 10. This is best shown in **Fig. 12(b)** where the number of levels M and branches N are chosen such that the frequency multiplication factors $(M-1)\cdot N$ are close together. As a result of matching the effective switching frequencies, the different FCCs exhibit a similar f_{sw}, $\widetilde{v}_{\mathrm{o,RMS}}$ behaviour.

Countering the output voltage ripple $\widetilde{v}_{\mathrm{o,RMS}}$ is the control bandwidth $B_{\text{control threshold}}$, for which the number of levels M and branches N are also affecting the minimum switching frequency following **Fig. 13**. For a given control bandwidth threshold $B_{\text{control threshold}}$, increasing the number of levels M and/or branches N nets a lower minimum switching frequency $f_{\mathrm{sw,min}}$. When matching the effective switching frequencies (**Fig. 13(b)**), the behaviour becomes independent of the number of levels and branches, identical to the f_{sw}, $\widetilde{v}_{\mathrm{o,RMS}}$ behaviour discussed above. This indicates that the output voltage ripple and control bandwidth are related to the effective switching frequency $f_{\mathrm{sw,eff}}$ rather than the exact number of levels and branches.

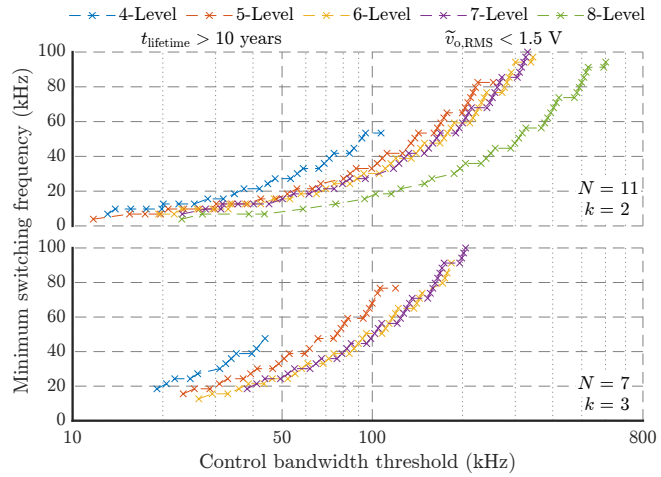


(a) $M = 4, \ldots, 8$-Level FCCs with $N = 11$ Branches and $k = 2$ parallel FETs (top) and $N = 7$ Branches and $k = 3$ parallel FETs (bottom) showing similar results to **Fig. 11**.

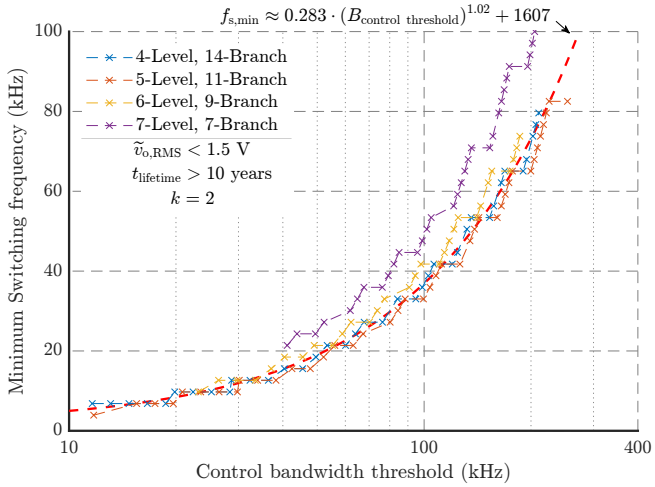


(b) FCC designs with a varying number of levels and branches such that the frequency doubling effect is approximately consistent across the different number of levels. Showing how the relationship between switching frequency and output voltage ripple is not necessarily dependent on the number of branches and levels but rather on the effective switching frequency, a combination of the two.

Fig. 12. Minimum switching frequency as a function of RMS output voltage ripple



(a) $M = 4, \ldots, 8$-Level FCCs with $N = 11$ Branches and $k = 2$ parallel FETs (top) and $N = 7$ Branches and $k = 3$ parallel FETs (bottom).



(b) FCC designs with a varying number of levels and branches such that the frequency doubling effect is approximately consistent across the different number of levels.

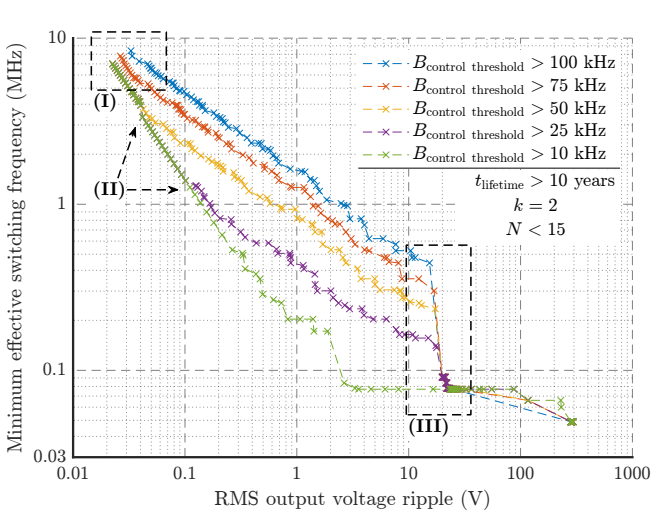
Fig. 13. Minimum switching frequency as a function of control bandwidth

2) Effective Switching Frequency: The direct link between effective switching frequency and output voltage ripple is presented in **Fig. 14(a)** for various control bandwidth thresholds. This link can largely be described by (5), (9), and (11). Stripped of constants, the relations are as follows

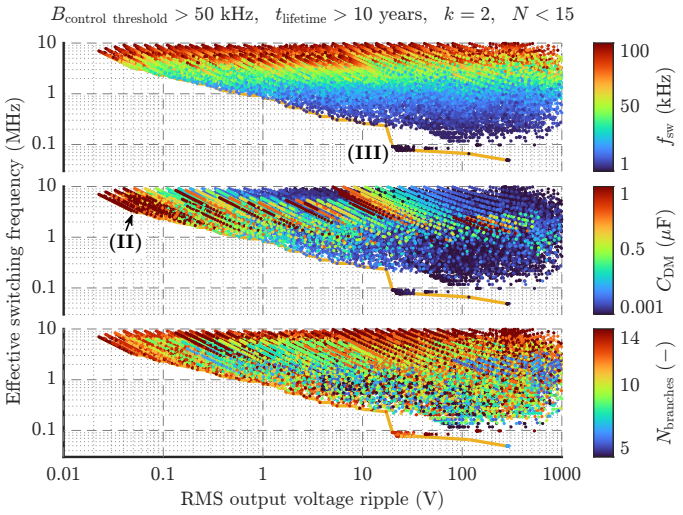
$$B_{\text{control threshold}} \propto \frac{(M-1) \cdot \sqrt{f_{\text{sw}}}}{\pi \sqrt{C_{\text{DM}}}}, \qquad (25)$$

$$f_{\text{sw,eff}} = f_{\text{s}} \cdot (M-1) \cdot N.$$

All lines are converging at point **(I)**, here the switching frequency f_{sw}, the output capacitance C_{DM}, and the number of branches N, are maximized. The reason they converge becomes clear when looking at **(II)** in **Fig. 14(b)**. While the (effective) switching frequency starts to lower, the output capacitance is at its maximum until the kink at **(II)**, where the control constraint starts taking effect. Both the converging **(I)** and the kinks **(II)** are therefore by-products resulting from the maximum $C_{\text{DM}} = 1\,\mu\text{F}$. The lines would presumably stay parallel (on a log scale) if not for this artificial limit. In the range $0.1\,\text{V} < \widetilde{v}_{\text{o,RMS}} < 10\,\text{V}$ both the switching frequency and the output capacitance drop with their ratio bound by (25) due to the control bandwidth thresholds. The cliff **(III)** is a result of the linear scale of the f_{sw} range, the jump from $f_{\text{sw}} = 3.9\,\text{kHz}$ to $1\,\text{kHz}$ is a factor 4, again an artefact as a result of the chosen

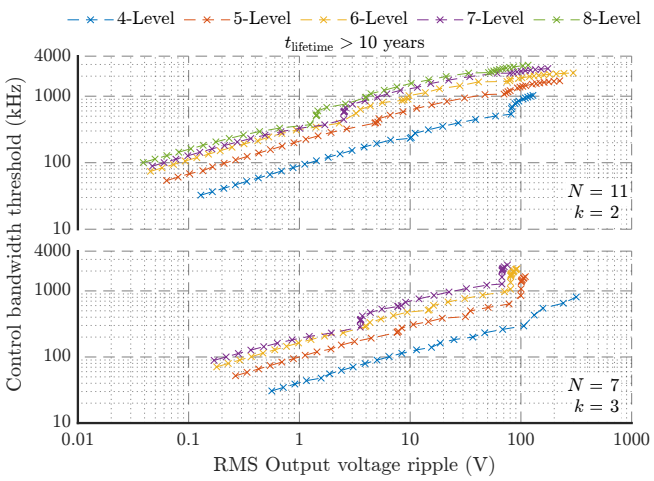


(a) Showing the effect of the control bandwidth threshold on the relationship between the effective switching frequency and the RMS output voltage ripple. Higher control bandwidths, generally require a higher effective switching frequency to achieve the same output quality. Three points of interest are marked, **(I)** where all lines converge, **(II)** apparent kinks in the yellow and purple lines, and **(III)** a sudden cliff in the effective switching frequency. These points are explained through the help of **(b)** in **Section IV-A2**.



(b) Detailed views of the source of the yellow line in **(a)** where $B_{\text{control threshold}} > 50$ kHz. Each dot is an FCC design that meets all listed constraints and variable limits, the yellow line is the same as in **(a)**. The colors represent different design variables in each of the different plots. On top, it is obvious how the switching frequency f_{sw} is distributed vertically, following the effective switching frequency. The middle plot displays the spread of the filter capacitance C_{DM} along the edge of the front, decreasing with an increase in ripple. Finally, the high branch count N on the boundaries is shown in the bottom figure.

Fig. 14. Minimum effective switching frequency as a function of RMS output voltage ripple for various control constraints **(a)** and elaborated in **(b)** for the case where $B_{\text{control threshold}} > 50$ kHz.



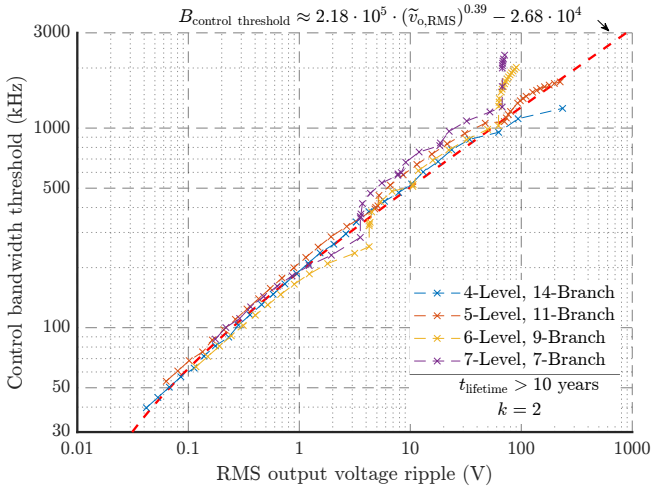


Fig. 15. Trade-off between RMS output voltage ripple and control bandwidth, showing how, independent of the exact number of levels and branches, an FCC with a larger output ripple has a larger potential control bandwidth given an effective switching frequency.

variable ranges. One final interesting note is how along the boundary, the number of branches N is almost always close to, or at the maximum (**Fig. 14(b)** bottom). It only lowers when the switching frequency is already at its minimum, implying that the number of branches has a larger effect on the output voltage ripple than the switching frequency does.

The output voltage ripple and control bandwidth can be seen as a design trade-off. At a fixed effective switching frequency, decreasing the ripple requires a reduction in control bandwidth and vice versa. The relationship is shown in **Fig. 15**.

B. Optimal Design

Despite all the discussed trade-offs and relationships between various parameters, choosing an optimal design is still not straightforward. In the industry, the manufacturing cost is commonly used to choose between various designs. Knowing how the cost scales with the constraints can help define the constraints themselves, and resulting from that, an optimal design can be selected. The cost in relation to the control bandwidth $B_{\text{control threshold}}$, output voltage ripple $\widetilde{v}_{\text{o,RMS}}$, lifetime t_{lifetime}, and total loss $P_{\text{loss,max}}$ is

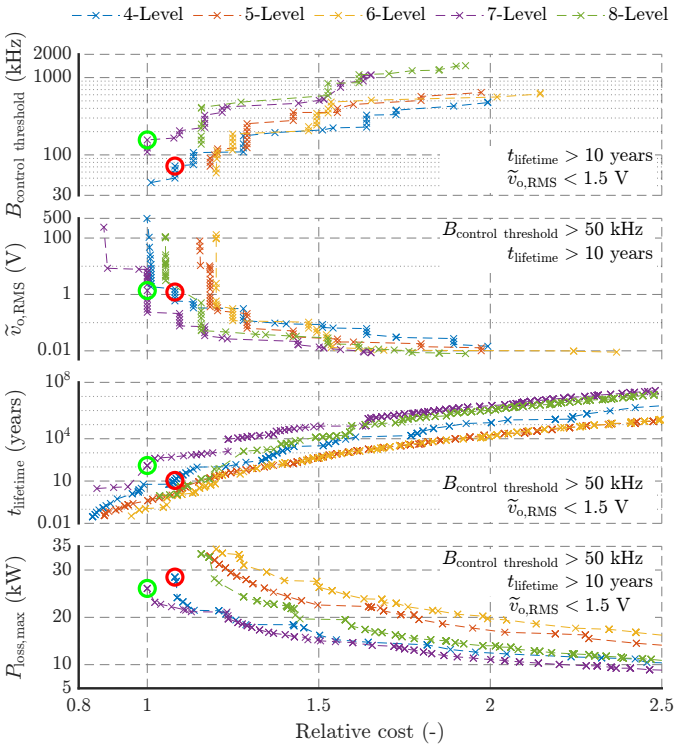


Fig. 16. Influence of cost on control bandwidth, $B_{\text{control threshold}}$, RMS output voltage ripple, $\widetilde{v}_{\text{o,RMS}}$, lifetime, t_{lifetime}, and total loss, $P_{\text{loss,max}}$. Two designs have been marked with a circle, the lowest cost 4-Level and 7-level designs that satisfy all default constraints (24), also visible in the bottom plot. In most cases, the 7-level design has the best result for the lowest cost.

presented in **Fig. 16**. Total loss refers to the sum of the worst-case losses of each of the components. These results will be elaborated using two example designs marked with the red and green circles, the lowest cost 4-Level and 7-level designs that satisfy all default constraints (24). As the 7-Level design has the lowest cost, it has a relative cost of 1, the marked 4-Level design is 8% more expensive than this design.

In almost all cases, the 7-Level designs are the most optimal, with only the 4-Level and 8-Level designs getting close in some cases. This can largely be explained by the bus voltage $V_{\text{bus}} = 2400\,\text{V}$ and the semiconductor blocking voltage, or more specifically, the margin between the blocking voltage V_{blk} and the maximum drain source voltage $V_{\text{ds,max}} = V_{\text{bus}}/(M-1)$, otherwise known as the FET voltage margin. The 7-Level design has a voltage margin of $r_{\text{V,FET}} = 38.5\%$ versus 33.3% for the 4-Level design. The semiconductor losses are bound by the lifetime constraint $t_{\text{lifetime}} > 10\,\text{years}$, meaning a larger voltage margin (i.e. a reduced drain source voltage) increases the maximum possible switching frequency for a given number of branches, and parallel FETs. An increased switching frequency f_{sw} has the benefit of lowering the required filter inductances L_{DM} (7), reducing their cost and therefore striking a better balance between semiconductor and inductor costs. Having a larger potential switching frequency range also results in a more flexible design due to how directly it affects the control bandwidth threshold and RMS output voltage ripple,

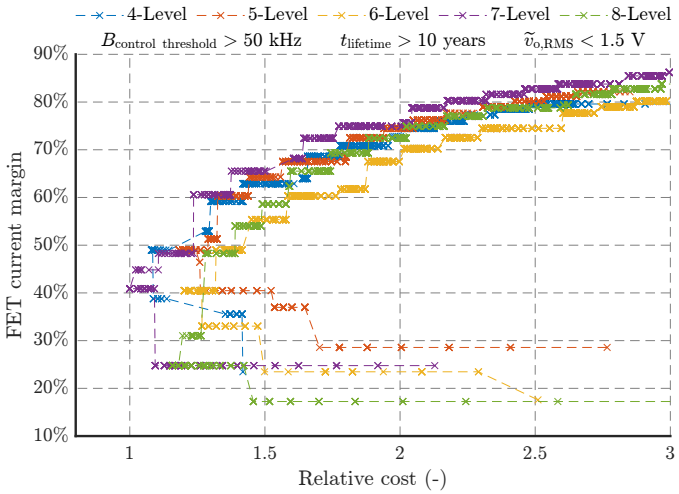


Fig. 17. FET current margin as a function of relative cost, showing that ideally, the current margin is between 40% and 50%, independent of the number of levels. The 8-level designs are the only exception due to their relatively high FET voltage margin.

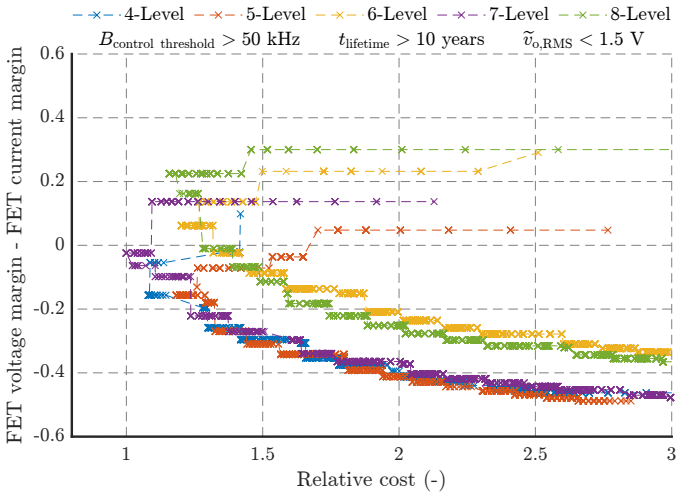


Fig. 18. Difference between FET voltage margin and FET current margin as a function of relative cost. Negative values imply a larger current margin while positive values imply a larger voltage margin. The most optimal design has approximately equal valued margins. Independent of the number of levels, the most optimal designs are always in the range -20% to 20%.

as is discussed in **Section IV-A**. As the 7-Level designs can already hit the maximum switching frequency $f_{\text{sw}} = 100\,\text{kHz}$ (**Figs. 12, 13**), there is little benefit to moving up to the 8-Level design in this regard. For the (semiconductor) cost, the FET current margin is also of importance (**Fig. 17**). The ideal current margin is between $r_{\text{I,FET}} = 40\%$ and 50%. What is most interesting however is the relationship between the difference in voltage and current margin and the relative cost in **Fig. 18**. The most optimal designs have approximately equal voltage and current margins, which when combined with the ideal current margin, makes for a very clear design goal for cost-optimal FCC designs.

The reason the 4-Level design can get close to the 7-Level design is due to its comparatively low semiconductor count (144 vs 168), and requiring fewer, and thus cheaper, flying

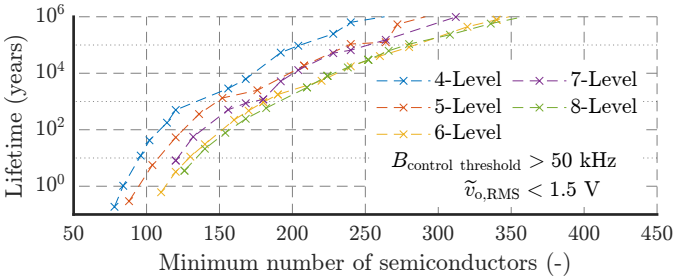


Fig. 19. Relationship between the minimum number of semiconductors $2(M-1)\cdot N\cdot k$ and lifetime, showing how a longer lifetime requires more semiconductors, and how having more levels also increases the minimum semiconductor count for a given lifetime.

capacitors than the 7-Level variants. The lifetime as a function of semiconductor count is displayed in **Fig. 19**, showing how the higher level counts require more semiconductors to achieve the same lifetime. What is interesting however is that the increased semiconductor count does not directly translate to a more expensive amplifier (due to the lower voltage FETs being less expensive), shown by the fact that the optimal 7-Level design is less expensive than the most optimal 4-Level design.

V. Validation

The value of the insights discussed in the previous section depends on the correctness of the model, which is where validation can step in. As shown, the lifetime of the amplifier is a very restricting constraint. Therefore, this is the area where validation is the most important. The focus is put on the validation of the semiconductor losses and the thermal model, as combined they result in the average junction temperature and temperature swing that define the lifetime. For both, first, the validation method will be explained, followed by the results. The validation was done on an experimental prototype 4-Level, 1-Branch FCC with 2 parallel FETs. The full specifications and tested operating points are listed in **Table VII**.

A. Semiconductor Losses

Losses in a switching semiconductor are inherently hard to measure, especially for very fast switching wide bandgap devices such as SiC and GaN FETs [16]. This is why a calorimetric approach as discussed in [16] is used. The essence of the method boils down to the following: 1) Measure the steady-state package temperature at various non-switching operating points (FETs in continuous on-state), where the loss is easy to measure, to be able to relate temperature to loss. 2) Measure the steady-state package temperature at switching operating conditions and use the previously found relation to extract the losses. The measurement point for the temperature can be anywhere in the thermal network, but preferably as close as possible to the semiconductor, as long as the placement and the environment are not changed between measurements. For this measurement, thermocouples were glued on top of 6 of the SiC MOSFET casings as illustrated in **Fig. 20**. The measurement setup is depicted in **Fig. 21**.

TABLE VII
FCC Amplifier Prototype Specifications and Operating Conditions

Specification	Value
Levels	4
Branches	1
Parallel FETs	2
Switching frequency	30 kHz
V_{bus}	[1800 V, 2100 V, 2400 V]
$I_{\text{o,RMS}}$	[5 A, 10 A, . . . , 35 A, 40 A]

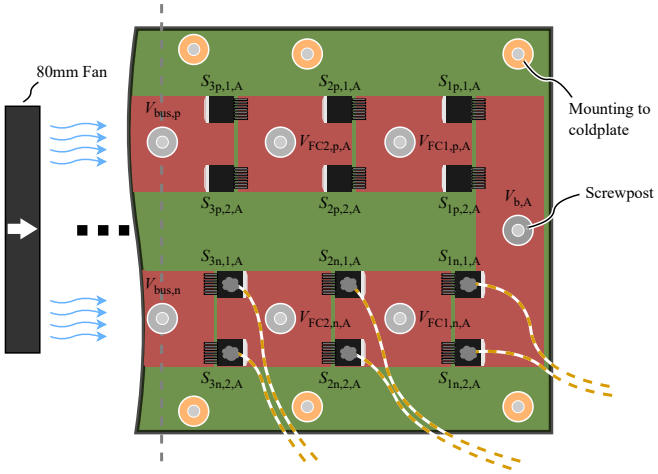


Fig. 20. Schematic overview of the experimental prototype metal core PCB and the layout of the SiC MOSFETs for a 4-Level, 1-Branch, 2-Parallel FET design. One PCB contains 24 FETs, 12 for each side (A/B) of the amplifier. Only the A side is depicted here, the B side is identical but mirrored along the grey dashed line. The 6 FETs with the thermocouples attached are also shown. The orange holes are where the PCB is screwed onto the coldplate while the grey holes are screw posts where cables or the flying capacitors are attached. The red areas roughly depict the current path from $V_{\text{bus,p}}$ to $V_{\text{bus,n}}$, note that this is not an actual PCB layout and merely serves to give the reader an idea of what the tested PCB looks like. In addition to the water cooling through the attached coldplate, airflow is provided by an 80 mm fan that is fixed in place to cool components on other PCBs in the measurement setup (not depicted here).

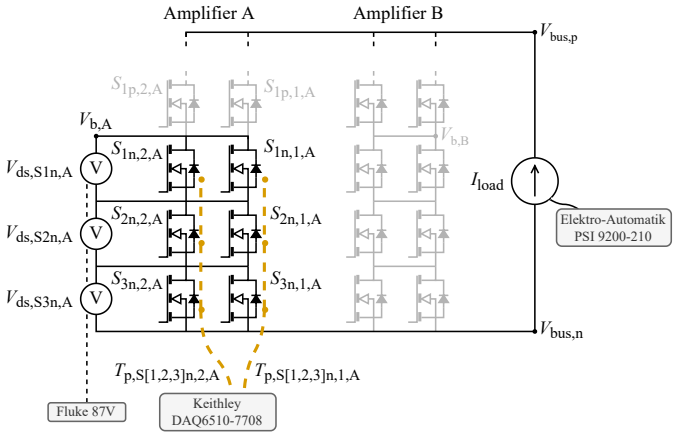


Fig. 21. Measurement setup used to measure the T_{p}, P_{loss} relation from **Fig. 22**.

For the steady-state calibration measurements, the FETs are all forced in an on-state, and a varying constant current is applied from $V_{\mathrm{bus,p}}$ to $V_{\mathrm{bus,n}}$ using an Elektro-Automatik PSI 9200-210 power supply. Once the package temperatures, measured with T-Type thermocouples on a Keithley DAQ6510-7708 ($\pm 1\,^{\circ}\mathrm{C}$), stabilize, the drain-source voltages are measured with a Fluke 87V multimeter. From the applied current and the measured voltage, the loss can be calculated. Here it is assumed that the current is equally shared between the parallel FETs due to the positive temperature coefficient of $R_{\mathrm{ds,on}}$. Resulting is a map from package temperature to loss (**Fig. 22**) and a measurement for steady-state conduction loss that closely matches the simulations (**Fig. 23**). As an extra validation, the steps in constant current are measured both in an increasing and decreasing order, yielding identical results.

The mapping is very similar between the 6 measured FETs, with only one outlier. This can easily be explained by thermocouple placement, as there is a $20\,^{\circ}\mathrm{C}$ temperature gradient on top of the FET casing, which is only around $1\,\mathrm{cm}^2$ in size. A thermal camera could result in a more consistent measurement across the different FETs, however, this was not possible in the measurement setup. Moreover, the placement of the FET on the PCB will also affect its cooling capability, due to where the clamping force to the coldplate is applied (orange holes in **Fig. 20**), and the distance to the cooling fan. This also affects the measured package temperature. These differences do not affect the usage of the mapping as the thermocouples are fixed in place using super glue, meaning their measurements will be done on the same point every time.

Next, this mapping is used to extract the total losses (switching + conduction) from the package temperature at the various switching operating conditions listed in **Table VII**. A limited RMS output current range $I_{\mathrm{o,RMS}}$ is used as the flying capacitors of the FCC prototype can not sustain a higher current long enough for the package temperatures to stabilize ($\approx 2\,\mathrm{min}$). The results are shown in **Fig. 24**. At $V_{\mathrm{bus}} = 2400\,\mathrm{V}$, the intended bus voltage for this FCC, and $I_{\mathrm{o,RMS}} = 40\,\mathrm{A}$, the simulations show a loss between 1% and 48% higher than the measured losses depending on the FET. At lower currents, the difference is even larger, implying that designs that do not significantly utilize the FETs current carrying potential (and are therefore already less optimal from a cost perspective), perform better than the model would suggest. The reason for this error is hard to determine as the setup used to measure the switching losses in the manufacturer-provided data is not known. Also, the spread between the different FETs is not insignificant. It could partially be explained by manufacturing variations between the FETs, but the inconsistent cooling capability (due to the clamping force), also plays a role here as it affects the junction temperature. This hypothesis is reinforced by the fact that the FETs furthest away from the edge ($S_{3\mathrm{n},1}$ and $S_{2\mathrm{n},1}$) have the highest losses in all measurements. In all cases, the simulations predict a higher loss than what is measured, making the simulations a worst-case.

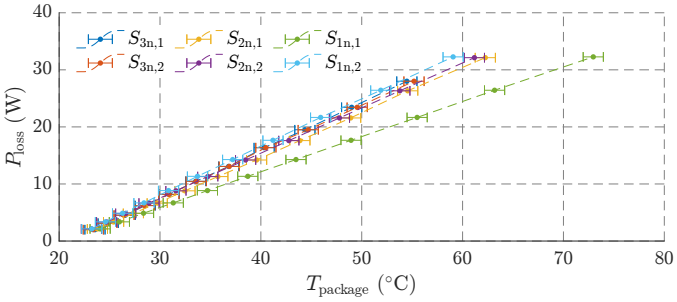


Fig. 22. Mapping from measured steady-state package temperature to losses for the 6 listed FETs, shown with temperature measurement error. Most FETs show the same behavior with only $S_{1\mathrm{n},1}$ reading a significantly higher package temperature.

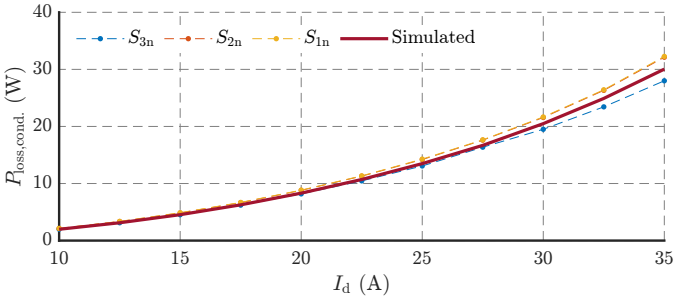


Fig. 23. Comparison between measured and simulated steady-state conduction loss at various drain currents, showing a clear match.

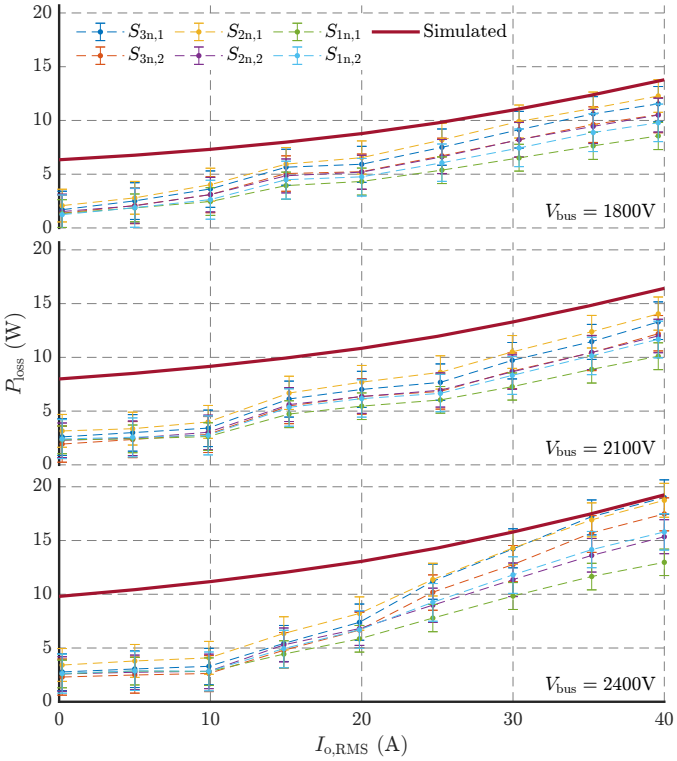


Fig. 24. Comparison between extracted and simulated steady-state loss (switching + conduction) at various RMS output currents and three bus voltages. The simulations always predict a higher loss than measured, matching more closely at higher output currents. The error margin, due to the temperature measurement error of both the calibration and this steady state measurement combined, is also shown in the form of error bars.

B. Thermal Impedance

To estimate the thermal impedance from junction to ambient (coldplate water) of the prototype, the junction temperature needs to be measured. As this is not directly possible on the used packaged SiC MOSFETs, a temperature-sensitive electrical parameter should be used as a proxy measurement. The forward body diode voltage V_{sd} is used for its linear dependence on junction temperature [17]. By varying the coldplate temperature, a junction temperature can be forced onto the FETs. By also measuring the diode voltages, this linear behavior can be extracted.

Roughly following the steps in [18], the measurements are performed as follows. The 6 FETs are forced in the non-conducting state by applying $-4\,\mathrm{V}$ to the gates, next the coldplate water is fixed at a set $20\,^{\circ}\mathrm{C}$. A small reverse reference current $I_{\mathrm{ref}} = 100\,\mathrm{mA}$ ($50\,\mathrm{mA}$ per FET) is applied and the drain source voltages are measured. This is repeated for $T_{\mathrm{coldplate}} = [20\,^{\circ}\mathrm{C}, 25\,^{\circ}\mathrm{C}, \ldots, 40\,^{\circ}\mathrm{C}]$ making sure the package temperatures of the FETs have settled to the new coldplate temperature between each step. Resulting is the linear relationship between forward voltage and junction temperature for each of the 3 switching elements (consisting of 2 parallel FETs each). The measurement setup is depicted in **Fig. 25** where SW is kept open during this calibration.

After this calibration is completed, the coldplate water is set back to its normal $20\,^{\circ}\mathrm{C}$, SW is closed, and $I_{\mathrm{load}} = 30\,\mathrm{A}$ is applied through the FETs in reverse (while also keeping I_{ref} enabled). After stabilization of the package temperatures, SW is opened again and V_{sd} is continuously measured to extract the junction cooldown transients using the calibration. The loss $P_{\mathrm{loss,S[1,2,3]n,[1,2],A}}$ in each of the FETs at the moment SW is opened can be retrieved from the package temperature using **Fig. 22**. By inverting the junction cooldown curves and shifting them into the origin, they become heating curves to which a second order Foster model,

$$Z_{\mathrm{th,ja}}(t) = \frac{T_{\mathrm{j}}(t) - T_{\mathrm{a}}}{P_{\mathrm{loss}}} = R_{\mathrm{th},1} \cdot \left(1 - \mathrm{e}^{\frac{-t}{R_{\mathrm{th},1} \cdot C_{\mathrm{th},1}}}\right) + R_{\mathrm{th},2} \cdot \left(1 - \mathrm{e}^{\frac{-t}{R_{\mathrm{th},2} \cdot C_{\mathrm{th},2}}}\right), \tag{26}$$

can be fitted using the estimated $P_{\mathrm{loss,S[1,2,3]n,[1,2],A}}$. Resulting is the thermal impedance as a function of time/frequency shown in **Fig. 26**. The frequency range on which the impedance can be estimated accurately is dependent on the measurement frequency of V_{sd}, which in the case of the used Keithley DAQ6510-7708 is around $3.25\,\mathrm{Hz}$. Meaning any effects with a higher frequency will not be captured by these measurements, this can also clearly be seen in **Fig. 26**. However, as the transient thermal impedance $> 10\,\mathrm{Hz}$ is dominated by the FET itself, the data for which is extracted from the datasheet, this shortcoming is acceptable. The differences between the measured and the simulated impedance can be explained by earlier mentioned differences in clamping force, voiding in the solder, and radiation to the air, none of which are accounted for in the simulation.

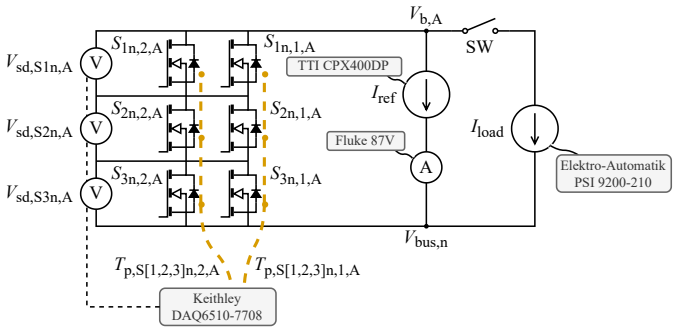


Fig. 25. Schematic measurement setup used to estimate the thermal impedance of the prototype. During the calibration of the V_{sd}, T_{j} curve, SW is kept open. To heat the FETs, SW is closed and I_{load} is applied, afterwards, SW is opened again and V_{sd} is continuously measured to extract the cooldown curve.

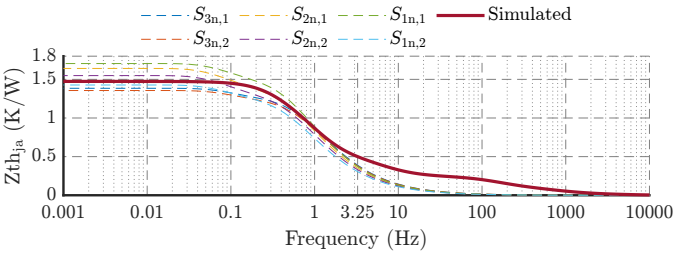


Fig. 26. Comparison between measured and simulated thermal impedance. The measurement was done at $3.25\,\mathrm{Hz}$, meaning any effects faster than that were not able to be captured. Up until this point, the measured impedance matches the simulated impedance closely.

VI. Conclusion

The relationships between design parameters (i.e. number of levels, branches, and parallel FETs, switching frequency, and filter design) and constraints related to output quality, control bandwidth, and lifetime have been investigated in this work. Furthermore, the effect of these constraints in the context of a cost-based optimization have been covered.

It has been shown that control and output-quality constraints bound the switching frequency, the number of levels, and the number of branches of potential FCC designs through the effective switching frequency. Reducing the RMS output voltage ripple from $10\,\mathrm{V}$ to $1\,\mathrm{V}$, doubles the minimum effective switching frequency that is required. Increasing the control bandwidth by a factor of 10 from $10\,\mathrm{kHz}$ to $100\,\mathrm{kHz}$ also requires the effective switching frequency to increase by one order of magnitude. These general relations have been shown to hold independently of the exact switching frequency, number of levels, or number of branches, as long as the effective switching frequency is correct. Similarly, the control and output-quality constraints are shown to limit each other for a fixed effective switching frequency, meaning that for an FCC design the maximum ratio between these two constraints is fixed. This ratio can be used to tweak an existing optimized FCC design to tailor to different constraints. This is most easily achieved through the switching frequency, making designs with a large potential switching frequency more flexible and thus easier to adapt to various requirements.

Despite not directly affecting the control and output-quality constraints, the number of levels is important for the cost optimization. As shown, the number of levels has a significant impact on the relationship between cost and control bandwidth, output voltage ripple, lifetime, and loss. It has been determined that this is due to the voltage margin on the semiconductor blocking voltage. For the optimal FCC, with 7 Levels and $650\,\mathrm{V}$ FETs, this margin is 38.5%. This large margin allows the FETs to sustain a higher switching frequency, lowering the costs of the filter inductors, and resulting in a flexible design. The more cost-effective designs have a FET current margin very close to their voltage margin, with the ideal 7-Level design having a negligible margin difference. This makes for a very clear design target for cost-effective FCC designs. The general constraint-cost relations are also valuable in the early stages of an FCC design optimization; knowing the cost implications of a certain constraint can motivate a potential customer to relax the requirement.

Acknowledgment

The author would like to thank Prodrive Technologies for providing the opportunity and support to conduct this very interesting research.

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