Comparison between logic families for multiphase clocking applications

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***Abstract*—IoT technology has created a need for low power consumption and high selectivity resulting from low phase noise. The Windmill frequency divider is a circuit that takes two input clocks, LO+ and LO- that are at 50% duty cycle and produces four 25% duty cycle signals with half the frequency of input clocks and having non-overlapping phases. [1] The windmill circuit is currently implemented using CMOS 22nm NOR gates; thus, this paper investigates the design of the exact windmill circuit but now also using a different logic family class namely PFSCL (positive feedback source coupled logic). [1] The two families of NOR gates are then designed to have the same operating speed of 6Ghz 10ps rise/fall time to have a fair comparison of power dissipation and phase noise. After that the CMOS NOR gate's maximum operational speed was found to be 40Ghz at 3ps rise/fall time. The PFSCL NOR was then designed to operate at this max operational speed by scaling. The phase noise and power dissipation were then plotted vs the input frequency for both logic families at 40Ghz and at 5 other frequencies below that to compare the behaviour of CMOS and PFSCL NOR. In the end, it was then determined that phase noise performance of the PFSCL was not too different compared to CMOS. However, PFSCL NOR dissipated 15.6 times more power than the CMOS NOR gate while keeping their speeds the same. The different family NOR gates were then used to construct entire Windmill circuits. The circuits were simulated using Cadence Virtuoso.**

***Index Terms*—NOR Gate, Impedance Scaling, Windmill Frequency divider, logic family, power dissipation, phase noise**

I. Introduction

The N-path filter is a circuit that can act as a narrow band band pass filter, and it requires N clock signals with N different phases that are non-overlapping clock phases with a 100/N percent duty cycle to turn ON or OFF the switches in figure 1 at the correct time. [2] The focus is on the N=4 or 4-path filter seen in figure 1 that requires four non-overlapping clock phases with a 25 percent duty cycle. [1] The standard oscillator signal has a 50 percent duty cycle clock, so in order to derive the 25 percent duty cycle clocks from the oscillator, An efficient circuit called the windmill frequency divider, as shown in figure 3 has been invented to produce these four clock signals [1]. Currently, the windmill circuit is implemented with CMOS logic, so this paper aims to design the same windmill circuit but with Positive Feedback Source Coupled Logic (PFSCL) . Consequently, a performance comparison between the CMOS and PFSCL versions of the circuit in figure 3 is made in order to see if there are any potential benefits to using such a PFSCL over CMOS logic in terms of power dissipation and phase noise. Because the fundamental unit of the windmill circuit is the NOR gate, the performance of the NOR gate of each logic family will be simulated and compared. Section II will describe briefly how the windmill frequency divider circuit. The section III will dive into the analysis of the CMOS NOR gate and Section IV will analyze the PFSCL NOR gate. The simulation results showing the difference in performance between the logic types will be shown in Section V. Section VI will a discuss the results and finally the conclusion will be drawn in Section VII to address the hypothesis that PFSCL logic type has better performance in terms of power consumption or phase noise when compared with conventional CMOS logic.

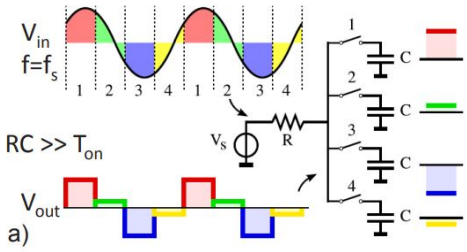

Fig. 1. 4-path circuit [2]

II. Working principle of a windmill frequency divider circuit

The Windmill frequency divider system takes in two inputs signals and produces four output signals. As can be seen in figure 2, the two inputs are the two differential 50 percent duty cycle local oscillator signals LO+ and LO- and the four outputs signals are Q1, Q2, Q3 and Q4 with non-overlapping phases and 25 percent duty cycle each. The entire circuit of the windmill frequency divider, as shown in figure 3 is composed of units like in figure 4 which is basically an **SR-latch** with one of its outputs connected to an **output NOR gate**. The SR latch is in turn is made up of NOR logic gates which makes the NOR gate the fundamental unit of the Windmill frequency divider circuit so designing and optimizing the **output NOR gate** circled in figure 5 for optimal speed or power would make the entire Windmill frequency divider circuit optimized for speed or power. This is the reason the focus of this paper will be first on designing and simulating each logic families

output NOR gate. Once the design specifications of this NOR gate is met then the output NOR gate is used as a building block to make the entire Windmill divider circuit. The NOR logic gate has two inputs **A** & **B** and one output **Q** with a truth table shown in Table I. In figure 4 the SR-latch produces an Enable signal E_1 that goes into one of the inputs of the output NOR gate, and the other input is the local oscillator clock $LO-$. The SR latch is made up of two NOR gates itself, which when the Q2 signal goes "High", and the Q4 signal is "Low", then the Enable is set to a "High" signal until Q4 goes "High" causing the Enable signal to go back to "Low". This process repeats producing E1 signal as shown in figure 4. When E1 and the LO- signal goes "Low" at the same time, this will cause the Q1 signal to go "High" as can be seen in figure 5, and this has the effect of every other "Low" of LO- causes Q1 to go "High". This way, the connection of four latches and four output NOR gates in figure 3 produces the four outputs Q1, Q2, Q3, and Q4 that have non-overlapping phases and a 25 percent duty cycle that the 4-path filter can use.

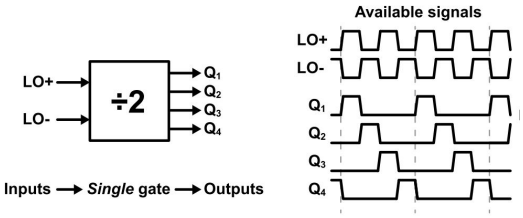

Fig. 2. Black box system of windmill frequency divider [1]

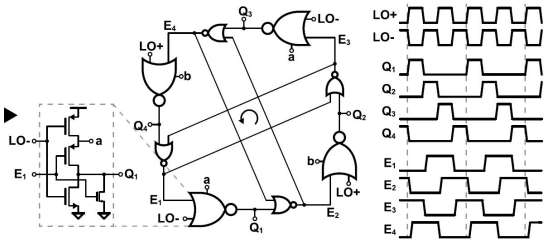

Fig. 3. The Windmill frequency divider circuit [1]

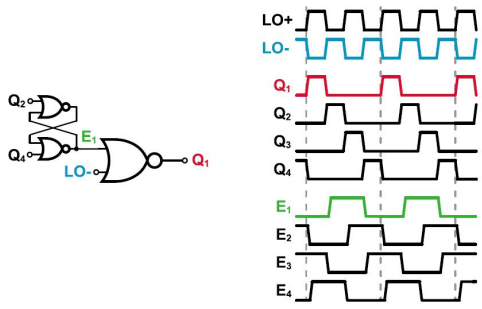

Fig. 4. The single unit of the frequency divider [1]

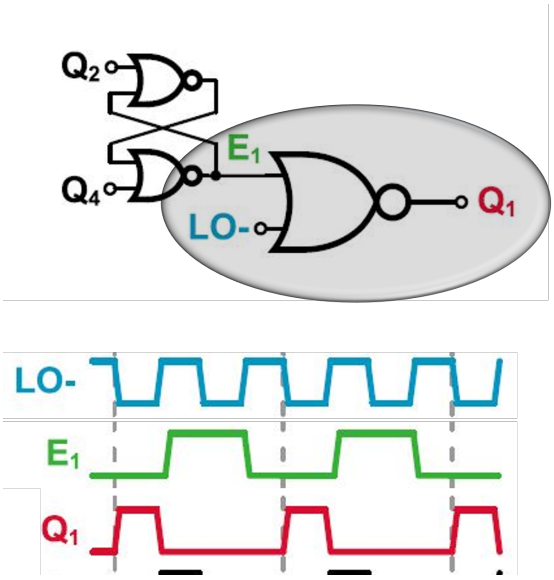

Fig. 5. The Output NOR gate is the circled NOR gate with LO and En as inputs [1]

TABLE I
TRUTH TABLE FOR A NOR GATE

input A	input B	output Q
0	0	1
0	1	0
1	0	0
1	1	0

The output NOR gate setup used to design for both CMOS and PFSCL in upcoming sections will look like figure 6 with vdd set as 0.8V, load capacitor $C0$ at 10fF and the parameters of V1 (Enable) and V2 (LO) shown in table II. The red variables such as P and F in table II are the design variables that will be changed in the Analog Design Environment (ADE) depending on the design specifications needed.

TABLE II
LO AND ENABLE PARAMETER VALUES

name	***V1 (En)***	***V2 (LO)***
Voltage 1	0V	0V
Voltage 2	800mV	800mV
Period	1/(F*0.5)	1/F
Rise time	1/(P*F)	1/(P*F)
Fall time	1/(P*F)	1/(P*F)
Type of rising & falling edge	halfsine	halfsine

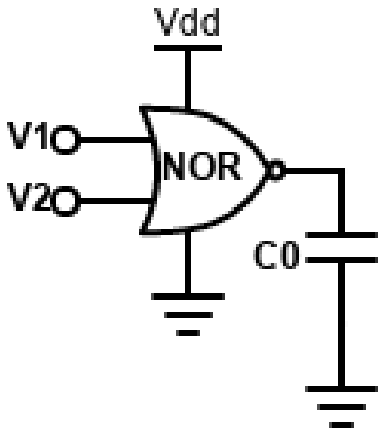

Fig. 6. The Output NOR gate setup used for both CMOS and PFSCL is shown here

III. CMOS Analysis

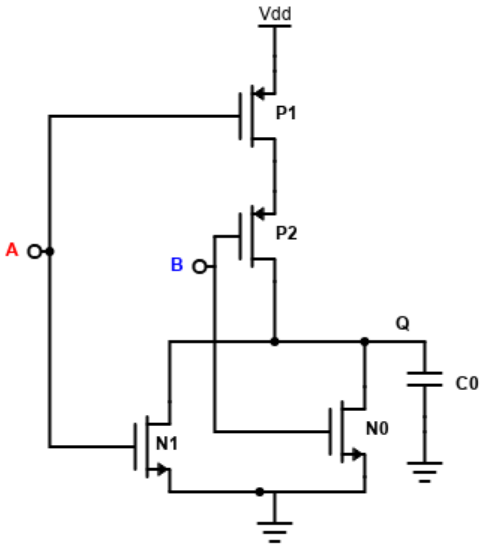

Fig. 7. NOR gate implemented with CMOS logic [1]

A. CMOS NOR-gate working principle

The output NOR gate of figure 5 is a CMOS-NOR gate as shown in figure 7 where A = LO- and B = EN are inputs to the nor gate, and Q is the output. The P1 and P2 are both PMOS transistors that turn ON when a "Low" logic is applied at the gate whereas the N1 and N0 are both NMOS transistors that turn on when a "High" logic is applied at the gate. This means output Q is either pulled up to the supply ("High") or pulled down to the ground ("Low") depending on the value of inputs A and B. The working of the CMOS NOR gate can be summarised by Table III.

TABLE III
TRUTH TABLE AND TRANSISTOR STATE FOR A CMOS NOR GATE

input A	input B	P1	P2	N1	N0	output Q
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

The actual schematic used in the cadence simulator can be seen in figure 8

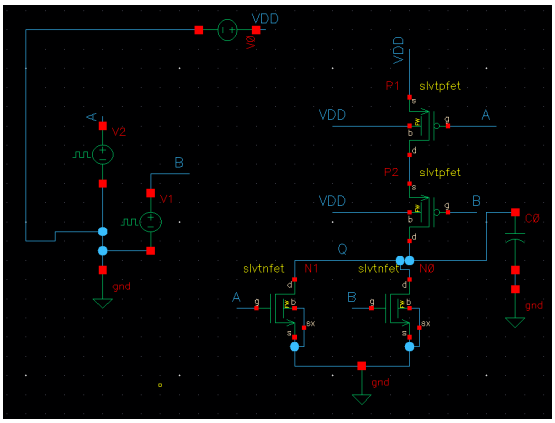

Fig. 8. CMOS NOR setup in cadence

B. Sizing the PMOS transistors to achieve equal rise & fall times

As can be seen in figure 7, the pull-up path consists of PMOS transistors P1 and P2 in series and similarly the pull-down path consist of NMOS transistors N1 and N0 in parallel. The effective resistance of the pull-up path R_{pullU} must match the effective resistance of the pull down path R_{pullD} in order to have equal rise & fall times. [3] If all of the transistors are set as minimum sizing so gate finger width is set as 80nm then lets assume for simplicity that the resistance of each PMOS and NMOS is R as shown in left of figure 10. However in general this is not the case due to the slight difference in $\mu_{eff}C_{ox}$ of NMOS and PMOS. Looking at left of figure 10, It can be seen that the NMOS pull-down impedance's are in parallel, so the effective pull-down resistance is $R_{pullD} = \frac{R}{2}$ and the PMOS pull-up impedance's arranged in series, so the effective pull-up resistance is $R_{pullU} = 2R$. This means that R_{pullU} is significantly larger than R_{pullD} which causes the rise time to be larger than the fall times as can be seen in figure 9 with gate finger width set to 80nm and nf (integer number of fingers) is scaled up for all the transistors. Equal rise and fall time can be achieved by reducing the effective pull-up Resistance of the PMOS to also be $\frac{R}{2}$ which means each pull-up PMOS transistor should have a resistance of $\frac{R}{4}$ as shown in right side of figure 10. This decrease in resistance R_{pmos} in eq 1 by a factor of four is achieved by increasing

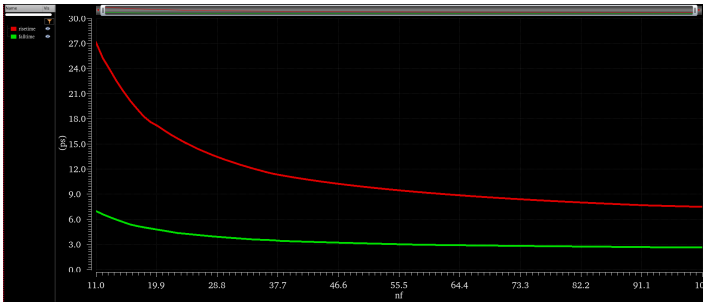

Fig. 9. Rise/fall time before sizing PMOS

TABLE IV
TRANSISTOR PARAMETER VALUES OF CMOS NOR GATE

name	***P1 & P2***	***N0 & N1***
Description	Super-low Vt PFET	Super-low Vt NFET
Multiplier	M	M
Dimension Mode	FingerWidth	FingerWidth
Gate Finger Width	400nm	80nm
Length	20nm	20nm
number of gate fingers	nf	nf

gate finger width W or aspect ratio of both PMOS transistors by a factor four as shown in figure 11. But this is under the assumption that the resistance of the PMOS R_{pmos} and NMOS R_{nmos} in eq 2 are equal for the same aspect ratio but this is not the case in reality because $\mu_{eff}C_{ox}$ of the PMOS is different than that of the NMOS transistor so to compensate for this difference the W or gate finger width of PMOS is increased by five times (W = 400nm) instead of four times (320nm).The final parameter values of the transistors of CMOS-NOR gate is shown in table IV.

$$R_{pmos} = \frac{1}{\mu_{eff}C_{ox}\frac{W\times nf}{L}(V_{GS} - |V_{th}|)} \quad (1)$$

$$R_{nmos} = \frac{1}{\mu_{eff}C_{ox}\frac{W\times nf}{L}(V_{GS} - V_{th})} \quad (2)$$

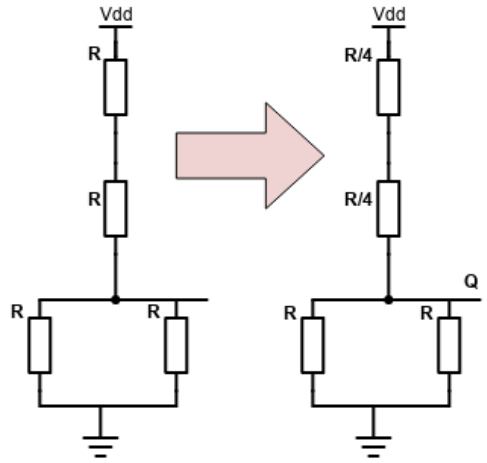

Fig. 10. (left) $R_{pullU} \neq R_{pullD}$. (right) $R_{pullU} = R_{pullD}$

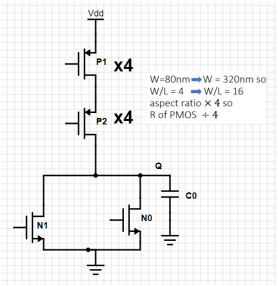

Fig. 11. W of PMOS is increased to 320nm from 80nm would theoretical mean resistance of PMOS is reduced by factor of 4

C. Design Approach to get a 6Ghz output with 10ps rise and fall time

TABLE V
ADE VARIABLE VALUES FOR CMOS 6GHZ OUTPUT WITH 10PS RISE/FALL TIME

ADE variable	***Value***
F	12G
P	9
M	1
nf	8
Harm	20

To get a 6Ghz output the input LO signal must have a frequency of 12Ghz so the variable F is set to 12Ghz as can be seen in the ADE table V. The previous subsection III-B made the rise/fall times equal even when nf impedance scaling is done as can be seen in the figure 12. Looking at equation 1 or 2, It can be seen that nf is an integer number that gets multiplied with Width W which has the effect of decreasing resistances of all the transistors by the same factor nf. This Reduction in the R_{pullU} & R_{pullD} in turn reduces the $\tau_1 = R_{pullU}Cout$ (influencing rise time) and $\tau_2 = R_{pullD}Cout$ (influencing fall time) at the beginning. [3]

This improvement to the rise/fall time at the beginning (small nf) is due to the fact that the 10fF load capacitance $C0$ is still dominating the increase in MOSFET parasitic capacitance C_p when the gate width is increasing by nf as can be seen in figure 14. After around nf = 30, this C_p will begin to dominate the 10fF $C0$ and reach a steady state rise/fall time value. At this point the rise/fall time doesn't improve anymore because the rate at which the R_{pullU}/R_{pullD} decreases will be the same as the rate C_p increases. Now increasing or decreasing rise/fall time to the desired value if a matter of scaling all the transistors equally with nf. To get a 10ps rise and fall time all the transistors can be scaled up by increasing the number of fingers to 8 to get 10ps as can be seen in figure 12. The transient waveform of the output Q at 6Ghz and 10ps rise/fall time can be seen in figure 13.

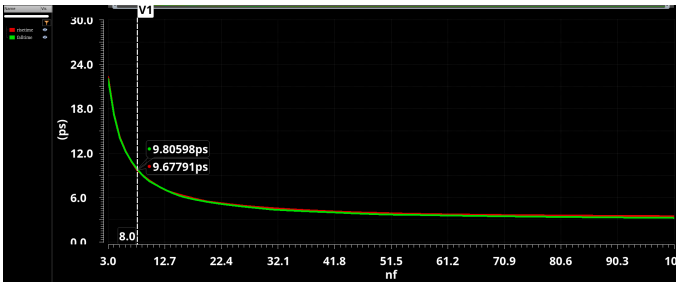

Fig. 12. number of fingers = 8 gives a rise&fall time around 10ps

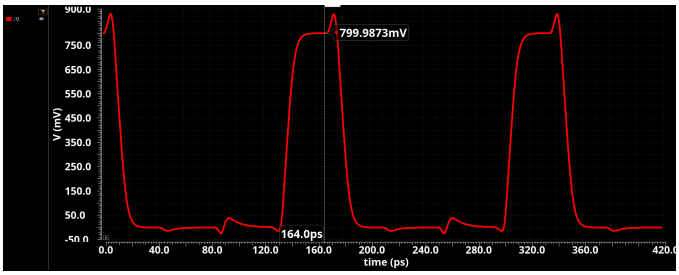

Fig. 13. Transient response of the output Q at 6Ghz with 10ps rise/fall time

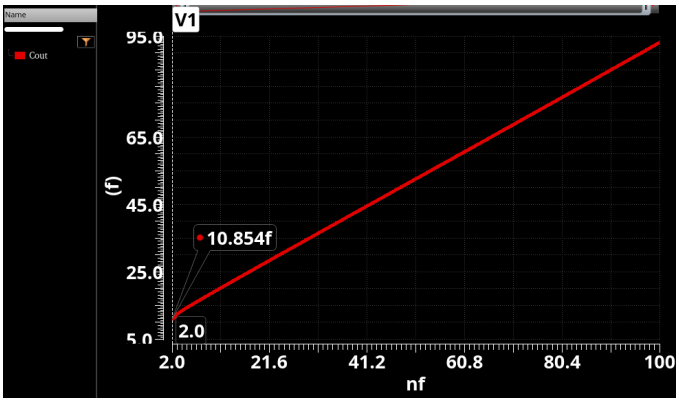

Fig. 14. cout = cload at the beginning but as you scale up the parasitic capacitance increases

D. Measuring power dissipation for the 6ghz and 10ps rise/fall time output Q

The power dissipation in the case of CMOS NOR gate is mainly due to the charging and discharging the capacitors (parasitic and load) meaning there is a current spike when charging and then the energy is dumped into ground when the capacitor discharges. [4] The current only spikes when charging the capacitors and at other times there is no static current flow therefore the nor gate is not consuming any power when the output is at logic "High" or "Low" but only consumes power when switching from "High" to "Low" and vice versa therefore the static power dissipation is zero. [4] The main power dissipation is mainly dynamic power dissipation due to charging and discharging the capacitor (switching) and the formula to calculate this can be found in equation 3. [4] The capacitance C_{out} is the total capacitance which includes the parasitic and the 10fF load capacitance. This capacitance can be calculated by first measuring the current at the node (circled in green) coming out from the voltage source vdd in figure 16. This measured current (green waveform) can be seen in figure 15 for a single period of Q (red). This current is integrated for a a single period of Q and then dividing the integral result by the supply voltage V_{DD} as can seen in equation 5. This equation is basically the element equation of a capacitor which is equation 4 rearranged to make C_{out} the subject.

$$\begin{aligned} P_{dynamic} &= C_{out} * V_{DD}^2 \times f \\ &= 17.09fF * 0.8^2 * 6Ghz \\ &= 65.63\mu W \end{aligned} \tag{3}$$

$$V = \frac{1}{C_{out}} \int_0^T idt \tag{4}$$

$$C_{out} = \frac{1}{V_{DD}} \int_0^T idt \tag{5}$$

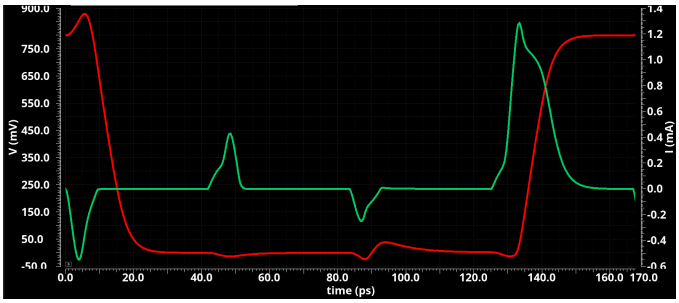

Fig. 15. Current taken from the pss

E. Measuring phase noise for the 6ghz and 10ps rise/fall time output Q

The periodic steady state (Pss) analysis and Pnoise are the tools used when analysing noise. The pss linearises the circuit around a periodic steady state operating point. Phase noise

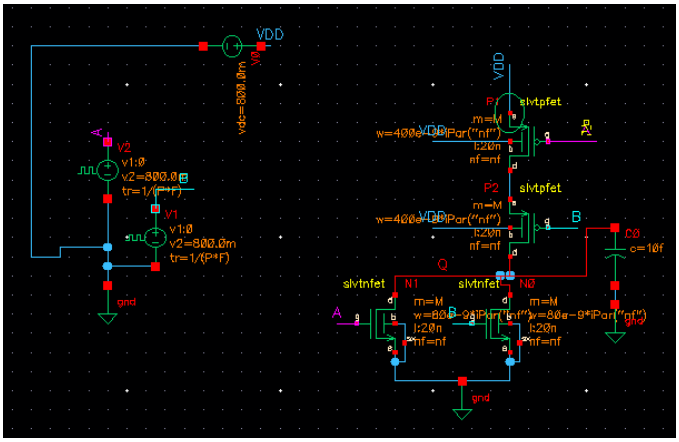

Fig. 16. Current spike in figure 15 measured at the node circled in green causing dynamic power dissipation

is short term random changes to the phase of the output waveform which is caused by jitter. phase noise is in the frequency-domain of the noise spectrum surrounding the clean oscillator signal in this case the input LO signal Whereas jitter is a time domain variation from its original zero crossing. [5] [6] The flat part of the phase noise curve is the most important because that's the side band or unwanted frequencies. A clean signal would be just a single vertical peak and not have these side bands. the relative frequency at which the phase stagnates is 100Mhz as can be seen in figure 17 which gives a phase noise of -162.2 dBc/Hz.

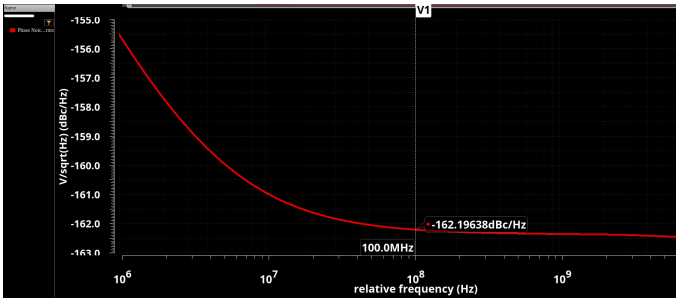

Fig. 17. phase noise of the CMOS-NOR gate at 100Mhz relative frequency

F. Design approach to find the maximum operating speed of CMOS NOR gate

The maximum operational frequency can be found by sweeping the frequency from 20Ghz to 60Ghz and then observing the output Q waveforms to see at which frequency the waveform still giving a proper 0.8V swing and staying at 0.8V for some time (flat section). Also not having a significant peaking effect caused by the clock feed through. Looking at figure 18 this was found to be 40Ghz.

To get the maximum speed the rise/fall time must be as small as possible. This done by scaling up the nor gate to see the CMOS max operating speed where the rise and fall time stagnates (parasitic's dominate over the load capacitor)

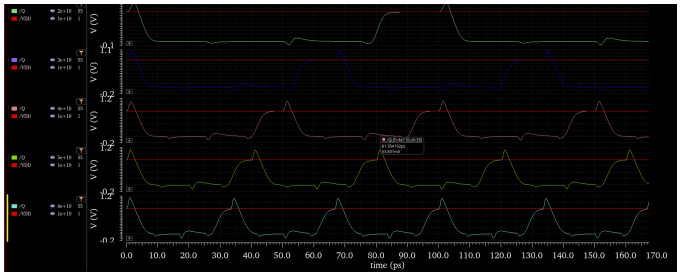

Fig. 18. 40Ghz chosen as maximum operating frequency

and this happens because the rate at which resistance of the transistors decreases is same as the rate at which capacitance increases by increasing the nf (scaling up) for all the transistor. At the beginning the parasitic capacitance keeps increasing but the load capacitance is still dominating. Its also important to choose nf that's reasonable because doubling nf would double the power dissipation with little to no improvement in the rise/fall time therefore nf = 55 was chosen as can be seen in figure 19 which gave the a rise/fall time of around 3ps.

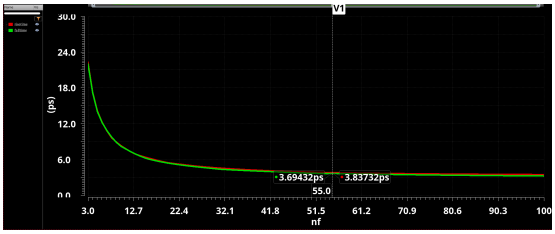

Fig. 19. nf = 55 chosen to get maximum operating speed of 3ps rise/fall time

IV. PFSCL ANALYSIS

TABLE VI
TRUTH TABLE AND TRANSISTOR STATE FOR A PFSCL NOR GATE

A	B	N2	N0	N1	$I_{ss}flow$	output Q
0	0	OFF	OFF	ON	Right branch	1
0	1	OFF	ON	OFF	Left branch	0
1	0	ON	OFF	OFF	Left branch	0
1	1	ON	ON	OFF	Left branch	0

A. PFSCL NOR-gate working principle

The PFSCL (Positive feedback source coupled logic) NOR-gate can can be seen in figure 20 where A = LO- and B = EN are inputs to the nor gate, and node Q is the output. The Cadence setup is shown in figure 21. Looking at figure 20, when both the inputs A and B are logic "Low" (0v), the transistor's N2 and N0 is OFF, and therefore output Q is at the logic "High" (V_{dd} this means the feedback transistor N1 turns ON, steering all bias current I_{ss} to the right branch. When inputs A and/or B are logic "High" (0.8v), N2 and/or N0 draws the bias current I_{ss} on the left branch and Q is at the logic "Low" ($Vdd - R_dIss$) due to the voltage drop across output load resistor R_1. Therefore, the logic swing or

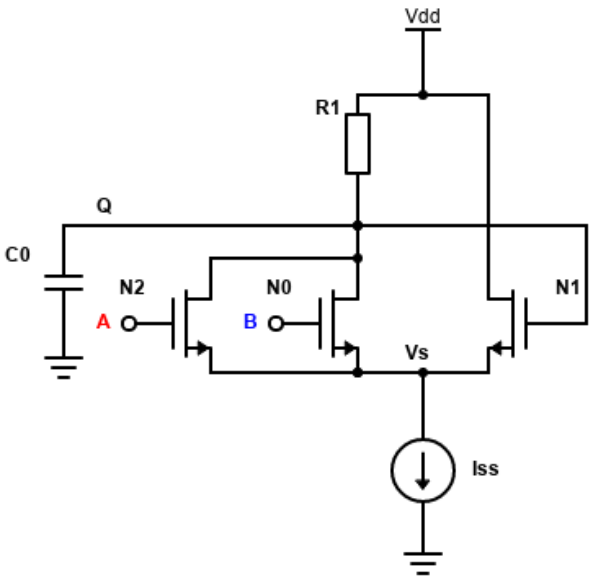

Fig. 20. PFSCL Output NOR gate

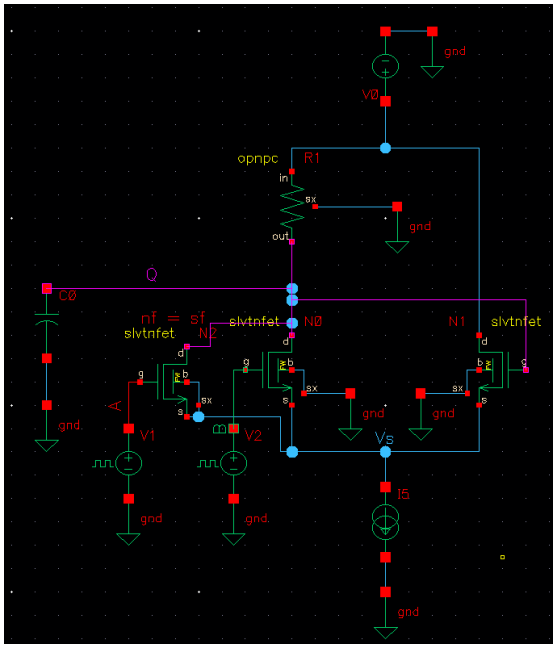

Fig. 21. PFSCL NOR setup in cadence

V_{swing} is given by $I_{ss}R_1$. To get this full V_{swing} the feedback transistor N1 should be fully OFF so that all of the tail current I_{ss} flows through the left branch. This can be accomplished if the V_{GS} of N1 is less than its threshold voltage of 0.2V. One of the reasons V_s in figure 20 should be large enough so at 0.2V is to make sure that the V_{GS} is less than or equal to the threshold voltage and the other reason is to have enough headroom for the tail current source I_{ss}. The working of the PFSCL NOR gate can be summarised by Table VI. Taking all of this into consideration the following design requirements are formulated in Table VII.

TABLE VII
PFSCL REQUIREMENTS

Design Variable	***Value***
$QHigh = V_{dd}$	0.8V
$V_{swing} = I_{ss}R_1$	0.4V
$QLow = V_{G_{N1}} = V_{dd} - V_{swing}$	0.4V
V_s	0.2V
c_0	10fF
duty cycle	25%

B. Clock feedthrough affecting rise and fall time and duty cycle

The ADE variable P in Table XI was initially set to 16 to have input rise/fall times be 1/16th of the input period of LO which is very small but this led to undesirable peaking behaviour shown in the red output signal in figure 23. The phenomenon is called **Clock Feedthrough** which is caused by the coupling capacitance from the gate to both the source and drain of the MOSFET transistor as shown in fig 22 . When the clock becomes logic "Low", a capacitive voltage divider forms between the gate/drain and load capacitor C0 which results in ripples at the output (circled in purple) in figure 23. [7] The difference between the ON flat part (0.8V) and the max peaking is called the clock feedthrough voltage error. This effect is caused by parasitic capacitance of the MOSFET which explains why the clock feedthrough voltage error becomes larger with the number of fingers and at higher frequencies. When the input voltage falls almost instantaneously, the parasitic capacitance's opposes this sudden change of the voltage at the output causing a distortion to the output resulting in unequal rise/fall times. [8] A slower input voltage signal means a longer time for the MOSFET currents to compensate for the coupling voltage, resulting in a reduction in the clock feedthrough voltage error. This is done by reducing P to 9 to have a slower input voltage signal giving the green output voltage signal with reduced clock feedthrough voltage error as can be seen in figure 23.The duty cycle does increases because the off time is being eaten by the increased rise/fall time. [8]

C. Sizing transistors, load and tail current to get correct NOR-gate function

For this part inputs A and B are both set as 0.8V DC voltages and R1 is set as 2500Ω. In order to achieve the requirement of Vswing = 0.4V, the Iss is set to $\frac{Vswing}{R1} = \frac{0.4V}{2500\Omega}$ as can be seen in ADE table XI. Also the gate finger widths of all the three transistors are by default minimum sized so W = 80nm and all lengths are 20nm. But since the PFSCL gate in figure 20 is basically like a differential pair, the MOSFET on the left must match the equivalent MOSFET on the right branch just like the PFSCL inverter. [10] That is why the parallel NMOS transistors N2 and N0 gate have

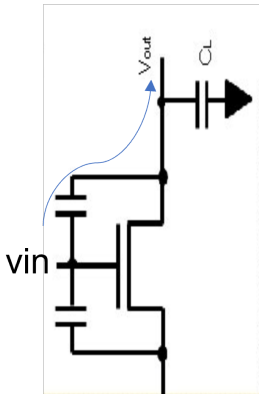

Fig. 22. Coupling capacitor [9]

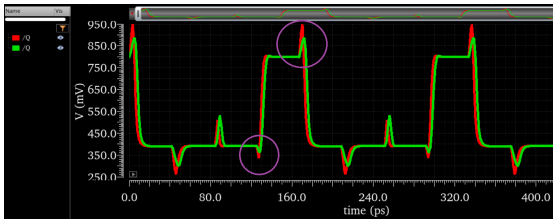

Fig. 23. Distortion introduced by feedthrough reduced (green) by increasing slew rate

their gate finger width doubled to 160nm while keeping the single NMOS transistors N1 with gate width 80nm on the right branch. But these sizes gives a Vs voltage of only 136mV which is not large enough to reduce the Vgs of the feedback MOSFET N1 below its threshold voltage (V_{th}). This means some of Iss still flows through the right branch and the left branch gets only a part of Iss so decreasing voltage drop acrross R1 and therefore reducing Vswing. The Vs voltage can be set to a value larger that 136mV by increasing all transistors gate fingers widths by a factor K as shown in figure 24. It turns out that $K = 3$ gave a Vs = 296mV as seen in figure 25 which makes $VgsofN1 = 400mV - 296mV = 104mV$ which is less that the V_{th} of 200mV ensuring that N1 is OFF and all Iss flows though the left branch as shown in the last three rows of table VI and also ensuring a maximum Vswing of 0.4V and headroom for the tail current source. The final transistor, resistor and tail current parameter values for the PFSCL-NOR gate is shown in table VIII, IX and X.

TABLE VIII
TRANSISTOR PARAMETER VALUES OF PFSCL NOR GATE

name	*N0 & N2*	*N1*
Description	Super-low Vt NFET	Super-low Vt NFET
Multiplier	M	M
Dimension Mode	FingerWidth	FingerWidth
Gate Finger Width	480nm	240nm
Length	20nm	20nm
number of gate fingers	sf	sf

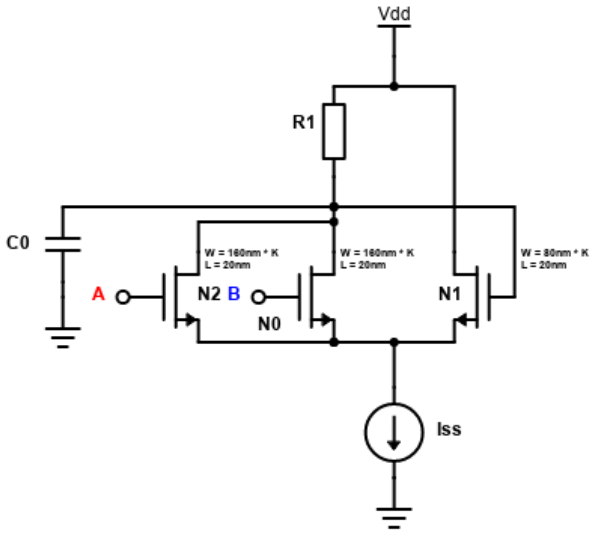

Fig. 24. transistor gate finger widths increased by factor K

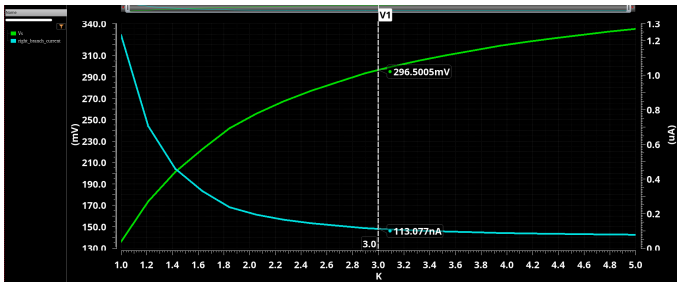

Fig. 25. K = 3 is chosen since Vs is 296mV and right branch current goes to zero

D. Design Approach to get a 6ghz output with 10ps rise and fall time

Using the parameters in table VIII with sf and M set to 1 gives a max operating speed of around 3Ghz because the signal starts loosing it flat portion after that. To get a 6Ghz output the A = LO signal must have a frequency of 12Ghz so the variable F in ADE table XI is set to 12Ghz. The R1 is

TABLE IX
OPNPCRES RESISTOR PARAMETERS

name	*R1*
Strip Width	265.6e-6/Rd

TABLE X
BIAS CURRENT SOURCE PARAMETERS

name	*I5*
DC current	iss

the output impedance of the PFSCL circuit and it is part of the time constant τ so reducing the R1=Rd value will increase the speed of the NOR gate by reducing rise/fall times. [11] The way the impedance scaling works is similar to CMOS but this time the R of the MOSFET and the R1 decreases while Iss increases to maintain the voltage swing. PFSCL NOR gate is scaled as shown in figure 26. When sf is increasing at the start the load capacitance is still dominating that is why the decrease in Rd improves the rise/fall times until the point where the parasitic capacitance starts to dominate the load and causing rise/fall to not improve anymore. The scale factor sf is increased to 8 to get to get 10ps rise fall time as can be seen in figure 27. Note that the sf is the number of fingers parameter in table VIII. The sf is also used to scale up Iss to maintain Vswing of 0.4V. The implementation of this scaling can be seen in the ADE in figure XI.

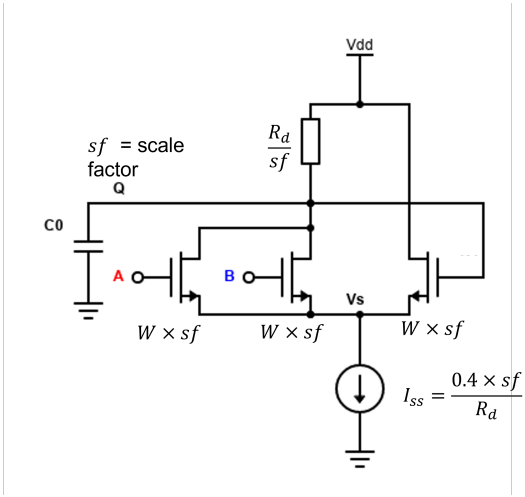

Fig. 26. scaling rule for PFSCL

TABLE XI
ADE VARIABLE VALUES FOR PFSCL 6GHZ OUTPUT WITH 10PS RISE & FALL TIME

ADE variable	*Value*
F	12G
P	9
M	1
sf	8
Rd	2.5K/sf
iss	0.4/Rd

E. Measuring power dissipation for the 6ghz and 10ps rise/fall time output Q

Unlike CMOS for PFSCL there is constant current Iss flowing through the circuit at all times even when the input is not switching between "High" and "Low" signals. This mode of power is called static power dissipation calculated as shown in eq 6. [4]. There is also some dynamic power dissipation caused by the input switching between "High" and "Low"

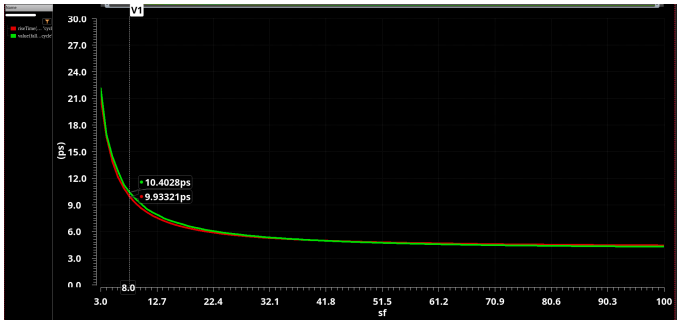

Fig. 27. scaling factor = 8 gives rise&fall tine around 10ps

power dissipation when charging and discharging the load and parasitic capacitance's. This dynamic power is calculated by first measuring the power when switching (P1) which includes static + dynamic power and then measuring the power when not switching (P2) which is only static power and then the difference is the dynamic power as calculated in equation 7.

$$\begin{aligned} P_{static} &= V_{DD} \times I_{ss} \\ &= V_{DD} \times \frac{V_{swing}}{R_D} \\ &= 0.8V \times \frac{0.4V}{312.5\Omega} \\ &= 0.8V \times 1.28mA \\ &= 1.024mW \end{aligned} \tag{6}$$

$$\begin{aligned} P_{dynamic} &= P1 - P2 \\ &= 1.058mW - 1.024mW \\ &= 34\mu W \end{aligned} \tag{7}$$

F. Measuring phase noise for the 6ghz and 10ps rise/fall time output Q

The phase noise for PFSCL measurement can be seen in figure 28. The relative frequency at which the phase noise stagnates is 100Mhz as can be seen in figure 28 which gives a phase noise of -157.2 dBc/Hz.

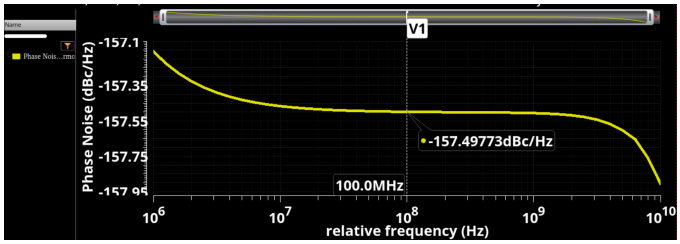

Fig. 28. phase noise of the PFSCL-NOR gate at 100Mhz relative frequency

G. Design approach to match the CMOS maximum operational speed

The solution is to the set the LO Frequency F to 40Ghz and scale up sf to a reasonable value to reduce the Rd and therefore reduce the rise/fall time to around 3ps. A reasonable

value for sf = 55 was found because increasing sf more than this introduces undesired peaking in the output waveform and increases static power dissipation with little to no improvement in rise/fall times.

TABLE XII
ADE VARIABLE VALUES FOR PFSCL 20GHZ OUTPUT WITH 4PS RISE & FALL TIME

ADE variable	*Value*
F	40G
P	9
M	1
sf	55
Rd	2.5K/sf
iss	0.4/Rd

V. RESULTS

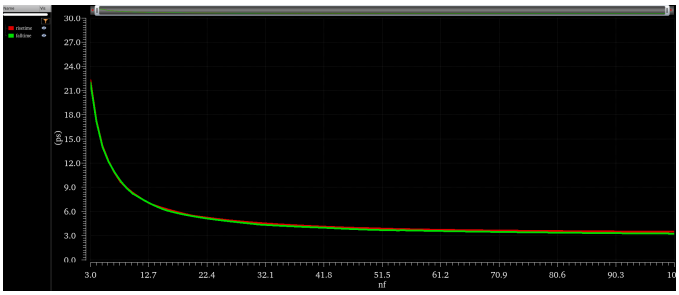

Fig. 29. CMOS: equal Rise/fall time after sizing as shown in table IV

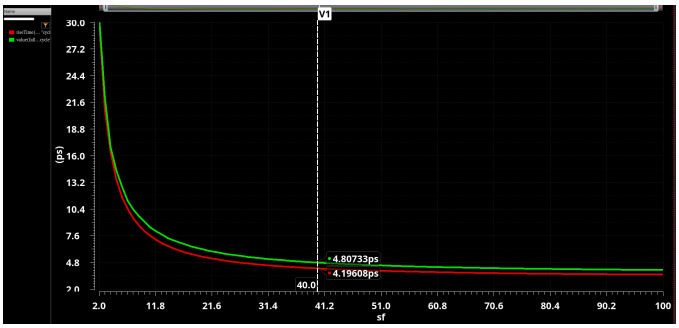

Fig. 30. PFSCL: not equal Rise/fall time when P = 16

TABLE XIII
POWER DISSIPATION AND PHASE NOISE COMPARISON AT 12GHZ 10PS RISE/FALL TIME

Family	*Power*	*phase noise*
CMOS NOR	65.63μW	-162.2 dBc/Hz
PFSCL NOR	1.024mW	-157.2 dBc/Hz

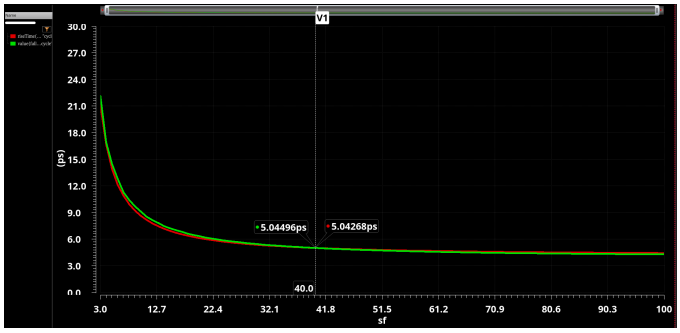

Fig. 31. PFSCL: equal Rise/fall time after P is increased to 9 as shown in table XI

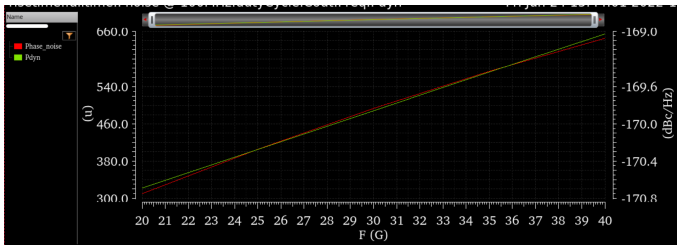

Fig. 32. Dynamic Power dissipation and phase noise plotted against frequency for CMOS

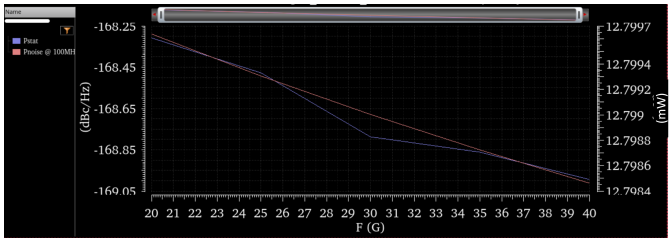

Fig. 33. Static Power and phase noise plotted against frequency for PFSCL

TABLE XIV
PFSCL 12GHZ 10PS OUTPUT$_{c}haracteristics$

Name	*Value*
Rise time	9.941ps
Fall time	10.4ps
Pstat	1.024mW
Pnoise@100Mhz	-157dBc/Hz
DutyCycle	29.19%
feedthrough peak value	851mV
Vswing	403.8mV
Vgs of N1	198.9mV
Freq	6Ghz

TABLE XV
CMOS 12GHZ 10PS OUTPUT$_{c}haracteristics$

Name	*Value*
Rise time	9.597ps
Fall time	9.634ps
Cout	16.78fF
Pdyn	63.76uW
Pnoise@100Mhz	-162.4dBc/Hz
DutyCycle	28.45%
Freq	6Ghz

VI. DISCUSSION

The values in table XV & XIV are all the output characteristics of PFSCL and CMOS at 12Ghz and 10ps rise /fall time and the nor gates seem to work as expected. It can be seen that the rise/fall times have been fixed for both PFSCL and CMOS in figures31 & 29. It can be seen in Table XIII that the CMOS NOR gate consumes 15.6 times less power than the power dissipation of the PFSCL nor gate for the same speed. Looking at figure 32 and figure 33 it can be seen that at the maximum frequency of CMOS, The CMOS has a smaller power dissipation of 660uW and phase noise of -169 dBc/Hz whereas PFSCL has a power dissipation of 12.8mW and phase noise of around -169 dBc/Hz. This result is only accurate for the last frequency because its nf is not reduced for the lower frequencies so only the last point can be used to fairly compare the NOR-gates.

VII. CONCLUSION

In conclusion the performance of NOR gates for PFSCL and CMOS are compared. By looking at the obtained results it can be concluded that the CMOS logic family is the better logic family when compared to PFSCL due to extreme low power consumption. The phase noise was found to be about the same for both PFSCL and CMOS. An attempt was made to combine the NOR gates to form the windmill divider as can be seen in the Appendix in order to optimize them but due to time constraints this was not explored further. The final conclusion did not agree with the original hypothesis that PFSCL could be a better logic type than CMOS logic family for this application.

VIII. APPENDIX

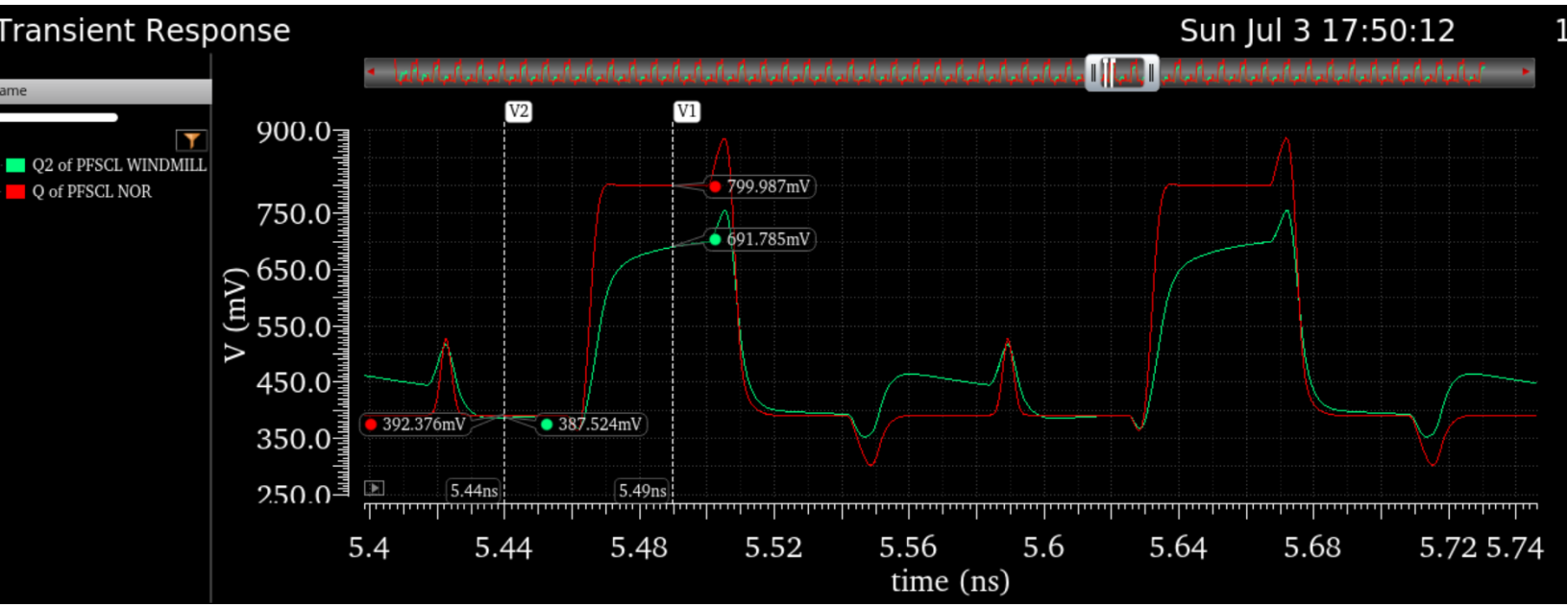

Fig. 34. Q waveform of a single PFSCL NOR gate vs Q2 of PFSCL Windmill divider for sf = 55 12Ghz Input

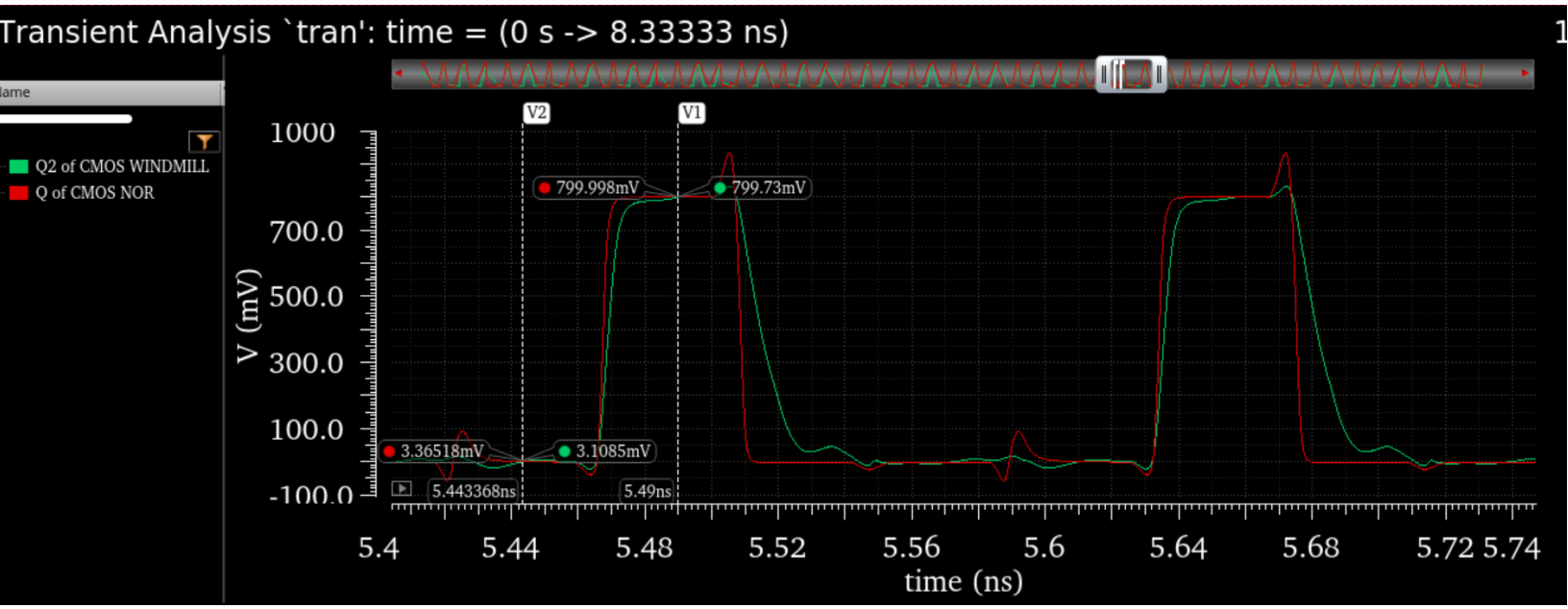

Fig. 35. Q waveform of a single CMOS NOR gate vs Q2 of CMOS Windmill divider for nf = 55 12Ghz Input

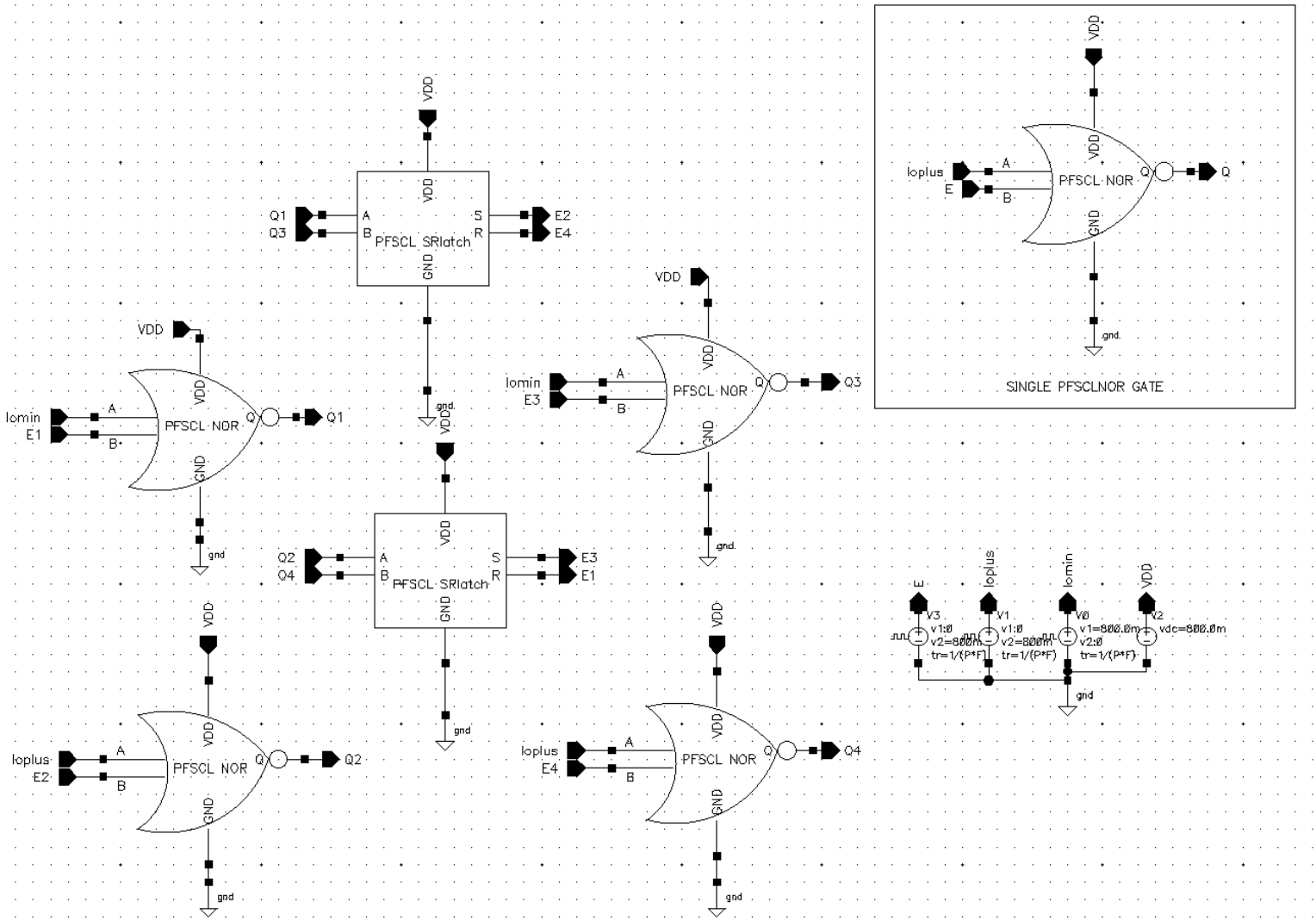

Fig. 36. PFSCL windmill

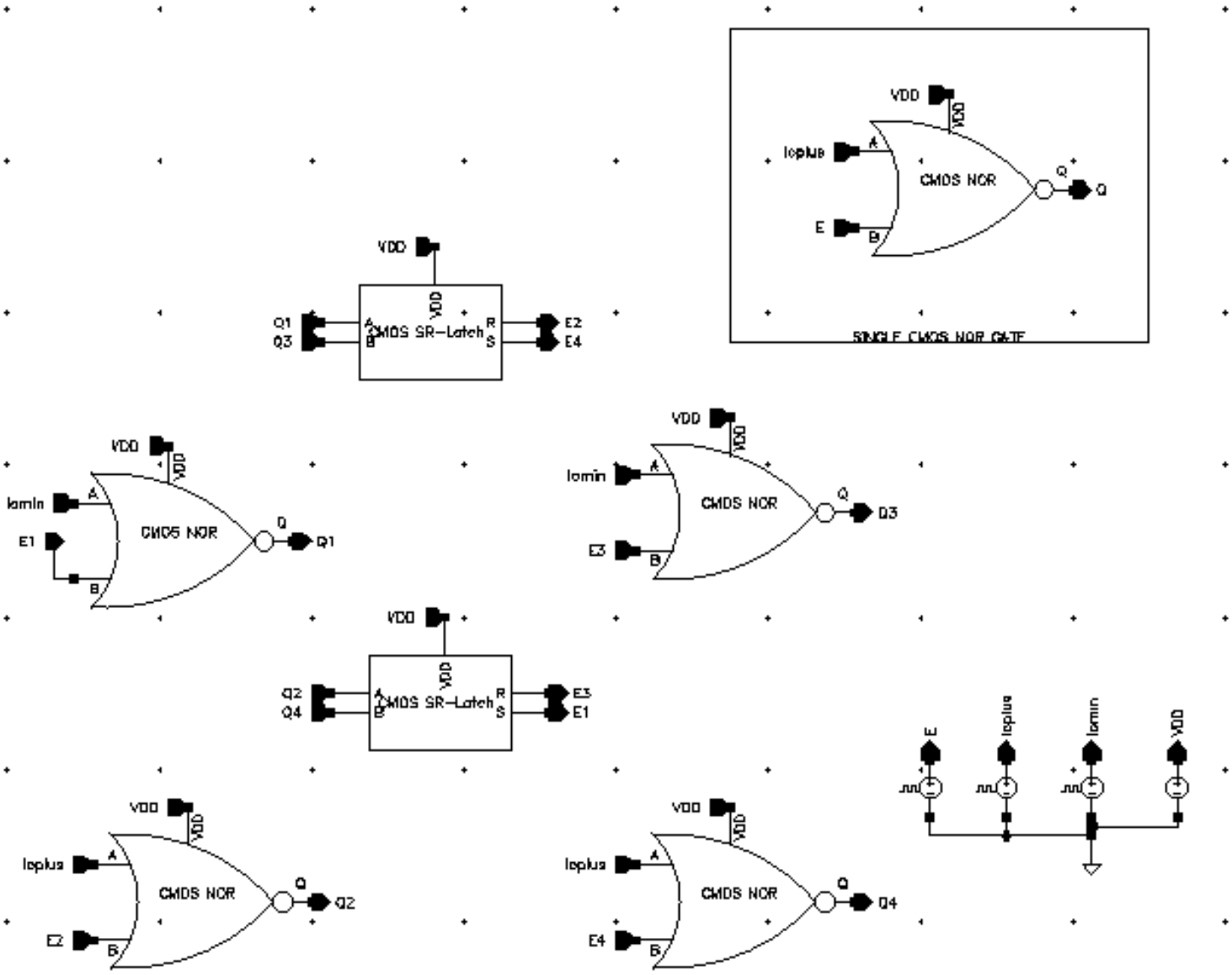

Fig. 37. CMOS windmill

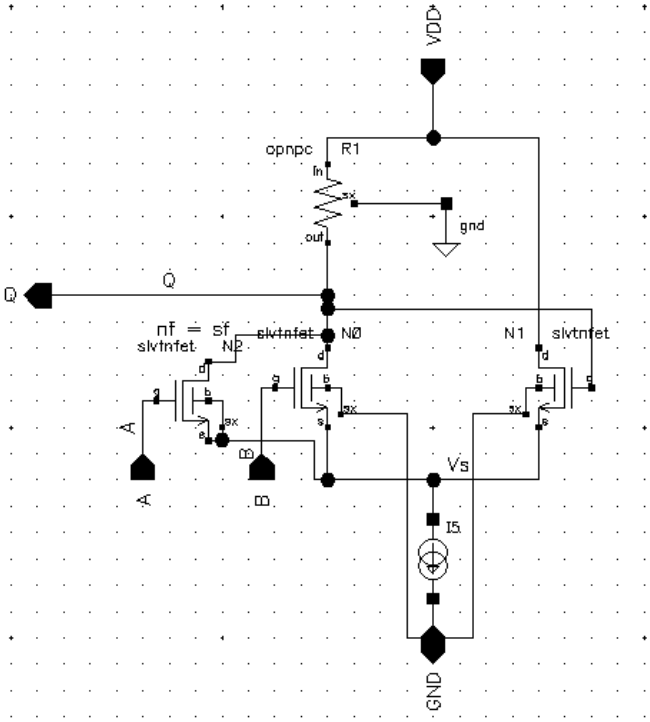

Fig. 38. PFSCL NOR Symbol

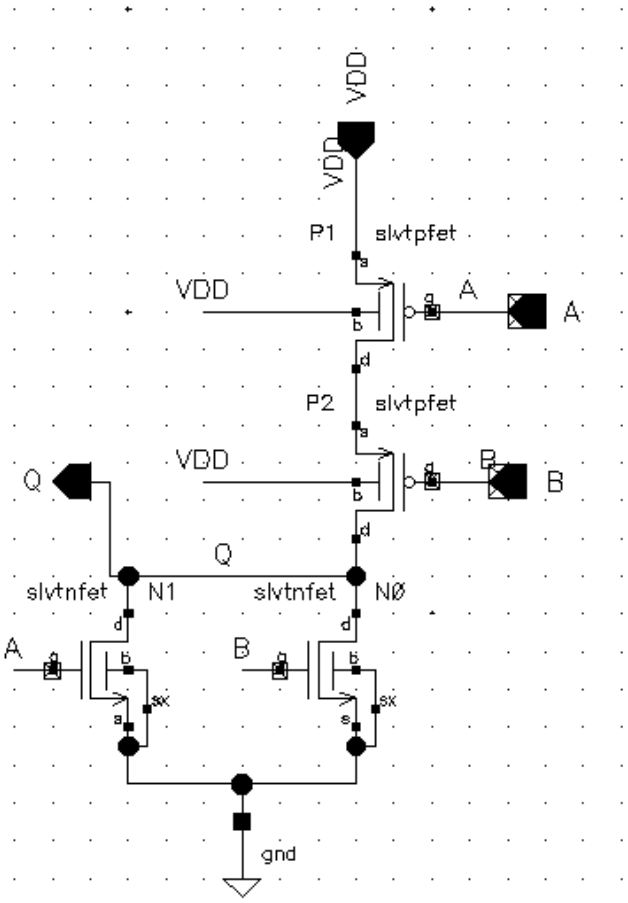

Fig. 39. CMOS NOR Symbol

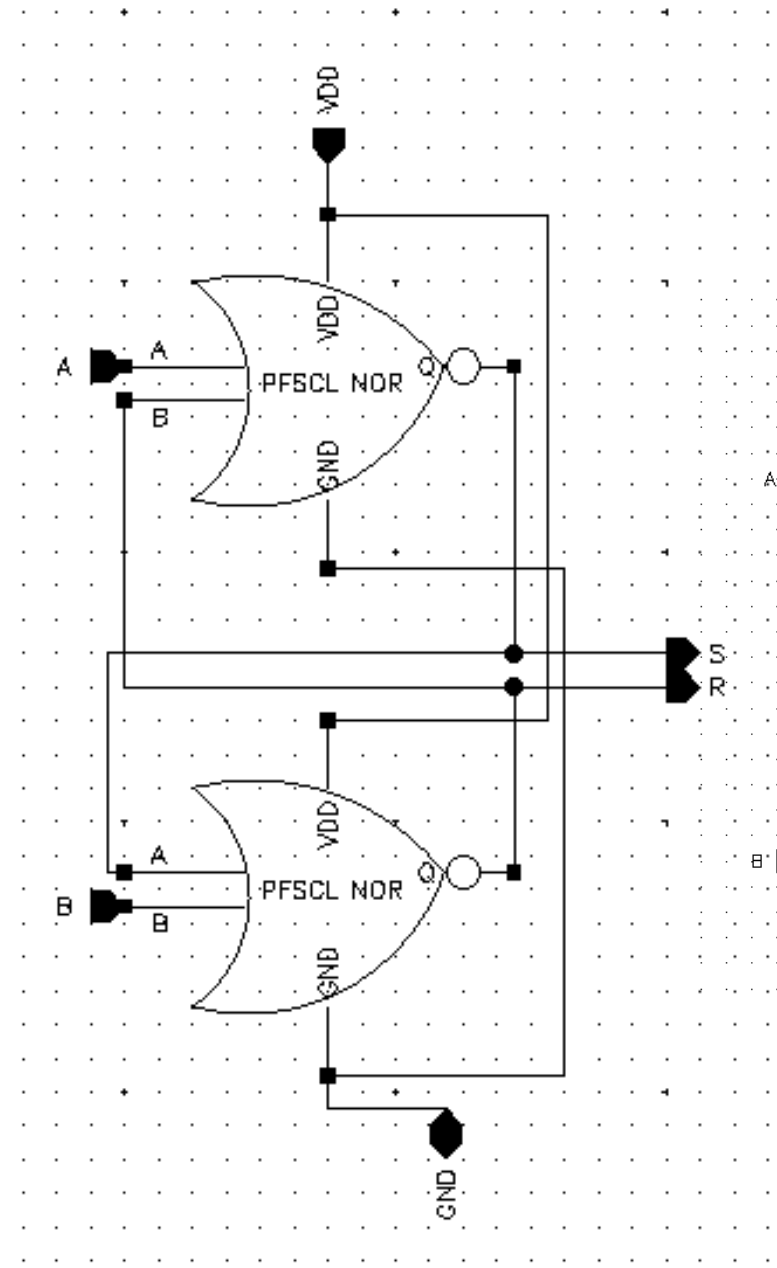

Fig. 40. PFSCL LATCH Symbol

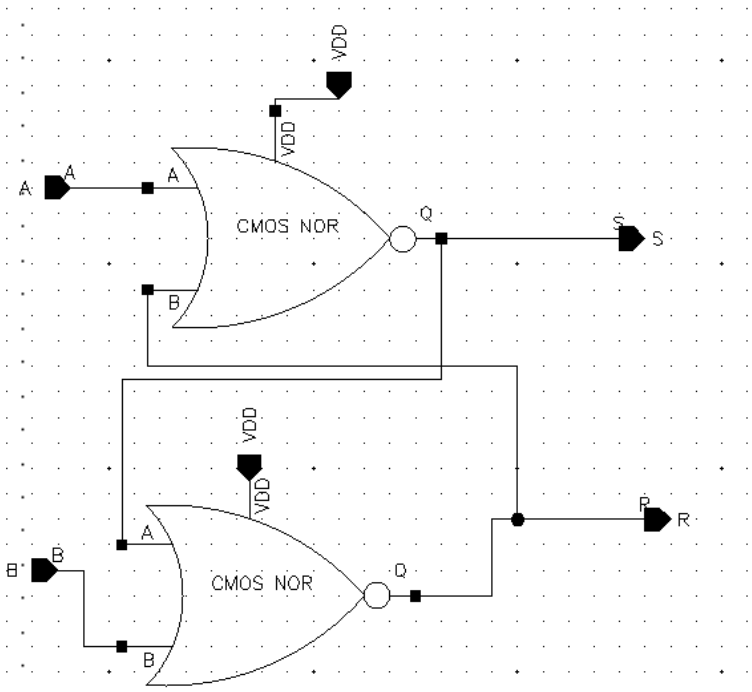

Fig. 41. CMOS LATCH Symbol

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