

# **UNIVERSITY OF TWENTE.**

Faculty of Electrical Engineering, Mathematics & Computer Science

## GNSS-Based Time Synchronisation for Distributed Radio Localisation on Software-Defined Radio

Matthijs Aanen M.Sc. Thesis May 2023

> Supervisors University of Twente: André B. J. Kokkeler, Anastasia Lavrenko, Zaher Mahfouz, Nikolaos Alachiotis

> Radio Systems Group Faculty of Electrical Engineering, Mathematics and Computer Science University of Twente P.O. Box 217 7500 AE Enschede The Netherlands

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## **Chapter 1**

## Introduction

In time of flight (ToF) localisation systems, the time interval between the transmission and reception of a signal is used to measure the distance the signal has travelled. This is possible due to the constant propagation speed of the signal through air. When combining three or more different ToF measurements between anchor points positioned at known locations and a target, a point solution for the unknown position of the target can be found (trilateration and multilateration). [1]

To measure the time interval between the moment a signal is transmitted by a radio and received by another, both radios must have a common sense of time. When these radios are co-located, this can be achieved by sharing a local clock, or through synchronisation with a common time reference signal over cables. However, challenges arise when the radio transmitter and receiver are distributed (i.e., positioned at different physical locations) and no physical connection between them is possible. In this case, time synchronisation must be achieved via wireless means.

It is important that the clocks of the radio nodes (transmitter and receiver(s)) are synchronised accurately, because any time offset between them will directly contribute to an error in the observed propagation time of the signal. In other words, the accuracy of the observed ToF is highly dependent on the accuracy of the synchronisation between the two radio nodes. In air, where the signal propagation speed is near the speed of light, an offset of 1 ns will result in approximately 30 cm of error in the observed propagation distance.

Radio synchronisation is important not only for localisation but also in communication systems where multiple users share a frequency spectrum. Frequency-division multiple access (FDMA) can be used to prevent interference without time synchronisation, but time-division multiple access (TDMA) requires precise synchronisation for efficient use of the spectrum. Without accurate time synchronisation, transmissions may overlap and or leave gaps where the spectrum is unused.

A commonly used technique for time synchronisation is to use global navigation satellite systems (GNSSs) which rely on highly accurate atomic clocks [2]. Time signals based on these clocks are transmitted from orbiting satellites to the Earth's surface, where they can be used for positioning and as time reference. This thesis addresses the possibilities and limitations in timing accuracy between radio nodes that use GNSS receivers as a source of a common time reference. The objective is to find out how well physically separated radio nodes can be synchronised using GNSS for the purpose of radio localisation.

#### 1.1 Related Work

When a GNSS receiver has derived a sense of time from satellite signals, it can present that time in a pulse per second (PPS) signal in which the passing of each second is represented by a digital pulse. The PPS signal can be used by other electronic devices to synchronise their local sense of time with; i.e. by slowing down or speeding up their clocks when it leads or lags with respect to the reference (respectively). Other electronic devices can use this signal as a reference to synchronise their local clocks with. Niu, Yan, Zhang, *et al.* [3] have proposed a method to evaluate the accuracy of a PPS signal using a highly stable chip-scale atomic clock (CSAC) as a reference. The GNSS receiver provides an estimate of its own timing error, which the authors have extracted via a serial interface. Through these methods, the stability and jitter of PPS signals generated by three different receiver models are investigated.

The error of the PPS period from the three GNSS receivers reported in [3] by Niu, Yan, Zhang, *et al.* has a standard deviation (STD) ranging from 1.5 ns to 17.2 ns. Niu, Yan, Zhang, *et al.* also state that the time error estimate reported by the receiver matches the error observed by the PPS measurements. Furthermore, temporal quantisation imposed by the receiver clock and its drift are identified as significant sources of error. However, the measurements in this study have been obscured by quantisation error themselves. The PPS signal is observed in discrete time at a rate of 390 MHz, corresponding to a temporal resolution of 2.56 ns. This resolution lies in the same order of magnitude as do some of the observed errors. Furthermore, while the authors have reported on period jitter, cycle-to-cycle jitter and long-term stability (up to a day), they have not measured the instantaneous offset of the clock (absolute jitter). This last quantity is important for the performance of ToF localisation, as will be explained in Section 2.1.

The research in [3] provides the order of magnitude of the accuracy of the PPS signal that can be expected. Additionally, [3] provides insights into the approach with which the accuracy of the PPS signal can be evaluated in conjunction with the reported error estimate. An accurate error estimate indicates that the PPS error is (at least partially) deterministic and that there is a possibility for it's reduction or compensation. In order to make any quantitative conclusions on this hypothesis, the PPS signal should be measured with a higher temporal resolution. Finally, there exists a need for the PPS signal accuracy to be represented by a metric that is relevant to the context of ToF localisation: the absolute jitter.

The PPS signal generated by a GNSS receiver can be used as a time reference for electronics. This makes it possible for physically separated devices, like radios in a distributed radio localisation system, to synchronise their clocks without sharing an oscillator or being connected with cables. There are different methods with which electronics can interface with the PPS signal. The digital format of the PPS signal lends itself well for

usage in embedded systems. Embedded systems are generally based on synchronous (clocked) digital hardware like microcontrollers or field-programmable gate arrays (FP-GAs), which have digital interfaces that can accept the PPS signal (provided it's voltage levels correspond with that of the device). After interfacing with the PPS signal, a (digital) phase-locked loop (PLL) can be used to synchronise the local oscillator (LO) with the reference. Software-defined radios (SDRs)-radios in which one or more signal processing components are implemented with (embedded) software [4]-often feature dedicated ports that serve as an input for reference clock signals. However, when such an interface is not available, synchronisation of SDRs with a PPS signal is not achieved easily. In [5], Kaderka and Urbanec have solved this problem by injecting the PPS signal at the intermediate frequency (IF) stage of a low-cost SDR that does not feature a dedicated reference clock input. The time pulse is directly sampled and recovered through cross-correlation with the expected impulse response of the system. While still receiving radio signals on the same channel, Kaderka and Urbanec have been able to measure the pulse time with an accuracy of 2.1  $\mu$ s, or 0.42  $\mu$ s when applying additional post-processing. However, the authors conclude that this accuracy is not sufficient for localisation on the ground because the resulting position uncertainty is too large.

In [6] (Andrich, Bauer, Ihlow, *et al.*), a time pulse is measured with a similar method where the PPS signal is directly sampled by a receiving channel of an SDR. However, a higher grade SDR is used and the channel is not shared with a radio signal anymore, but dedicated to the pulse measurement. Furthermore, the authors of [6] have employed an interpolation technique in order to improve the resolution beyond the sampling frequency. A drastically improved performance in accuracy is achieved compared to [5], as [6] reports a STD of down to 21.5 ps. However, the SDR selected for this thesis has a single receiving channel and a dedicated synchronous input for time reference signals. Given that the application for this research is radio localisation, the receiving channel should be available for radio signals. This means that the method of [5] is not a good candidate due to the poor accuracy. Furthermore, the technique proposed in [6] is not an option either due to the lack of an available dedicated receiving channel. This creates a need to evaluate the achievable accuracy for the dedicated time reference input of the selected SDR.

In [7], two SDR devices are synchronised using a common PPS signal which is generated by an off-the-shelf GNSS receiver. The PPS signals are connected to synchronous inputs of a complex programmable logic device (CPLD), which is embedded on the SDR. The authors have evaluated the degree of synchronisation between the two SDRs by configuring them to receive the same signal and using post-processing to derive an estimation of the time offset between their clocks. A STD of the synchronisation offset of 20.62 ns is achieved. However, the measurements are conducted with co-located SDRs, and are synchronised with a common PPS signal. For distributed SDRs, there is no possibility to connect the devices with cables, and a different approach is required.

While the previously mentioned studies have been focused on time pulse reference signals, Overman has achieved synchronisation of ultra wideband (UWB) radios with a different technique in [8]. Through wireless transmission of UWB packets, a reference anchor periodically broadcasts its current local time (time of transmission (ToT)) to other distributed radios. These radios record the time of arrival (ToA) relative to their own clock. The difference between the ToT and the ToA carries information on the offset between the two clocks and the propagation time of the signal between the two radios. The error between these clocks is caused by deterministic clock parameters like clock drift and frequency drift [9]. Different estimation methods are proposed to find the clock parameters and the distance between the anchors. This synchronisation is not performed in realtime, as the local clock times are not controlled to match the reference clocks. Instead, digital post-processing is used to compensate for deterministic errors in the system. As Overman shows, deterministic timing errors can be compensated for in distributed radio localisation systems. This means that it would be important to not only look at the accuracy of GNSS-receiver-generated PPS signals and the time offset between synchronised SDRs, but also at whether or not these errors are deterministic.

Besides the synchronisation accuracy of clocks, the timing of transmissions or receptions in an SDR is influenced by the latency in the system, especially if these delays are dynamic. In a study conducted by Truong and Yu [10], the round-trip time (RTT) of samples through an SDR and its host computer is measured. The authors have observed mean RTT values that range up to approximately 30 ms while the RTT STD lies in the range of single-digit milliseconds. These values are significantly larger than those of the clock errors in the previously mentioned publications, but it should be noted that the authors of [10] have identified the software running on the host computer as a dominating factor. Truong and Yu have decomposed the latency into contributions made by different elements, like software, data transfer and hardware. However, the actual moment at which radio frequency (RF) samples are transmitted or received is not included in the measurements. The also authors do not report on the individual contributions to the total observed STD. Furthermore, [11] shows that scheduling can be used to omit latency caused by the host software, hardware setups and buffering, by performing these steps in advance and then holding off with transmission or reception until the scheduled time is reached. Further research into the latency of the SDR hardware, including the radio front ends, is required in order to make these results relevant to the application of ToF localisation.

In short, there have been studies on the jitter and stability of PPS signals and the manners in which they can be measured with SDR. Research on the latency of SDRs has also been covered. However, these results are not entirely suited to determine whether or not GNSS-based time synchronisation is suitable for ToF localisation. For this, a study with an approach similar to that of Overman [8] is required on all processes in a radio node that are critical to its timing accuracy. By identifying and characterising the sources of error, a judgement can be made to find out if they form an absolute limit on the performance, or if they can be compensated for.

### 1.2 Research Questions and Contributions

The main question this thesis addresses is how well physically separated SDR nodes can be synchronised using GNSS-based time references, for the purpose of ToF localisation. While there is previous research on the relevant topics (i.e., timing accuracy of PPS signals [3] and PPS-based synchronisation of SDRs [5]–[7]), these studies do not fully address the research question because they do not consider the radio node configuration as a whole, with the same constraints as in the distributed ToF localisation scenario, or do not provide results that are directly applicable to ToF localisation. To fill this gap, the study presented in this is conducted, assuming a radio node configuration consisting of an off-the-shelf GNSS receiver and an SDR. With this in mind, the following intermediate research questions have been defined:

- 1. What are the limitations and sources of error in GNSS-based time synchronisation?
- 2. How can a time synchronisation error between radio nodes be measured?
- 3. How can the error behaviour be modelled and subsequently used to improve localisation performance?

By virtue of answering these questions through theoretical analysis (Chapter 2) and measurements (Chapters 3 and 4), the following contributions to the research subject have been made:

- a theoretical analysis of the two primary radio node components (GNSS receiver and SDR);
- a method for evaluating synchronisation accuracy of GNSS receivers and SDRs;
- a model of the synchronisation error between two radio nodes.

## 1.3 Outline

**Chapter 2** is used to provide background theory and terminology on the subject of ToF localisation, clock modeling and clock synchronisation. In Section 2.1, the theory on ToF localisation is provided. First, a general explanation of the technique is provided, followed by two methods that can be used to obtain a point solution for the position of a target. Section 2.2 then covers a general model for clocks in electronics and provides some practical information on how clock synchronisation is commonly achieved. The next sections are focused on the topics of SDR and GNSS (Sections 2.3 and 2.4, respectively) and cover how time keeping and clock synchronisation are achieved specifically with the devices used in this research.

**Chapter 3** introduces a number of experiments that have been designed to validate and extend on the theoretical models introduced in Chapter 2. The problem of synchronisation error is dissected into two components: *a*) The error originating from the GNSS receiver and its PPS signal is investigated in Section 3.2. The experiments look at the influence of GNSS signal quality, different operating modes and quantisation error. *b*) Error originating from the SDR and the synchronisation process. Section 3.3 provides the experiments that are used to investigate how accurately the SDR's front end is timed and how timing errors can originate from synchronisation with a PPS signal. The experiments involve configurations with up to five GNSS receivers, SDRs or GNSS-SDR pairs in both indoor and outdoor environments.

**Chapter 4** provides the results from the experiments in Chapter 3. As with Chapter 3, the results are organised in two corresponding categories. First, the measurement regarding the accuracy of the GNSS receiver and its PPS signal, as described in Section 3.2, are provided in Section 4.1. Then, Section 4.2 covers the results of the experiments aimed at the SDR, described in Section 3.3.

**Chapter 5** considers the collected knowledge regarding the synchronisation of SDR nodes based on GNSS. In line with the research questions, the chapter discusses the identified limitations and sources of error in the investigated GNSS-based time synchronisation technique. It also reflects on the developed methods for measuring the error of time synchronisation of the two components of the radio node: the GNSS receiver and the SDR. Lastly, by virtue of the established understanding of the synchronisation process, recommendations are made on how the process can be adapted in favour of the accuracy.

## Chapter 2

## Theory

#### 2.1 Time-of-Flight Localisation

In radio localisation, the properties of a received signal that has been transmitted, or reflected, by a target are used to find geometric information about the target's position in space. These properties can be the received signal power, angle of arrival, frequency and time of arrival. The latter is the focus of this thesis.

The ToF can be used as a measurement of distance due to the constant propagation speed of electromagnetic waves in a uniform medium, e.g. air or vacuum. In a vacuum, the time at which a signal arrives at the receiver radio,  $t_{Rx}$ , can be described as follows:

$$t_{\rm Rx} = \frac{d}{c} + t_{\rm Tx},\tag{2.1}$$

where  $t_{Tx}$  is the time at which the signal is transmitted, *d* is the distance it has propagated between the radios and *c* is the speed of light in vacuum [12]. Equation (2.1) can be rewritten to solve for *d*:

$$d = (t_{\mathrm{Rx}} - t_{\mathrm{Tx}}) \cdot c. \tag{2.2}$$

The ToF ( $T_{\text{ToF}}$ ) is then defined as the total propagation time of the signal from transmission to reception:

$$T_{\rm ToF} = t_{\rm Rx} - t_{\rm Tx}.$$
 (2.3)

Due to processes like noise or clock drift, the observed (or estimated) time of transmission and reception can deviate from the actual values. The estimated values of  $t_{\rm Tx}$  and  $t_{\rm Rx}$  are  $\hat{t}_{\rm Tx}$  and  $\hat{t}_{\rm Rx}$ , respectively. The errors are then denoted as  $\varepsilon_{\hat{t}_{\rm Tx}}$  and  $\varepsilon_{\rm t_{Rx}}$ . Thus, we have

$$\hat{t}_{Tx} = t_{Tx} + \varepsilon_{\hat{t}_{Tx}}$$

$$\hat{t}_{Rx} = t_{Rx} + \varepsilon_{\hat{t}_{Rx}}.$$
(2.4)

Now, the influence of these errors on the estimated distance  $\hat{d}$  can be found by solving Eq. (2.2) with estimated values:

$$\hat{d} = (\hat{t}_{\text{Rx}} - \hat{t}_{\text{Tx}}) \cdot c$$

$$= \left( t_{\text{Rx}} + \varepsilon_{\hat{t}_{\text{Rx}}} - t_{\text{Tx}} - \varepsilon_{\hat{t}_{\text{Tx}}} \right) \cdot c.$$
(2.5)

The relative time offset between the two radios determines the error in the observed distance, as can be demonstrated by finding the partial derivative of  $\hat{d}$  with respect to the

relative timing error:

$$\frac{\partial \hat{d}}{\partial \left(\varepsilon_{\hat{\mathbf{t}}_{\mathrm{Rx}}} - \varepsilon_{\hat{\mathbf{t}}_{\mathrm{Tx}}}\right)} = c.$$
(2.6)

This is an indication of the importance of time synchronisation in ToF localisation: if the timing error between the transmitting and receiving radio is off by one nanosecond, the resulting error in observed propagation distance is approximately 30 centimetres.

In a radar-based localisation system, the receiving and transmitting radios can be placed either at the same place (co-located), or physically separated. The former case is called monostatic radar and is explained in Section 2.1.1. The latter scenario is referred to as bistatic radar, and will be covered in Section 2.1.2.

#### 2.1.1 Monostatic Radar

In monostatic positioning, the transmitter and receiver are co-located at one radio node, also called an anchor, with a known position  $(s_n)$ . The path that the signal travels is that from the anchor to the target (located at  $s_{target}$ ), and back to the anchor. If the distance between the anchor and the target is  $r_n$ , calculated as the Euclidean norm of the distance vector:

$$r_{\rm n} = \left\| \mathbf{s}_{\rm n} - \mathbf{s}_{\rm target} \right\|,\tag{2.7}$$

then the time it takes for the signal to travel back and forth is given as

$$T_{\rm ToF} = \frac{2r_{\rm n}}{c}.$$
 (2.8)

The geometric solution of this equation takes the form of a circle (in two-dimensional space) with a radius of  $r_n$  around the anchor at  $s_n$ , as shown in Figure 2.1a. This solution is ambiguous since it does not resolve to a single point. To remedy this, more anchors should be added. In a two-dimensional space, at least three anchors are required to find a point solution for the position of the target (trilateration), as is shown in Figure 2.1b.

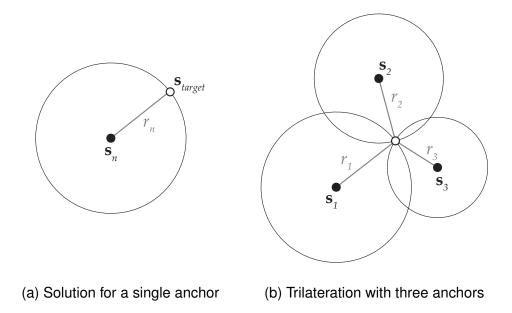


Figure 2.1: Geometric solutions for monostatic radar in two-dimensional space

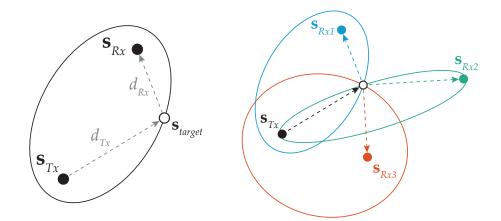
In monostatic radar, synchronisation of the transmitting and receiving radios is relatively simple, since they are co-located at the anchor point. The transmitting and receiving radios could share a clock and local oscillator, or share a common time reference via a cable.

#### 2.1.2 Bistatic Radar

A different method for positioning with propagation distances is bistatic radar, in which the transmitting radio and receiving radios are not at the same location but at points  $s_{Tx}$  and  $s_{Rx}$ , respectively. The signal travels from the transmitter to the target (distance  $d_{Tx}$ ), and then from the target to the receiver (distance  $d_{Rx}$ ). The ToF is directly proportional to the total propagation distance:

$$T_{\rm ToF} = \frac{d_{\rm Tx} + d_{\rm Rx}}{c}.$$
(2.9)

In two-dimensional space, the solution of this equation takes the shape of an ellipse, with the foci being the two radio nodes  $s_{Tx}$  and  $s_{Rx}$ . This is shown in Figure 2.2a. As in the monostatic setup, three solutions are required to find a single point solution for the target in two-dimensional space. This is demonstrated in Figure 2.2b, where three ellipses intersect in at the position of the target. The system in Figure 2.2b consists of one transmitting and three receiving anchors, forming three ellipse solution. However, any unique combination of transmitter-receiver anchor pairs can be used.



(a) Solution with a single transmitting (b) Trilateration with one transmitting and receiving anchor pair. and three receiving anchors

Figure 2.2: Geometric solutions for bistatic radar in two-dimensional space. For each transmitter-receiver pair, the target's position can be anywhere on an ellipse. When combining three of these ellipses, a point solution can be found for the position of the target.

While both the monostatic and bistatic configurations require time synchronisation of the transmitting and receiving radio, this problem is less trivial in bistatic radar, since these radio's are not co-located. An advantage of bistatic radar is that a node can consist of a single radio (transmitter or receiver), instead of two. This can be beneficial in situations where there are constraints on commodities like weight, volume or power. Such a case would be the when the radio node is the payload for an unmanned aerial vehicle.

### 2.2 Time Keeping in Electronics

This section will be used to introduce how time keeping is generally implemented in electronic devices. First, a model of a clock is introduced, as well as metrics that can be used to assess the clock's accuracy. Second, the general method with which clocks can be synchronised is presented along with the definition of the pulse per second (PPS) signal format, which is can be used for this purpose.

#### 2.2.1 Clock Model

To keep track of time, a clock or clock signal can be used. Clocks are often implemented using an oscillator with a known frequency. The current time is then maintained by counting the periods. In electronics, oscillators are often based on crystal resonators and referred to as the LO. Using digital circuitry, a count of the period is maintained in a register.

The passing of time can be represented and distributed as a clock signal in the form of a pulse wave. For an oscillator with frequency  $f_{LO}$  the current time is given by:

$$t_{\rm clock}[n] = \frac{n}{f_{\rm LO}},\tag{2.10}$$

where n is the count of LO periods. However, due to ageing of the oscillator or changes in the environment, the frequency of the clock can deviate from its ideal value. This can cause an offset between the true time and the clock's time. The instantaneous offset of a clock can be described with the following equation: [9]

$$x(t) = x_0 + y_0 t + \frac{1}{2}Dt^2 + \epsilon(t).$$
(2.11)

This model, based on a second-order Taylor expansion, separates the offset into systematic clock attributes ( $x_0$ ,  $y_0$  and D) and a zero-mean noise component  $\epsilon(t)$ , called jitter. A visual representation of the clock attributes and jitter is provided in Figure 2.3. In the following paragraphs, the individual components are further elaborated.

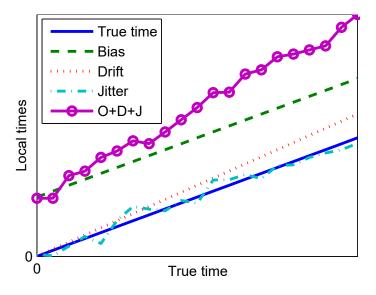


Figure 2.3: A demonstration of the contribution of time offset, drift and jitter to the error of a clock from true time. From [13].

#### Clock Bias (x<sub>0</sub>)

The time bias is the static component of the clock offset, denoted as  $x_0$  in Equation (2.11). It can be caused by the initial state of the clock, but also due to delay of the clock signal. It is highly deterministic, because it does not change over time. This makes it easy to compensate for through calibration. For this reason, this thesis puts little effort into characterisation of the clock bias.

#### Clock Drift (y<sub>0</sub>)

Clock drift, time drift or, for short, drift, corresponds to the first derivative of the clock offset. This linear component is mainly attributed to frequency offset of the LO. Frequency offset can be caused by factors like temperature, power supply voltage, as well as mechanical phenomena like acceleration and atmospheric pressure [14]. Drift is often provided in the parts-per notation, or in ns/s.

#### Frequency Drift (D)

In LO-based clocks, the second derivative approximation of the clock offset is given by the frequency drift (D in Equation (2.11)). It represents the linear change in LO frequency over time.

#### Jitter (ε)

An important component of clock offset is jitter ( $\epsilon(t)$  in Equation (2.11)). Jitter has zero mean, and is often modelled as random noise [9]. It can be caused by truly random phenomena like thermal noise, flicker noise and shot noise [15]. However, it can also have deterministic causes like distortion and inter-symbol interference [16].

#### **Clock Metrics**

The accuracy or stability of a clock can be described in multiple metrics. First of all, the instantaneous clock offset can be measured, and compiled to a root mean square (RMS) value. If one is not interested in the clock bias, the STD or variance of the offset can be used. The attributes can also be considered seperately. For example, stability of oscillators is often provided by manufacturers in the parts-per notation, corresponding to the drift. Jitter can be measured in different metrics. When considering clock signals, observed jitter is time discrete, corresponding with the pulse edges. The difference between the observed pulse edge and the ideal clock edge is defined as the absolute jitter, or time interval error (TIE) jitter. This is equal to the variable  $\epsilon(t)$  observed at the ideal time of the clock edge. Similarly, the period jitter is the difference between the interval of consecutive observed clock edges and the ideal clock period. Lastly, the cycle-to-cycle jitter is denoted by the difference in consecutive observed periods. The period jitter can be found from numerical differentiation of the absolute jitter and the same holds for cycle-to-cycle jitter and period jitter (respectively). [17]

A more detailed metric of stability of a clock is the Allan variance. With the clock offset definition of Equation (2.11), the Allan variance is given by: [9]

$$\sigma_{\rm y}^2(\tau) = \frac{1}{2} \operatorname{E}\left[\left(\frac{x_{\rm t+\tau} - x_{\rm t}}{\tau}\right)^2\right],\tag{2.12}$$

where  $\tau$  is the time interval and E the expectation operator. It describes the stability of a clock or oscillator as a function of interval between consecutive observations. It is useful for distinguishing between long-term stability (often considered as the  $x_0$ ,  $y_0$ and D coefficients) and short-term stability which is associated with jitter. However, it is normalised with the sample interval  $\tau$  to relate it to frequency stability. An alternative for the Allan deviation, that is not normalised with  $\tau$ , is the time deviation (TDEV) [18]. The TDEV denotes stability in time instead of phase or frequency. The TDEV is defined as

$$\sigma_{\rm x}(\tau) = \tau \cdot \operatorname{mod}\sigma_{\rm y}(\tau)/\sqrt{3},\tag{2.13}$$

where the  $mod\sigma_y$  operator denotes the modified Allan deviation [19]. The modified Allan deviation is a modified implementation of the Allan deviation that allows distinction between error noises that are differently distributed over the spectrum (like white noise and flicker noise).

#### 2.2.2 Clock Synchronisation

To achieve long-term stability in time keeping an accurate lower frequency clock can be used as a reference. The local time can be compared with that of the reference to determine if it is lagging or leading. Then, the local time can be set to match the reference. This can be done digitally. Another method to synchronise the local time with the reference is by adjusting the frequency of the local clock. With a voltage-controlled oscillator the frequency can be increased to catch up with the reference time (if lagging), or reduced to fall back in synchronisation with it (when leading).

#### **Pulse-per-Second Signals**

A commonly used signal format for distribution of a time reference is the pulse per second (PPS), shown in Figure 2.4. As the name suggests, this signal has a period of one second. The signal is a square wave in which a sharp rising or falling edge marks the start of the next period. To interface with digital circuitry, the voltage levels often conform to voltage level standards like transistor-transistor logic (TTL) or complementary metal–oxide–semiconductor (CMOS) [20].

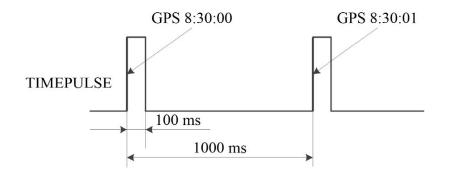


Figure 2.4: An example of a PPS signal where every rising edge denotes the start of a second period. In this case, the pulse-width is 100 ms. From [21].

### 2.3 Software-Defined Radio

For the experiments in this research, a software-defined radio (SDR) platform is used. In an SDR, one or multiple IF or RF signal processing components in a radio chain are implemented in software [22]. This adds flexibility and allows the radio to be used for many applications. In this thesis, the *USRP b200-mini* by Ettus Research is selected (Figure 2.5). This device is pocket sized and is powered and controlled over a universal serial bus (USB) link. It has two coaxial ports for RF signals, one for receiving, and one that can be configured for either receiving or transmitting. It has one coaxial socket that allows the device to be synchronised with an external time or frequency source.

In this section, the software and hardware architecture of the device will be explained. Then, the relevant time-keeping and control mechanisms are treated.



Figure 2.5: Photo of the universal software tadio peripheral (USRP) B200-mini softwaredefined radio. From [23].

#### 2.3.1 Architecture

A high-level diagram of the hardware architecture of the SDR device is provided in Figure 2.6. The two primary integrated circuits (ICs) are the radio front end and a FPGA. The radio front end provides the interface between low frequency digital data stream and the up-converted radio frequency signal. The FPGA is a central component in the system: it controls the radio front end, regulates the streaming of samples and schedules these operations. However, it also performs synchronisation of the systems clock signal with the reference time signal.

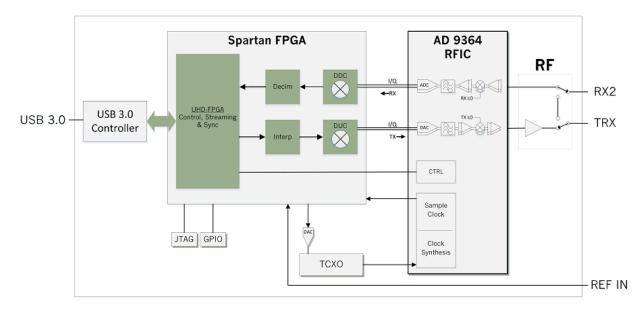


Figure 2.6: High-level block diagram of the USRP B200-mini. From [23].

#### **Radio Front End**

The front end of the radio consists of the *AD9364 RFIC* by Analog Devices. A diagram of this device is shown in Figure 2.7. It features a receive and transmit radio chain that can be operated simultaneously. Both the transmitting and receiving chains have digital filters for decimation and interpolation, in the shape of configurable 128-tap finite impulse response (FIR) filters. Digital in-phase and out-of-phase samples are supplied and send to the FPGA via a parallel data port. A slower SPI connection is used to configure the filters and amplifiers.

One important feature of this IC is that it also contains the PLLs that are used to synthesise the master clock signal. It has an interface for an oscillator as an input. Then, via the PLLs, a digital clock signal is generated with a configurable frequency. This clock signal is used internally, but also presented as an output.

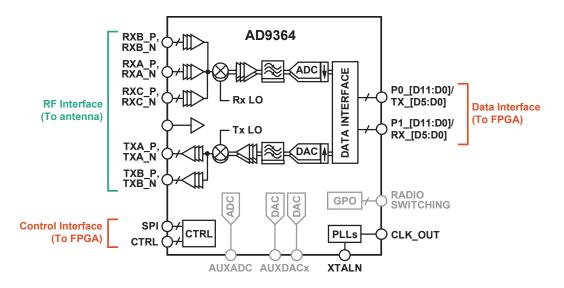


Figure 2.7: Diagram showing the interfaces and internal architecture of the AD9364 front end IC. All unused interfaces and components are greyed-out. Adapted from [24].

#### **FPGA**

The FPGA is a device that provides programmable digital hardware. It features logic elements and latches that can be interconnected with configurable routing. These elements can be combined to create larger functions like arithmetic operations and memory. Furthermore, it has a set of digital general-purpose input/output (GPIO) banks that are used to interface with the device.

The FPGA used in the B200-mini is the *Spartan-6 XC6SLX75* by Xilinx. It plays a central role in the device since it is used for scheduling and execution of instructions. Furthermore, the device hosts DSP functions like digital up and down converters, i.e. allowing smaller step sizes in centre frequency.

#### 2.3.2 Control

#### **UHD Software**

The SDR receives instructions from a host computer over a USB connection. This is done using the open-source hardware driver USRP hardware driver (UHD) software which handles configuration of the device and arranges the streaming of samples on the host computer. The UHD software is written in C and C++. It can be used directly in those languages, but is available to other software via an application programming interface (API). For this research, Python scripting is used in combination with the UHD API. [11]

#### **Radio Core**

The sense of absolute time in the SDR is maintained by a piece of FPGA firmware called the *radio core* [25]. This architecture contains a 64-bit register that holds the clock period count. The radio core directly controls the radio front end and arranges streaming of samples within the FPGA and at its interfaces.

#### **Timed Commands**

The UHD driver and USRP firmware also allow for scheduled operation using *timed commands* [25]. These commands are instructions paired with a timestamp that are sent from the host computer. They are then stored in a queue in the radio core architecture. When the scheduled time of the command arrives, the command is executed and removed from the queue. Timed commands allow scheduling of changes to the settings of the transceiver IC, but also the timed start of transmission or reception. Timed commands are the best way to achieve precise timing with the USRP SDR, and are therefore used in all experiments in this research.

#### Latency

USRP SDRs are controlled from a host computer via a USB connection. Latency between the host computer and radio front end that is experienced during transmission and reception is investigated in [26]. Note that while the exact model and firmware of the model does not match that of the SDR that is used in this thesis, they are in the same USRP product series and have an overlap in hardware architecture and firmware [11]. The latency found in [26] is dominated by the host driver software and USB throughput, and is highly irregular. The authors have reported standard deviations in the range of several milliseconds, far exceeding the required timing accuracy in the nanosecond regime. This means that real-time control of the radio with scheduling on the host-computer is a poor choice.

#### 2.3.3 Clock

The clock architecture for the FPGA and the radio front end is shown in Figure 2.8. The SDR uses a 40 MHz crystal oscillator to generate a digital clock signal for the digital circuitry and analog-to-digital/digital-to-analog converters. The crystal can be controlled by voltage, allowing for tuning of its resonance frequency. The voltage control is performed with a 16-bit digital-analog converter (DAC) which is controlled by the FPGA firmware. A passive low-pass filter is put in between the DAC and the crystal, presumably to suppress spectral components generated by the frequency modulation.

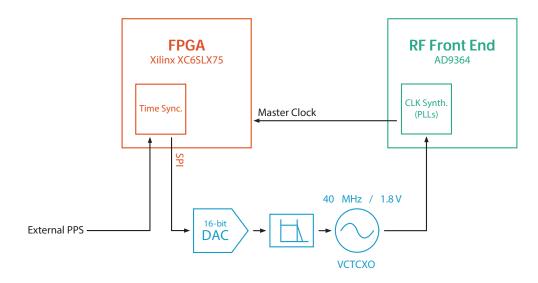


Figure 2.8: Clock generation on the USRP SDR. A voltage controlled oscillator is tuned by the FPGA. Then the PLLs of the front end IC are used to generate the master clock for itself and the FPGA. The FPGA firmware can synchronise with an external PPS signal. Adapted from [23], [27].

#### **Digital Phased-Locked Loop**

To synchronise the local oscillator with the external reference signal, a digital PLL is implemented on the FPGA firmware. This system accepts a 10 MHz or 1 Hz PPS clock signal as the input reference and works as follows. Given the desired LO frequency, a predetermined amount of LO periods will fit in a reference signal period. From the difference between this number and the actual period count, the firmware can calculate whether the LO is leading or lagging. If the count is too low, the LO frequency is too low and vice versa. The digital PLL then adjusts the LO frequency through the DAC to compensate for the error.

One limitation of the synchronisation method employed by the USRP is that it is limited to the temporal resolution imposed by the FPGA clock. When measuring the time at which the rising edge of the incoming reference signal, it cannot distinguish times within a single clock period.

When the probability density of quantization error of a sample is distributed uniformly over a the span of a least significant bit (LSB) level width a width of  $A_{\rm LSB}$ ,

$$f_{\rm Q}(q) = \frac{1}{A_{\rm LSB}} \cdot \Pi\left(\frac{q}{A_{\rm LSB}}\right), \qquad -\frac{\overline{A_{\rm LSB}}}{-\frac{A_{\rm LSB}}{2}} \qquad (2.14)$$

1

the RMS of the error is given by [28]

$$\epsilon_{\rm Q,RMS} = \frac{A_{\rm LSB}}{\sqrt{12}},\tag{2.15}$$

where  $A_{\rm LSB}$  is the physical size of the least significant bit. In the case of temporal quantization by the FPGA clock signal,  $A_{\rm LSB}$  is equal to the clock period. The frequency at which the reference signal is sampled is 200 MHz [11], which yields

$$\epsilon_{\rm Q,RMS} = \frac{5 \times 10^{-9}}{\sqrt{12}} = 1.44 \,\mathrm{ns.}$$
 (2.16)

Similarly, the STD can be calculated:

$$\sigma_{\rm Q} \equiv \sqrt{\mathrm{E}\left[\left(Q - \mu_{\rm Q}\right)^2\right]} = \sqrt{\int_{-\infty}^{\infty} \left(q - \mu_{\rm Q}\right)^2 f_{\rm Q}(q) \, dq} \tag{2.17}$$

$$= \sqrt{\int_{-A_{\rm LSB}/2}^{A_{\rm LSB}/2} \frac{q^2}{A_{\rm LSB}}} \, dq$$
 (2.18)

$$=\frac{A_{\rm LSB}}{\sqrt{12}}.$$
(2.19)

The theoretical RMS and STD values for the quantisation error are equal since the mean of the error distribution is zero.

### 2.4 GNSS-Based Time Synchronisation

Global navigation satellite systems consist of satellites that orbit the Earth. They are equipped with atomic clocks from which time signals are derived. Atomic clocks are suitable time references due to their good stability at long intervals [2]. The time signals are transmitted at radio frequency down to the Earth's surface. Here, the signals can be captured with an antenna and processed by a GNSS receiver. Often using a form of Bayesian statistics (i.e. Kalman filtering) [29], multiple ToF observations are combined to create a solution that estimates the state of the receiver in terms of position, velocity and time (PVT). When using a Kalman filter, this solution of the state comes with a covariance matrix that estimate the accuracy of the solution. [12]

The *global time* derived from GNSS signals can be used as a common time reference available to the electronics in a radio localisation node. For this purpose, a receiver is required that can relay the GNSS-based sense of time in an accessible form, like the PPS format. The PPS signal can be used by the SDR as a time reference to synchronise with. This configuration (shown in Figure 2.9) is the subject of this thesis.

#### 2.4.1 GNSS Signal Quality

The accuracy of the PVT solution is dependent on the accuracy of observations that it is derived from. Thus, the GNSS signal quality will have an effect on the PPS accuracy. The quality of GNSS signals can be affected by different phenomena, which will be elaborated in the following sections. In order to quantify the signal quality, a number of metrics are presented.

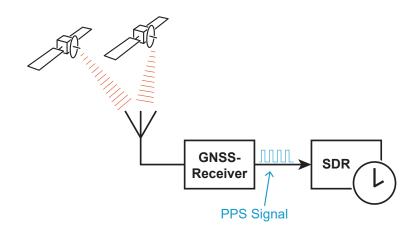


Figure 2.9: How GNSS receivers are used to relay time signals from satellite as a digital clock reference signal for the software-defined radio.

#### **Degradation Phenomena**

The quality of GNSS signal can be affected by different phenomena. In a broad sense, one should consider noise and distortion. Noise can come form external sources, that radiate in the same frequency band as the GNSS signal. The largest external source of interfering signals is man-made noise [30]. Man-made noise can come from devices that transmit in the same frequency band as the GNSS signal, either on purpose or inadvertently, e.g., through spectral leakage or electrostatic discharge (ESD) [31]. However, also natural sources exist, such as cosmic background radiation from space [32]. The radios used to transmit and receive the GNSS signals also degrade the signal. Phenomena like thermal noise and flicker noise also interfere with the signal [33]. Furthermore, nonlinearities of these devices will add distortions.

Beside these mechanisms that degrade the signal itself, the information about the propagation distance (range) carried by the ToF of the signal is affected by the medium. In vacuum, the phase velocity of electromagnetic waves is constant and frequency independent, which means that the linear relation between propagation time and propagation distance holds. However, in Earth's atmosphere, the medium is non-uniform and frequency dependent. This means that the signal can be distorted due to dispersion, but more importantly, it can change the perceived propagation delay from the satellite to the GNSS receiver, causing an error in the observed range.

An important cause of signal degradation is multipath propagation. Due to reflections of the signal on objects in the environment, the signal can arrive at the receiving antenna at different moments in time. This causes considerable distortions and fading of the signal and can add delay to the ToF, especially when the direct propagation path along the line of sight (LOS) is obscured. The effect of multipath is the greatest in urban areas, but can be reduced with directional antennas that reject reflected signals originating from lower elevation angles. [12], [34]

#### **GNSS Signal Quality Metrics**

There are different metrics that can be used to (indirectly) measure and represent the quality of the GNSS signal and solution. Many of these can be estimated by the receiver itself. For one, GNSS receivers can calculate the signal-to-noise ratio (SNR) for each tracked satellite [35]. Furthermore, when calculating the PVT solution using a Bayesian estimation (like the Kalman filter), the not only the expected state is estimated, but also its probability density function (PDF). These distributions, representing the estimated accuracy of the solution. [36]

A different metric for the quality of the GNSS signal is the dilution of precision (DOP). It describes how error in the measurements (the received GNSS signals) propagates to the error of the PVT solution. In other words, it represents the proneness of the solution to observation error. The DOP is a measure of the quality of the signals in the sense that it is dependent on the amount of satellites that are being tracked by the receiver, and their geometric distribution in the sky [37]. The time-DOP (TDOP) is defined as: [38]

$$TDOP = \frac{\sqrt{\sigma_{\hat{t}}^2}}{\sigma_{obs}},$$
(2.20)

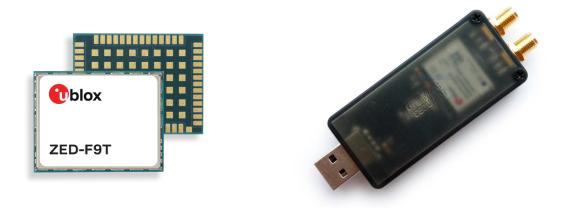
where  $\sigma_{t}$  denotes the standard deviation of the time estimate  $\hat{t}$  and  $\sigma_{obs}$  represents the standard deviation of the observations from which the time estimate is derived, also called the user range error (URE). With a solution for the TDOP and the URE (or  $\sigma_{obs}$ ), an estimate of the accuracy of the receiver's clock ( $\sigma_{t}$ , or tAcc as denoted in [35]) can be found from the product of the two [39].

#### 2.4.2 Differential GNSS

In differential GNSS, multiple receivers collaborate to improve the accuracy of their time and position solutions. Atmospheric effects and errors in the satellite's clock or position are highly correlated when observed around the same time and location. From the position and time solution of one dedicated reference receiver (often fixed in a known position) corrections for these errors can be derived. Broadcasting these corrections and using them at nearby receivers greatly reduces the error of their solutions relative to that of the reference. If the solution of the reference receiver is accurate, the accuracy of the slave receiver is increased in the absolute sense too. [12]

#### 2.4.3 Receiver

The receiver used in this research is the ZED-F9T module by u-blox (Figure 2.10a), which is an off-the-shelve receiver. The module is embedded on a USB dongle (Figure 2.10b. Besides being used for transfer of data and instructions, the USB interface powers the device. Lastly, it has a two sockets for coaxial cables: one serves as an output of the PPS signal and the other is the antenna input. The high high-level architecture of the module is shown in Figure 2.12.



- (a) ZED-F9T IC module. From [40]
- (b) ZED-F9T USB dongle. From [41]

Figure 2.10: The ZED-F9T GNSS receiver as an IC module and embedded in a USB dongle

#### **Differential Timing Mode**

The ZED-F9T receiver supports a differential timing mode in which one receiver is appointed as the master reference station. Via a serial communication interface, this receiver can transmit correctional data. Through a communication link, these corrections can be delivered to slave receivers which increases the accuracy of time synchronisation between the receivers. [35]

#### **PPS Temporal Resolution**

The receiver uses a master clock with a frequency of 125 MHz, translating to a temporal resolution of 8 ns [42]. The PPS signal is driven from this clock signal, meaning that their rising edges are aligned, as shown in Figure 2.11. This quantisation error shifts the rising edge of the PPS signal between -4 ns and 4 ns away from the intended moment in time. Using Eq. (2.17), this is equivalent to an STD quantisation error of 2.3 ns.

However, the digital tracking and estimation system on the module has a resolution smaller than the clock period, and can make an estimation on the quantisation error [35]. The receiver can be configured to periodically report this quantisation error via serial communication for every pulse. This should reduce the resolution down to 1 ps, and the STD quantisation error to 0.29 ps.

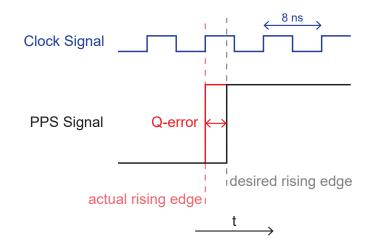


Figure 2.11: Diagram of the rising edge of the PPS signal based on the internal clock of the GNSS receiver. Not to scale.

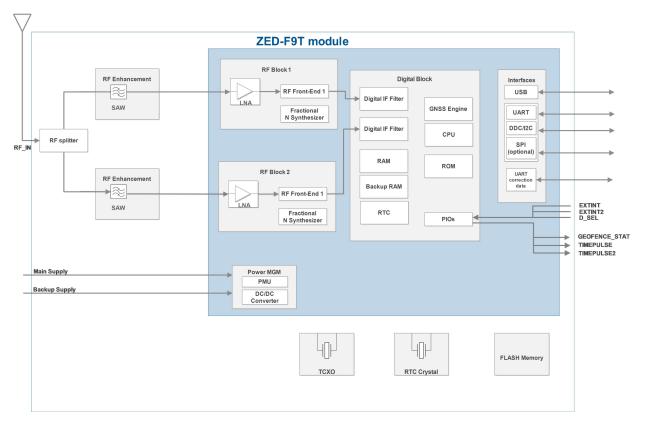


Figure 2.12: High-level diagram of the used GNSS receiver. From [42].

## **Chapter 3**

## Methodology

### 3.1 General Approach

Consider Figure 3.1 in which two radio nodes (node A and node B) are depicted. Both nodes consist of a GNSS receiver and an SDR. The objective is to align their local sense of time, which is maintained by their clocks. During synchronisation of the SDRs with satellite clocks, error is accumulated in virtually every part of the process. Signals are degraded during propagation (noise and attenuation of the channel), at device interfaces (quantisation) and by device internals (random noise, LO imperfections). Thus, the SDR clock time only represents an estimate of the true time (denoted by the hat operator). If the clock times of nodes A and B are represented by  $\hat{t}_{A,SDR}$  and  $\hat{t}_{B,SDR}$ , respectively, then the error between these two clocks is defined as  $\Delta \hat{t}_{SDR}$ . The same goes for the time estimate represented by the PPS signals from the GNSS receivers  $\hat{t}_{A,PPS}$ ,  $\hat{t}_{B,PPS}$  and their relative error  $\Delta \hat{t}_{PPS}$ .

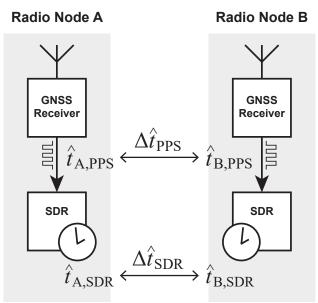


Figure 3.1: Two radio nodes with their relative timing errors in PPS pulse edge ( $\Delta \hat{t}_{PPS}$ ) and SDR clock time ( $\Delta \hat{t}_{SDR}$ )

To measure and characterise the synchronisation errors in this system, it is important to understand the individual error sources. For instance, the sense of time of the GNSS receiver is propagated via the PPS signal to the SDR. Any error accumulated in this chain will end up contributing to the SDR clock error. Therefore, the GNSS receiver and the SDR will be investigated both separately and when operating in conjunction. The first experiments, explained in Section 3.2, aim at evaluating the GNSS and the PPS signal it generates. The purpose of these experiments is to investigate the accuracy of the PPS signal ( $\hat{t}_{\rm GNSS}$  and  $\Delta \hat{t}_{\rm GNSS}$ ) and how it is influenced by the quantisation error, signal reception and differential GNSS operation.

After these experiments, the focus is shifted from the GNSS receiver to the SDR itself. An experiment is conducted to investigate the timing error between the SDR platform front end and the FPGA clock, as will be explained in more detail in Section 3.3. Then, in the next experiment, the clock synchronisation model described in Section 2.3.3 is investigated by characterising SDR time offsets within and across multiple PPS periods. Lastly, an experiment is carried out to evaluate the synchronisation accuracy of the SDR in conjunction with the GNSS receiver.

To emulate the steady state of the localisation system, all experiments are started after the devices have been running for at least 5 minutes. This allows the GNSS receivers to find satellites to track and get an initial estimate on their time and position. Furthermore, this also excludes the temperature change after the startup of cold devices from the measurements.

Long-term stability is considered not to be of interest in this thesis. First, because the GNSS reference is based on atomic clocks, which are generally trusted to be very stable. Second, the errors considered in long-term stability are slow changing in nature which makes them easy to compensate for. Therefore, long-term stability is not considered a limit for the achievable accuracy in ToF localisation. Instead, this thesis evaluates short-term stability of (synchronised) clocks, with intervals up to 30 min.

In characterising the time offsets, one of the aims is to evaluate to what degree the error is systematic. Deterministic error can be removed by fitting a model of the offset (like Equation (2.11)) to observations. However, random error that is nondeterministic cannot be compensated for. Distinguishing between deterministic error and random error allows the limit of achievable synchronisation accuracy to be found.

### 3.2 GNSS Receiver & PPS

#### 3.2.1 Quantisation Error

The first source of error that will be investigated is the quantisation error of the PPS signal generated by the GNSS receiver. To characterise this error, Experiment 1 is conducted. This experiment evaluates the timing error between two PPS signals simultaneously with the quantisation error of these signals that is estimated by the GNSS receivers themselves. The results can be used to characterise the quantisation error by itself and the effect is has on the total accuracy of the PPS signal.

#### **Experiment Configuration**

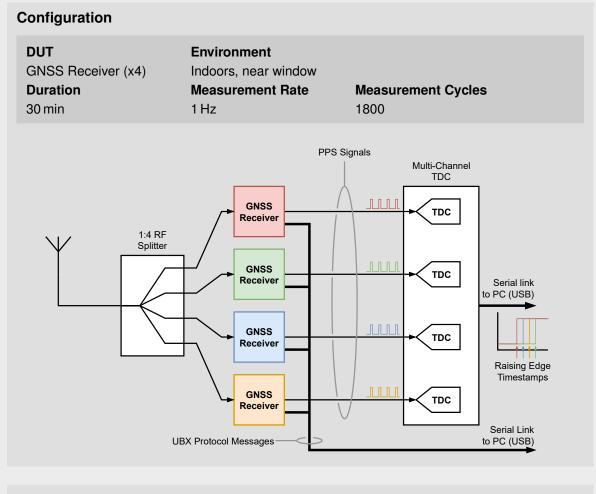
In Experiment 1, four ZED-F9T GNSS receivers are operating in parallel. The four receivers are provided with the same GNSS signal of one antenna by means of a 1-to-4 RF splitter. This removes the effect of potential inter-device differences in signal quality from the results. The time of the rising edge of each PPS signal is measured with a multichannel time-digital converter (TDC): the *TimeTagger Ultra* by Swabian Instruments. This device can record pulse edges with a digital resolution of 1 ps and a jitter noise RMS of 42 ps. The TDC has 18 channels with 50  $\Omega$  impedance. The TimeTagger can be interfaced from a host computer through a USB connection. [43]

The quantisation error of the PPS signal, as described in Figure 2.11, is reported by the ZED-F9T over the USB interface according to the UBX protocol messages shown in Appendix A. A Python script is used to interface with the TimeTagger and the ZED-F9T. The script pairs the reported pulse edges with the corresponding quantisation error to be analysed after the experiment.

# Experiment 1 PPS Quantisation Error

#### Objective

Characterise the quantisation error in GNSS receiver-generated PPS signals



Quantity	Source	Measurement Device	Resolution [ps]	Jitter (RMS) [ps]
Time of rising edge PPS	GNSS Recvr.	TDC	1	42
Quantisation error	GNSS Recvr.	GNSS Recvr.	1	0.29

#### 3.2.2 Signal Quality

Another mechanism that could influence the accuracy of the PPS signal is the quality of the GNSS signals arriving at the receiver. While it is important to understand how signal quality is influencing the accuracy of the PPS signal, investigating all the phenomena mentioned in Section 2.4.1 would be a complex and time-consuming endeavour. Instead, the effect of the signal quality on the PPS accuracy is evaluated by using the high-level data provided by the receiver. This is possible by virtue of the ZED-F9T GNSS receiver, which makes an estimate of the DOP and accuracy of its local time. These values are available outside of the device through a serial communication link (e.g., USB).

In Experiment 2, the timing error between PPS signals is measured in conjunction with the recording of GNSS-reported DOP and accuracy estimates (denoted tDOP and tAcc, respectively). The experiment results can then reveal how the quantities are related, which, in turn, provides an indication of the effect of signal quality on PPS timing accuracy.

The accuracy of the PPS signals are not measured in an absolute sense, but relative to each other. Between receivers A through D, ten pair combinations are possible. For the measured time offset between a pair of receivers, there exist also a pair of tAcc and a pair of tDOP values. The tAcc values represent an estimate of the absolute accuracy of the GNSS receiver's clock in ns [35]. To aid with finding the relation between signal quality and timing accuracy, multiple methods of combination are investigated. The tDOP values are combined by taking the mean and maximum value of the pair. The sum of the values is not considered, as it is merely a scaled alternative of the mean, and would not lead to new insights when used for cross-correlation. While it is not explicitly mentioned in [35], it is assumed that tAcc is a standard deviation. This means that the error between the two devices, with the assumption that it is normally distributed and independent between devices, can be combined as the sum of their variances:

$$\sigma_{X+Y}^2 = \sigma_X^2 + \sigma_Y^2, \tag{3.1}$$

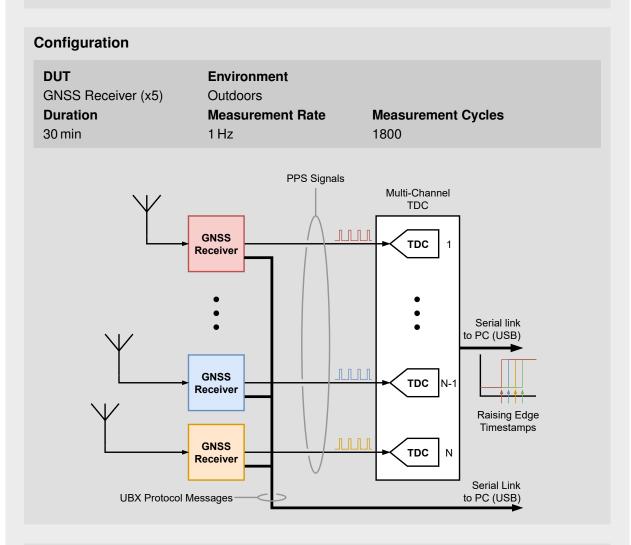
or the euclidean norm of their STDs:

$$\sigma_{\rm X+Y} = \sqrt{\sigma_{\rm X}^2 + \sigma_{\rm Y}^2}.$$
(3.2)

## Experiment 2 GNSS Signal Quality v. PPS Accuracy

#### Objective

Investigate the relation between GNSS signal quality and PPS signal timing accuracy

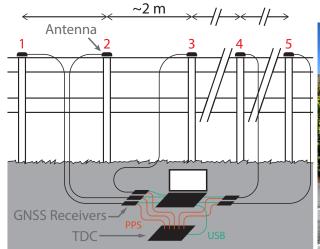


#### **Observed Quantities**

Quantity	Symbol	Source	Measurement Device	Resolution	Jitter (RMS) [ps]
Time of rising edge PPS		GNSS Recvr.	TDC	1 ps	42
Quantisation error	qErr	GNSS Recvr.	GNSS Recvr.	1 ps	0.29
Clock bias	clkB	GNSS Recvr.	GNSS Recvr.	1 ns	n/a
Clock drift	clkD	GNSS Recvr.	GNSS Recvr.	1 ns/s	n/a
Time accuracy estimate	tAcc	GNSS Recvr.	GNSS Recvr.	1 ns	n/a
Time DOP	tDOP	GNSS Recvr.	GNSS Recvr.	0.01	n/a

#### **Experiment Configuration**

Experiment 2 is setup with five ZED-F9T GNSS receivers each equipped with their own antenna, as shown in Figure 3.2. All receivers provide a PPS signal, each of which is measured on a separate channel of the TDC. These measurements are streamed to the host personal computer (PC) where they are recorded. Simultaneously, the GNSS receivers are configured to broadcast the messages shown in Appendix A, which are also recorded by the host. These messages include the receiver-estimated quantisation error of the PPS signal (which will be removed from the measured PPS timing error), as well as two indirect measurements of the signal quality: tAcc and tD0P.



(a) Diagram of the setup



(b) Picture of antenna arrangement and the test environment

Figure 3.2: Setup of Experiment 2 showing the antennas placed on fenceposts and connected to the hardware (host PC, GNSS receivers and the TDC) on the ground.

The experiment is conducted outdoors to achieve signal quality that is representative of that observed during a real-world deployment. The antennas are positioned on a line, spaced approximately 2 m apart, spanning 8 m in total. Even though the experiment is conducted in an urban location with nearby shrubbery and low-rise buildings (see Figure 3.2), all antennas have an unobstructed view of the sky in all directions from an angular elevation down to at least ~45°. To introduce a variation in signal quality during the experiment, some antennas are purposely and temporarily obscured. Two antennas are covered with aluminium foil, and one antenna was placed upside down under an air-conditioning unit for a part of the experiment time span.

#### 3.2.3 Differential Operation

The ZED-F9T GNSS receiver also supports differential operation [35], as introduced in Section 2.4.2. For this mode, one receiver must be designated as the master reference station, which broadcasts GNSS correction information to receivers with the slave station role. The slave stations use the received timing information to compute their time relative to the master. The expected increase in accuracy of time synchronisation between receivers operating in differential timing mode is investigated in Experiment 3. The timing accuracy between two GNSS receivers is evaluated in the default (absolute) mode and with the two in a differential configuration.

#### **Experiment Setup**

Experiment 3 consists of two GNSS receivers with their own separate antennas. The antennas are placed in the same window sill approximately 1 m apart. Both have a connection with the host computer on which the *u*-center program is running. This is the evaluation software for the ZED-F9T receiver. The u-center software arranges the forwarding of differential GNSS messages from the master device to the slave over the USB interface. The first half of the 30-minute measurement, the two receivers operate together in the normal (absolute) mode and there is no communication between the two devices. Then, after 15 minutes, the differential timing mode is activated and correction data is relayed from the master to the slave through the host computer.

### Experiment 3 Absolute v. Differential-Mode GNSS

#### Objective

Investigate the effect of the GNSS receiver's differential timing mode on the accuracy of the PPS signal

Configuration						
DUT GNSS Receiver (x2) Duration 30 min	Indoor	onment s, near windov urement Rate	Меа	Measurement Cycles 1800		
	GNSS Receiver (Master) PPS Signa Multi-Ch TDC	annel		Host Computer		
Observed Quantities						
Quantity	Source	Measurement Device	Resolution [ps]	Jitter (RMS) [ps]		
Time of rising edge PPS	GNSS Recvr.	TDC	1	42		

## 3.3 Software-Defined Radio

After having investigated the accuracy of the PPS signal, focus shifts to the SDR, where the timing accuracy is directly responsible for the accuracy of ToF observations. The experiments in this section are aimed to identify how timing error of the PPS signal is carried over to the local clock of the SDR (through the digital PLL), and subsequently, how the error of the of the local clock carries over to the front end of the device (through the digital interface and RF chain).

### 3.3.1 Front End

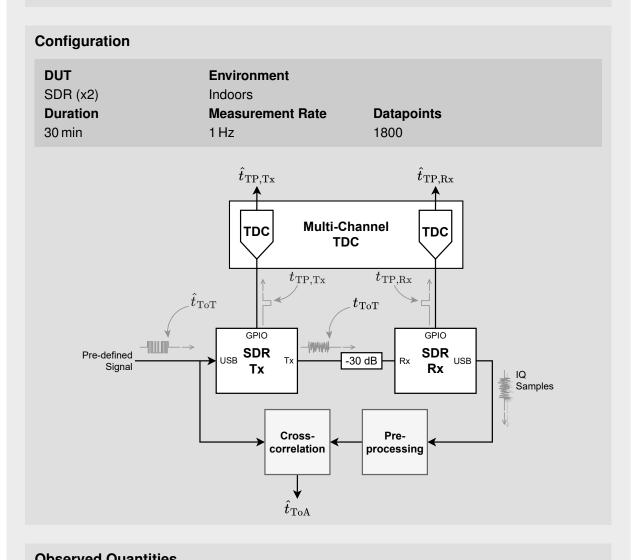
When considering the architecture of the USRP SDR, timed streaming of RF samples is handled by its FPGA. However, the digital interface of the FPGA only allows transfer of signals in baseband or intermediate frequency. The front end IC provides the interface between these low frequency samples and the up-converted RF signal. The jitter that a sample accumulates when propagating through the front end can be found by measuring the time interval between the moment it enters and leaves the device. This is done in Experiment 4, where jitter of the digital interface of the FPGA is measured in conjuction with the jitter of the RF interface. The difference between these values represents the jitter of the front end chain. Observing the front end jitter contributes to the research questions in two ways:

- 1. The timing offset between the two interfaces (GPIO and RF) of the front end denote to what degree a direct measurement of FPGA timing can be used to represent the timing accuracy of the SDR in the RF domain.
- 2. The timing behaviour of the SDR front end can be understood, contributing to the complete model of synchronised radio nodes.

## Experiment 4 Timing of SDR RF front end and GPIO

#### Objective

Evaluate timing offset between two SDR interfaces: the GPIO (time pulse) and the front end (RF signal)



Observed Quantities								
Quantity	Symbol	Observation Type	Source	Measurement Device				
Time at start of RF transmission	$\hat{t}_{\mathrm{ToT}}$	Estimation	Pre-defined	n/a				
Time at start of RF arrival	$\hat{t}_{\mathrm{ToA}}$	Measurement/Estimation	SDR Rx	SDR Rx & Host Software				
Time pulse at transmission	$\hat{t}_{\mathrm{TP,Tx}}$	Measurement	SDR Tx GPIO	TDC				
Time pulse at reception	$\hat{t}_{\rm TP,Rx}$	Measurement	SDR Rx GPIO	TDC				

#### **Experiment Setup**

In Experiment 4, two SDRs are in a cascaded configuration. During a measurement cycle, a known signal is transmitted from the first device (Tx) to the second (Rx) via a short ( $\sim$ 30 cm) cable and a –30 dB attenuator (to provent damage to the receiver). The signal used for the measurement is a maximum length sequence (MLS). The auto-correlation properties of this signal make it convenient for recovering its time shift [44]. The signal is modulated with a binary phase-shift keying (BPSK) scheme.

The Tx SDR is instructed to start transmission at  $\hat{t}_{\text{ToT}}$ . This instructed time serves as the estimate of the true ToT ( $t_{\text{ToT}}$ ). The Rx SDR is also instructed to start reception at  $\hat{t}_{\text{ToT}}$ . After the transmission and digital processing, a measurement of the true ToA ( $t_{\text{ToA}}$ ) is estimated from cross-correlation of the received signal with the MLS (see Appendix B).

The estimated ToF is now given by

$$\hat{t}_{\text{ToF}} = \hat{t}_{\text{ToA}} - \hat{t}_{\text{ToT}}, \qquad (3.3)$$

where  $\hat{t}_{\text{ToF}}$  represents an estimate of jitter between the RF interfaces of the SDRs.

Simultaneously with the measurements of the RF signal's ToT and ToA, the time offset between the two SDRs is measured from the digital interface of their FPGAs. For this, the GPIO bank is used, because it is exposed on the SDR (see Appendix C). To do so, both SDR devices are instructed to send a digital time pulse via the GPIO at  $\hat{t}_{\text{ToT}}$ . These time pulses are measured with a TDC, yielding  $\hat{t}_{\text{TP,Tx}}$  and  $\hat{t}_{\text{TP,Rx}}$ . Similar to  $\hat{t}_{\text{ToF}}$ , a measurement of the time offset between the GPIO interfaces is defined as

$$\Delta \hat{t}_{\rm TP} = \hat{t}_{\rm TP,Rx} - \hat{t}_{\rm TP,Tx}.$$
(3.4)

Finally, the contributions of the front ends to the time offset is given by  $\hat{t}_{\text{ToF}} - \Delta \hat{t}_{\text{TP}}$ .

Additional details about the techniques used in Experiment 4 are provided in Appendix B and Appendix C.

### 3.3.2 Synchronisation Accuracy over Time

The implementation of the control loop in the digital PLL of the SDR is a reason to assume that the synchronisation accuracy does not stay constant over time. By employing the GPIO used in Experiment 4 at a higher frequency, the clock offset can be characterised as a function of time during the course of a PPS interval, thus extending the synchronisation model. This is done in Experiment 5.

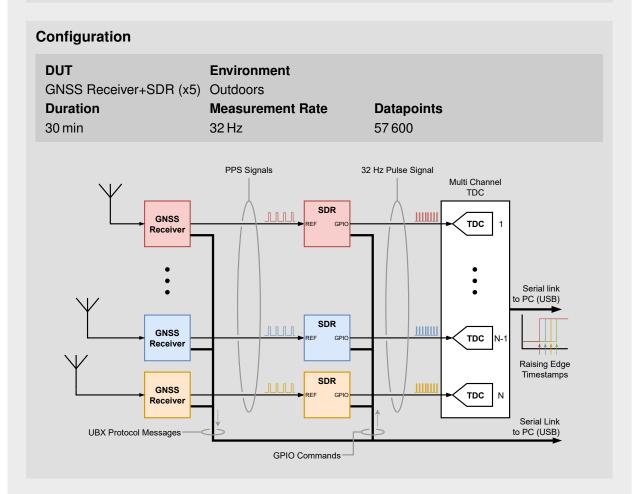
#### **Experiment Setup**

Similar to Experiment 2, five GNSS receivers are paired with their individual antennas. However, instead of directly measuring their PPS output signals, they are used as a time reference for five SDRs. The host computer is then used to instruct the SDRs to generate a GPIO time pulse at 32 Hz, similar to Experiment 4. The measurement rate of 32 Hz (a total of 160 commands per second) is chosen heuristically as a compromise between temporal resolution and prevention of scheduling or throughput conflicts. While there is no direct measurement of the PPS pulses, UBX messages with the clock parameters and the PPS quantisation error are collected from the receivers over the serial interface.

## Experiment 5 Jitter during Synchronisation Interval

#### Objective

Characterise clock jitter between PPS-synchronised SDRs as a function of time



#### **Observed Quantities**

Quantity	Rate [Hz]	Source	Measurement Device	Resolution	Jitter (RMS)
Time of rising edge time pulse	32	SDR	TDC	1 ps	42 ps
Quantisation error	1	GNSS Recvr.	GNSS Recvr.	1 ps	0.29
Clock bias	1	GNSS Recvr.	GNSS Recvr.	1 ns	n/a
Clock drift	1	GNSS Recvr.	GNSS Recvr.	1 ns/s	n/a
Time accuracy estimate	1	GNSS Recvr.	GNSS Recvr.	1 ns	n/a
Position and time DOP	1	GNSS Recvr.	GNSS Recvr.	0.01	n/a

# **Chapter 4**

# **Results and Discussion**

### 4.1 GNSS Receiver & PPS

### 4.1.1 PPS Quantisation Error

In Experiment 1, four GNSS receivers (labelled *A*, *B*, *C* and *D*) are connected to the same antenna and their PPS synchronisation signals are measured using the TDC (see Section 3.2.1). The total jitter between devices *A* and *B* during the measurement duration of 30 min with quantisation (quantised) and with the quantisation error removed in digital post processing (unquantised) is displayed in Figure 4.1. From visual inspection of Figure 4.1, one can already see that removing the quantisation error significantly reduces the jitter. The standard deviation of the absolute jitter between all pairs is 4.492 ns, while removing the quantisation error reduces this down to 3.030 ns. This reduction in timing error variation corresponds to an improvement in distance estimation error from 1.347 m to 0.908 m, respectively with and without quantisation error.

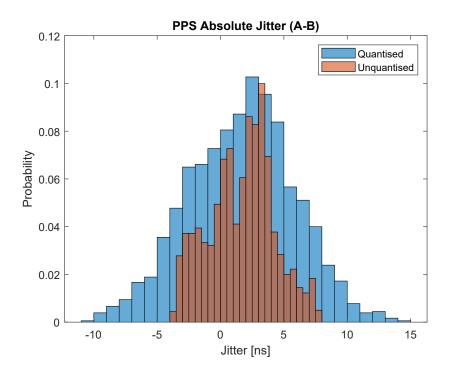


Figure 4.1: Absolute jitter between the GNSS modules A and B during the 30-minute measurement period.

The results are more interesting when one investigates the period jitter, instead of the absolute jitter (Figure 4.2). The period jitter is calculated by differentiating the measured absolute jitter in time. Figure 4.2 shows that the error between consecutive PPS pulse edges is dominated by the quantisation error. The observations show that the period jitter experiences a greater improvement than the absolute jitter through the removal of quantisation error. This is an indication that quantisation error has a greater influence on short-term stability than long-term stability.

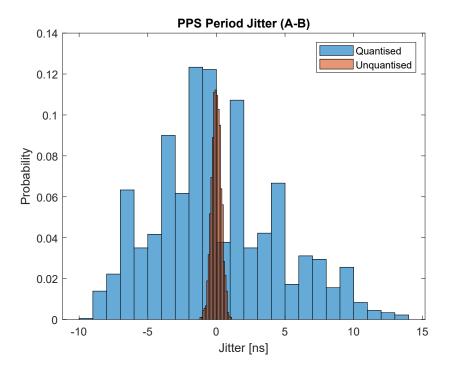


Figure 4.2: Period jitter between the GNSS modules *A* and *B* during the 30-minute measurement period.

This hypothesis is supported by the results in Figure 4.3, where the TDEV is used to indicate the stability between the devices as a function of the time interval, calculated from the absolute jitter. For the shortest measured interval of 1 s, the improvement gained by removing quantisation error seems the largest. The difference in TDEV between the measurements with and without quantisation error shrinks as the time interval increases. After a period of roughly 100 s, the difference has almost disappeared.

To support the results from Figure 4.3, the TDEV is also calculated for every pairing combination of devices *A* through *D*. These are displayed in Figure 4.4 and show that the stability increase gained by removing quantisation error occurs for all pairs of devices. The irregular TDEV at the larger intervals can be attributed to the smaller amount of data points of intervals that approach the total span of the experiment of 30 min.

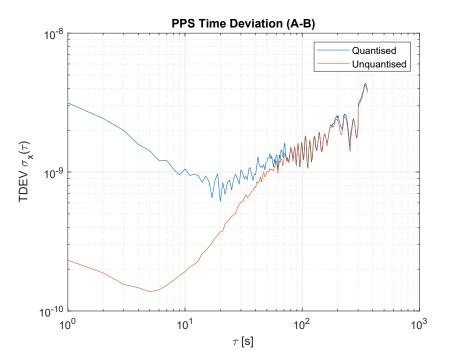


Figure 4.3: TDEV between the clocks of device A and B, measured from their PPS signals

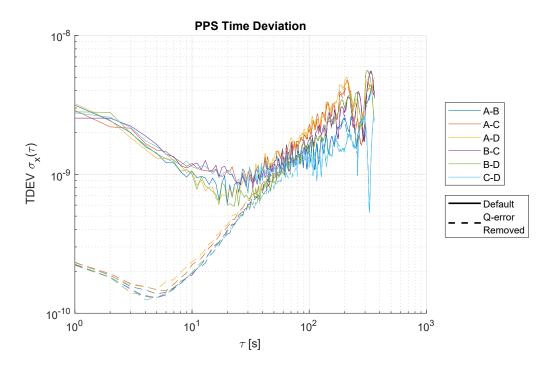


Figure 4.4: TDEV between the clocks of all devices in Experiment 1

The distribution of the reported quantisation error is shown in Figure 4.5a. It can be argued that the reported error approaches a uniform distribution between the -LSB/2 to LSB/2 interval (-4 ns to 4 ns). This means that the theoretical STD of the quantisation error (Equation (2.17)) should hold, which is equal to 2.3 ns. Both receivers have quantised their signal, meaning that the clock offset between the two devices combines the errors of both. The combined quantisation noise variance of devices A and B ( $\sigma_{Q,A+B}^2$ ) is calculated from the sum of their separate variances ( $\sigma_{Q,A}^2$  and  $\sigma_{Q,B}^2$ ):

$$\sigma_{\mathrm{Q,A+B}}^2 = \sigma_{\mathrm{Q,A}}^2 + \sigma_{\mathrm{Q,B}}^2 \tag{4.1}$$

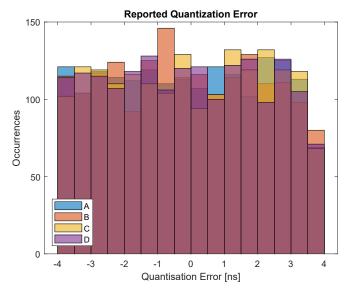
$$= (2.3 \,\mathrm{ns})^2 + (2.3 \,\mathrm{ns})^2 \tag{4.2}$$

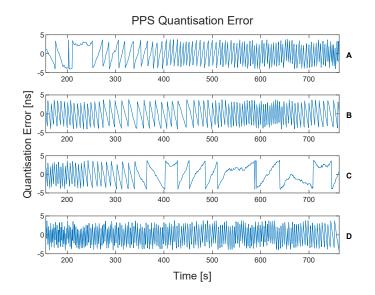
$$= 10.6 \, \mathrm{ns}^2,$$
 (4.3)

with the assumption that  $\sigma_{Q,A}$  and  $\sigma_{Q,B}$  are independent and have zero mean. This corresponds to the summarised observations in Figure 4.6a, which show an approximate 10.6 ns<sup>2</sup> reduction in variance of the absolute jitter when removing quantisation error. This is evidence that the quantisation error is independent of the unquantised component of the jitter.

However, the reported quantisation error is not undeterministic, as can be seen in Figure 4.5b. Here, the reported quantisation error is plotted during a period of the experiment for each receiver. The plot shows clear trends in the quantisation error, where the curves are wrapped at the edges of the quantisation step of 8 ns. Most likely, this behaviour is caused by the drift of the local clock. If this drift is constant, each PPS cycle it will shift the phase offset between the true time and the local clock phase with a constant amount too. This phase offset is then wrapped around the edges of the 8 ns clock period, causing an aliasing type effect. When the phase drift of the local clock during a PPS period is near a multiple of the clock period, it will generate the shallow slope seen in Figure 4.5b (the aliasing effect). Due to this high dependence between consecutive quantisation error values, the variance calculated in Equation (4.1) cannot be subtracted from the period jitter.

The spread (STD and variance) of both the absolute and period jitter between the paired GNSS receivers, summarised in Figures 4.6a and 4.6b, correspond with earlier made observations that the quantisation error has the most influence on short time scales. This can be seen from the fact that the difference between quantised and unquantised jitter spread is larger for period jitter than it is for absolute jitter. By removing the quantisation error, the mean absolute jitter STD has been reduced from 4.51 ns down to 3.09 ns. The mean period jitter of 4.265 ns (STD) was reduced to 0.34 ns. These results are also presented in Tables D.1 and D.2.





(a) Distribution of reported quantisation error for all devices (A through B) during the 30 minute experiment.

(b) Reported quantisation error of GNSS receivers A through D plotted over a duration of the experiment

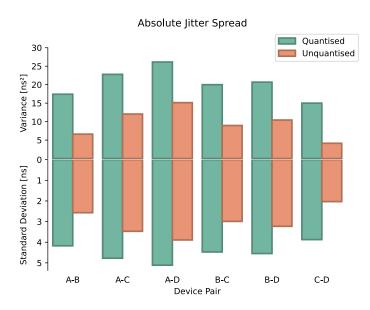
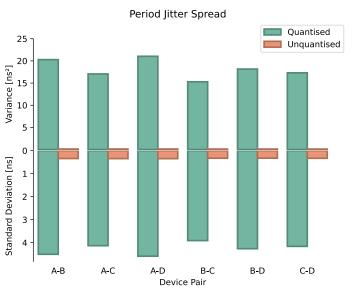


Figure 4.5: Quantisation error reported during Experiment 1



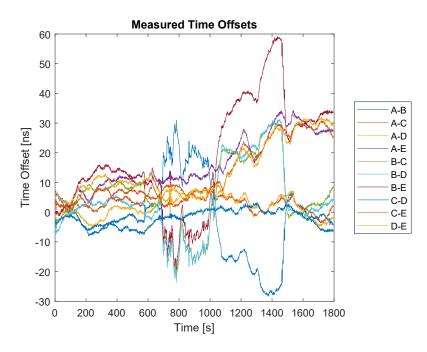
(a) Distribution of reported quantisation error for all devices (A through B) during the 30 minute experiment.

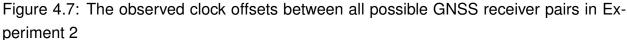
(b) Reported quantisation error of GNSS receivers A through D plotted over a duration of the experiment

Figure 4.6: Spread of jitter values measured during Experiment 1. The upper axes show the spread in variance, while the lower axes show STD.

#### 4.1.2 Signal Quality

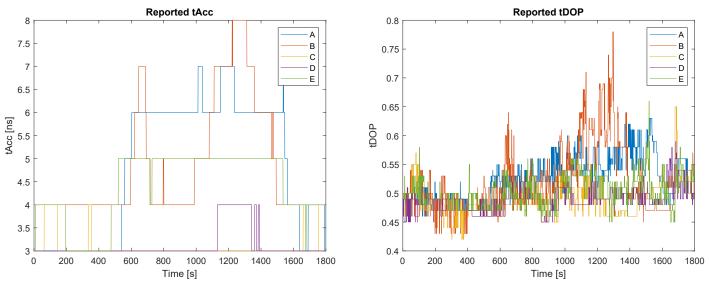
In Experiment 2, the alignment between PPS pulse edges from five GNSS receivers (A through E) are measured. Simultaneously, indicators of signal quality (reported DOP and time accuracy estimates) as well as the quantisation error are recorded from the receivers. This allows the PPS accuracy to be related to the signal quality, which is the focus of this experiment. Since the GNSS local time is derived from atomic clocks, which have excellent long-term stability, it is reasonable to assume that the clock offset is dominated by jitter and thus has a mean of zero. Figure 4.7 shows the measured time offsets between the receivers in all possible pairing combinations. The pairings with receiver B show the largest offsets, which can be attributed to the antenna having a partially to fully obstructed view of the sky during the experiment, including being temporarily placed upside-down.





As described in Section 3.2.2, during Experiment 2 multiple estimates are extracted from the receivers (see Appendix A), including the tAcc (time accuracy) estimate in nanoseconds and the unitless tDOP (TDOP). These values have been recorded and are shown in Figure 4.8. The reported time accuracy (tAcc) seen in Figure 4.8a ranges between 3 ns to 8 ns with a resolution of 1 ns. Due to the small range of the observed values with respect to the resolution, only 6 distinct tAcc levels are present in the measurements. The TDOP that is reported by the GNSS receiver (tDOP) can be seen in Figure 4.8b. The TDOP ranges between 0.42 and 0.78. The highest values again have been observed at receiver B. For each pair of tAcc values, assumed to be STDs, a combined value is found

from the euclidean norm (Equation (3.2)), resulting in values higher than 8 ns. The combined tAcc values have been discretised in 1 ns bins. This allows the the two-dimensional distribution of the PPS offset with respect to the signal quality estimates to be represented by a series of boxplots.



(a) The reported time accuracy estimate (tAcc) values

(b) The reported TDOP estimate (tDOP) values

Figure 4.8: The signal quality indicators tAcc and tDOP as reported by the GNSS receiver during Experiment 2

Now, for every clock offsets measurement, a corresponding tAcc is available. This allows the distribution of clock error to be evaluated as a function of tAcc. Figure 4.9 shows the distribution and standard deviation of the clock offsets in the experiment with respect to the combined tAcc values. As expected, the range of the clock offset expands as tAcc increases. However, the standard deviation of the clock offset is not monotonous. A local minimum appears at a reported time accuracy of 7 ns. Furthermore, at 10 ns and 11 ns, the standard deviation is significantly lower, but this is most likely to be caused by the small amount of samples observed in this region. Figure 4.9 shows that the tAcc value can be used as an indication of the absolute jitter, but does not serve as an accurate representation. In Figure 4.10, the measured clock offset is numerically differentiated to produce the period jitter. In contrast to Figure 4.9, the distribution of the samples shows little change as tAcc increases. This is not an unexpected result, as the tAcc described the instantaneous clock offset, and not its derivative.

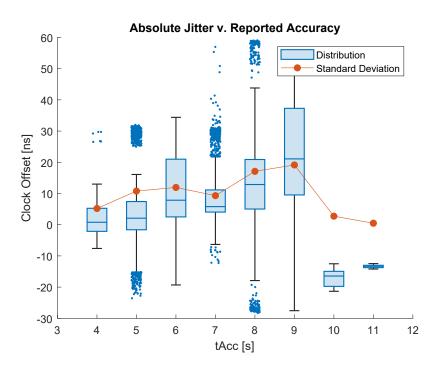


Figure 4.9: Distribution and standard deviation of absolute jitter, measured as clock offset between pairs of GNSS receivers in Experiment 2, plotted against the combined time accuracy reported by those receivers (square norm).

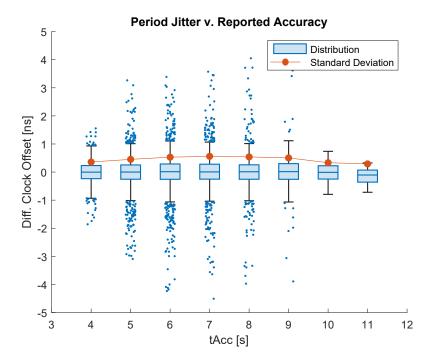


Figure 4.10: Distribution and standard deviation of period jitter, found by taking the derivative of the measured clock offset between pairs of GNSS receivers in Experiment 2, plotted against the combined time accuracy reported by those receivers (square norm).

Next, a similar method is applied to the tD0P signal quality indicator, in order to observe the distribution of the clock offset with respect to the TDOP. The tD0P values are combined in two manners: through their mean and from the maximum of the two. Similar to tAcc, the combined tD0P values are discretised so that the distribution of the timing error can be represented in boxplots. The clock offset with respect to the reported TDOP value (tD0P) is displayed in Figure 4.11. As with the previously results, monotonicity does not occur at larger values of the mean tD0P, most likely due to the low sample size (only 4 samples with a mean tD0P value of 0.7 have been observed). Therefore, only the mean tD0P values up to 0.65 should be considered. Lastly, the measurements from Experiment 2 are processed to show the relation between the TDOP and the period jitter in Figure 4.12. The non-monotonicity in the standard deviation hints that there is no linear relation between the two. Furthermore, the change in distribution is very small, especially in the 0.55 tD0P region that has the largest sample size.

During Experiment 2, the estimated clock parameters of the GNSS receivers were also recorded. These can be seen in Figure 4.13. The upper plot shows the unmodified drift. These curves suggest that there is a nearly constant, or slowly-changing offset between the drift values. When this constant component is removed by subtracting the mean from each individual drift curve, the lower plot is created. This plot shows that there is a strong correlation between the zero-mean component of the drifts. This could be explained by the fact that the receivers are in the same environment in terms of temperature and supply voltage. The receivers are all placed within approximately 1 m (same ambient temperature), and are powered by the same host laptop via USB. This might have affected the results, because it could cause individual clock errors to be dependent on each other. In a more realistic environment, where the devices are spaced further apart and separately powered, higher clock offsets could be observed.

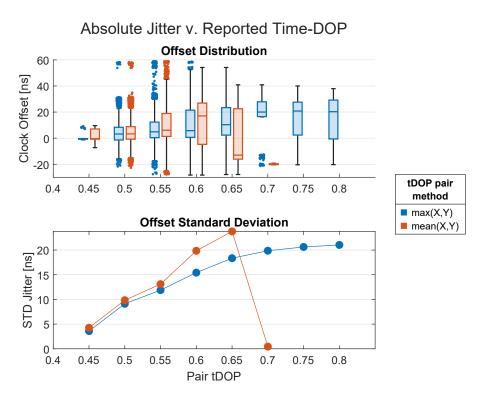


Figure 4.11: Distributions of absolute jitter plotted as a function of the discretised combined tDOP (through the mean and maximum of the pair)

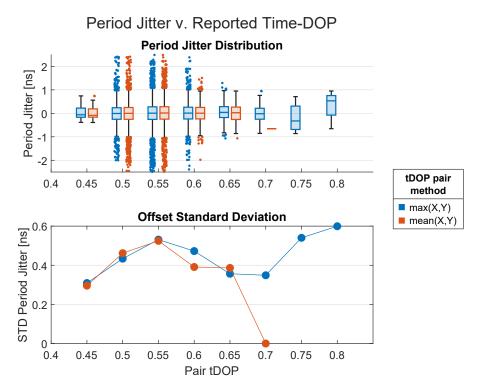


Figure 4.12: Distributions of period jitter plotted as a function of the discretised combined tDOP (through the mean and maximum of the pair)

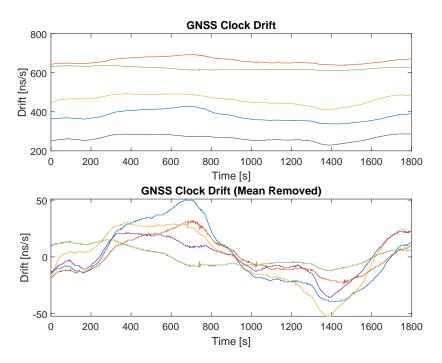


Figure 4.13: Reported clock drift of 5 GNSS devices acquired over serial link with the UBX protocol

#### 4.1.3 Absolute and Differential Mode

In Experiment 3, the jitter between GNSS-receiver-generated PPS signals is evaluated with two devices operating both separately and in the cooperative differential mode. The quantisation error of the signal has not been recorded in this experiment. Unexpectedly, the differential mode causes an increase in the absolute jitter STD (Figure 4.14a). This could be attributed to changes in environmental circumstances (weather conditions or satellite orientation) or random deviations (slow trends in clock offset) during progression of the experiment. A small decrease in period jitter STD is observed, as can be seen in Figure 4.14b. This is an indication that the differential mode has a bigger impact on short-term stability than it has on long term stability, similar to the effect of quantisation error.

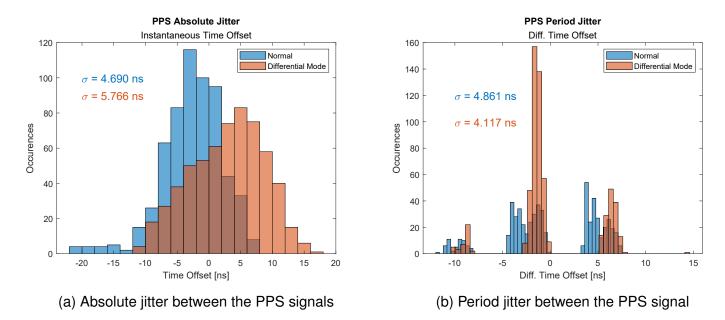


Figure 4.14: Time offset between two PPS signals generated by GNSS receivers operating in the default individual mode, and the cooperative differential mode

While the quantisation error has not been recorded from the GNSS receivers in this experiment, its effect can be subtracted from the absolute jitter. The results of Experiment 1 have shown that the quantisation error behaves like an independent variable and that its variance (Equation (4.1)) can be subtracted from that of the observed absolute jitter to find the unquantised jitter variance. This yields the results presented in Section 4.1.3. Removing the theoretical quantisation variance causes the relative difference between the normal and differential mode to grow even further. However, the absolute spread values are close to those observed in Section 4.1.1. This is an indication that the true spread of the gathered measurements is probably close to that of the calculated value. However, the degree to which the gathered measurements provide a true representation of the difference between the two modes is questionable.

	Quantised		Unquantised		
<b>Operation Mode</b>	Variance [ns <sup>2</sup> ]	STD [ns]	Variance [ns <sup>2</sup> ]	STD [ns]	
Normal	21.996	4.690	11.416	3.379	
Differential	33.247	5.766	22.667	4.761	

Table 4.1: Variance and STD of the clock offsets (absolute jitter) observed in Experiment 3, both with and without subtraction of the theoretical quantisation error.

## 4.2 Software-Defined Radio

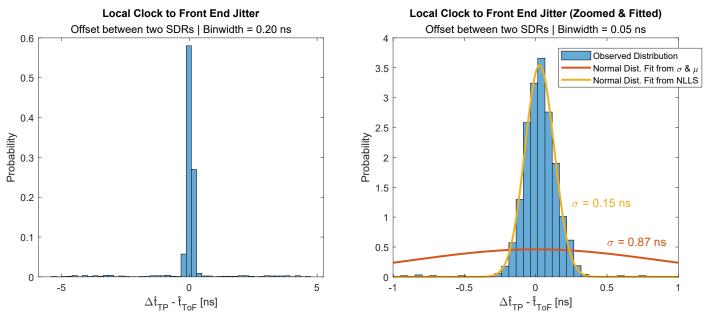
In this section, the results of Experiments 4 and 5 are discussed, both of which are related to the timing error of the SDR. First, the timing accuracy of the RF front end is measured, after which the SDR clock jitter is measured as a function of time.

### 4.2.1 Front End

In Experiment 4, an estimate is made on the jitter that occurs between the SDR's local clock and its front end. This jitter is represented by the (mean-removed) difference between the time interval measurements of the front end ( $\hat{t}_{\text{ToF}}$ ) and two GPIO-generated time pulses measured by the TDC ( $\Delta \hat{t}_{\text{TP}}$ ). The jitter is displayed in Figure 4.15. The jitter shown in Figure 4.15a is concentrated around 0 ns but has outliers up to approximately 5 ns away from the mean. It is possible that these outliers are a product of the estimation error of  $t_{\text{ToF}}$ , described in Appendix B. In Figure 4.15b, the absolute jitter has also been fitted to a normal distribution using two methods:

- a) By using the numerically calculated standard deviation and mean as  $\sigma^2$  and  $\mu$  of a normal distribution, respectively. This solution is heavily influenced by the outliers due to their large deviation from the mean.
- b) Using the non-linear least squares method. In this method, the outliers have a reduced contribution to the resulting standard deviation [45].

Method a) yields a standard deviation of 0.87 ns, while the more optimistic method b) yields a reduced STD of 0.15 ns. The difference can be attributed to the aforementioned measurement outliers. If these outliers are indeed a product of measurement error, then the lower STD would be the most representative of the two.



(a) Histogram showing the spread of  $\hat{t}_{\mathrm{ToF}} - \Delta \hat{t}_{\mathrm{TP}}$ 

(b) Zoomed-in view of the distribution with overlaid fitted normal distribution

Figure 4.15: Distribution of  $\hat{t}_{TOF} - \Delta \hat{t}_{TP}$  measured during Experiment 4

#### 4.2.2 Synchronisation Interval

In Experiment 5, the local clock offset between two SDRs is recorded at a frequency of 32 Hz. This reveals how the offset behaves as a function of time. The offset between two SDR clocks for a 16 s section of the experiment is displayed in Figure 4.16. The PPS reference pulse times are marked as vertical grey lines. Visual inspection reveals that linear trends (drift) occur during each 1 s synchronisation period, aligned with the PPS edges. This is caused by the digital PLL implemented on the SDR which periodically adjusts the local oscillator frequency.

Figure 4.17 shows the distribution of the clock offset for every PPS cycle, aligned and superimposed on one period. The graph shows that the accuracy is the lowest at the edges of the period (before and after the PPS rising edge). Towards the middle of the period, the accuracy is at its highest. A possible cause for this is the quantisation error of the PPS reference signal, which directly contributes to the phase error observed by the digital PLL. When the observed phase error is increased by the quantisation error, the control loop's correction will be too strong, causing an overshoot at the start of the following 1 s period. Evidence of this is provided in Figure 4.18 where the correlation between reported quantisation error and the clock offset at the start of the following PPS period is shown in a scatter graph. A linear fit was performed. The slope of this fit is -1.7. Since the magnitude of the slope is larger than 1, the quantisation error is amplified by the PLL.

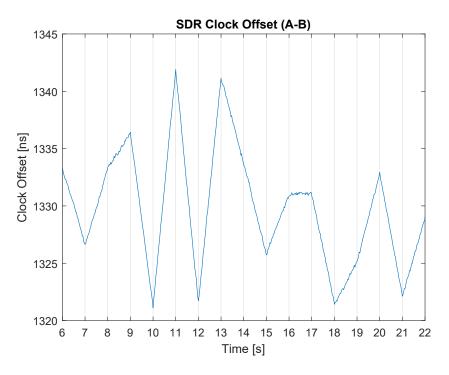


Figure 4.16: Offset between the clocks of devices A-B over time

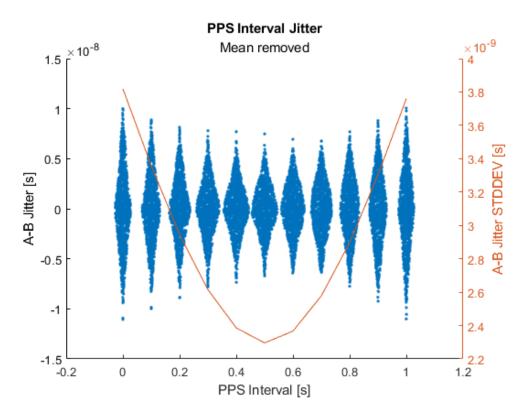


Figure 4.17: Accuracy of A-B timing during the interval of a PPS synchronisation period of 1 s

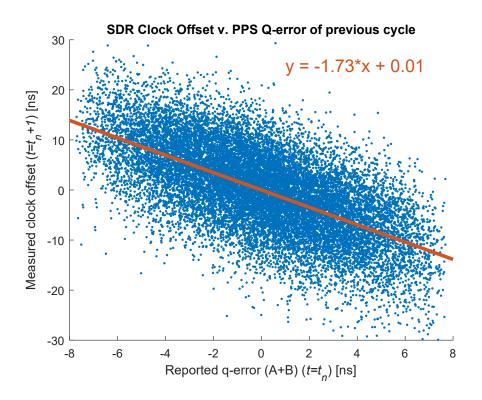


Figure 4.18: Scatter graph showing the correlation between reported quantisation error, and clock offset at the start of the following PPS period.

With a measurement of the clock offset at the PPS marks, yielding two measurements per PPS period, the bias and drift can be compensated for. This is shown in Figure 4.19, where the linearly interpolated PPS periods are subtracted from the original time series. While the mean standard deviation between all receiver pairs was 7.411 ns, compensating for the drift has lowered this value down to 0.186 ns. It is worth noting here that While higher order of drift could be compensated for in a similar way, it would require an additional offset measurement during the PPS period. In Figure 4.20, the drift-compensated offset between devices A and B during 150 PPS intervals is superimposed on a single PPS period. From the visual inspection, the remaining error in this plot is caused by a slight negative frequency drift and a seemingly random jitter.

These results show that the achievable accuracy of synchronisation between SDRs can go down to at least 0.186 ns. However, there is the availability for reduction of higher order clock attributes (frequency drift). However, a possible limitation in synchronisation is the seemingly random noise component of the offset.

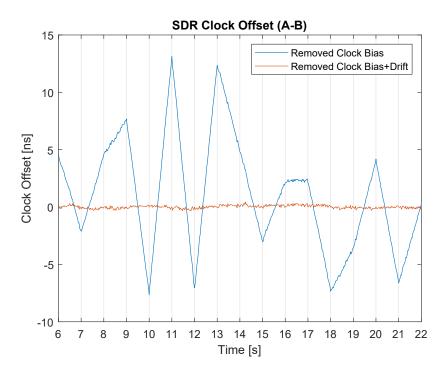


Figure 4.19: Clock offset between devices A and B during Experiment 5 with compensation for clock bias, and when compensated for both clock bias and drift.

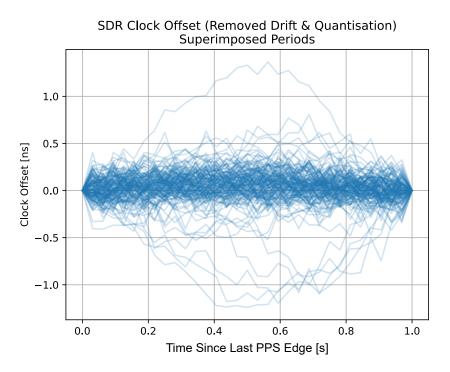


Figure 4.20: Super imposed A-B time offset with 1st degree polynomial de-trending (removed drift & offset) showing clock drift rate during the synchronisation period

# **Chapter 5**

# **Conclusions & Recommendations**

After a theoretical analysis of the implementation of time keeping and synchronisation of the ZED-F9T (u-blox) GNSS receiver and the USRP B200-mini (Ettus Research) SDR, as well as physical experimentation with these devices, the main research question

What are the limitations and sources of error in GNSS-based time synchronisation?,

can be revisited. The research has been split in the following three aspects:

- limitations and error sources in SDR time synchronisation using GNSS receivers
- methodology for the measuring timing error in PPS signals and SDR clocks
- modelling and validation of the timing error in radio nodes composed of a GNSS receiver and a SDR

In Chapter 2, theoretical background is provided on the topics of ToF localisation, time keeping and time synchronisation. This is done in a general sense, but also applied to the selected hardware. In subsequent research, a methodology for evaluation of synchronisation accuracy between different components of the radio node is developed (Chapter 3). Measurement results have been documented in Chapter 4. Based on these results, conclusions and recommendations are made, which are presented in this final chapter.

### 5.1 Limitations and Sources of Error

When a clock in electronics is derived from a LO, the accuracy of the clock is affected by deterministic offsets such as clock drift and frequency drift, as well as random zero-mean offsets that may be caused by undeterministic effects such as thermal noise. The GNSS receiver used in this study, the u-blox ZED-F9T, derives its sense of time from radio signals of satellites, and its accuracy is thus dependent on the quality of these signals. The accuracy is affected by the number of satellites and their geometric distribution (represented by the dilution of precision), as well as noise of the channel or receiver. In the case of the PPS time signal generated by the GNSS receiver, an important source of error is quantisation of the signal by the local clock.

Furthermore, the investigation of the architecture of the Ettus Research b200-mini SDR revealed the workings of the digital PLL used to synchronise the local clock with

the PPS signal. This PLL is implemented on synchronous hardware and also quantises the PPS signal, adding more noise to the system. While the PLL adds jitter to the clock offset, this noise is demonstrated to be largely deterministic and can be compensated for, leaving seemingly random noise sources as the limiting component.

### 5.2 Measuring Synchronisation Error

The next issue that this thesis addresses is the manner in which synchronisation error between radio nodes can be evaluated. In Experiment 4, the timing offset between two SDRs was measured using two methods simultaneously:

- a) from a known RF signal transmitted from the first SDR to the second,
- b) with time pulses generated by each SDR's GPIO, measured with a TDC.

The difference between these two measurements represents the twice jitter between the SDR's FPGA and front end (FPGA to front end for the transmitting SDR, and vice versa for the receiving SDR). The results show that the offset has a standard deviation of 0.87 ns. However, assuming that the distribution is normal and that outliers are caused by the measurement method, a new solution for the fitting of a normal distribution can be found with a standard deviation of 0.15 ns. This error is very small with respect to the lowest absolute jitter observed between SDRs in Experiment 5, which was approximately 2.3 ns STD. This leads to the conclusion that measurements of the clock offsets between SDRs through their GPIO output are representative of the timing error between their front ends.

The main advantage of method a) is the simplicity of the hardware configuration; measuring the offset between two SDRs only requires a single coaxial cable from the first device to the second. However, even though methods a) and b) have yielded very similar results, measuring the time offset of SDRs through the front end has proven to be an impractical method because it requires post-processing. Furthermore, the frequency with which it can be executed and the duration of the experiment is constrained by the throughput of the USB interface, storage space for samples and speed at which the samples are processed. These limitations also cause the method to scale up poorly when measuring multiple clock offsets simultaneously.

In contrast, the developed method b) has several advantages. First, it does not require post-processing. Additionally, it has been employed at a rate of 32 Hz without any issues, while method a) has proven problematic at just 1 Hz due to USB throughput. Method b) also scales well with the number of devices because, after the initial addition of a multi-channel TDC, only an adapter (see Appendix B) and coaxial cable is required for each device added to the experiment. Given its advantages, method b) has been employed for all experiments involving the SDRs in this thesis.

## 5.3 Error Model

After gaining a theoretical understanding of the selected hardware and the involved sources of error, in addition to having developed a method for the evaluation of these errors, experiments have been conducted to quantify them. Consecutively, the results have been used to evaluate to what degree the error sources are deterministic and whether they can be compensated for.

### 5.3.1 GNSS Receiver

#### **Quantisation Error**

The first experiments were focused on the GNSS receiver and the PPS signal it generates. Results of Experiment 1 have shown that quantisation error contributes to the PPS signal jitter significantly. However, the experiment also shows that it can be compensated for by extracting information from the receiver via a serial communication link. For the absolute jitter between two PPS signals, an improvement of 1.46 ns (STD) was achieved by removing the quantisation error (4.49 ns to 3.03 ns). An even greater reduction was achieved in the period jitter, which was reduced from 4.26 ns to 0.337 ns.

#### **Time Accuracy Estimate and Dilution of Precision**

From the results of Experiment 2, the relation between the PPS timing error and the signal quality indicators tAcc and tDOP has been evaluated. The spread of the absolute jitter shows a correlation with tAcc, but it is not monotonous. While the two values are on the same order of magnitude and represent the same physical quantity in a practical sense, the observations show that one can only be a rough indication of the other. This is less true when comparing the period jitter with tAcc; the distribution of the period jitter shows little observable change as tAcc is increased, and the two do not share the same order of magnitude. However the standard deviation of absolute jitter is strongly correlated with the reported tDOP. It can be concluded that for accurate time synchronisation between GNSS receivers, there is a demand for good TDOP. Furthermore, the tDOP can be used as an indicator of the achievable timing accuracy. The non-monotonicity when plotting the period jitter as a function of tDOP is also an indication that there is no direct relation between these two quantities.

#### **Differential Mode**

It is difficult to draw conclusions from the results of Experiment 3 because the results are unexpected. Instead of a decrease in clock offset STD, a small increase was observed. This could be attributed to random fluctuations of the environment and obscuring of the

results due to quantisation error. However, a small decrease in period jitter was observed, indicating that short-term stability benefits more from the differential mode than long-term stability does.

To get a better understanding of the effect of the differential mode on the PPS accuracy, Experiment 3 should be repeated. However, to acquire more reliable data, both modes (the default mode and differential mode) should be tested simultaneously. This could be done using multiple receivers and RF splitters. Furthermore, the quantisation error should be recorded and removed, similar to Experiment 1.

### 5.3.2 Software-Defined Radio

#### Radio Front End

In Experiment 4, the front end of the SDR is subject to investigation. Previously mentioned time offsets between GNSS receivers, and following offsets between SDR devices are significantly larger than the jitter observed between the FPGA GPIO output and the front end's RF interface. The observed standard deviation of this jitter is 0.87 ns. However, with the assumption that the measurement method adds error, outliers can be filtered out resulting in an even smaller spread of 0.15 ns (STD). This jitter is a minor contribution to timing offset between radio nodes.

#### Digital Phase-Locked-Loop

In contrast, the digital PLL of the SDR has been identified as a major source of timing error. Experiment 5 reveals that the clock offset between two SDRs jumps around its mean with a standard deviation of 7.411 ns. However, the experiment has also shown that the offset is highly deterministic in two manners. First, it is heavily influenced by the quantisation error of the PPS reference signal. The quantisation error forces the control loop of the PLL to overshoot, causing the error to re-appear in the clock offset in an amplified manner. Secondly, during the 1 s interval between two PPS edges, the clock offset follows an approximately linear path. Using the clock offsets observed at the two PPS edges, the drift during this period was removed in post-processing. This process has reduced the absolute jitter from 7.411 ns down to 0.186 ns (STD).

Two conclusions can be drawn:

 When timing accuracy is not required to be real time, meaning post-processing can be used, the clock offset is not limited by the digital PLL or jitter of the reference signal. It can be greatly reduced through linear interpolation of the offset between PPS periods. This requires a measurement of the phase difference between the PPS reference signal and the SDRs local clock, which is available through the firmware [11]. • When time synchronisation must be achieved in real-time, it is crucial to limit the jitter of the PPS reference signal since errors in this signal end up at the SDR local clock in an amplified manner.

### 5.4 Recommendations for Real-Time Implementation

During the synchronisation process between the clock of the GNSS receiver and the clock of the SDR, a significant contributor to error has been identified to be the quantisation noise of the PPS signal. It has been concluded that this error can be compensated for both real time and during post-processing. For a real-time solution, it is possible to communicate the quantisation error to the SDR's FPGA and compensate for it digitally, as seen in Section 4.1.1. This requires a change in the FPGA firmware that implements a serial interface with the GNSS receiver and adapts the PLL so that it removes the quantisation error.

As shown in Section 4.2.2, when post processing is available, or synchronisation can be performed near real time (when the time estimate of a moment is available with a delay from the moment at which it occurred), any jitter in the PPS signal can be compensated for with two observations of the clock offset with respect to the reference signal, after which the local clock offset during the preceding period can be found through interpolation. This leaves only the errors caused by (random) jitter and higher order drift of the local clock. The fact that jitter in the time reference is tolerated in this method opens the door for other references like serial communication and indirect measurement methods like joint position-clock estimation, where ToF observations are not only used to measure range, but also deterministic clock parameters.

An alternative approach for real-time synchronisation would be to have the receiver and SDR share a single clock directly. This can be achieved by using the internal clock signal of the GNSS receiver as a master clock at the SDR. However, this would require a change in hardware because both the GNSS receiver and the SDR do not have an output and input (respectively) for an external clock. Alternatively, GNSS signals can be received and processed by the SDR directly.

## 5.5 Comments on Suitability of GNSS-based Time Synchronisation for Localisation

Experiments in this study have shown that the largest sources of error for time synchronisation of SDR devices with GNSS receivers are deterministic, and can be compensated for. However, for each step in the synchronisation process between the GNSS receiver and the SDR, jitter is added. Compensation for these error sources adds to the complexity of the solution and poses new constraints.

The results presented in this thesis indicate that with the GNSS-based synchronisation method, given the availability of (near) real-time post-processing, it is possible to achieve time synchronisation between distributed SDRs that is accurate enough for distributed ToF-based localisation applications. The experiments have shown that, depending on the environment, the time offset between SDRs can be reduced to sub-nanosecond levels, leading to ranging errors in the centimetre range.

### 5.6 Further Research

In scenarios where post-processing is available, there might also be different synchronisation methods available that are less complex in their implementation. Synchronisation methods that utilise the already-present hardware like an overhead communication link and both on-board and central digital hardware, like the *White Rabbit* protocol or joint position-clock estimation, could provide a viable alternative to GNSS-based time synchronisation in such scenarios.

Owing to practical constraints of the SDR firmware, time synchronisation was achievable solely by employing a PPS (1 Hz) reference signal. It is worth exploring the performance of the SDR's digital PLL at reference pulse wave frequencies beyond the current limitations (both higher and lower). Correspondingly, the accuracy of the reference pulse wave signal could be measured as a function of its frequency.

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## Acronyms

API application programming interface. 19

BPSK binary phase-shift keying. 39, 73

CMOS complementary metal-oxide-semiconductor. 16

CPLD complex programmable logic device. 6

CSAC chip-scale atomic clock. 5

DAC digital-analog converter. 20, 21

DOP dilution of precision. 24, 32, 47, 70

DSP digital signal processing. 19

ESD electrostatic discharge. 23

FDMA frequency-division multiple access. 4

FIR finite impulse response. 18

**FPGA** field-programmable gate array. 6, 18–22, 29, 37, 39, 60, 62, 63

**GNSS** global navigation satellite system. 4–9, 22–36, 40, 42, 43, 45, 47, 48, 50, 52, 53, 59, 61–64, 78

GPIO general-purpose input/output. 19, 37-40, 54, 60, 62

IC integrated circuit. 18-21, 25, 37

IF intermediate frequency. 6, 17

LO local oscillator. 6, 13-15, 21, 28, 59

LOS line of sight. 23

LSB least significant bit. 21

MLS maximum length sequence. 39

PC personal computer. 34

- **PDF** probability density function. 24
- PLL phase-locked loop. 6, 18, 21, 37, 40, 55, 59, 60, 62–64
- **PPS** pulse per second. 5–9, 13, 16, 17, 21, 22, 25, 26, 28–34, 36, 37, 40–45, 47, 48, 53, 55–57, 59–64, 78
- **PVT** position, velocity and time. 22, 24
- **RF** radio frequency. 7, 17, 30, 37–39, 54, 62
- **RMS** root mean square. 15, 21, 22, 30
- RTT round-trip time. 7
- **SDR** software-defined radio. 6–9, 17–22, 28, 29, 37–41, 54, 55, 57, 59, 60, 62–64
- **SNR** signal-to-noise ratio. 24, 73
- SPI serial peripheral interface. 18
- **STD** standard deviation. 5–7, 15, 22, 25, 26, 32, 45–47, 52–54, 60–62, 78
- **TDC** time-digital converter. 30, 34, 39, 42, 54, 60
- **TDEV** time deviation. 16, 43, 44
- **TDMA** time-division multiple access. 4
- **TDOP** time-DOP. 24, 47, 48, 50, 61
- TIE time interval error. 15
- ToA time of arrival. 7, 39, 73
- **ToF** time of flight. 4, 5, 7–12, 22, 23, 29, 37, 39, 59, 63, 64
- **ToT** time of transmission. 7, 39
- TTL transistor-transistor logic. 16
- **UHD** USRP hardware driver. 19, 20
- **URE** user range error. 24
- **USB** universal serial bus. 17, 19, 25, 30, 32, 35, 50, 60
- USRP universal software tadio peripheral. 17–21, 37, 70, 73
- **UWB** ultra wideband. 7

# **Appendix A**

# **UBX Protocol Messages**

The following three tables contain the formats of UBX protocol messages that are transmitted from the u-blox ZED-F9T GNSS receivers to the host computer periodically during experiments.

UBX-N	UBX-NAV-CLOCK (20 bytes)						
Bytes	Name	Unit	Description				
4	itow	ms	GPS time of week of the navigation epoch				
4	clkB	ns	Clock bias				
4	clkD	ns/s	Clock drift				
4	tAcc	ns	Time accuracy estimate				
4	fAcc	ps/s	Frequency accuracy estimate				

Table A.1:	UBX	protocol	message	format	for	clock	parameter	estimates.	Summarised
from [35].									

UBX-N	AV-DOP (*	18 bytes)	
Bytes	Name	Unit	Description
4	itow	ms	GPS time of week of the navigation epoch
2	gDOP	-	Geometric DOP
2	pDOP	-	Position DOP
2	tDOP	-	Time DOP
2	VDOP	-	Vertical DOP
2	hDOP	-	Horizontal DOP
2	nDOP	-	Northing DOP
2	eDOP	-	Easting DOP

Table A.2: UBX protocol message format for dilution of precision values. Summarised from [35].

Bytes	Name	Unit	Description
4	towMS	ms	Time pulse time of week according to time base
4	towSubMS	ms	Submillisecond part of TOWMS
4	qErr	ps/s	Quantization error of time pulse
2	week	weeks	Time pulse week number according to time base bitmask (Time base GNSS/UTC, Availability UTC,
1	flags	-	(T)RAIM information)
			Time reference information (GNSS reference
1	refInfo	-	information, UTC standard identifier)

**UBX-TIM-TP** (16 bytes)

Table A.3: UBX protocol message format for information about the PPS signal, including an estimate of its quantisation error. Summarised from [35].

# **Appendix B**

# **Through-Radio Delay Measurements**

This chapter elaborates on the techniques used in Experiment 4.

## B.1 Pulse Code

To recover the ToA of the signal, the delay will be found using cross-correlation. To optimise the SNR, the full bandwidth should be used. For this purpose, pulse compression is used.

A maximum length sequence is used as the signal code. This binary time-discrete signal has the property that it uses the full spectrum. Furthermore, its auto-correlation approaches the Dirac delta function [44]. The code has an arbitrarily chosen length of 65 536 samples with a sample frequency of 56 MHz (the highest possible baseband frequency of the USRP), resulting in a duration of 1.2 ms. The digital signal is modulated using the BPSK scheme, and upconverted with a carrier frequency of 2.8 GHz.

## B.2 Pre-Processing

### B.2.1 Cropping

A signal received by device Rx is shown in Figure B.1. Most of the samples are taken when device emphTx was not transmitting. These samples are cropped out by creating an envelope of the signal power and cutting off the low amplitude parts before and after the transmission. These samples carry no information about the delay. Removing them reduces the computational load of following steps.

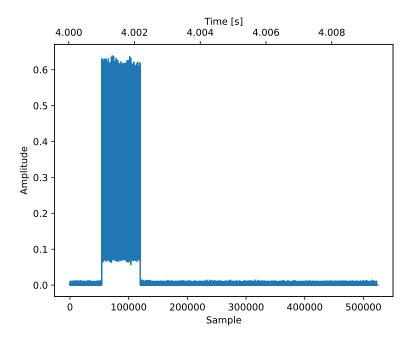


Figure B.1: Sampled and down-converted pulse as received by the sdr

#### B.2.2 I/Q Alignment

#### Method

Due to phase and frequency offset of the local oscillators of *Tx* and *Rx*, the symbols of the pulse code have been phase-rotated in the complex plane. In this form, cross-correlation with the MSL will not provide in the desired result. Therefore, the samples should be realigned with the real-axis, after-which the real part of the signal can be cross-correlated with the MLS.

Re-alignment with the real axis is done by measuring the phase rotation of the constellation. This relatively straightforward with the rotational symmetric BPSK constellation of two points:

$$\theta[i] := \operatorname{Arg}\left(x[i]\right) \mod \pi,\tag{B.1}$$

where  $\theta[i]$  is the instantaneous estimated constellation phase angle, x[i] is the received discrete signal and the function Arg denotes the two-argument arctangent of a complex number. The modulo of  $\pi$  is used to make sure the -1 and 1 symbols result in the same observed phase angle. To filter out high frequent noise, the detected phase angle is smoothed with a moving average filter. Through empirical means, a window length (N) of 1000 samples is chosen as a balance between noise reduction, computational complexity and preservation of the deterministic trend in phase deviation. This yields  $\theta_{\text{smooth}}[i]$ :

$$\theta_{\text{smooth}}[i] = \left. \frac{\theta[i] * \text{rect}_{N}[i]}{N} \right|_{N=1000},$$
(B.2)

where

$$\operatorname{rect}_{N}[i] = \begin{cases} 1, & \text{if } -\frac{N}{2} > i \ge \frac{N}{2} \\ 0, & \text{otherwise} \end{cases}.$$
(B.3)

Finally, the estimated phase offset is corrected for by rotating the samples back with  $\theta_{\text{smooth}}[i]$  as follows:

$$x_{\text{aligned}}\left[i\right] = x\left[i\right]e^{-j\theta_{\text{smooth}}\left[i\right]} \tag{B.4}$$

#### Problems

The described alignment method has two known flaws:

- a) The implementation of the moving average filter through convolution with a rectangular filter does not properly handle the edge cases. At the beginning and end of the filtered sequence  $\theta_{\text{smooth}}[i]$ , where the signal and the rectangular window do not completely overlap, boundary condition are occurring due to zero-padding.
- b) If  $\theta[i]$  passes through 0 or  $\pi$ , a jump of  $\pm \pi$  is introduced because of the wrapping behaviour of the Arg function and the  $\pi$  modulo. In the smoothed signal  $\theta_{\text{smooth}}[i]$ , this can throw off the phase angle estimate because values on both sides of the discrepancy are averaged together.

Flaw a) has the property that it systematically occurs in every measurement cycle. It is expected that the phase noise introduced at the edges of the sampled signal contributes to the spread of the observed delay, shown in Figure 4.15b.

Due to the arbitrary phase offset of the local oscillators of Tx and Rx, the amount of phase wrappings during a transmission, as described in problem b), can be different between measurement cycles. If the error occurs sporadically, then problem b) could be the cause for the outliers observed in Figure 4.15.

### **B.3 Cross-Correlation**

because the signal is band-limited, a perfect reconstruction can be made using sinc interpolation before or after calculating the cross-correlation

in Figures B.2 and B.3, interpolation is performed after cross-correlation. however, in the experiment, the order has been reversed in order to speed up processing. instead, a bisect optimalisation alrogithm is used to perform cross correlation on signals has have been time-shifted in fourier domain

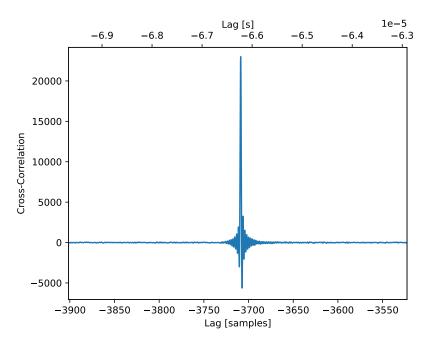


Figure B.2: Whittaker–Shannon interpolated cross-correlation of the MLS code with the demodulated signal received at Rx SDR

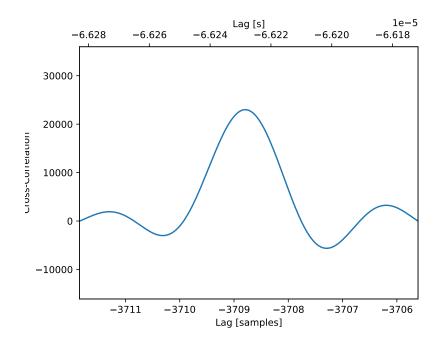


Figure B.3: Whittaker–Shannon interpolated cross-correlation of the MLS code with the demodulated signal received at Rx SDR (Close-up of the peak)

# Appendix C

# Interfacing with the SDR GPIO

The available GPIO pins on the USRP are using the *LVCMOS* (pull-up) interface standard at 3.3 V [11]. This pin is available through a 1.25 mm pitch header on the USRP circuit board. Through coaxial cabling ( $Z_0 = 50 \Omega$ ), the signal should be connected to a load with the same impedance. The termination resistance of 50  $\Omega$  can be driven by the Spartan FPGA [46]. However, a physical interface between the two sockets is still required. For this reason, a custom adapter was designed and realised. The adapter, shown in Figure C.1, features a wire-to-board socket for the connector that is used on the SDR. The 3.3 V wires on this cable are shorted to ground with ceramic capacitors to have them available as a return path for high-frequency components of the signal.

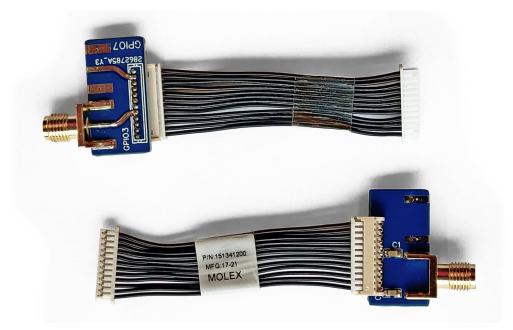


Figure C.1: Custom designed adapter for connecting the USRP GPIO to the TimeTagger

# **Appendix D**

# **Additional Results of Experiment 1**

Jitter Variance [ns <sup>2</sup> ]		Abso	olute	Period	
Qua Device Pair	Quantised evice Pair		No	Yes	No
	A-B	17.414	6.600	20.286	0.117
	A-C	22.791	12.041	17.057	0.120
	A-D	26.133	15.132	21.041	0.120
	B-C	19.999	8.940	15.280	0.109
	B-D	20.684	10.426	18.156	0.110
	C-D	15.000	4.129	17.306	0.110
	Mean	20.337	9.545	18.188	0.114

Table D.1: Variance of the absolute and period jitter between paired GNSS receivers observed during Experiment 1. The PPS signals are compared during a time span of 30 minutes.

Jitter STD [ns]	Abs	olute	Period	
Quantised Device Pair	Yes	No	Yes	No
A-B	4.173	2.569	4.504	0.342
A-C	4.774	3.470	4.130	0.346
A-D	5.112	3.890	4.587	0.347
B-C	4.472	2.990	3.909	0.330
B-D	4.548	3.229	4.261	0.326
C-D	3.873	2.032	4.160	0.331
Mean	4.492	3.030	4.258	0.337

Table D.2: STD of the absolute and period jitter between paired GNSS receivers observed during Experiment 1. The PPS signals are compared during a time span of 30 minutes.