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Electrostatic Simulation of Bi-Implanted Silicon Single-Electron Transistor Nanodevices

Bachelor's Thesis by

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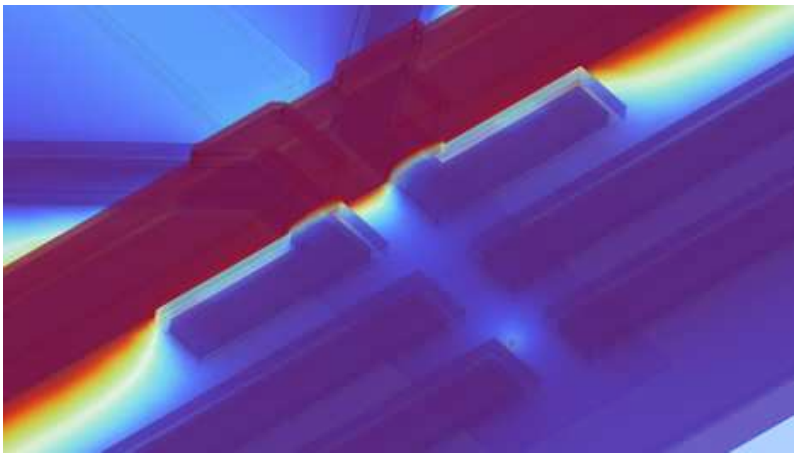

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Abstract

Although donor-based qubit devices show promise for scalable quantum computing, fabrication uncertainties impede the reliability of such devices, therefore restricting large-scale usage. Models and simulations can play a vital role in improving device robustness by allowing for verification of device operation, identification of potential fabrication errors and defects, and triangulation of specific donor atom locations, so they can be used as qubits.

In this research, we create an electrostatic model of a bismuth-implanted silicon nanodevice consisting of a single-electron transistor (SET) and a number of gates. The SET is used for precise charge sensing of bismuth (donor) atoms, which is needed to use them as qubits. After extracting capacitance data from experimental measurements of the nanodevice, we refine the model's geometry to better represent the fabricated device, revealing potential misalignment of two fabrication layers in the order of 10 nm. Next, we perform donor triangulation by varying simulated donor position and matching simulated capacitances to experimental data. We are able to estimate the position of a donor within a region of approximately 10 nm $\times$ 10 nm — a factor of 400 times more accurately than the predicted donor implantation window prior to simulations. Additionally, we conduct strain simulations, and, in conjunction with triangulation results, identify a potential unintentional strain-induced quantum dot in the vicinity of the SET.

We conclude that electrostatics simulations can be used to significantly enhance knowledge of donor positions, though they do not suffice for prediction of donor depth within the silicon substrate.

Acknowledgements

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Contents

Chapter 1
Introduction

The advent of quantum computing presents the possibility of solving a variety of challenges in science and engineering fields with greater speed and efficiency than classical computing [1]. While there are numerous means of implementing quantum computing architectures, donor-based architectures in silicon are particularly interesting due to their long coherence times [2], and potential scalability [3]. In such systems, donor atoms act as qubits, the fundamental building blocks of a quantum computer, where information can be encoded in the donor atom's nuclear spin [4] or electron spin [3]. Using spin-to-charge conversion, a single-electron-transistor (SET) can be used to infer the electron spin of donor atoms. This is because an SET can act as a precise charge sensor, making it able to detect whether a given donor atom is in a neutral or ionized state [4].

Despite the aforementioned points of interest regarding donor qubit systems, current experimental setups do not exhibit the required reliability to function as robust quantum computers [2]. This is partially attributed to uncertainties in the fabrication processes of these devices, such as the precise position of the doped donor atoms [2]. This substantiates the importance of models and simulations when attempting to fabricate these kinds of devices, as they can offer crucial insights into device verification, donor position, and potential fabrication errors.

The goal of this research is to create an electrostatic model of a Bismuth donor qubit device in order to verify device operation and perform donor triangulation based on experimental capacitance data. Moreover, we investigate the extent of accuracy with which we can determine the donor position using just electrostatics simulations, performed using COMSOL® Multiphysics software. The relevance of strain effects to device operation is also investigated by simulating the thermal contraction of the modelled geometry when it is cooled from annealing to operating temperature.

Note that while simulations for these kinds of devices also often take into account quantum-mechanical effects, such as donor electron wavefunctions and hyperfine splitting [2], we choose to focus on just electrostatic and strain models in this research.

In this thesis, we first go over relevant theoretical background in chapter 2, followed by an overview of the specific device being studied, both in terms of architecture and theoretical analysis, in chapter 3. The general methodology followed throughout the thesis as well as simulation details are presented in chapter 4, and an analysis of simulated and experimental results is conducted in chapter 5. This includes both model adjustment based on experimental data, as well as donor triangulation. Finally, future insights and concluding remarks are presented in chapter 6.

Chapter 2
Theoretical Background

In this chapter, we detail some of the relevant theoretical background to this thesis. We first provide a brief overview on SETs and quantum dots. Next, we address the Maxwell capacitance matrix, and how it used to analyze a system with multiple conductors by means of their various capacitive couplings. Lastly, strain effects on solid-state devices are discussed, including the emergence of strain-induced quantum dots.

2.1 SETs & Quantum Dots

Single-electron transistors are electrical devices in the nanometer regime, which employ the physical phenomena of quantum confinement and tunneling to achieve single-electron transport [5]. The general structure of an SET consists of source, drain, and gate electrodes, all capacitively coupled to an island, referred to as a quantum dot [6]. The source and drain electrodes are separated from the quantum dot by insulating material which serves as a tunneling barrier, through which electrons can tunnel upon suitable gate and source-drain voltage application [5]. A schematic circuit representation of an SET can be seen in Figure 2.1.

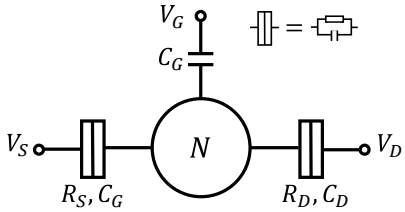

Figure 2.1: Schematic circuit diagram of an SET. The island is represented by the circle in the centre, with N denoting the number of electrons on the island. The source, drain, and gate potentials are defined as V_S, V_D, and V_G respectively, each node with its respective mutual capacitance C_i to the island. Source and drain leads also have respective tunnel resistances R_i to the island. The total SET capacitance is defined as $C_\Sigma = C_G + C_D + C_S$.

When sufficiently high tunnel barriers are present, the wavefunctions of electrons on the dot do not extend far beyond the tunnel barriers, causing the number of electrons N on the island at a given time to be a well-defined integer [6]. Current flow in an SET hence occurs sequentially, where for a small enough source-drain bias, the number of electrons on the island fluctuates between N and $N+1$, as electrons tunnel from source to island to drain. Since the system always tends towards minimum energy, current flow only occurs when it is energetically equivalent for the system to have either N or $N+1$ electrons [5]. These degeneracy points can be seen in Figure 2.2 (A). For gate voltages that do not result in degeneracy points, the Coulomb repulsion between electrons results in too high of an energy requirement to add an electron to the island [6]. This is referred to as Coulomb Blockade [6].

Note that an SET must be operated at low temperatures (near 0K) to be used for precise charge sensing. If the thermal energy of an electron is larger than the charging energy, which is the electrostatic energy needed to add or remove an electron from the island ($kT > E_c$, where k is the Boltzmann constant and T is the temperature), electrons on the island become less localized [5]. Thus, electrons are able to travel through the SET due to thermal excitation, making it no longer viable for precise charge sensing.

2.1.1 The Constant Interaction Model

The Constant-Interaction (CI) model, which is a simple model used to describe the electronic states of quantum dots, assumes that the Coulomb interactions between electrons on the dot are independent of N [6]. It posits that the ground-state (GS) energy $U(N)$ of a single quantum dot with one gate is given by [6]:

$$U(N) = \frac{[e(N - N_0) - C_G V_G]^2}{2C_\Sigma} + \sum_i^N E_i(B). \tag{2.1}$$

Here, C_Σ is the sum of all mutual capacitances to the island. It is important to note that the CI model assumes a constant C_Σ which is relevant to all Coulomb interactions between electrons on the dot and all other electrons in the system, both within and beyond the island [6]. In this context, we define $Q_0 = eN_0$ as the offset charge on the island; $N_0 = N|_{V_G=0}$. The second term in equation (2.1) denotes the energies of the quantum states occupied by the electrons on the island, as a function of the magnetic field B [6]. These energies are addressed in more detail in Section 2.1.2. Figure 2.2 (A) shows $U(N)$ plotted against V_G for various values of N.

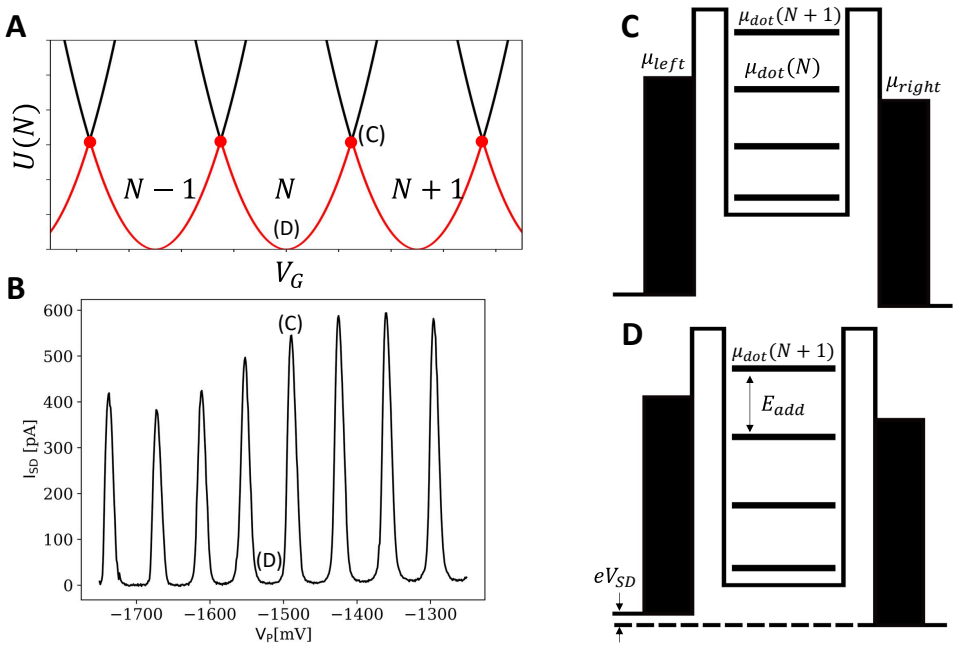

Figure 2.2: Summary of current flow mechanism in an SET. (A) Ground-state energy of an SET plotted against gate voltage. Current flow occurs at the marked degeneracy points, where two adjascent parabolas intersect. The system tends towards the number of electrons on the island which would minimize its energy, thus remaining on the lines marked red. **(B)** Coulomb peaks of an SET operated near 0 K. These peaks correspond to the degeneracy points in (A) and are interspersed by regions of Coulomb blockade, which is visualized in (D). **(C)** Diagram of a potential landscape at which current can flow, where μ_{dot} lies between the source and drain potentials. **(D)** Potential landscape for Coulomb blockade, where there is no number of electrons for which μ_{dot} resides between the two electrode potentials. This case corresponds to a higher V_G compared to (C). E_{add} is shown here as the difference between two successive μ_{dot} values.

The SET electrochemical potential can be defined as $\mu_{\text{dot}}(N) \equiv U(N) - U(N-1)$ [6]. Defining $eV_{SD} = \mu_{\text{left}} - \mu_{\text{right}}$, where μ_{left} and μ_{right} denote the electrochemical potentials at the source and drain respectively, current is allowed to flow in the SET when $\mu_{\text{left}} > \mu_{\text{dot}} > \mu_{\text{right}}$ [6]. Let's suppose a certain V_G value satisfies this condition, resulting in the potential configuration shown

in Figure 2.2 (C). This would correspond to the degeneracy point marked (C) in Figure 2.2 (A). If we increase the value of V_G, while maintaining V_{SD}, the ladder of μ_{dot} values is shifted downwards. At a certain gate voltage, we end up with the configuration shown in Figure 2.2 (D), which is equivalent to Coulomb blockade. Here, it is more energetically favorable for the SET to have a fixed number of electrons. As the gate voltage is further increased, a new degeneracy point is encountered, where there is a window of gate voltages at which μ_{dot} is between the two gate potentials. These periodic windows of V_G which facilitate current flow can be seen as spikes in the current, with regions of almost zero conductance (corresponding to Coulomb blockade) between them [5] [6], as shown in Figure 2.2 (B).

Separation between two peaks in conductance is proportional to the addition energy E_{add} [6]:

$$E_{\text{add}} = \mu_{\text{dot}}(N+1) - \mu_{\text{dot}}(N) = E_C + \Delta E. \tag{2.2}$$

This follows from Figure 2.2 (C), where the periodic nature of Coulomb peaks is observed; adding (a multiple of) E_{add} to μ_{dot} results in current flow. Here the charging energy is defined as:

$$E_C = \frac{e^2}{C_\Sigma}, \tag{2.3}$$

which is the electrostatic energy required to add or remove an electron from the island [7]. Moreover, ΔE is the difference in quantum energy levels between two successive quantum states [6]; $E_N = \sum_N E_i - \sum_{N-1} E_i$ and $\Delta E = E_{N+1} - E_N$.

It is useful to know the spacing between Coulomb peaks as a function of the varied gate voltage. Consider a gate voltage V_G at which a peak is observed. This corresponds to a certain μ_{dot} value, and a number of electrons N. For the consecutive peak, at which the gate voltage is $V_G + \Delta V_G$, the number of electrons is $N+1$. Since we assume a small bias, the μ_{dot} value corresponding to both peaks should be equal, such that current flow (and hence a peak) is observed. We can thus derive ΔV_G as follows [7]:

$$\begin{aligned} \mu_{\text{dot}}(N) \equiv U(N) - U(N-1) &= \frac{e^2(N - N_0 - \frac{1}{2})}{C_\Sigma} - |e|\frac{C_G}{C_\Sigma}V_G + E_N, \\ \mu_{\text{dot}}(N, V_G) &= \mu_{\text{dot}}(N+1, V_G + \Delta V_G) \\ \therefore \Delta V_G = \frac{1}{|e|}\frac{C_\Sigma}{C_G}E_{\text{add}} &\overset{\Delta E \to 0}{=} \frac{|e|}{C_G}. \end{aligned} \tag{2.4}$$

This can also be generalized to show the change in island potential due to an arbitrary change in a gate potential [4]:

$$\Delta\mu_{\text{dot}}(N) = -|e|\frac{C_G}{C_\Sigma}\Delta V_G = -|e|\alpha_G \Delta V_G. \tag{2.5}$$

Here, E_{add} is replaced by $\Delta\mu_{\text{dot}}(N)$ since we're interested in an arbitrary change in potential, not specifically the difference between two consecutive levels. We define α_G as the gate lever arm for a single dot, which is a measure of how strongly a gate is coupled to the island.

2.1.2 Quantum Energy Levels

The quantum energy levels of electrons on the island, as seen in (2.1), can be obtained by solving the Schrödinger equation for the confinement potential. For a circular quantum dot, for example, this can be approximated as a two-dimensional harmonic oscillator, the solutions of which are known as Fock-Darwin states [6]. We can also approximate the island as a 2D box of size L, as done by [7], which results in

$$\Delta E = \frac{\hbar^2\pi^2}{\pi m L^2}, \tag{2.6}$$

as an approximation for ΔE, where m is the mass of an electron on the island [7]. This can be used alongside equation (2.4) to find the capacitance of a gate to the SET island.

In addition to each energy state of such dots being two-fold spin degenerate, there are a number of degeneracies which can occur for different combinations of the associated quantum numbers.

This is what results in the electron energies having an atom-like shell structure [6]. Analogous to atoms, Hund's rule results in corrections to classical energies if a quantum dot. This causes values of N with the maximum number of electrons with the same spin to be more stable than others in the same shell [5]. Thus, there is an associated reduction in the quantum dot's ground-state energy for certain values of N, as a result of the exchange interaction between electrons with parallel spins, which is unaccounted for by the CI model [6].

2.2 The Maxwell Capacitance Matrix

The Maxwell capacitance matrix is an essential tool for the analysis of systems with a large number of conductors. It provides a means of relating the voltages and charges of all conductors in the system [8]. If we index the conductors from 1 to n, we can define (2.7) [8],

$$\mathbf{Q} = \mathcal{C}\mathbf{V},$$
$$\mathbf{Q} = \begin{pmatrix} q_1 \\ q_2 \\ \vdots \\ q_n \end{pmatrix} \quad \mathbf{V} = \begin{pmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{pmatrix} \quad \mathcal{C} = \begin{pmatrix} \sum_{i=1}^{n} c_{1,i} & -c_{1,2} & \cdots & -c_{1,n} \\ -c_{2,1} & \sum_{i=1}^{n} c_{2,i} & \cdots & -c_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ -c_{n,1} & -c_{n,2} & \cdots & \sum_{i=1}^{n} c_{n,i} \end{pmatrix}, \tag{2.7}$$

where $\mathbf{Q}, \mathbf{V} \in \mathbb{R}^n$ are the charge and voltage vectors respectively, and $\mathcal{C} \in \mathbb{R}^{n \times n}$ is the Maxwell capacitance matrix. Here, q_i and v_i denote the charge and potential on the i^{th} conductor respectively, $c_{i,i}$ the self-capacitance of the i^{th} conductor, *i.e.* its capacitance to infinity [8], and $c_{i,j} = c_{j,i}$ the mutual capacitance between the i^{th} and j^{th} conductors.

It is possible to transform the Maxwell capacitance matrix into the mutual capacitance matrix, where the (i, j) element of the matrix is simply $c_{i,j}$. While both forms effectively contain the same information, in this thesis, we opt for extracting the Maxwell capacitance matrix from COMSOL due to its convenience in the context of SETs. For example, if the SET island is defined as terminal 1, then the total SET capacitance C_Σ would simply be given by the (1,1) element of the Maxwell capacitance matrix, whereas it would be the sum of all elements in the first row or column of the mutual capacitance matrix.

2.3 Thermal Strain & Unintentional Quantum Dots

Unintended effects can arise when quantum dot devices are cooled to cryogenic temperatures due to strain which results from mismatch of the coefficients of thermal expansion (CTE) of the materials in the device. Examples of these effects include changes in electron mobility in silicon, and alteration of band structure [9]. The crystal band structure can experience tensile stress (positive strain) or compressive stress (negative strain), which results in changes in the energy levels of the conduction band (CB) [10]. For example, a metal-semiconductor interface can result in compressive strain on the semiconductor and tensile elastic strain on the metal, as metals usually have greater CTEs than semiconductors, meaning they contract more upon cooling [9].

Given the strain in the three Cartesian spatial directions, the change in minimum CB energy of silicon E_{CB} can be determined using:

$$\Delta E_{CB} = \Xi_u \epsilon_z + \Xi_d(\epsilon_x + \epsilon_y + \epsilon_z), \tag{2.8}$$

where Ξ_u and Ξ_d are the uniaxial and dilation deformation potentials respectively [9] [10]. For silicon, the CB energy is found to change by around 1 meV for each 0.01% strain in ϵ_z [9]. When the changes in energy are large enough to create tunnel barriers, unintentional quantum dots are formed, due to the confinement which occurs as a result of the potential changes. The exact energy change required to induce a quantum dot depends on the temperature and size of the interface which creates a local minimum in potential, though a typical order is 10 meV [9]. This indicates that changes in strain in the order of 0.1% in silicon could result in strain-induced quantum dots.

Chapter 3
Device Architecture and Analysis

This chapter provides an overview of the device modelled in this thesis and its operating principles. We first present the device architecture, followed by the charge sensing mechanism of the SET in the device. We then conduct a brief analysis of the device's electrostatics building on theory addressed in chapter 2.

3.1 Device Architecture

A schematic representation of the device architecture is shown in Figure 3.1. In the top-view (see Figure 3.1 (A)) the eight gates of the device are labelled; lead gate, plunger (P), two barrier gates (B1 and B2), and four donor gates (D1 through D4). Bismuth atoms are implanted using ion implantation in a 200 nm × 200 nm window, marked by the square in the vicinity of the four donor gates.

The device is fabricated on a silicon wafer of thickness 500 µm, with an intermediate insulating layer of SiO_2 between the Si and the metallic gates. All gates are fabricated in the same layer, except the lead gate which goes on top of the barrier gates. Each gate consists of a thin layer of titanium followed by a thick layer of palladium. Furthermore, insulating Al_2O_3 is deposited over the first layer of gates to separate it from the lead gate, as well as over the lead gate to act as protective coat. Figure 3.1 (B) shows a cross-section of the device at the blue line marked in (A), depicting the relevant layers and their respective thicknesses.

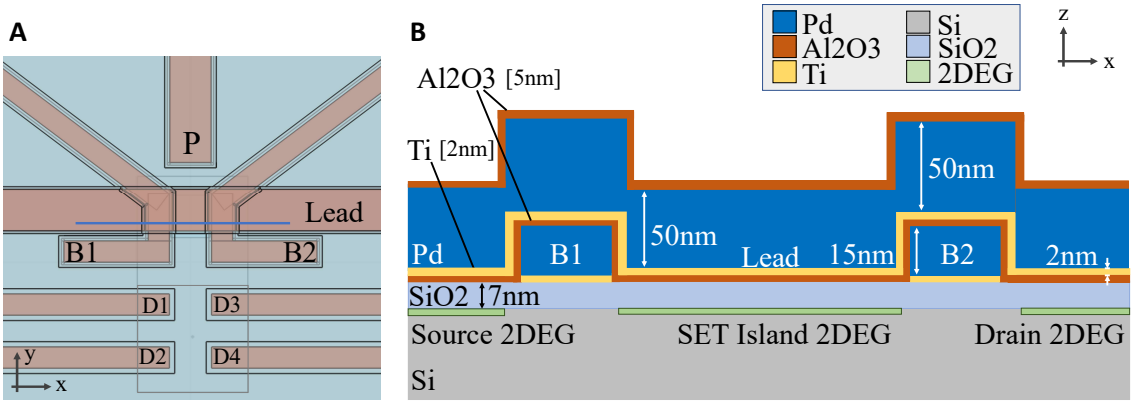

Figure 3.1: Device Architecture. (A) Top-view of the simulated device with labelled gates. The square at the donor gates represents the implantation region. **(B)** Schematic cross-section of the device at the indicated blue line in (A), showing the materials constituting each layer.

The function of the plunger, lead, and barrier gates is to form an electrostatically defined SET in the silicon layer. Applying a positive potential to the lead gate attracts electrons in the Si layer to the Si/SiO_2 interface. This forms a two-dimensional electron gas (2DEG) underneath the lead gate, which is a region in which electrons are free to move along the x-y plane, but are restricted in the z-direction [11]. A more negative voltage can then be applied to the two barrier gates to repel electrons from directly underneath them, separating the previously formed 2DEG into three regions. The central region can thus act as the SET island (quantum dot), which is separated

from the two other regions, namely the source and drain leads, by the finite barrier potentials, through which electrons can tunnel [4]. The plunger gate is used to control the electrochemical potential of the island and to tune its shape; a more negative plunger voltage restricts the extent of the island along the y-direction. This is discussed further in Section 5.2. The size of the region in which the SET 2DEG can form between the barriers and under the lead gate is 80 nm × 80 nm.

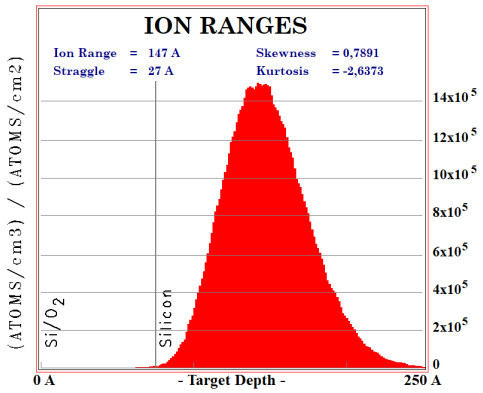

Figure 3.2: Concentration of implanted donor atoms against depth within the device.

Donor atoms are doped within the implantation region, with a varying concentration as seen in Figure 3.2, peaking around 7 nm below the Si/SiO_2 interface. The four donor gates are used to control the electrochemical potentials of donors within this region, thereby allowing for tuning and control of the eventual qubits. Furthermore, because different donor atoms will have different capacitive coupling to the donor and SET gates depending on the donor position, these capacitances can be used to triangulate specific donors.

3.2 SETs for Charge Sensing

When the charge state of a nearby donor atom changes, this affects the electrochemical potential of the SET island due to the capacitive coupling between the donor and the SET. This can result in a change in the the source-drain current I_{SD} of the SET, thereby allowing detection of changes in the state of donor atoms [4]. This change is best observed in charge stability diagrams, an example of which is depicted in Figure 3.3.

When varying a certain gate voltage, we expect to observe Coulomb peaks, as discussed in section 2.1.1. Varying two gate voltages at once and observing the current results in charge stability diagrams, where Coulomb peaks shift diagonally and represent equipotential lines for the quantum dot. This is because a certain current value is associated with a specific island electrochemical potential, assuming a fixed source-drain bias. If this island potential is to remain constant while varying two gate potentials, the change in island potential incurred by one gate must be mitigated by the change caused by the other gate [4]. These diagonal lines are clearly observed in Figure 3.3 (A). Furthermore, since the spacing between Coulomb peaks as a function of one gate potential is dependent on its lever arm, it follows that the slope of these lines is given by the ratio of each gate's lever arm to the island [4].

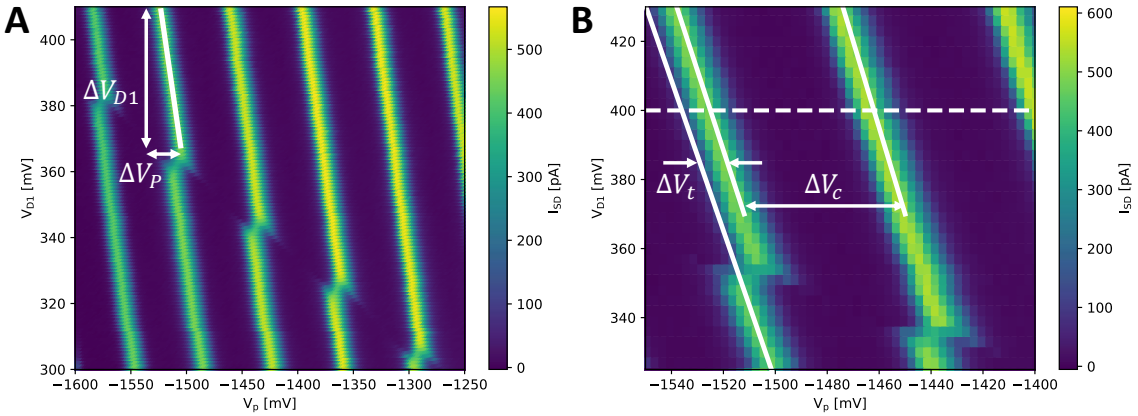

Figure 3.3: Charge stability diagrams. (A) Donor gate 1 (D1) and plunger (P) voltages varied simultaneously, resulting in diagonal equipotential lines. The slope of these lines ($\Delta V_{D1}/\Delta V_P$) is given by the ratio of gate lever arms to the island. The transition observed results from a change in the electrostatic environment of the SET, such as a change in donor charge state. **(B)** Zoomed in plot of a different charge stability diagram. The ratio of ΔV_t to ΔV_c depends on how strongly the donor/charge trap is coupled to the SET.

The slopes of the equipotential lines, which we will here-on refer to as "SET slopes," can be derived from equation (2.5). We impose a net zero change in island potential as a function of two gates, resulting in:

$$\begin{aligned} \Delta\mu_{\text{dot}}(N) &= -|e|(\alpha_{D1}\Delta V_{D1} + \alpha_P \Delta V_P) = 0 \\ \therefore \frac{\Delta V_{D1}}{\Delta V_P} &= -\frac{\alpha_P}{\alpha_{D1}} = -\frac{C_P}{C_{D1}}, \end{aligned} \tag{3.1}$$

where $C_{P(D1)}$ represents the mutual capacitance between the island and the plunger (first donor gate). See figure 3.3 (A) for an example of ΔV_{D1} and ΔV_P for one of the Coulomb peaks.

In Figure 3.3, we can also clearly observe a discontinuity in all the equipotential lines. This transition results from a change in the offset charge Q_0 on the island (introduced in Section 2.1.1). A change in offset charge occurs when the electrostatic environment of the island changes, such as when a donor changes from an ionized to a neutral state, or an electron tunnels onto a charge trap, for example [4]. Assuming that the observed transition indeed results from a donor atom, we can model the donor atom as a second quantum dot which is capacitively coupled to the SET island. The slope of the transition line can be derived to be the ratio of lever arms of each gate to the donor atom, with a similar line of reasoning as used to derive equation (3.1). Note that a more horizontal transition line would indicate stronger coupling to the donor gate, and hence closer proximity of a donor to D1 than to the plunger.

Additionally, the strength of the transition Δq, quantified by the ratio $\Delta V_t/\Delta V_c$ in Figure 3.3 (B), is a function of how strongly the island is capacitively coupled to the donor [4]. It is given by

$$\Delta q = \frac{\Delta V_t}{\Delta V_c} = \frac{C_m}{C_d}, \tag{3.2}$$

where C_m is the mutual capacitance between the donor and SET island, and C_d is the total donor capacitance, analogous to C_Σ for the SET island [4]. By detecting these charge transitions, it is thus possible to determine if a donor atom changes its state using the SET. Furthermore, the various slopes and capacitance ratios can be used in conjunction with simulations in order to triangulate the location of a donor atom within the implantation window.

3.3 Electrostatic Model

Here we present an electrostatic model of the device, in which the SET island and donor are modelled as a double quantum dot. The model is shown in Figure 3.4, with the relevant gate voltages and mutual capacitances depicted. Since only the four donor gates and the plunger are varied experimentally, only they are relevant to model. This is because we can only extract capacitances which couple the donor/SET to the potentials we vary, and not the ones kept constant.

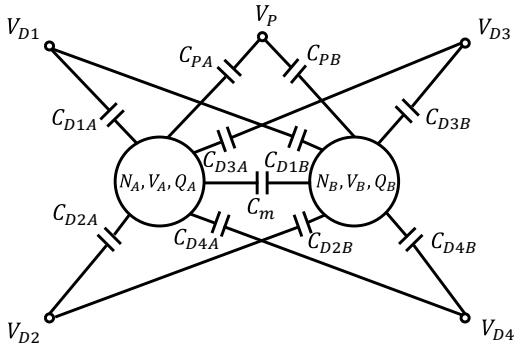

Figure 3.4: Electrostatic model of the SET and donor as a double-dot system. Here we only consider the four donor gates and the plunger, as those are the only potentials that are varied experimentally. We use labels A and B for the two dots to simplify notation.

The goal of this analysis is to derive the ratio of lever arms of certain gates to the SET/donor for the device we study, assuming C_m is non-negligible. These ratios can be extracted from SET slopes and transition slopes in measured charge stability diagrams, as discussed in the previous section. Based on equation (2.5), we can generalize the lever arm definition to:

$$\alpha_{k,\mathrm{dot(donor)}} = -\frac{1}{|e|}\frac{\partial \mu_{\mathrm{dot(donor)}}(N)}{\partial V_k}. \tag{3.3}$$

To derive the lever arms, we need expressions for the electrochemical potentials of the dot and donor respectively. Following the analysis of a double-dot by [12], we express the total charge on each island and rewrite it in matrix form:

$$\begin{gathered} Q_{A(B)} = \sum_{i=1}^{4} C_{DiA(B)}(V_{A(B)} - V_{Di}) + C_{PA(B)}(V_{A(B)} - V_P) + C_m(V_{A(B)} - V_{B(A)}), \\ \begin{pmatrix} Q_A + C_{PA}V_P + \sum_{i=1}^{4} C_{DiA}V_{Di} \\ Q_B + C_{PB}V_P + \sum_{i=1}^{4} C_{DiB}V_{Di} \end{pmatrix} = \begin{pmatrix} C_{\Sigma A} & -C_m \\ -C_m & C_{\Sigma B} \end{pmatrix} \begin{pmatrix} V_A \\ V_B \end{pmatrix} \equiv \mathcal{C}_{cc}\mathbf{V_c}. \end{gathered} \tag{3.4}$$

Note that $Q_{A(B)} = Q_{0,A(B)} - |e|N_{A(B)}$, and $C_{\Sigma A/B}$ is defined as in chapter 2. Rewriting for $\mathbf{V_c}$, we can find the electrostatic energy of the system $U(N_A, N_B)$ using [12]:

$$U(N_A, N_B) = \frac{1}{2}\mathbf{V_c} \cdot \mathcal{C}_{cc}\mathbf{V_c}. \tag{3.5}$$

The electrochemical potential of each island as a function of N_A and N_B can then be calculated as $\mu_A = U(N_A, N_B) - U(N_A - 1, N_B)$, and similarly $\mu_B = U(N_A, N_B) - U(N_A, N_B - 1)$. Finally, we calculate the relevant lever arms using equation (3.3). The ratio of lever arms of any two gates to one island can thus be determined. For example, for gates $D1$ and P to island A, we have

$$\frac{\alpha_{D1,A}}{\alpha_{P,A}} = \frac{C_{\Sigma B}C_{D1A} + C_m C_{D1B}}{C_{\Sigma B}C_{PA} + C_m C_{PB}} \overset{C_m \to 0}{=} \frac{C_{D1A}}{C_{PA}}. \tag{3.6}$$

Ratios of other lever arms follow the same form as equation (3.6). This indicates that if C_m is small enough, we can ignore the effect of coupling between the two dots, and use equation (3.1), assuming a single dot. For large C_m, we expect the slopes in charge stability diagrams to deviate from equation (3.1), especially if there are more than two coupled dots in the system.

Chapter 4
Simulations and Methodology

In this chapter, we present the simulation methodology we follow throughout the thesis. We also provide an overview of the simulation setup and details, as well as the reasoning behind some modelling choices. Finally, we briefly address the methods we use for processing of both experimental and simulated data.

4.1 General Methodology

We begin the simulation process by first constructing the geometry based on ideal dimensions and layers, as listed in section 3.1. We then conduct electrostatic simulations where the gate voltages used in the experimental setup are applied in the simulations. This allows us to extract plots of the potential landscape at the Si/SiO_2 interface, where we expect the SET 2DEG to form. This provides and indication of the size and shape of the SET island. The potential landscape is also observed as a function of the plunger voltage, to identify relevant changes to the island's geometry as this voltage is varied.

Based on the estimate of the SET island geometry from potential landscape simulations, we add the 2DEGs representing the SET island and leads to the model. Electrostatics simulations are thus expanded such that we can extract mutual capacitances between all conductors in the system. Relevant capacitances include C_p and C_{Di} (plunger and donor gate capacitances to the SET), as these can be estimated from the spacing in experimental Coulomb peak data. Moreover, C_{Di}/C_P ratios are extracted and compared to SET slopes from charge stability diagrams. In addition to the SET island shape, we study the effect of other model parameters on extracted capacitances. This includes the thickness of the Si layer, the position of the SET island, and the extent of the device modelled along the x-direction. We then follow an iterative process of adjusting model parameters, extracting capacitances, and comparing to experimental results, until the geometry is tuned to sufficiently represent experimental results, taking into account the inherent limitations and approximations of this modelling method.

Subsequently, triangulation can take place. First, we model a single donor atom in the simulation. We then vary the position of the modelled donor atom within the implantation region and plot the capacitance ratios $C_{P-\text{donor}}/C_{Di-\text{donor}}$ and C_m/C_d as a function of donor position. These ratios are matched to experimentally extracted transition slopes and Δq values, respectively, from charge stability diagrams. Intersections of corresponding locations from multiple plots are taken to estimate the position of the donor.

We also vary the position of the donor atom beyond the implantation region as a means of predicting capacitive coupling to potential unintentional dots/charge traps. Following the same procedure, simulated ratios are compared to charge stability diagrams to acquire an indication of the location of these unintentional dots. It is assumed that the model used for the donor atom suffices to roughly estimate the locations of these defects, because minor variations in the size and geometry of the modelled donor does not significantly affect extracted capacitances [13].

Lastly, we conduct strain simulations, where the primary output of concern is the strain profile along certain lines within the geometry. By plotting strain in x, y, and z directions along a given line, we can estimate the CB energy change using equation (2.8), allowing us to predict the formation of potential strain-induced dots. We especially address regions close to the SET where we predict unintentional dots from the experimental data and electrostatic simulations, as a means of testing if such dots could be strain-induced.

4.2 Geometry Construction

The device geometry is first constructed in COMSOL Multiphysics starting with the base silicon layer and building upwards. All thicknesses and dimensions are implemented, as described in Figure 3.1. Global parameters are used such that the geometry is as modular as possible and can be adjusted if needed. We construct most of the structure using cuboids, where unions between adjascent elements of the same material were taken to minimize interior boundaries.

The "extrude" feature is used to implement both aluminium oxide layers as well as the lead gate in the geometry. For example, after the plunger, barrier gates, and donor gates were constructed on top of the SiO_2 layer, all external faces were extruded orthogonally by 5 nm (the desired Al_2O_3 thickness). This proved to be the easiest method to construct this layer. Nevertheless, it did create issues for the model's modularity, because extruded objects depend on the indexing of the faces in the geometry. Changes to some model parameters would result in alteration in this indexing, making it necessary to rebuild the oxide layer from scratch if such parameter changes were to be implemented. A specific example of this is addressed in section 5.2.

While the gates of the fabricated device are expected to have their top edges rounded off as opposed to being perfectly rectangular (see [14] for examples of this gate rounding), this curvature is not accounted for in the model. This was decided primarily to simplify the geometry construction process, and also because the relevant fillet tool in COMSOL was not available. We acknowledge that this model simplification can affect the accuracy of simulated results, particularly for strain simulations. For electrostatics, however, we assume that ignoring this curvature should not yield significant changes, as the areas of interest are within the silicon layer, and hence relatively far from the would-be curved surfaces.

4.3 Meshing

Simulations carried out make use of the Finite Element Method (FEM), in which a mesh of the structure being modelled is created. We use a tetrahedral mesh, and assign different meshing resolutions to different regions within the model; a finer resolution results in more accurate solutions. For electrostatics simulations, a fine meshing region which contains both the implantation region and the SET is defined, as shown in Figure 4.1 (A). In this region, an "extremely fine" mesh with a minimum element size of 0.48 nm is used. This is because a high resolution in this area is required to triangulate the donor accurately, and because the vicinity of the SET is of the greatest interest in experiments. For the rest of the geometry, a "coarse" mesh is used, with a minimum element size of 67.2 nm. This significantly reduces simulation times as compared to using a finer mesh. The usage of a coarse mesh was ensured to have minimal effect on simulation results by simulating the entire device with a fine mesh and observing the changes in extracted capacitances. Most capacitance values differed by $0.3 - 3\%$, with the largest deviation being approximately 5%. This was concluded to be a disproportionately small improvement in accuracy considering the consequent increased simulation times, and thus a coarse mesh is used for the geometry outside the fine meshing region in electrostatics simulations. An example of a fine mesh used for the entire geometry is shown in Figure 4.1 (B).

Care was taken to define the fine meshing region before the coarse one within COMSOL, as this constrains the boundary meshes, ensuring that the entirety of the fine meshing region is meshed with sufficient resolution. Reversing this order results in lower resolution within the fine meshing region near its borders with the rest of the model, which is not desirable.

For strain simulations, the same fine meshing region and settings as in electrostatics were used. The only change was that the rest of the geometry was assigned a "normal" meshing size, with minimum element size of 21.6 nm, as opposed to a "coarse" mesh as used for electrostatics. This yielded smoother strain profile plots, as they were noticeably jagged for a coarse mesh.

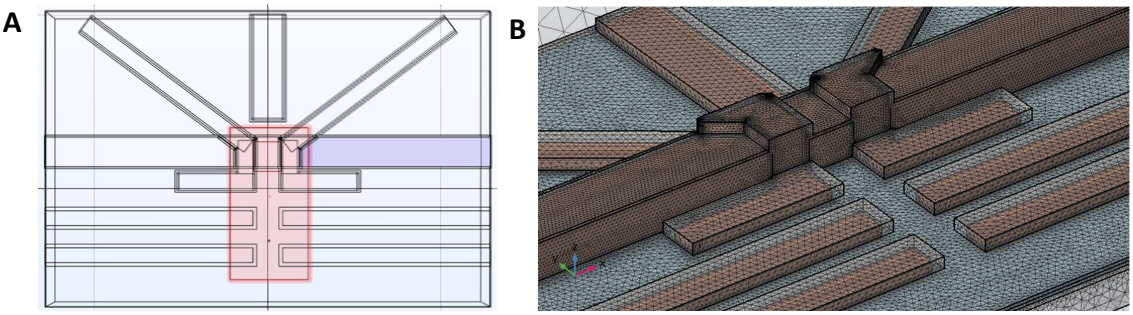

Figure 4.1: Meshing Details. (A) Wireframe rendering of the model showcasing the fine meshing region marked in red, and the shape of the drain lead 2DEG in blue. **(B)** Example of a fine tetrahedral mesh applied to the entire simulated geometry.

4.4 Simulation Details

4.4.1 Electrostatics

For electrostatics simulations, we use the AC/DC module of COMSOL. There are two main kinds of outputs we obtain from electrostatics simulations: the potential landscape of the device, and capacitance values.

To carry out potential landscape simulations, electrostatic terminals are defined for all gates in the simulation. For capacitance extraction simulations, the same set of terminals are defined, in addition to four more conductors which are added to the simulations. The additional conductors are the three SET 2DEG regions (source, drain, and island), as well as a donor atom. The three 2DEGs are modelled as grounded metallic layers at the Si/SiO_2 interface with a 1 nm thickness, as this is found to be a reasonable approximation of the behaviour of a 2DEG within a finite-element model [4]. The source and drain leads are modelled directly underneath the lead gate with the same shape as it, each extending from the edge of the simulated geometry until the closest barrier gate, as indicated in Figure 4.1 (A). The SET island is modelled between the two barrier gates, and its exact shape and size is determined based on the potential landscape as well as verification with some experimental results, as is shown in section 5.2.

The donor atom is modelled as a grounded metallic sphere with a radius of 2.5 nm. This approximately corresponds with the Bohr radius of an electron in a shallow (bismuth) donor in silicon [15]. While the exact value proposed by [15] is 2.38 nm, the minimum element size of the mesh used is around four times larger than the 0.12 nm difference, so we do not expect significant deviations from this change. Another reason the exact size of the donor model is not of great importance is that small variations in its size yield negligible changes in extracted capacitances [13].

We extract relevant mutual capacitances from the simulation by carrying out an electrostatic terminal sweep, in which the principle of superposition is used to calculate the mutual capacitance between each terminal and all other terminals, one at a time. To speed up simulations, we only sweep across the terminals corresponding to the SET island and the donor atom (terminals 5 and 12 respectively). The outputs are thus the 5^{th} and 12^{th} columns of the Maxwell capacitance matrix, from which all capacitances and ratios relevant to experiments can be extracted.

For donor triangulation, the position of the modelled donor atom is varied using a COMSOL parameter sweep for its x, y, and z coordinates. Since we only have access to experimental charge stability diagrams for P and D1, we only observe the capacitance ratios $C_{P-\text{donor}}/C_{D1-\text{donor}}$ and C_m/C_d in these plots.

4.4.2 Strain

For strain simulations, the Thermal Expansion Multiphysics node is used, which uses both the Solid Mechanics and the Heat Transfer in Solids COMSOL modules. The bottom Si layer of the geometry is fixed, and a zero force boundary condition is used for the rest of the geometry boundaries, as done by [9]. The device is simulated while cooling from annealing temperature (673 K) to operating temperature (100 mK), and also from room temperature (∼300 K) to operating temperature. Since more strain is experienced when cooling over a larger temperature range, we expect predictions of the existence of unintentional dots when cooling from room temperature to hold even if simulating the cooling from annealing temperature is more physically accurate. For this reason, results shown in section 5.4 primarily correspond to simulations with an initial temperature of 300 K. Simulating from annealing temperature is also avoided as fabrication occurs in multiple steps, some at different temperatures than others. It would therefore be an approximation in all cases to simulate the cooling of the entire device from one temperature to the operating temperature.

4.4.3 Material Parameters

Table 4.1 shows an overview of the material properties used in simulations. Permittivity values are relevant to the electrostatics simulations, whereas all other parameters are relevant to strain simulations.

While the permittivity of Al_2O_3 ranges from 7.8 to 11.1[16], a common value in literature is 9 [17]. It was found that simulated capacitances changed by a maximum of around 5% for a change of $\epsilon_r = 7.8$ to $\epsilon_r = 9$, and by a maximum of around 9% for $\epsilon_r = 9$ to $\epsilon_r = 11.1$. The commonly used value of $\epsilon_r = 9$ is chosen for simulations as it yields values in between the minimum and maximum, and there is no motivation to specifically choose a different value.

Table 4.1: Material Properties used in simulations

Material	**Relative Permittivity ϵ_r**	**Young's Modulus E (GPa) [10]**	**Poisson's Ratio (kg/m^3) [10]**	**CTE ($\times 10^6$/K) [10]**
Si	11.9 [18]	130	0.27	-
SiO_2	3.9 [18]	73	0.17	0.49
Al_2O_3	9 [17]	300	0.22	5.4
Pd	1	73	0.44	11.8
Ti	1	-	-	8.6 [19]

All CTE values in Table 4.1 were taken from [10], except that of Titanium, which was taken from [19]. Additionally, all entries in the table marked with "-" are not explicitly defined as the respective materials in COMSOL already included predefined temperature-dependent values for these parameters. Due to difficulty in implementing temperature dependent CTEs for all materials, however, material parameters for room temperature are used for the remaining materials [9]. This simplifies the simulation, and should yield an accurate approximation when simulating the thermal contraction from temperatures much higher than room temperature (where CTEs are higher) to temperatures lower than room temperature (where CTEs are also lower) [9].

Note that it suffices to use material properties as opposed to conducting atom-level simulations, as such properties are used for stress and strain simulations within the transistor modelling industry for devices of similar sizes [9].

4.4.4 Extent of the Model

An important choice for simulations is where to cut off the model *i.e.* selecting the bounds of the simulation. This was done by extending the created geometry in a given direction and observing the effect on relevant extracted capacitances, specifically those mentioned in section 4.1. This was first done in the x- and y-directions, where it was found that beyond 1.2 µm along x and 0.8 µm

along y, changes in capacitance values were negligible. For the z-direction, the only geometric entity to extrude was the base silicon layer. Thus, we examined the effect that the silicon layer thickness had on extracted capacitance values. This was found to be significant, as variation from 50 nm to 850 nm yielded a maximum change of 400%, where the capacitance between far donor gates ($D2$ and $D4$) and the SET island increased from around 0.18 aF to around 0.7 aF. This agrees with expectations as silicon has a considerably larger permittivity than air, so increasing its thickness would increase capacitance values. This effect was found to be particularly significant for the far donor gates, as most of the coupling between them and the SET island occurs through this increased silicon thickness. The capacitance of the island to the closer donor gates ($D1$ and $D3$), on the other hand, exhibited an increase of around 170% for the same change in silicon thickness. This also aligns with expectations, as the closer the gates are to the island, the more the coupling is dominated by the region in between them as opposed to regions farther in the environment. Beyond the modelled thickness of 850 nm, capacitance values appeared to converge, so it was chosen as the model limit along the z-direction.

4.5 Data Processing

Here we present an overview of how we process both experimental and simulated data to obtain our results.

Firstly, for Coulomb peak data, we use the `find_peaks` functionality of the `scipy` Python module. This allows us to identify the peaks, such that the spacing between peaks is automatically extracted. For this method, we specify a threshold along the y-axis, below which peaks are not considered, as well as a tolerance along the x-axis, within which no more than one peak can be identified. This allows tuning of the peak identification in case of significantly varying peak heights and double peaks, where two peaks are closely adjacent. A disadvantage of this method, however, is that for double peaks, one of the two adjacent peaks is arbitrarily selected, resulting in uneven peak extraction. The implications of this method are addressed in section 5.1.1.

For slope extraction from charge stability diagrams, straight lines are manually input onto the graph and adjusted until they appear to coincide accurately over the desired Coulomb peak or transition, as seen in Figure 5.2, after which their slopes are read off. Since this method is purely visual, it is subject to error, as it is difficult to discern if a line most accurately represents the slope being extracted, or if it requires minor adjustment. It is therefore also difficult to quantify the slope error. We thus take a number of parallel Coulomb peaks to calculate an average SET slope and a respective error range when possible. We also examine transitions with nearly identical slopes and similarly take the average. For determination of Δq values, we use the manually added lines over Coulomb peaks as shown in Figure 3.3 (B), and determine the points of intersection of each line with a horizontal line, such as the dashed one shown in the same figure. We can thus determine the relevant parameters to calculate Δq.

Lastly, for simulations, relevant data is exported from COMSOL into text files which are parsed using Python. Using a comma-delimited format as opposed to a column-delimited format in the COMSOL export settings results in data that is easier to parse, as scripts written for `.csv` files are easier to adapt and reuse for different exports.

Chapter 5
Results and Discussion

In this chapter we present the results acquired from both simulations and experiments. We address discrepancies in experimental and simulated capacitance values and their potential causes. Lastly, we present our conclusions with regards to triangulation, including our estimated prediction of where a donor atom and an unintentional dot might be in the fabricated device.

5.1 Experimental Results

Before addressing simulation results and findings, we present the experimental results against which we compare simulations.

5.1.1 Coulomb Peaks

We first analyse Coulomb peak data for the plunger voltage V_P and the four donor gate voltages V_{Di}. To use equation (2.4) to find the respective capacitances of each gate to the island, we first estimate ΔE using equation (2.6). Note that while the exact shape and size of the SET island is addressed in section 5.2, we can approximate it as a 2D square with side $L \approx 80\,\text{nm}$ based on the dimensions of the modelled geometry, to obtain an order of ΔE as compared to E_C. Using $C_\Sigma \approx 50\,\text{aF}$, which is in the order of simulated values, we find that $\Delta E/E_C \approx 0.015$, indicating that it is safe to assume $\Delta E \approx 0$ when extracting capacitance values from Coulomb peak data. We thus extract the following capacitances, shown in Table 5.1.

Table 5.1: Capacitance data extracted from Coulomb peaks, where capacitances are between each gate and the SET island respectively. Data corresponds to the plunger voltage swept between $-1.7\,\text{V}$ and $-1.3\,\text{V}$, and donor gates between $-1\,\text{V}$ and $0.3\,\text{V}$. For the ratios in the two last entries, only the average value is displayed. Additionally, they are only shown for $D1$ and $D2$, since $D3$ and $D4$ respectively result in nearly identical values.

C_P [aF]	C_{D1} [aF]	C_{D2} [aF]	C_{D3} [aF]	C_{D4} [aF]	C_P/C_{D1}	C_P/C_{D2}
2.55 ± 0.15	1.05 ± 0.15	0.8 ± 0.2	1.08 ± 0.2	0.82 ± 0.15	2.43	3.15

A key result from this data is the symmetry between $D1$ and $D3$, as well as between $D2$ and $D4$, which indicates that the former pair are the gates closer to the SET island (due to their larger capacitances), and the latter pair are those farther away. This was an important takeaway from analyzing this set of data, as the donor gate numbering was initially mixed up. It is also inline with expectations that the capacitance to the plunger is larger than that to the donor gates, considering proximity to the SET island.

It is worth noting the relatively large variation in peak spacing obtained, which gives a significant degree of error in capacitance values. We propose four possible causes for this. Firstly, there could be coupling of the SET island to a nearby quantum dot with non-negligible inter-dot coupling [7]. While this could be a donor atom, it could also be a nearby charge trap or strain-induced dot. Figure 5.1 (A) shows one of the experimental sets of Coulomb peaks, and Figure 5.1 (B) shows an image taken from [7], depicting Coulomb peaks for a series double-dot, where the topmost image is that of a "weakly coupled" system. Similarities can be observed between Figure 5.1 (A) and the topmost two images in (B), indicating that it might indeed be a tunnel-coupled system, where transport can occur in series between the two dots. We do not consider this explanation to be solely satisfactory, however, as the SET island is located directly between the source and drain, so a series double dot is unlikely to occur.

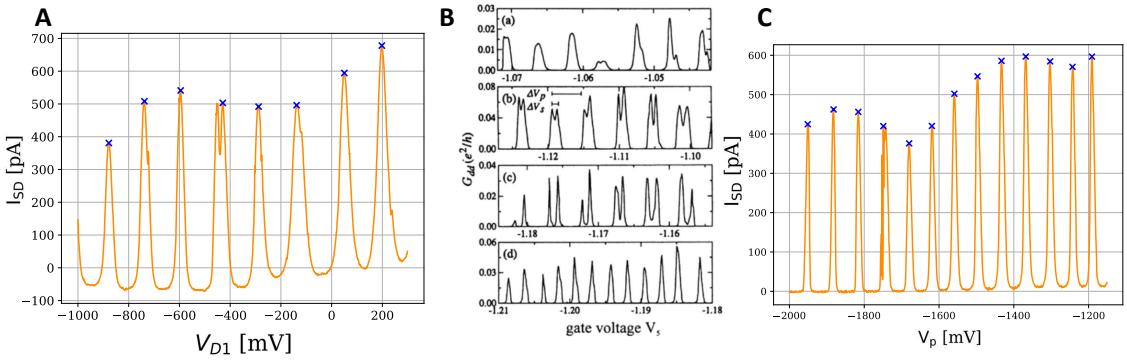

Figure 5.1: Coulomb peaks. (A) Current plotted against V_{D1} showcasing unevenness of peak spacing and some double peaks. Blue crosses mark the peaks used to estimate capacitance values. **(B)** Image taken from [7], showing Coulomb peaks for a series double dot system with increased coupling going downwards. **(C)** Current against V_P for a large voltage range. We can observe that spacing tends to decrease as voltage increases.

A second cause of the uneven spacing obtained is that while sweeping a relatively large voltage range, it is possible that we can no longer assume the CI model. This would mean that the mutual capacitances to the island are dependent on the number of electrons on the island, and would hence result in variation in peak spacing [6]. We would expect that significantly increasing a gate voltage would result in increased SET capacitance, as it would result in a larger number of electrons on the island, which is equivalent to increasing the island's effective diameter [6]. This corresponds to observing smaller peak spacing for larger voltages, which is indeed observed when varying the plunger voltage over a large range, as seen in Figure 5.1 (C). Consequently, we choose a smaller range of plunger voltages to extract C_P; we particularly observe the range between $-1.7\,\mathrm{V}$ and $-1.3\,\mathrm{V}$[1] as that is the range where most transitions in charge stability diagrams occur. It hence corresponds to the capacitance we care most about modelling, as we use simulations to triangulate the causes of transitions within this range. Note that we do not observe a significant smooth decrease in peak spacing when varying the donor gates, and so we use the full range swept for them to extract their respective capacitances, such that we have as many data points as possible. This is also inline with expectations, as the donor gates are less strongly coupled to the island. This means we observe less peaks than we do for the plunger over a given voltage range, so we need a much larger range to observe peak spacing smoothly decrease for the donor gates.

The third potential cause we propose is the existence of nearby dots/charge traps which are capacitively coupled to both the gates varied and the SET island, causing changes in the offset charge Q_0 at certain voltages. Examples of this are already observed in charge stability diagrams as transitions, such as in Figure 3.3 (A). Coulomb peak measurements are simply akin to taking a horizontal or vertical cut-line through a charge stability diagram, keeping one voltage constant. If such a line were to pass through a transition (or multiple, see Figure 5.2 (B)), we could observe both double peaks and uneven spacing. This explanation differs from the first one we proposed in that it does not require a series double-dot, but rather that the island is simply coupled to nearby dots/defects, which can alter Q_0. Since this is supported by observations of charge stability diagrams, we consider this the most likely explanation for the uneven spacing we obtain.

Lastly, an additional contributor to the uneven spacing is the means of peak extraction we use, namely the `find_peaks` functionality of `scipy`. As observed in Figure 5.1 (A), where there is a double-peak, one of the peaks is chosen while the other is neglected. This causes spacing to the peaks before and after it to differ significantly. A potential fix to this would be taking the spacing to the average voltage of such double peaks; however, this would not be possible for double peaks that are less distinct, such as the second peak in the figure. Thus, a point for future improvement is developing more rigorous means for peak extraction.

[1] The Coulomb peak data used to extract the C_P value and range in Table 5.1 is in fact that from Figure 2.2 (B).

5.1.2 Charge Stability Diagrams

Next, we analyze the slopes obtained from charge stability diagrams. We first address SET slopes in order to help in choosing model parameters, followed by transition slopes for donor triangulaton.

SET Slopes

To extract capacitance ratios from SET slopes, we use equation (3.1). Note that we do not use the more complex formulation proposed in equation (3.6), as simulated values of C_m were in the order of 0.03 aF, compared to C_d in the order of 3 aF, and C_P and C_{Di} as shown in Table 5.1. Mutual capacitance values to the donor were hence too small to consider a significant effect on the obtained slopes.

Figure 5.2 shows two charge stability diagrams from which slope data was extracted. In Figure 5.2 (A), the red line was used to extract the SET slope which corresponds to the ratio C_P/C_{D1}. This was done for a number of diagrams for various voltage ranges all within $V_{D1} \in [-0.2, 0.4]$ V, and $V_P \in [-1.7, -1.25]$ V. The resulting ratio was found to be around 2.3 ± 0.2. The extracted SET slope is found to be in reasonable agreement with the average ratio of 2.43 obtained from Coulomb peaks, as seen in Table 5.1. The reason we obtain a range of ratios is partially due to the slope determination method, which is naturally error prone as explained in section 4.5. A potential improvement to this method could be to use machine learning to identify the lines representing Coulomb peaks and to use a curve fit. This could enable access to more quantitative insights, as we could determine the coefficient of determination of the fit, for example.

Furthermore, since we determine the slopes for various peaks and average them, we observe some variation between slope values. This can be attributed to different gate voltages corresponding to different SET island tuning (size and shape), thus resulting in slightly different capacitance ratios. The range of slopes obtained could also be due to multiple coupled dots/charge traps within the SET vicinity, as this would increase the complexity of the expression needed to accurately describe the SET slopes. We conclude, however, that the effect of these factors is minor due to the relatively small range of slopes obtained.

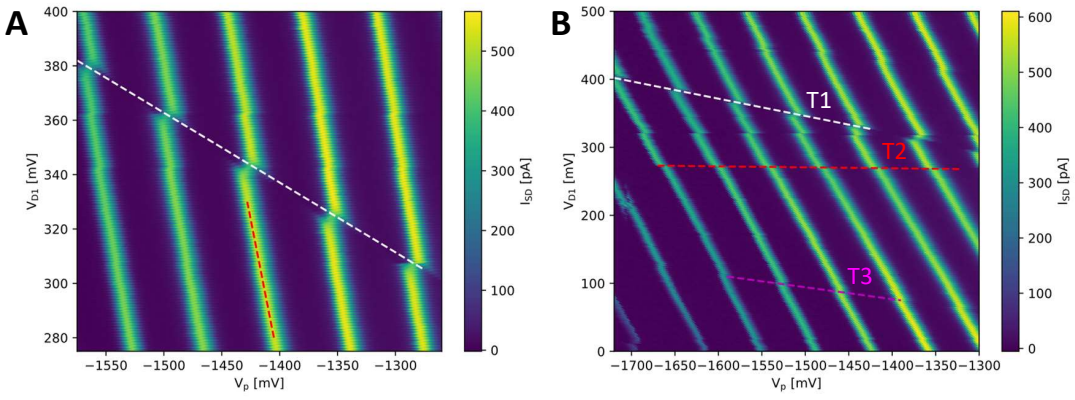

Figure 5.2: Slope extraction from charge stability diagrams of V_{D1} against V_P. **(A)** Marked in red is the line from which the SET slope is derived, whereas the white line was used to derive the transition slope. **(B)** Here, we identify three main transitions and label them T1 through T3. Each transition has its own slope and Δq, both of which can be used for triangulation of each transition's respective dot/trap.

Transition Slopes

For transition slopes, we observe three main transitions, labelled T1 through T3, shown in Figure 5.2 (B). We summarize the transition slopes and Δq values obtained for each of these trans-

itions in Table 5.2 below. Note that the transition observed in Figure 5.2 (A) corresponds to T1 from (B), as it has the same slope. In fact, transitions with the same slope as T1 were observed throughout multiple measurements in different voltage ranges. This indicates that it could be an unintentional dot being charged with a number of electrons, as opposed to just a charge trap or donor with only two possible charge states. We discuss this further in section 5.3 and 5.4.

Table 5.2: Transition slopes and Δq values of the three transitions identified in Figure 5.2 (B). In the first column, we show the theoretical ratio each quantity corresponds to between parentheses.

Transition	T1	T2	T3
Slope ($C_{\text{P-donor}}/C_{\text{D1-donor}}$)	0.25	0.014	0.175
Δq (C_m/C_d)	0.17	0.087	0.062

We can also observe a transition in Figure 5.2 (B) between T1 and T2 which is almost horizontal. These kinds of fluctuations are observed throughout the measured charge stability diagrams, and could result from charge traps or variations in material growth in the device [20]. We also posit that such switches could be attributed to measurement artifacts, and thus they are not of interest for triangulation. We do consider T2 which also has a near-zero slope, however, as a means of verifying with simulations that these kinds of transitions are unlikely to be caused by donor atoms.

5.2 SET Island

Potential Landscape

As mentioned in chapter 4, the potential landscape of the device is simulated and observed at the Si/SiO_2 interface, such that the shape and size of the SET island can be estimated. This is shown in Figure 5.3, where we can see the region of high potential (around 2 V) between the lower potential due to the barrier gates (around 1 V). While this image depicts the potential for a plunger gate voltage $V_P = -2\,\text{V}$, we also observe how the landscape varied up to $V_P = -1.25\,\text{V}$, as $[-2, -1.25]$ V is the maximum range of voltages experimentally applied whenever V_P is varied. We find no significant change in the potential landscape within this range, and thus assume that the island shape and size could be kept constant in simulations, once established.

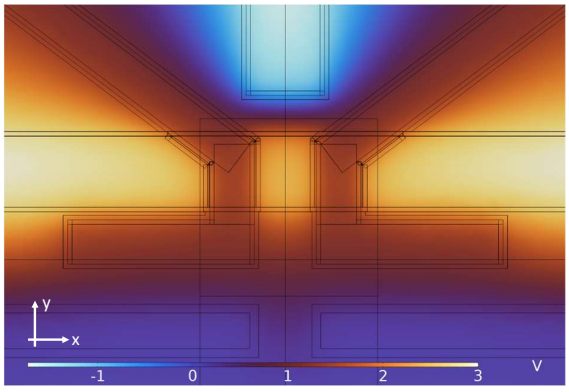

Figure 5.3: Simulated potential landscape of the SET, used to predict island shape and size.

It can be seen from Figure 5.3 that the shape of the island would be approximately square/rectangular, as expected from the geometry of the gates, as opposed to being a more rounded circular shape. We can also see, however, that the high potential region extends more in the negative y-direction due to the plunger restricting it from the positive y-direction. Based on these observations, we choose to test the variation of extracted capacitances based on the shape of the SET

island, by modelling it as one of three geometries. These are: circular, square, and rectangular, which is identical to the square shape, but 5 nm longer along the negative y-direction. The rectangular shape is used to represent the observed potential "leakage". These three geometries are shown in Figure 5.4. We also expect from the potential landscape that the island occupies the majority of the area between the barrier gates (80 nm × 80 nm), which we can verify using capacitance data.

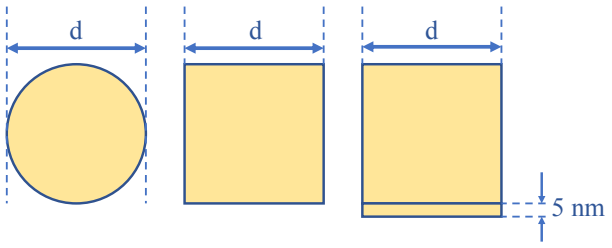

Figure 5.4: The three island geometries we test in simulations.

Square and Circular Islands

We first address the total SET capacitance C_Σ as a function of the island size for both circular and square islands, as shown in Figure 5.5. Here, we also plot an approximation typically made in literature, where the self-capacitance of an isolated ideal disc is given by $C = 4\epsilon_r\epsilon_0\pi d^2$, with ϵ_0 the permittivity in free space, and d the diameter of the disc [6]. We can see that for small island sizes, up to around 40 nm, the circular island is in reasonable agreement with the ideal disc approximation, whereas is deviates further as diameter increases. Moreover, the total capacitance of the square island is consistently larger than both the circular island and the disc approximation. A possible explanation for why the approximation deviates from the simulated island capacitance is that it does not account for surrounding gates and structures. As the island size increases, the island is essentially closer to surrounding structures (less isolated), thus increasing their contribution to the total capacitance, resulting in the observed deviation for increasing island size. Additionally, the ideal approximation is expected to be less accurate for the square island, as it assumes a circular cross-section. Since a square of side length d by definition has a larger area than a circle of diameter d, it is also in agreement with expectations for the square island to exhibit larger capacitance.

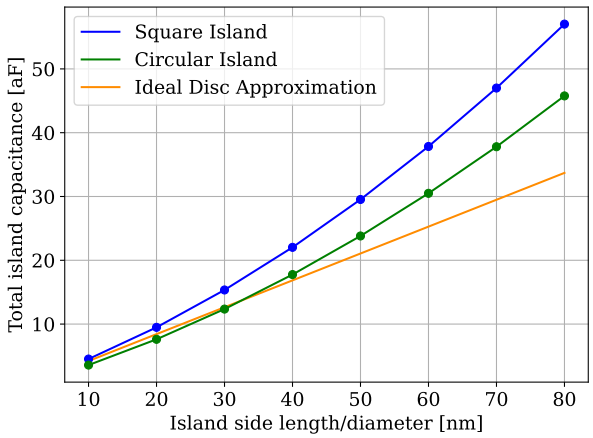

Figure 5.5: Simulated total island capacitance as a function of island shape and size. We simulate square and circular islands, and compare to the self-capacitance of an ideal disc.

We can conclude from this that the ideal disc approximation is a good means of estimating the order of magnitude of SET island capacitance, especially for small circular islands. For larger islands with nearby gates and structures, it does not suffice to provide an accurate estimation.

Following, we analyze the variation in simulated C_P/C_{Di} ratios as a function of island size and geometry. These were found to be approximately equal for both square and circular islands. Since the potential landscape also indicates a more square-shaped island, we proceed with only variations to the square island, and no longer model a circular island. Additionally, we primarily focus on the C_P/C_{D1}, as we do not have access to experimental charge stability diagrams for the three other donor gates.

Lead Gate Offset

The C_P/C_{Di} ratios were found to be approximately constant while varying island side length from 50 nm to 80 nm, exhibiting a change of only around 5%, as shown for C_P/C_{D1} in Figure 5.6 (A). This means we cannot use SET slope data from charge stability diagrams to verify the island size, since there is little variation in the simulated ratio for a significant change in size. We can see, however, that the simulated ratio of around 3.23 exceeds experimental values which are in the regime of 2.3 ± 0.2. We thus plot simulated C_P values as a function of island side length and compare simulated and experimental C_P values. This allows us to see if the simulated island size that corresponds to experimental C_P values is in agreement with the potential landscape, and thus determine if the discrepancy in the C_P/C_{D1} ratio is due to C_P or C_{D1}. This is shown in Figure 5.6 (B), where experimental C_P values from Table 5.1 are shaded in grey. The corresponding simulated island size is shaded in blue, indicating values between 64 nm and 68 nm. These values are significantly smaller than the expected size which is close to 80 nm. This leads us to suspect that there may be a fabrication error in the device, namely misalignment of the lead gate layer. If this layer were shifted in the negative y-direction, the SET island would also be shifted, making it closer to the donor gates and farther from the plunger gate. We would thus expect an increase in C_P, and a reduction in C_P/C_{D1} upon simulating this shift, thereby reducing the discrepancy with experimental results.

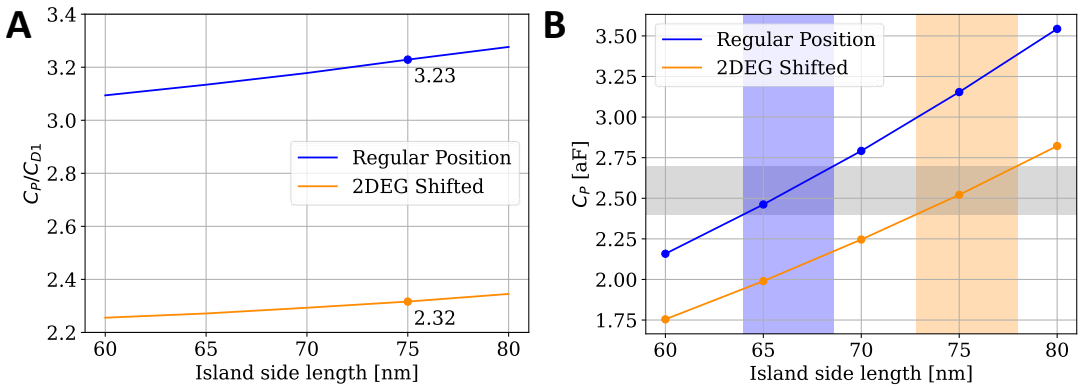

Figure 5.6: Simulations of as SET island shifted by 10 nm in the negative y-direction. **(A)** C_P/C_{D1} plotted against island size. We can see that the ratio of the shifted island matched more closely to experimental values. While there is a data point from simulations for every 5 nm change in island size, we only emphasize the points for a side length of 75 nm due to their relevance. **(B)** Simulated plunger capacitance C_P plotted against island size. The grey rectangle indicates the experimentally extracted range of C_P. Blue and orange rectangles indicate the simulated island sizes that correspond to this capacitance range in simulations, both for the regular island and the shifted one.

Shifting the entire lead gate layer in simulations proves difficult due to the geometry construction issues discussed in chapter 4. We thus shift only the SET 2DEG in the simulation as a means

of testing whether such a shift could indeed reduce the experimental discrepancy, indicating potential misalignment, and not as a means of accurately establishing the extent of said misalignment. This is because capacitance changes due to just shifting the 2DEG are not entirely accurate, but we assume it still provides a reasonable indication, especially because most of the lead gate volume is metallic, which is modelled to have a $\epsilon_r = 1$. This means that shifting the lead gate to a location previously occupied by air (which is also modelled to have $\epsilon_r = 1$) should not significantly change surrounding capacitances; only the Al_2O_3 layer over the lead gate would affect surrounding capacitances. Figure 5.6 (A) and (B) thus also shows plots for C_P/C_{D1} and C_P respectively for a 2DEG shifted by 10 nm, which is a typical order for misalignment of fabrication layers. Resulting ratio values in the range of 2.32 match experimental values more closely. Furthermore, as seen in Figure 5.6 (B), experimental C_P values correspond to a simulated island size in the range of 75 nm, which is in greater agreement with the potential landscape simulations.

We thus conclude it is likely that the lead gate layer was slightly misaligned in the negative y-direction during fabrication. The magnitude of misalignment is expected to be in the order of 10 nm, but cannot be determined with greater accuracy, as the effect of misalignment was only estimated by simulating a shifted island 2DEG and not the entire lead gate. To further verify this conclusion, shifting the lead gate in simulations can be carried out, and an atomic force microscopy (AFM) image of the fabricated device can also be taken for visual verification. The effect of this misalignment on triangulation is discussed in section 5.3.

Note that in addition to a misaligned lead gate, a number of hypotheses were tested as an attempt to explain the obtained discrepancy between simulated and experimental capacitance ratios. This includes testing different permittivity values and adjusting the extent of the simulated model, as is discussed in chapter 4. While these issues did not resolve the obtained discrepancy, they resulted in useful insights as explained in their respective sections.

Rectangular Island

We also investigate the effect of adding a 5 nm extension to the island in the negative y-direction (see Figure 5.4) as a means of more accurately representing the potential landscape. This is done after the 2DEG is shifted to account for the predicted lead gate offset. We observe a 5% reduction in the C_P/C_{D1} ratio, with a value of around 2.2 as compared to the previously obtained 2.32, for a side length of 75 nm. We also observe an increase in C_{D2} from 0.75 aF to 0.8 aF, which is closer to the average C_{D2} value from Coulomb peak data. Since all changes in relevant capacitances and ratios were found to be within predicted error margins, we can conclude that this change in geometry is relatively inconsequential. It is included in triangulation simulations in order to match the potential landscape, but has a minimal effect on final results.

5.3 Donor Triangulation

As presented in chapter 4, we perform sweeps of the donor position in simulations, and plot capacitance ratios corresponding to transition slopes ($C_{\text{P-donor}}/C_{\text{D1-donor}}$) and Δq (C_m/C_d). We first sweep position within the implantation window, labelled with "1" in Figure 5.7 (A), with the centre of this square denoting the (0,0) coordinates of the donor. Figure 5.7 (B) shows an example of the obtained capacitance plots, specifically C_m/C_d, where (x_d, y_d) are the coordinates of the donor atom. It is in agreement with expectations that the mutual capacitance of the donor would increase as it gets closer to the SET island, as is observed.

All sweeps presented are carried out for a donor atom 7 nm below the Si/SiO_2 interface. This is the depth at which donors are most likely implanted, as mentioned in section 3.1. We observe that simulated capacitance ratios exhibit negligible change when the depth of the donor is varied, with $C_{\text{P-donor}}/C_{\text{D1-donor}}$ approximately constant, and C_m/C_d increasing by a maximum of around 3% for a 6 nm increase in depth. We thus conclude that the current electrostatic simulations in conjunction with experimental data from one donor gate are not sufficient for triangulation along the z-direction. Focus is hence on triangulation within an x-y plane.

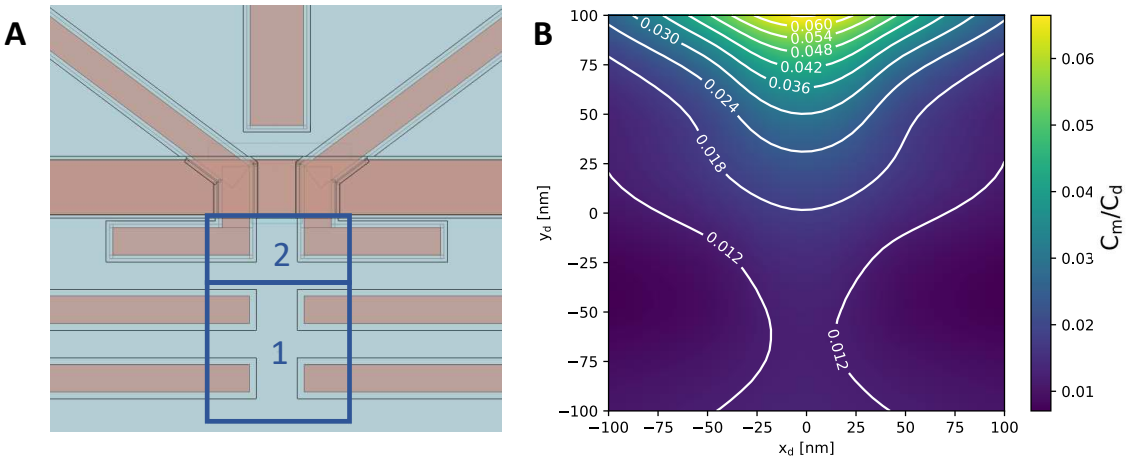

Figure 5.7: Triangulation simulation. (A) We define two "sweep regions", labelled 1 and 2 respectively, within which the position of a donor atom is swept to perform triangulation. **(B)** An example of the simulation output, showcasing the C_m/C_d ratio plotted as a function of donor position within sweep region 1.

Island Geometry Used

The final SET island parameters used for donor triangulation are a square island of side length 75 nm with a 5 nm extension in the negative y-direction. The 2DEG offset to account for potential lead gate misalignment was not implemented for the displayed triangulation plots. This is because shifting just the 2DEG might not yield accurate capacitances, as previously mentioned, and only serves as an indication of the potential fabrication error. We still investigate the effect that the 2DEG offset has on triangulation, as it also provides an indication for the potential change in estimated donor position we obtain if the lead gate offset were implemented.

It was found that minor changes in island geometry (side length changes within 10 nm, adding/removing the 5 nm extension) yielded negligible changes to C_P/C_{D1} ratios. This is expected, as this ratio is primarily dependent on the position of the plunger, D1, and the donor atom. The ratio was hence also minimally affected by implementing the 2DEG offset. We can thus use transition slopes for triangulation with confidence, as potential errors in island geometry are relatively inconsequential.

While minimal changes to island geometry were also found to negligibly affect C_m/C_d ratios,

implementing the 2DEG offset had more significant effects. The maximum C_m/C_d value within the implantation region changed by 12.1 % from around 0.066 to 0.074. This can significantly impact triangulation results, and thus we account for this error when using C_m/C_d plots.

Triangulation

See below Table 5.2 restated for convenience.

Table 5.2: Transition slopes and Δq values of the three transitions identified in Figure 5.2 (B). In the first column, we show the theoretical ratio each quantity corresponds to between parentheses.

Transition	T1	T2	T3
Slope ($C_{\text{P-donor}}/C_{\text{D1-donor}}$)	0.25	0.014	0.175
Δq (C_m/C_d)	0.17	0.087	0.062

Figure 5.8 (A) shows the simulated $C_{\text{P-donor}}/C_{\text{D1-donor}}$ ratio within the implantation region (area 1 from Figure 5.7). Combining this plot with Figure 5.7 (B), we can locate a region within the implantation window where $C_{\text{P-donor}}/C_{\text{D1-donor}}$ matches an experimental transition slope, and C_m/C_d matches the corresponding Δq of the same transition. This is shown in Figure 5.8 (B), which matches T3 from Table 5.2. We use an error margin of around 10% to account for the slope extraction method used for determining experimental transition slopes, and thus show the contour lines of 0.16 and 0.19, between which is the experimental slope of 0.175. For C_m/C_d, we use an error of around 20% to similarly account for the slope extraction method, as well as for the potential lead gate offset, which is expected to yield changes in simulated ratios in the order of 12%, as discussed in the previous section of this sub-chapter. We thus plot a contour at 0.049 as a lower bound; the upper bound of 0.062 is outside of the simulated region. Using these margins to account for relevant errors, we can estimate the donor resulting in transition T3 to be within the region marked white in Figure 5.8 (B). This is an area in the order of 10 nm × 10 nm, which is around 400 times smaller than the x-y area of the implantation region.

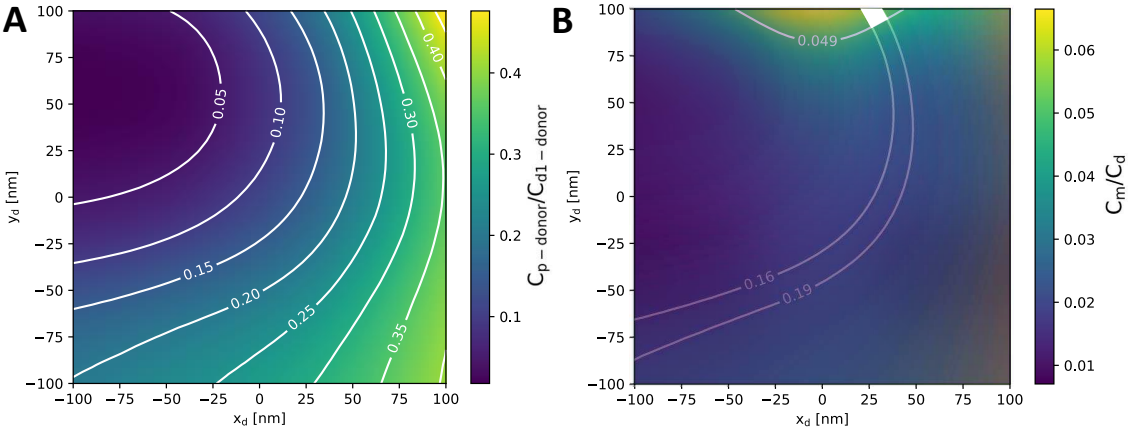

Figure 5.8: Donor Triangulation within Implantation Region (A) Simulated $C_{\text{P-donor}}/C_{\text{D1-donor}}$ ratio in implantation region. **(B)** Identified area in simulation which corresponds to experimental transition T3 shaded in white.

Note that we do not observe regions which correspond to transitions T1 and T3 within the implantation region; there is no combination of the two ratios which intersect. Moreover, all simulated C_m/C_d values are much smaller than the experimental Δq value of transition T1. This leads us to extend the range of donor positions we sweep across, as a means of potentially identifying the position of a charge trap or unintentional dot, as explained in section 4.4.1. Since T1 exhibits

both a relatively large slope and Δq, we sweep the donor position within area 2, as defined in Figure 5.7; we expect larger Δq values nearer to the SET island.

Figure 5.9 (A) and (B) shows the simulated $C_{\text{P-donor}}/C_{\text{D1-donor}}$ and C_m/C_d ratios respectively, for sweep region 2. Taking similar error margins around the experimental values as done for region 1, we obtain Figure 5.9 (C), in which we identify two areas (shaded white) which correspond with experimental values from transition T1. From this we can infer the possibility of an unintentional dot/charge trap within (one of) these areas, which results in transition T1. We predict that it is more likely to be an unintentional dot than a charge trap, due to the fact that transitions with the same slope as T1 appear multiple times throughout different voltage ranges, as discussed in section 5.1.2. We thus consider the region between the barrier gates to be of interest when performing strain simulations, so as to identify whether T1 could be a result of a strain-induced dot. This is addressed in the following section.

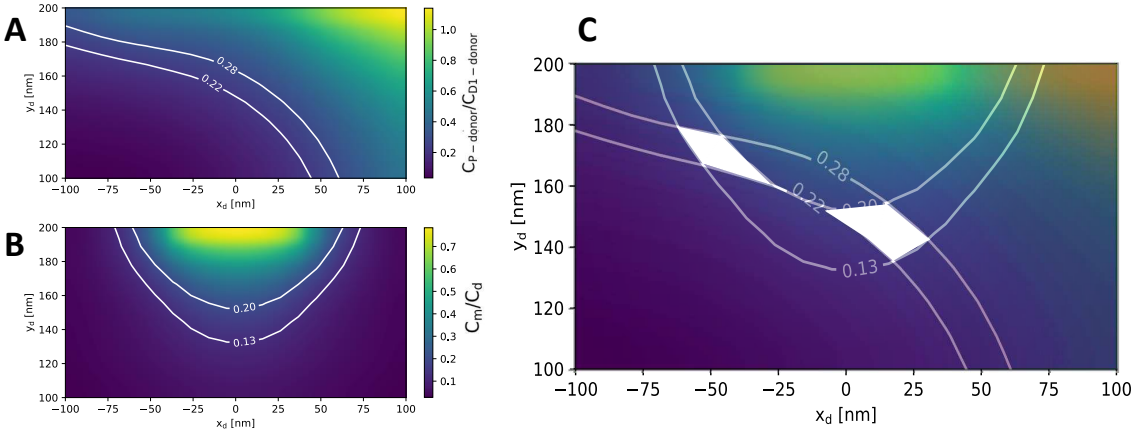

Figure 5.9: Triangulation of trap/unintentional dot beyond implantation region. **(A)** & **(B)** Simulated $C_{\text{P-donor}}/C_{\text{D1-donor}}$ and C_m/C_d ratios respectively, within sweep region 2, as defined in Figure 5.7 (A). **(C)** Identified areas in simulation which correspond to experimental transition T1.

Since no match could be made in simulations for T2 within the two simulated sweep regions, we can make one of two conclusions. Transition T2 is either caused by a charge trap somewhere outside of these regions, or it is caused by an electronic measurement artifact, as is expected to be the case for the transition between T1 and T2, for example, due to being almost perfectly horizontal. While this was not investigated further, the position of the donor atom can be varied within larger regions in the simulation as a means of verifying one of the two proposed conclusions regarding T2.

Additionally, as discussed in section 4.1, a potential improvement could be adjusting the donor atom model while sweeping its position outside of the implantation region, such that it instead better models a specific kind of charge trap. For example, a number of kinds of traps can form at the Si/SiO_2 interface, such as P_b centres and E' centres [14]. Future work can involve investigating electrostatic models specific to these defects, such that claims of identified traps/unintentional dots in simulations can be made with greater confidence.

5.4 Strain

We simulate the strain profile along the red line shown in Figure 5.10 (A) in order to evaluate the likeliness of a strain induced dot in this region. The line is defined 1 nm below the Si/SiO_2 interface as done by [10], and it was found that varying line depth by a few nm resulted in negligible changes in the strain profile. We use equation (2.8) along with $\Xi_u = 10.5$ eV and $\Xi_d = 1.1$ eV [10] to estimate the change in conduction band minimum energy, as shown in Figure 5.10 (B). As explained in chapter 2, a valley in ΔE_{CB} in the order of 10 meV can result in formation of an unintentional dot. This means that transition T1 could indeed be a result of a strain induced dot, as we see the white shaded area to the left in Figure 5.10 (B) corresponds with the expected valley in ΔE_{CB}. The right shaded area, however, does not closely correspond to the second valley. We would thus require experimental data from more donor gates to exclude this region (by obtaining less intersections which match for all experimental data), and to confirm that all data indeed matches the first strain-induced valley.

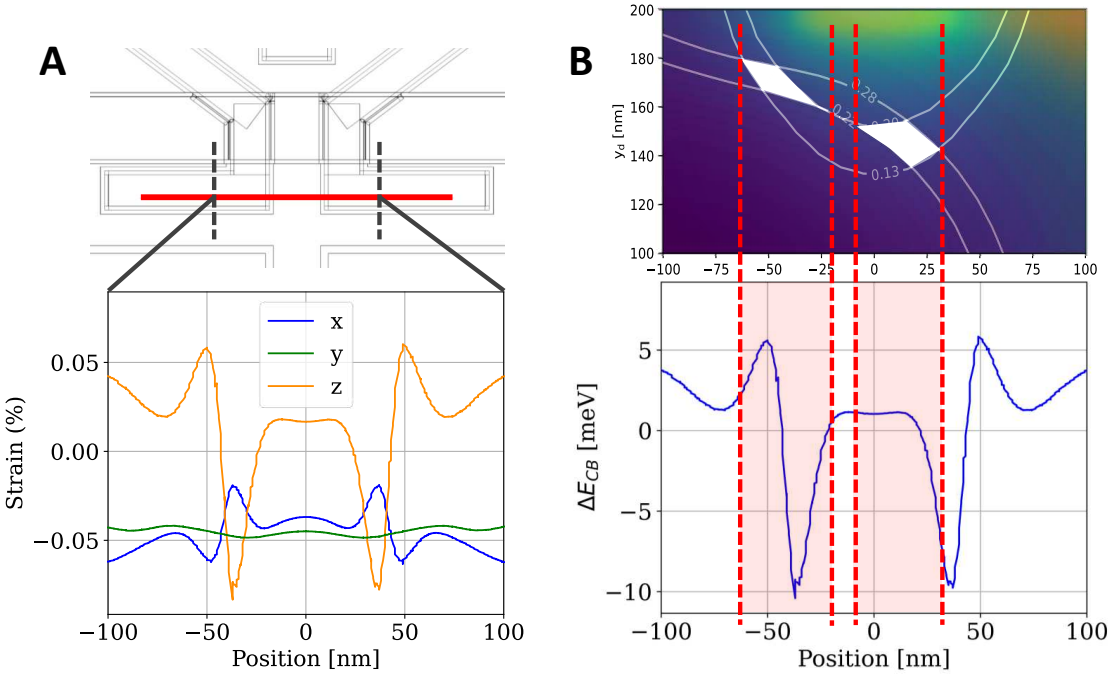

Figure 5.10: Strain simulations between the barrier gates. **(A)** Simulated strain in Cartesian directions along the red line between the two dashed lines in the geometry. Strain is simulated 1 nm below the Si/SiO_2 interface. **(B)** Estimated change in conduction band minimum energy based on simulated strain profile. Regions shaded red represent expected locations of an unintentional dot from electrostatics simulations. Both graphs here have the same x-axis.

It is also worth noting that this order of ΔE_{CB} minima is observed throughout various lines in the simulated model, specifically at the boundaries of gates with the silicon substrate. It is thus a possibility that the simulated strain profile is over-exaggerated due to the gate curvature being neglected when constructing the model geometry. While it is possible that simulating gate curvature can significantly impact obtained strain profiles, we are unable to confirm this with the currently available COMSOL functionality. A point of future improvement is therefore to reconstruct the geometry while accounting for gate curvature, such that results from strain simulations can be used confidently.

Chapter 6
Conclusions

In this research we created an electrostatic model of a fabricated bismuth-implanted single-electron transistor nanodevice, and used it to perform donor triangulation. By sweeping donor position within the implantation region in simulations, we identified the location of a donor atom within an area of 10 nm × 10 nm. This is a factor of 400 smaller than area of the donor implantation window which was used in fabrication. Electrostatics simulations were found to be insufficient in determining donor depth within the silicon, however, as simulated capacitance ratios used for triangulation show negligible variation with simulated depth.

Through triangulation simulations, we found that $C_{P-\text{donor}}/C_{D1-\text{donor}}$ ratios tend to vary between 0.01 and 0.45, whereas C_m/C_d ratios vary in the range of 0.01 and 0.07. These ratios correspond to extracted values from charge stability diagrams, namely the slope of a transition and its Δq value respectively. Therefore, obtaining experimental values within these ranges in future measurements could indicate donors within the implantation region.

We also compared simulated and experimental capacitance data to verify that the model and device match. Through this process, we discovered a probable misalignment of the lead gate in the device which would have occurred during fabrication. The predicted misalignment is in the order of 10 nm. We approximated the effect of this misalignment by shifting the SET island in simulations. This resulted in negligible change in simulated $C_{P-\text{donor}}/C_{D1-\text{donor}}$ ratios which correspond to transition slopes in measured charge stability diagrams. We thus conclude that transition slopes can be confidently used for donor triangulation, even if there is uncertainty in potential fabrication errors. Simulated C_m/C_d values were, on the other hand, sensitive to the SET island position, meaning measured Δq values are more dependent on lead gate alignment.

By sweeping donor position outside of the implantation region in simulations, we obtained $C_{P-\text{donor}}/C_{D1-\text{donor}}$ ratios in the range of 0.1 to 1.2, and C_m/C_d ratios in the range of 0.1 to 0.8. These ranges of values can thus indicate a charge trap/unintentional dot between the implantation region and SET island. Using these results, we identified the location of a potential unintentional quantum dot near the SET island. This was found to match predictions of a strain-induced dot from strain simulations in the same location. We therefore conclude that it is probable for a strain-induced dot to have formed in that location.

The model created in this project can be used for future devices, following a similar procedure as adopted in this research to perform device verification, donor triangulation, and identification of potential defects and unintentional dots. This allows for better targeting of which transitions to address and what voltage ranges to use when attempting charge-to-spin conversion. The presented simulation methodology can thus aid in expediting the process of achieving donor qubit operation.

Recommendations

For future work, we present a number of recommendations to improve the simulation process and increase confidence in results.

Firstly, constructing the model geometry using a dedicated CAD tool can make the geometry more modular, allowing for easier testing of gate and layer misalignment for example. Additionally, gate curvature can be modelled using CAD tools, which can potentially impact strain simulations. Combined with a more extensive investigation of the choice of initial temperature and simulation of cooling over multiple stages, confidence in conclusions drawn from strain simulations will increase.

For electrostatics simulations, a point of interest is how to model different kinds of charge traps/unintentional dots more accurately, as opposed to using the same donor atom model in simulations. This could grant better understanding of which transitions are caused by donors, charge traps, or strain-induced dots.

A more systematic means of experimental slope extraction could reduce error margins and thus improve triangulation accuracy. Furthermore, having access to experimental data from more donor gates could provide narrower regions of intersection, thus also increasing triangulation accuracy. More donor gate data could aid in device verification as well, as it allows for examining whether data from all donor gates support a certain hypothesis, such as layer misalignment. Such hypotheses can also be visually verified by imaging the nanodevices.

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