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## A Comprehensive Study on System Level

 Active Balancing Methods for Lithium Iron Phosphate BatteriesMaaike F. Rijkeboer

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## Preface

This master's thesis research is conducted in collaboration with LFP battery developer and producer: Super B. By addressing real world problems concerning battery management systems this field of research was of great interest for me. My fascination with batteries stems from both academic curiosity and personal experience. I have personally converted my own campervan, for which I designed and implemented my own mini-grid complete with solar panels, an inverter and of course batteries. After months of travel, relying on my batteries to sustain me through temperatures even down to $-40^{\circ} \mathrm{C}$, it made me realize the great importance of safe and reliable battery systems. This realization ignited within me the desire to contribute to the advancement of this vital technology.

I would like to express my sincere gratitude to prof. dr. ir. T. B. Soeiro, my esteemed professor, for his expertise throughout this academic pursuit. Equally deserving of acknowledgment is ir. A. K. Iyer, my daily supervisor from the university, who guided me throughout the whole process and whose support and encouragement helped me to improve my academic skills. Gratitude is also owed to ing. W. Van Wijk, my daily supervisor at Super B, from who I gained valuable knowledge from his great expertise on battery technology. Further last I would like to thank all my other colleagues at Super B who supported me and gave me a warm welcome.

As I reflect on the journey, I am filled with profound gratitude for knowledge and experience that I have acquired during this valuable period in my life. It has contributed to my growth and development both personally and professionally and I am grateful for the opportunity. At last I would sincerely like to thank my loved ones who have supported and encouraged me throughout my entire education.

## Summary

This research has been executed to present the advantages of active battery balancing. The research focuses on active balancing on system level, so in series connected battery packs ( 12 V ) rather than on cell level ( 3.6 V ). The study focusses on the balancing process of Lithium Iron Phosphate batteries which are known for their flat voltage vs state of charge curve in the $10 \%-90 \%$ SoC region.

Evaluating different active balancing methods showed that the buck-boost converter based topology gives the best result for system level balancing. Where the energy from one battery is transported through the inductor of the buck-boost converter and consecutively supplied to the other battery. The topology is chosen because it scores good on modularity, economically feasibility, its ease of integration and its capability to balance regardless of voltage levels. Active balancing in general showed system improvements in the field of gained efficiency, less heat production, decreasing of weight and faster balancing times. It also showed that balancing with this topology on system level has financial benefits over balancing on cell level and is also more efficient.

A MATLAB model and Simulink model are designed of the buck-boost converter based balancer in order to estimate efficiencies and to see what parameters influence this. It also showed the flexibility to move charge in different directions and configurations. Additional, the balancing current can be tuned by adjusting the duty cycle of the converter, gaining full control of the balancing process. The results throughout the research indicate that the efficiency lies in the range between $72 \%$ and $94 \%$. The study did not provide an exact efficiency of the balancer, additional measurements would be needed for this. The most significant loss in the system was caused by the voltage drop over the diode.

The case study shows that the balancing time can be reduced down to $75 \%$ compared to passive balancing. The total system efficiency is increased, less heat is produced during the balancing process and weight can be saved on the battery system. To implement the balancer only one additional cable for each battery is required, combined with a few additional components which can be implemented on the existing battery management system.

For future research it is advised to execute additional measurements to obtain more accurate data on the efficiency of the balancer. It is also recommended to explore the possibilities on how the efficiency can be increased. For example, a smarter switching scheme in which the losses of the diode can be remedied.

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## Acronyms

| AC | Alternating Current |
| :--- | :--- |
| ADC | Analog Digital Converter |
| BMS | Battery Management System |
| CCD | Converter Based Current Diverter |
| CtC | Cell to Cell |
| CtN | Cell to Neighbor |
| CtP | Cell to Pack |
| DC | Direct Current |
| DCM | Discontinuous Conduction Mode |
| DoD | Depth of Discharge |
| DSCCD | Double Switched Converter Based Current Diverter |
| EIS | Electrochemical Impedance Spectroscopy |
| EMC | ElectroMagnetic Compatibility |
| EV | Electric Vehicle |
| LDO | Low Drop-Out |
| LED | Light Emitting Diode |
| LFP | Lithium Iron Phosphate |
| MATLAB | MATrix LABoratory |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| MTE | Multiple Transformers Equalizer |
| MWT | Multi Winding Transformer |
| N-034 | Nomada - 034 |
| N-035 | Nomada - 035 |
| OCV | Open Circuit Voltage |
| PCB | Printed Circuit Board |
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| SCE | Switched Capacitor Equalizer |
| SIE | Switched Inductor Equalizer |
| SoC | State of Charge |
| SoH | State of Health |
| SSC | Single Switched Capacitor |
| SWD | Serial Wire Debug |
|  |  |

## Chapter 1

## Introduction

With the desire to transition towards a sustainable future, batteries have emerged as a vital component in this process, and the demand for efficient and reliable energy storage systems has never been greater. Today's batteries are used for transportation, portable electronics, renewable energy storage and in many other fields [1].

Lithium-ion batteries are especially popular amongst the rechargeable batteries. They are widely used for example in portable electronics and for electrified transportation. Compared to other batteries like lead-acid or nickel-cadmium, Lithium batteries have a significantly higher energy density. Within the Lithium-ion family there exist many different chemistry's. In this thesis the focus will be on Lithium Iron Phosphate (LFP) batteries. They have a nominal cell voltage of 3.6 V [2], and it is necessary to connect multiple cells in series to meet the higher voltage requirements of the battery pack. When even a higher voltage is required individual battery modules can also be connected in series. However, there are slight differences between State of Charge (SoC), internal resistances and open circuit voltages of each cell due to manufacturing inconsistencies. Because of these inconsistencies, imbalance arises in the series string and this will only increase as the batteries are aging. This results in degradation of the battery due to over- and undercharging and it also increases the safety risks [3].

A Battery Management System (BMS) is therefore essential to keep the cells / batteries in balance. It monitors the cells and controls its charge to prevent over- and undercharging [4]. In batteries with series-connected cells, the cells are in balance if they all have the same SoC level. When this is not the case, if for example one cell in the string has a higher SoC level, then the cells are not in balance. The process of bringing the cells back to the same SoC level is called battery balancing. Battery balancing can be applied on cell level within a battery pack (cell level balancing) as well as on system level between multiple series connected battery packs (system level balancing). A distinction can be made between the two main concepts for battery balancing, which can either be done passively or actively. With passive balancing the excess energy is dissipated in the form of heat, whereas active balancing redistributes the excess energy amongst other cells / batteries [5]. The difference between the two methods is that in passive balancing the imbalance energy is lost in the form of heat, whereas in active balancing the energy is redistributed amongst the other batteries.

There is also another critical aspect of the LFP batteries which influences the balancing capabilities. A particular characteristic is namely that the voltage versus SoC curve of an LFP battery has a nearly flat graph in the $10 \%-90 \%$ SoC region. This is different compared to most other batteries which can be seen in figure 1. Multiple aspects of the voltage versus SoC behaviour make the balancing of LFP cells more complicated:

- Due to the nearly flat region in the charge / discharge cycle of LFP cells it is hard to determine the exact SoC based on voltage levels. From figure 1 it can be seen that a few mV difference can already result in a $10 \%$ SoC difference [39].
- Since the nominal voltage varies marginally throughout the whole cycle it is hard to use voltage based balancing techniques. It is possible to use certain techniques but it requires a higher change in nominal voltage in the operation cycle in order to balance, and thus, for an LFP cell this is only possible at the end of the charge cycle, where there is a change in voltage.
- As can be seen in figure 2 there is a hysteresis loop when an LFP cell is charged / discharged. This makes it even harder to determine SoC based on the Open Circuit Voltage (OCV) of the battery [40].


Figure 1 Voltage vs SoC curve LFP cell and LiNiCoMnO2 cell [39]


Figure 2 Hysteresis loop LFP cell charging and discharging [40]

- Finally, the charging behaviour of the end user is unknown in real life applications. It is not certain if the end user always charges their battery up to $100 \% \mathrm{SoC}$, or the balancing current may not always be constant / known, especially if the battery is charged with solar energy.


### 1.1 Research objectives

This research aims to find a suitable method for actively balancing LFP batteries on system level. The research will mainly focus on whether active balancing on system level is beneficial or not and what the possible gain in efficiency and other advantages can be. This question will be answered by first researching different active balancing topologies after which the most suitable one will be chosen for applications where multiple LFP battery packs are connected in series. It will be thoroughly researched and simulations and calculations will be conducted. An additional "nice to have" is to have a prototype to perform tests on it in order to validate the theoretical research. After this, a conclusion can be drawn about the benefits and features of active balancing on system level. Considering that this thesis focuses on real-world situations and on real life products the research is conducted in collaboration with LFP battery developer and producer: Super B.

Based on the above-mentioned challenges related to active balancing in LFP cells, the research aims to answer the following questions:

- In which situations is active balancing desired and what are the advantages?
- What are the trade-offs involved in the implementation of various active balancing techniques for system level balancing and which technique is most suitable for this research?
- What are the efficiencies that can be achieved, and what are the parameters that influence the efficiency?
- Is system level balancing more beneficial than balancing on cell level for a given battery system?

The different active-balancing techniques will be evaluated based on the following criteria:

- Balancing time
- Efficiency
- Balancing capacity between $90 \%$ and $10 \%$ SoC
- Amount of components needed (strongly relates to the system costs)
- Voltage stresses on the components (strongly related to the costs and component lifetime)
- Ease of integration on system-level
- Complexity (referring towards control intensity)
- Modularity


### 1.2 The company

Information about Super B can be found in Appendix A.

### 1.3 Importance of research

Transitioning towards a sustainable future, one of the most import aspects has become to save energy. As already known, active balancing is a way to achieve this. However, most research in this field has been conducted towards active cell balancing which is known to be expensive [8]. Less research has been conducted on active balancing on system level which might be more economical beneficial and potentially even more efficient. It is important to research this because active balancing could save energy worldwide. For example, according to [9] the battery efficiency can increase by $2 \%$ with most active balancing techniques in comparison with passive balancing. Research [10] predicts that the global demand for Lithium batteries will drastically increase, reaching over 2 terawatt-hours in 2030. Saving $2 \%$ may not seem a lot, but on the global demand this will be 40 Gigawatt-hours of energy that will be saved. Research [10] also shows that Lithium-ion battery packs cost 151 USD/kWh. This means that by making the batteries $2 \%$ more efficient also 6.040.000.000 USD can be saved globally based solemnly on efficiency gain.

Another important reason to execute this research is the need for high performance battery packs for electric transportation. Besides of course electric cars, also considering electric canal boats as proposed in [11]. Both applications require high voltage battery packs consisting of multiple batteries connected in series. These long series strings need to be balanced and it might not be optimal to do this passively. Since passive balancing of these battery packs can cause excessive heat dissipation which will increase the difficulty of thermal management [12]. Not only is active balancing more efficient, it is also faster. When there is for example a difference of $5 \% \mathrm{SoC}$ between two batteries. With passive balancing the whole $5 \%$ would need to be dissipated from the battery with the highest SoC. With active balancing, only $2.5 \%$ of the high SoC battery needs to be subtracted and supplied to the low SoC battery. Fast balancing is essential in multiple cases of electric transportation. Electric Vehicles (EV) have high current charge and discharge cycles so it is important that the batteries are balanced as quickly as possible. Another example is the World's first high speed electric ferry which runs in Norway, this ferry has to be able to charge and discharge its battery pack in an extremely short time, so the balancing time is a relevant factor here [13].

Because of all these aspects it is important to thoroughly research the potential of active balancing on system level. It is desired to know what a suitable technique is to achieve this and what the possible benefits are.

### 1.4 Thesis outline

Chapter 2 presents a literature research that shortly discusses passive balancing methods and discusses in detail multiple active balancing methods. The chapter ends, concluding with a comparison based on the abovementioned metrics. In chapter 3 the chosen topology is further researched, models have been made and simulations are executed in order to gain insight into the features and efficiencies. It also provides information on what parameters influence efficiency. In chapter 4 the information obtained in chapter 3 is used to set up the system requirements for the prototype, the designs is also showed and explained here. Chapter 5 contains the results in which section 5.1 presents the results obtained from the MATLAB model, giving insight on the influence of certain parameters on the efficiency of the balancer. section 5.2 gives the results of the simulations providing information on the flexibility of the system. Results section 5.3 and 5.4 show the experimental results of the prototype and the results of a case study. In Chapter 6 the research is concluded and chapter 7 gives recommendations for future research.

## Chapter 2

## Literature research

In this literature research the first two research questions will be answered. Namely, in which situations is active balancing desired and what are the advantages? And what is the best topology for active system level balancing based on the criteria of chapter 1.1.

After researching the need for active balancing, a short description will be given of the differences and advantages / disadvantages of passive and active balancing. Then seven different types of active balancing topologies will be discussed and evaluated. In chapter 2.4 the topologies will be compared and the best one for this research will be chosen.

### 2.1 Why active balancing

In chapter 1.3 the importance of researching active balancing on system level is discussed. This chapter provides insight in the essence of active balancing in different cases. It also shows when active balancing can be an improvement over passive balancing.

### 2.2.1 Efficiency

Active balancing is always more efficient than passive balancing [14], considering that with passive balancing $100 \%$ of the energy is wasted. So purely based on efficiency gain it could be said that active balancing is desired in every situation. However, the gained efficiency comes with a price, and active balancing techniques are almost always more expensive [15]. The question arises if the extra cost is worth the extra efficiency, and this is not always the case. As previously shown in [16], active balancing methods can on average add $2 \%$ to the total usable energy of the battery. In most cases where energy is not extremely scarce the benefits of active balancing do not outweigh the financial drawbacks. But in some cases it is an absolute advantage to have this extra $2 \%$, like in space industry. For example bringing a satellite in to orbit, the launch cost per kilogram to actually bring the satellite into space is tremendous [17]. Here, in comparison with the launch costs, the additional costs for active balancing are very slim, especially taking into account that the same battery capacity can now be reached but by using less batteries and thus, the total weight will decrease.

### 2.2.2 Balancing time

Balancing time is one of the most important aspects which make active balancing attractive. This is applicable in high power applications, mainly in which fast charging and discharging is required. As already explained is it with active balancing only necessary to move half of the excess charge of the high SoC battery to the low SoC battery. With passive balancing, all of the excess charge would need to be drained from the high SoC battery. Thus in high power applications like EVs, Electric boats / ferries, Electric city busses or other applications where fast charge / discharge cycles are necessary, active balancing can provide advantages. This is also a trend which is visible in the EV market. While passive balancing was the most common technique traditionally, EV manufactures are now shifting towards active balancing. [18].

### 2.2.3 Case study Super B

After interviews with the company some real-world applications where active system level balancing is desired were obtained. At first, when multiple batteries are connected in series, the on-board passive balancer of each battery communicates with the other batteries in the series string. When one battery has excess charge, it will be dissipated using the passive cell balancers of the battery. Like more companies, Super B is also considering to shift towards active-balancing on cell level. As a consequence, it is necessary to also have active balancing on system level because the passive cell level balances can now no longer be used for this. Another situation where active balancing on system level is desired is when one battery needs to be replaced in a series string. This battery will not be in-
balance with the other batteries at first. With active balancing it would be easier replace single batteries in a series string because it will be faster and less heat will be generated.

### 2.2.4 Case study

The last example of when active balancing is desired will be explained with a case study.
Super B has supplied batteries for electric canal boats. The battery packs of these boats consist of 54 batteries connected in series and 6 of these strings in parallel. The setup can be seen in figure 3 . In real life situations like these it could be that some batteries are situated for example at a warmer or colder place than other batteries. Considering that the string is so long and that some batteries are physically far away from each other. Imbalance will always arise but it is very well possible that imbalance on system level will be larger than on cell level because of environmental conditions and long cables etc. This is why it is important to balance the batteries. It is interesting to research the possibilities of doing this actively and what advantages it can have over passive balancing in this situation.

Presently, the Super B batteries are being passively balanced at the end of charge. This means that sometimes the balancers need to work really hard in order to get all the batteries back in balance again, generating a lot of heat. This research aims to contribute to a solution for this because it strives to find a suitable active system level balancing topology which can also balance in the flat region, assuming that accurate, non-voltage based SoC estimation is available in the future. The balancing currents can then be lower and less heat is generated.


Figure 3 Super B battery set up in electric canal boat [41]

### 2.2 Passive balancing

In chapter 2.2 and 2.3 the different types of cell balancing topologies are explained. Note that they are explained as cell level balancing topologies, this is because most research has been conducted in the field of cell balancing rather than on system level balancing, although there are some points that distinguish cell level balancing from system level balancing (which will later be discussed). The topologies have the same core functioning on cell level balancing as well as on system level balancing considering that one battery can basically be seen as one big cell. the different terms can therefore be interchanged.

First, three different passive balancing techniques will be discussed. They are all based on the shunting resistor cell balancing methods, which is the most straightforward equalization concept. When a cell in the series string reaches its overvoltage level the excess energy is dissipated in a resistor. The excess energy is not transferred to any other cell or the load, it is simply dissipated as heat in a resistor.

### 2.2.1 Fixed resistor

The most basic form of passive balancing is the fixed resistor method as seen in figure 4 . It has no switches and a resistor is placed in parallel with each cell. The resistor is utilized to remove the excess


Figure 4 Fixed resistor passive balancer topology [19]


Figure 5 Zener diode resistor passive balancing topology [20]


Figure 6 Switched resistor passive balancing topology [20]
charge, and it is released in the form of heat. The idea is that higher voltage cells will discharge faster than the lower voltage cells and so the system is balanced automatically. However a disadvantage is that charge will always be lost since the process is continuous because of the fixed resistor [19]. Also provides this method only a balancing solution at the end of charge of LFP cells because it balances using voltage differences which only occur at the end of charge in a LFP battery.

### 2.2.2 Zener diode resistor

An improvement of the previous method has a Zener diode connected in series with the resistor, figure 5 . The diode switches the resistor circuit ON when the voltage has reached the voltage threshold to prevent overcharging. This means that the balancer is not always on and thus it saves power. Advantages are the simplicity and the lack of complex control mechanisms, also is it low in cost. The downside of this technique is that it again, will not work optimal with LFP cells due to the voltage based balancing mechanism [20].

### 2.2.3 Switched resistor

The last passive balancing technique is the switched resistor, figure 6. The Zener diode is replaced by a controlled switch and this method works better for LFP batteries because the control does not solemnly rely on voltage differences. The switch is turned on either when the cell reaches the threshold voltage or when SoC information is available about arisen imbalances. The excess energy is then dissipated in the resistor. The design is more control intensive but it is also more flexible and it can perform more precise balancing [20].

The downside of all passive balancing techniques is the waste of energy, which may also cause problems in terms of heat generation. Additionally, most of the previously mentioned mechanisms only balance at the end of the charge cycle and thus, the battery needs to be fully-charged in order to balance the cells which is not always the case in user applications.

### 2.3 Active balancing

In active balancing techniques the excess charge is transferred to other cells rather than dissipated as heat. The advantage of this is that less energy is wasted, less heat is produced and it is usually faster. Also the ability balance outside the end of charge region, this is in general not necessary a property of active balancing itself but this research focuses on topologies that do have this feature. Disadvantages are that it is sometimes more complex, meaning that more active control is required, than passive balancing and that it is higher in cost. There exist multiple ways to transport the excess charges as well as multiple mediums to accomplish this transport. Different main principles are cell to cell, cell to neighbor and cell to pack balancing.

## Cell to Neighbor (CtN)

In this structure energy can only be directly transferred between adjacent cells. The cell with the highest energy transfers its charge through a medium which temporarily stores the energy, this
medium can for example be a capacitor or an inductor. Advantages are that it is generally easy to implement and almost no additional cable connections are needed, making it cheaper compared to Cell to Cell balancing. Disadvantages are that the balancing time is usually not high and with longer strings it can become less efficient because the charge then sometimes has to be transported through more cells.

## Cell to Cell (CtC)

In this balancing scheme, the most-charged cell can not only transfer energy to its adjacent cells but to any other cell in the pack. This generally makes the balancing process a lot faster and more efficient but it also makes it more control intensive and more expensive due to the need of more cables.

## Cell to Pack (CtP)

Cell to pack balancing redistributes the energy from one or more cells to the whole battery pack. This is a relatively easy and fast way of redistributing the energy. For a battery-pack with N -series connected cells, the downside is that $1 / \mathrm{N}$ part of the energy is also redistributed back to the cell which was already most charged. Also the components connected to the whole series string need to be rated to withstand high-voltage levels, as high as the sum of the voltages of all batteries in the series string, which makes the system more expensive.

Different active balancing schemes are discussed in the next sections.

### 2.3.1 Switched Capacitor Equalizer (SCE)

The SCE proposed in [21] is a form of CtN balancing. It involves switching a capacitor to consecutively-connected battery-cells to charge and discharge them through the capacitor. It is done evenly with a fixed duty cycle of $45 \%$ ( $10 \%$ dead time is included to avoid current shoot-through). The charge of the adjacent cells is divided equally over the cells in the series string. The switching scheme and basic topology are shown in figure 7. A disadvantage to this topology is that it is relatively slow compared to other active balancing techniques, because it is based on CtN balancing. Additionally it does not work for balancing LFP batteries between $10 \%$ and $90 \%$ SoC, considering that the voltage is almost equal in this entire region and that the capacitor needs a voltage difference in order to charge / discharge. Advantages are that there are no high voltage components needed because each switch only needs to handle the voltage of a single cell rather than the whole string voltage. The control of this topology is simple and the balancing process can take place when batteries are being charged or continuously during battery operation. The method is modular and easy to expand to long series strings. The scheme requires $\mathrm{N}-1$ capacitors and 2 N switches, where N is the amount of cells / modules in one string. As proposed in [22] it is also possible to have a double tiered switched capacitor equalizer. This provides more current paths for the charge to flow to other cells, creating a shorter alternative path to move charge to cells which are further away. In [22] the extra paths are merely used to reduce the balancing time but instead of creating more energy paths between the cells it is also possible to use the double tiered switched capacitor as a combination for cell and system level balancing. The first tier would then be used for cell level balancing whereas the second tier would be used for system level balancing.

### 2.3.2 Switched Inductor Equalizer (SIE)

The SIE proposed in [23] uses inductors to temporarily store the charge of the neighboring cell, which is a form of CtN balancing. Here all switches, except for one, are triggered together all the time which makes the control more control intensive compared to the SCE, especially in longer strings. This also enlarges the voltage stresses on the one switch that is not conducting because it has to withstand the voltage of all cells. These voltage stresses results in a limiting factor of the modularity and an additional safety risk considering that a DC short occurs if that switch fails [24]. The switching scheme and the basic topology can be seen in figure 8. Each switch is off for a fixed amount of time, approximately $1 / \mathrm{N}$, every cycle. Meaning that that the control intensity increases with the increase in the quantity of cells. Advantages are that $\mathrm{N}-1$ inductors are needed and only N switches, which is less than with the SCE. [23] shows a prototype evaluation where the equalizer is connected to a pack of


Figure 7 Switched Capacitor balancer topology and switching scheme [21]


Figure 8 Switched Inductor Equalizer topology and switching scheme [23]
twenty 2.2 Ah Li-ion cells, where five cells are connected in series and four of these strings are connected in parallel, creating a pack of $18 \mathrm{~V}, 8.8 \mathrm{~A}$. One of the cells is purposely drained 2 Ah to create imbalance. The results showed that with voltage based balancing the pack was in-balance again after 40 minutes. [23] states that the balancer can be improved by using a SoC estimator and that balancing based on SoC levels instead of voltage can decrease the balancing time down to 20 minutes with the given imbalance, so doubling the balancing speed. [23] also showed that a peak efficiency of $90 \%$ could be obtained at 7 W power transfer.

### 2.3.3 Converter based Current Diverter (CCD)

The CCD proposed in [25] is an extended version of the SIE with better options for modularity and it is also a form of CtN balancing. This method is based on a buck-boost converter topology which operates in Discontinuous Conduction Mode (DCM). The charging current be diverted away from a fully charged cell to the next cell in the stack. This allows the rest of the stack to be fully charged while avoiding overcharging of the full cell. It also allows to move charge between batteries while they are not being charged, freely choosing from which batteries to subtract / add the energy. A unidirectional version of this topology can be seen in figure 9a. For example, when battery VB1 is fully charged, switch Q1 is enabled and the charging current will be diverted to L1 in which the energy is stored. When Q1 is disabled the energy stored in L1 will be provided to battery VB2. This way, an uni-directional flow of the excess current is provided with the diverter modules, each consisting of a switch, a storage element and a freewheeling diode. Only for the last cell an isolated DC-DC converter module is required to provide a flow path for the charge of the last cell in the string. This charge will be provided back to the whole stack. In order to provide a more flexible structure and a bi-directional energy flow, the freewheeling diode can be replaced by a second switch, shown in figure 9 b . This also allows for balancing while charging, discharging and also when the batteries are not being used, this is because the balancer works as a buck boost converter, moving charge from the supply (one battery) to the load (the neighboring battery). Also no additional DC-DC converter is needed for the last cell. The operation stays the same as with the uni-directional diverter, only there is now the option to enable the second switch in the diverter module in order to transfer the energy in the opposite direction. The body diode (D1) of the other switch is then still used to conduct the current after Q2 is turned off. The currents in each period can be seen in figure 9 c . In this topology $\mathrm{N}-1$ inductors and $2 \mathrm{~N}-2$ switches are needed. Advantages are that it is a modular structure which can easily be expanded and the components experience no high voltage stresses. But the control intensity increases due to the need of measurements or predictive algorithms in order to determine from which cell the current should be diverted. However, this also gives more control in the $10 \%-90 \% \mathrm{SoC}$ region. The method also provides the feature to adjust the balancing current by tuning the duty cycle, which can be a useful option in various applications.


Figure 9a Uni- directional Converter based Current Diverter topology [25]


Figure 9b Bi-directional Converter based Current Diverter topology [25]


Figure 9c Converter based Current Diverter currents [25]

### 2.3.4 Double Switched Converter Based Current Diverter (DSCCD)

The DSCCD uses a different switching scheme as the abovementioned method but uses the same hardware. In the CCD the body diode of the second switch is used to conduct the current in the inductor towards the second cell. This will always give losses because of the voltage drop over the diode. These losses can be reduced by turning on the second switch instead of conducting the current through the diode. The current path is now through the closed switch instead of through the body diode of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) to ensure a more efficient and bi-directional operation. But this makes the switching scheme more complicated because instead of controlling one switch, now two switches need to be controlled. And when for example a duty cycle of $30 \%$ is applied to one of the two switches it is not possible to just have an inverse switching scheme for the second switch. This will cause the inductor current to keep building up in each cycle as can be seen in the simulation results figure 10a.

There are two ways to overcome the current build up without using the freewheeling diode. The first method matches the duty cycle exactly so that the inductor is charged and fully discharged at the end of one period, making it operate in boundary conduction mode. This gives the simulation results as can be seen in figure 10 b When two cells of the same voltage are being balanced this means that the duty cycle has to be $50 \%$. With this method there is no possibility that the current will built up in the inductor but there is also no option to adjust the amount of charge that is transferred. The second method has the possibility to control the amount of charge that is moved between cells, but requires zero-current switching at a high frequency of the complementary switch, which is more complex and requires precise control. For example, when the desired amount of charge corresponds to a duty cycle of $30 \%$ for the first switch. It means that Q1 has to be on till 0.3 T , after that Q 2 is on from 0.3 T till 0.6 T . Then when the inductor current is zero, both Q1 and Q2 need to be off from 0.6 T till T. This gives the simulation results as can be seen in figure 10c. The simulation shows that this method gives the same results for the inductor current as the CCD but with a more complicated switching method. But it also provides a higher efficiency and can still make use of the feature to have a variable balancing current set by the duty cycle.


### 2.3.5 Single Switched Capacitor (SSC)

The SSC proposed in [26] only uses one capacitor and has a relatively easy control strategy, which is a form of CtC balancing. This capacitor stores the energy of the highest voltage cell and redistributes it to the lowest voltage cell. The topology can be seen in figure 11. Each cell can be selected individually to charge or discharge the capacitor, in order to select the desired cell, $\mathrm{N}+5$ bi-directional switches are needed for this topology. Whereas the SCE needs 2N switches, meaning that the SSC becomes more attractive as the series string becomes larger. The voltage stresses on these switches will also remain low, even if the number of cells is increased. A disadvantage of this technique is that it is hard to balance in the flat region of a LFP cell because a voltage difference between the cells is needed in order to charge / discharge the capacitor. This problem can be solved by boosting the capacitor voltage between the charging and discharging pulses, which can be done with a small isolated DC-DC converter. Using this technique the flat region balancing issues can be overcome, however this adds to the costs and control intensity of the system. In a study conducted in [26], it was observed that the SSC can have up to $12 \%$ higher efficiency as compared to the SCE for LFP cells.


Figure 11 Single switched capacitor balancer topology [26]

### 2.3.6 Multi Winding Transformer (MWT)

The MWT is a form of CtP balancing. It makes use of a multi-winding transformer as proposed in [27]. The transformer has a separate winding for each battery cell or module on the secondary side and one winding on the primary side which is connected to the whole battery stack. The bidirectional capability of the transformer allows to balance in two directions. Namely from one cell to the whole pack, this is usually applied during charging to prevent overcharging of the weakest cell, or from the whole pack back to one cell, which is typically done while discharging. The proposed topology can be seen in figure 12. The desired cell to be either charged or discharged can be selected by using the switches, which are typically low voltage switches. Considering that there is no voltage difference


Figure 12 Multi Winding Transformer balancer topology [27]


Figure 13 Multiple Transformers balancer topology [28]
needed in order to transfer power, this method is suitable for balancing in the $10 \%-90 \%$ SoC region of LFP cells. Another advantage is the galvanic isolation that the transformer provides which enhances the safety of the system and there is also no need for precise and difficult control of the switches. Disadvantages of this method are the lack of modularity, considering that the multi winding transformer would need the same amount of windings on the secondary side as the amount of modules in the series stack. For balancing between cells this might not be an issue because this number is rather constant, however when balancing on system level this number has a larger variability. Also a multi winding transformer would cost more and is usually larger in physical dimensions than the components used in other active balancing methods. A transformer with N windings on the secondary side is needed, together with $\mathrm{N}+2$ switches.

### 2.3.7 Multiple Transformers Equalizer (MTE)

The MTE proposed in [28] can be seen in figure 13. It is a form of CtP balancing and each cell or battery module has its own transformer with a winding ratio of $1: 1$. The primary side of each transformer is connected to the single battery and the secondary side is connected to the whole battery pack. The advantage of this method is that it is efficient and it can start balancing in an early stage of the charging cycle [29].It has the capability to balance in the flat region and it can balance with high current rates. Also is this a modular structure considering that it can easily be expanded by adding more transformer blocks. One balancer block consist of N transformers, and 2 N switches. The downside of this method is that the secondary side of the transformer is connected to the battery pack, meaning that it should also be able to handle the voltages of the whole series string. Also is this method not easy to implement on large battery systems considering the need of many additional (long) cables which need to be connected from the secondary side of each transformer to the battery pack.

### 2.4 Comparison

The results of the previously discussed balancing topologies have been summarized in a comparison table based on the set criteria. For the criteria where it was not possible to have a quantitative score a rating system with ratings between 1 and 5 has been set up, with 1 meaning the lowest possible score for that criteria and 5 the highest possible score. These ratings are based on the performance level of: Modularity, safety, complexity (control intensity), efficiency and balancing time. It is still difficult to exactly judge the efficiency and balancing time of the topologies. Therefore research [9] is used, where nine different active balancing topologies are tested under the same test conditions. It is used to obtain an indication of the efficiency and balancing time of the topologies but no exact ratings are given for those criteria. A more detailed description of the aspects that are taking into account while grading is given below.

- Flat region balancing

Balancing in the flat region (with SoC between $90 \%$ and $10 \%$ ) determines the grading for this metric. With topologies where a voltage difference is required for the system to operate it is not possible to equalize the charge within this region.

- Number of components

The number of components strongly relates to the total system costs, it is therefore an important aspect when the system is commercialized. In table 1 N stands for the number of cells / batteries in the series strings.

- Voltage stresses

The voltage stresses on the components are either high or low. With low meaning that the components only need to withstand the voltage of a single cell / battery. When the voltage stresses are high it means that the components need to withstand the voltage of the whole series string. This can become significantly high, especially in longer strings. If the voltage stresses are high it will negatively affect the modularity and the cost of the system.

- Control intensity

The complexity of the system refers to the control intensity of the topology. The level of difficultness to determine the SoC is not taken into account, this is assumed to be a given input parameter.

- Modularity

The level to which extend it is possible to expand the series string without significantly increasing the complexity and costs. Also voltage stresses on components play an important role as well as the flexibility to have any number of batteries in the series string.

- Ease of integration

This study focusses on the ease of integration on system-level. For example, with certain schemes it is more difficult to create big systems due to the need of many long cables, whereas with other structures the length of the series string is not an issue.

- Balancing time

When judging the balancing time the maximum balancing current must be taken into account. Also the ability to already start balancing in the flat region of the LFP cells plays an important role when it comes to the balancing time, because then the system can start balancing in an earlier stage instead of only at the end of the charge cycle. The last important aspect is the topology structure, so whether it is, $\mathrm{CtN}, \mathrm{CtC}$ or CtP . Generally, the CtC is the fastest method, considering that here the charge is directly taken from the highest charged cell and delivered
back to the weakest charged cell, whereas with CtN and CtP are less time efficient because it either has to be transported through other cells or it is evenly divided other the whole series string.

- Efficiency

For the efficiency, the topology structure is an important aspect. When for example the charge has to be moved through every battery in the series string (and its corresponding balancing circuit) as in CtN it is of course less efficient then with CtC . But, it must be said that the efficiency is the hardest criteria to judge and compare, considering that the efficiency relies on many different factors such as: used components, balancing currents, ambient temperature and more. Even when hard numbers on the efficiencies are given in papers, it is unfair to compare them with results from other papers because the test conditions are not identical. Therefor an indication of the efficiency is extracted from [9], the test setup is constant when evaluating the different topologies. It however, only gives a rough comparison between the efficiencies of the different topologies rather than exact numbers.

It is important to note that some schemes will already score better or worse on certain criteria based on their fundamental characteristics. For example, CtN structures will not have the fastest balancing time and are usually not the most efficient but they are easy to control and are easy to integrate on system level. CtC structures have a shorter balancing time and can be more efficient but they are harder to install on system level and are more complex to control. CtP structures are also efficient and fast in balancing but they also score less good on system level integration [30].

Ofcourse some judgement criteria are of more importance than others. Considering that the balancing system is supposed to be applied in real life systems it is important that it is economically feasible. This means that the number of components is very important as well as the voltage stresses on these components because high power components are more expensive than low power components. Also the ease of integration on system level is important. If for example many additional cables are needed to install the system it might not be easy to install and makes it less attractive to use the system. Also modularity is an important criteria because the amount of batteries in a series string can differ in various applications.

Table 1 Comparison table between seven different active balancing topologies and set criteria

| Criteria | Flat region balancing | \# components | Voltage stresses | Control intensity | Modularity | Ease of integration |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SCE | !Possible | SW: 2N, C: N-1 | Low | 1 | 5 | 5 |
| SIE | Possible | SW: N, L: N-1 | High | 2 | 3 | 5 |
| CCD | Possible | SW: 2N-2,L: N-1 | Low | 2 | 4 | 5 |
| DSCCD | Possible | SW: 2N-2, L: N-1 | Low | 5 | 4 | 5 |
| SSC | Possible* | SW: N+5, C: 1 | High | 4 | 4 | 1 |
| MWT | Possible | $\begin{aligned} & \text { SW: } \mathrm{N}+2 \\ & \mathrm{~T}: 1 \text { ( } \mathrm{N} \text { windings) } \\ & \hline \end{aligned}$ | Low | 2 | 1 | 1 |
| MTE | Possible | SW: 2N, T: N | High | 2 | 4 | 1 |

* possible but extra measures are needed
! not
The comparison results can be seen in table 1 . Fields marked in green score explicitly good on a certain criteria whereas fields marked in red score explicitly bad on this criteria.


### 2.5 Chosen topology

Based on the results of table 1 it is clear that there is not one specific topology which scores immediately the best on all criteria and trade-offs will always have to be made. But there is one topology which has no criteria on which its scores explicitly bad, namely the CCD. And likewise, the closely related DSCCD only scores low on control intensity. Therefor the choice has been made to further invest in the CCD with possible future research to the DSCCD. Because they make use of the same hardware it is easy to expand the research from the CCD to the DSCCD.

The CCD also scores excellent on the three most important criteria for the system level balancer namely:

1) Economically feasibility - For the CCD each battery only needs to be equipped with two extra MOSFETs and one inductor. Due to the low component count and the use of cheaper components (cheap in comparison with a transformer for example), the method is financially attractive. Also is there no need for high voltage components because each component only needs to be able to withstand the voltage of two batteries, this also reduces the costs.
2) Ease of integration - The topology scores high on this aspect considering that only one balancer block, consisting of two MOSFETs and one inductor, needs to be added to the main BMS of the battery. With the balancer block installed, only one extra cable form one battery to the next one is required to make an operational system. Figure 14 shows the old setup compared to the new one.
3) Modularity - Considering the low voltage stresses on the components and the easy integration of the system, it is a highly modular topology which can easily be expanded to long series strings.


Figure 14 System setup without active system balancer vs new system setup with converter based system balancer

## Chapter 3

## Modeling and Simulations

This chapter describes the modeling and the simulation of the chosen topology. The model will be used to estimate efficiencies and what parameters influence this efficiency. The simulations will be used more to explore the functionality and flexibility of the system. It also answers the third research questing namely: What are the efficiencies that can be achieved, and what are the parameters that influence the efficiency?

In this chapter the two switches of the balancer blocks will be referred to as $\mathrm{S} \ldots$, the inductor will be L... and VB... are the battery packs.

### 3.1 MATLAB

The model is created by using MATLAB, in order to create the model, certain assumptions had to be made. To model the MOSFET conduction losses, a fixed $R_{D S_{o n}}$ value is used, rather than one which is varying over the amount of current that it is conducting. Further the frequency is assumed to be fixed as well as both the battery voltages with are set to be equal. This has been done purposely to model the flat region balancing. Cable losses and other resistive losses, that are not described, are not taken into account. Influences of temperature are also not taken into account.

### 3.1.1 Currents

A MATLAB model of the converter has been made in order to determine the influence of certain component parameters on the efficiency. The converter description is divided in three sections, figure 15 gives a visual representation of those sections.

1) $t_{o n}$ : This is when the MOSFET (S1, Figure 16) of the highest charged battery is conducting. The current path consist of VB1, S1 and L1. The current through the switch starts at 0 A and increases up to $\mathrm{I}_{\text {peak. }}$. Without the internal resistance of the MOSFET and the inductor it would increase linearly. But taken into account the resistances the path can be seen as an RL circuit and the current is modelled as:

Current $\mathrm{t}_{\mathrm{on}}[\mathrm{A}]$ :

$$
\begin{equation*}
i_{t_{o n}}=\frac{V B 1}{R_{D S_{o n}}+R_{\text {inductor }}} *\left(1-e^{-t * \frac{R_{D S_{\text {on }}}+R_{\text {inductor }}}{L}}\right) \tag{1}
\end{equation*}
$$

Where t is $\mathrm{t}_{\mathrm{on}}, \mathrm{L}$ is the inductance and $R_{\text {inductor }}$ and $R_{D S_{o n}}$ are the internal resistances of the inductor and the MOSFET.
2) $t_{\text {fff: }}$ This is when the energy stored in L1 is delivered to the lower energy battery, during this time S 1 is off and the body diode of S 2 is conducting. The current path now consist of L1, VB2 and D2. It decreases from $\mathrm{I}_{\text {peak }}$ down to zero because the converter is operated in DCM and it is again no linear function because of the internal resistances of L1 and D2. Also is the angle of the decaying graph slightly different due to the voltage drop over the diode. The current can be described as:

Current $\mathrm{t}_{\mathrm{off}}[\mathrm{A}]: \quad \quad i_{\text {toff }}=I_{\text {PEAK }}-\frac{V B 2+V_{F}}{R_{\text {Diode }}+R_{\text {inductor }}} *\left(1-e^{-t * \frac{R_{\text {Diode }}+R_{\text {inductor }}}{L}}\right)$
Where $t$ is $t_{\text {off }}$ and $V_{F}$ is the forward voltage drop over the diode.
3) $t_{\text {dead }}$ : When the current in the inductor is zero and no switch nor diode is conducting.


Figure 15 Inductor current with duty cycle $30 \%$ showing ton (blue line), toff (red line) and $t_{\text {dead }}$


Figure 16 Basic balancer block circuit

Figure 15 shows the graph of the inductor current where S 1 has a duty cycle of $30 \%$. The parameters for the inductor have been chosen such that is does not reach saturation and as can be seen, it behaves nearly linear.

### 3.1.2 Losses

With the currents described the losses can be calculated. The losses during $\mathrm{t}_{\mathrm{n} \text { n }}$ consist of the conduction loss of the S 1 , the switching losses of S 1 and the inductor losses.

The conduction loss of $S 1$ is calculated using the Root Mean Square (RMS) current through the switch. The loss is described with equation 3 where $i_{\text {ton }_{R M S}}$ is the RMS current during $\mathrm{t}_{\mathrm{on}}$. The switching loss is given in equation 4 . For ease, the inductor losses are estimated with Würth's REDEXPERT [38] loss calculation tool for power inductors. It uses the frequency, duty cycle, inductance, current ripple and average current in order to estimate the losses.

Conduction loss switch [W]: $\quad \operatorname{cLoss}_{S 1}=i_{t_{o n-R M S}}{ }^{2} * R_{D S_{o n}}$
Switching loss switch [W]: $\quad \operatorname{swLoss}_{S 1}=\left(0.5 * t r * I_{\text {Trise }} * f * V B 1\right) *\left(0.5 * t f * I_{\text {PEAK }} * f * V B 1\right) *$ $(f * Q r r * V B 1)$

Where $t r$ and $t f$ are the rise- and fall-time of the MOSFET. $I_{\text {Trise }}$ equals the current at the rise time, note that this is nearly zero because it switches zero current. $Q r r$ is the reverse recovery charge and $f$ is the switching frequency.

During $\mathrm{t}_{\text {off }}$ the losses are the loss of the diode, consisting the conduction loss which can be seen in equation 5. And the switching loss of the diode, seen in equation 6 .

Conduction loss Diode [W]: $\quad c \operatorname{Loss}_{D 2}=\frac{1}{T s} \int_{t_{o n}}^{t_{\text {off }}}\left(V_{F} * i_{t_{\text {off }}}(t)+R_{\text {Diode }} * i_{t_{o f f}}(t)^{2}\right) d t$
Switching loss Diode [W]: $\quad \operatorname{swL_{\text {Loss}}^{D2}}=\operatorname{Qrr} * f$
Where $\operatorname{Qrr}$ are the reverse recovery losses of the diode, $\mathrm{R}_{\text {Diode }}$ is the internal resistance of the diode and $T s$ is the period time. $\mathrm{t}_{\mathrm{on}}$ is at DTs and $\mathrm{t}_{\text {off }}$ is when the current in L reaches zero.

### 3.1.3 Efficiency

The average balancing current (which is specified as the current that is retrieved from the highest energy cell), $\mathrm{I}_{\text {peak }}, \mathrm{t}_{\text {off }}$, Power input, total losses and the efficiency are calculated with the following equations:

Balancing current [A]: $\quad I_{\text {balance }}=\frac{\int_{0}^{t_{o n}}{ }_{i_{\text {Ton }}(t) d t}}{T s}$
Peak current [A]: $\quad I_{P E A K}=\frac{V B 1}{R_{D S_{\text {on }}}+R_{\text {inductor }}} *\left(1-e^{-(D T s) * \frac{R_{D S_{\text {on }}}+R_{\text {inductor }}}{L}}\right)$
Time off [s]: $\quad t_{\text {off }}=-\frac{L}{R_{\text {Diode } e}+R_{\text {inductor }}} * \log \left(-I_{\text {PEAK }} * \frac{R_{\text {Diode }}+R_{\text {inductor }}}{V B 2+V_{F}}+1\right)$
Total losses [W]: $\quad$ TotalLosses $=c \operatorname{Loss}_{S 1}+s w \operatorname{Loss}_{S 1}+c \operatorname{Loss}_{D 2}+s w \operatorname{Loss}_{D 2}+\operatorname{Loss}_{L}$
Power input [W]: $\quad P_{\text {in }}=\frac{\int_{0}^{t_{o n}} i_{t_{\text {on }}}(t) * V B 1 d t}{T s}$
Efficiency [\%]: $\quad$ Efficiency $=\frac{P_{\text {in }}-\text { TotalLosses }}{P_{\text {in }}} \quad * 100 \%$
Where $I_{\text {balance }}$ is the average balancing current, $D$ is the duty cycle, $P_{\text {in }}$ is the total input power of the system and TotalLosses are all the modeled losses in the system.

All the equations combined provide a detailed description of the balancer topology and corresponding losses, balancing time, balancing current and parameters that influence the efficiency. The results of the model can be seen in chapter 5.1. The full code of the MATLAB model can be found in Appendix C.

From the model it can be concluded that certain trade-offs have to be made between different circuit parameters. For example, the relationship between $R_{D S_{o n}}$ and $\mathrm{Q}_{\mathrm{r} r}$. While decreasing $R_{D S_{o n}}$ is generally desirable for minimizing conduction losses it is also crucial to assess the impact of other parameters, such as $\mathrm{Q}_{\mathrm{r}}$, especially if the switching performance is critical. However it is usually the case that when one of these is decreased the other one will be increased. When for example the MOSFET is optimized for a lower $R_{D S_{o n}}$, other parameters, like the reverse recovery charge, might increase. If the MOSFET has a large conduction area this means that it has a low resistive path but on the other side it also means that it can increase the stored charge and, consequently, increase $\mathrm{Q}_{\mathrm{rr}}$. So it is essential to consider that certain parameters are interconnected and trade-offs have to be made [31]. It must be noted that $\mathrm{Q}_{\mathrm{r}}$ is a function of the body diode of the MOSFET which is conducting during toff. However when an additional diode is placed in parallel with the MOSFET the tradeoff between those parameters is no longer relevant.

Another important consideration is the switching frequency. It might be desirable to have higher switching frequency because this can reduce the size of passive components like the inductor. Also the current is then lower which results in lower conduction losses. However, increasing the switching frequency also leads to higher switching losses as can be seen in equations 4 and 6 . Finding an optimal value for the frequency is essential for achieving a good balance between component size and efficiencies. Therefor a frequency sweep between 10 kHz and 1 MHz is performed on the model in order to find the optimal balance between losses and frequency. During the test the values for the inductor, the duty cycle and the battery voltage stayed fixed. Also the parameters for the MOSFET and diode stayed fixed. The fact that the result for the frequency sweep will be different with different component choices is acknowledged. But this would add to many variables to the test making it even more complicated to find the right frequency. Therefore the components and associated parameters


Figure 17 Frequency sweep over total system losses
have been set fixed to the values seen in appendix C. The total losses as a function of the frequency can be seen in figure 17 .

From figure 17 it can be seen that there is an optimal switching frequency around 80 kHz . This is where the switching losses and conduction losses are equal to each other. At lower or higher switching frequencies the total losses increase. At lower switching frequencies the conduction losses are dominant. The conduction losses are calculated by taking the square of the RMS current and multiplying it by the ohmic resistance. The current is determined by the ON time and the ON time increases as the frequency decreases and thus the conduction losses increase. At higher frequencies the switching losses become dominant because they increase with the frequency. Choosing a switching frequency of around 80 kHz would therefore be a good choice in this situation.

### 3.2 Simulations

With the circuit parameters retrieved from MATLAB a Simulink model is constructed in order to validate the balancing concept and explore the possibilities. The model can be seen in figure 18. It consist of four 12 V battery modules: VB1, VB2, VB3 and VB4. The battery modules include the nonlinear voltage / SoC behavior in order to get the most realistic results. The voltage vs Depth of Discharge ( DoD ) curve of the batteries can be seen in figure 19 , the full design of the battery modules can be found in Appendix A. The control signal supplies a pulse to either one or none of the switches of one balancer block. The signal has a frequency of 80 kHz and a pulse width between $0 \%$ and $50 \%$. When the signal is applied to the upper switch of the balancer block, the charge is redistributed from the upper positioned battery to the lower battery. Vice versa, when the lower switch it toggled the charge is pumped from the lower positioned battery to the upper battery.

Whether a certain battery is either discharged or charged depends to which switch the control signal is applied and multiple switching schemes are possible. For example, when the signal is only provided to S1 of figure 18, then energy is transferred from VB1 to VB2. No energy is retrieved from or supplied to VB3 and VB4 because no control signal is applied to either of their switches of the corresponding balancer block.


Figure 18 Overview system setup with three balancer blocks, balancing four batteries


Figure 19 Voltage vs Depth of Discharge (DoD) curve of the used battery model

It is possible to transfer energy from one battery to its neighbor, for example from VB1 to VB2. But it is also possible to transport the energy from the upper battery down to the last battery in the series string, from VB1 to VB4. The energy is then transported through VB2 and VB3 but no net energy remains in those batteries. If for example one battery is significant lower in energy it is also possible to supply it with energy from two other cells. For example if the control signal is applied to S1 and S4 than the energy is retrieved from VB1 and VB3 and it is supplied to VB2. Examples of possible switching schemes can be seen in table 2 . Note that it is never possible to apply the same control signal to both switches of one balancing block, if this were the case than a short circuit between the two batteries will occur. It is therefore important that the system will be designed such a way that it is inherently safe and it is not possible to turn on both switches at the same time. The simulations results of the switching schemes marked in green in table 2 will be showed in results chapter 5.2.

Table 2 Switching schemes

| Controlled <br> switch | Transported energy |
| :--- | :--- |
| S1 | VB1-, VB2+ |
| S1,S3 | VB1-, VB3+ |
| S1,S3,S5 | VB1-,VB4+ |
| S1,S4 | VB1-,VB2++,VB3- |
| S1,S5 | VB1-,VB2+,VB3- <br> ,VB4+ |
| S2,S4,S6 | VB1+,VB4- |
| S3,S6 | VB2-,VB3++,VB4- |
| None | All stay the same |

## Chapter 4

## Prototype

The prototype has been designed in order to validate and test the system balancer. At first the prototype should show the core functioning of the system balancer, namely the balancing between two batteries by means of the buck/boost converter. Later, tests can be executed to determine other specifications such as efficiencies, balancing time, balancing current, etc.

### 4.1 Prototype requirements

Requirements have been set up to which the prototype should live up to, these are listed below:

- Balancing current - The balancing current which is now used in the Super B batteries lies between 0.8 A and 1.5 A . The balancing in the Super B batteries currently happens at end of charge, meaning that the imbalance has to be equalized in a short period of time. The new balancer is designed with the intention to do flat region balancing as well, meaning that the balancing current can be lower, simply because there is more time to equalize. The only sidenote is that with the present knowledge it is not yet feasible to get an accurate enough SoC estimation in the flat region in order to perform the balancing process there. Therefore in order to make the system also work under the current conditions the balancing current must be in the range of the pre-existing balancers. The minimum balancing current requirement has therefore been set to 1 A . In the future this may reduce, as a result of more accurate SoC information in the flat region.
- Voltage requirements - All the components have to be able to withstand the maximum voltages they are expected to experience. In the case of the CCD this is two times the battery voltage so at least 28 V , but some margin should be taken into account.
- Current measurement - Because the battery voltage does not give any clear indication about the current SoC of the battery it is necessary to precisely know the current which comes in and out each battery. With this coulomb counting technique the current SoC can be determined independent of the battery voltages. Therefore accurate current measurement is required if the balancer were to be implemented. For the prototype it is not a strict requirement because it will primarily be used to test the core functioning of the topology.
- Freedom of charge distribution direction - This means that the energy must be able to be transported in two directions. Either, for example, from VB1 to VB2 or from VB2 to VB1.
- Temperature and dimensions - No specific requirements have been set for this yet. The only importance is that the chosen components can survive the expected temperature ranges.
- Scalable balancing current - This is no requirement but a useful feature that comes with the chosen topology. Namly that size of the balancing current can be adjusted by tuning the duty cycle of the control signal. This way, more freedom is provided.


### 4.2 Schematic

The prototype is designed to balance only between two batteries. Also is the prototype a stand-alone product and a microcontroller, programming pins, power supply and other features are implemented. However, in a final design the system balancer should be integrated with the existing BMS and there is no need for the all the external components because they already exist on the BMS. Each battery is than equipped with only the extra components for system level balancing and there is no limited amount of batteries which can be balanced.

The system balancer prototype makes use of the STM32L072 microcontroller [32]. This microcontroller has been chosen because it offers several timer pins which are suitable to use for the Pulse Width Modulation (PWM) signal for the buck/boost converter balancer. Also, it offers a 12 -bit resolution Analog Digital Converter (ADC) which is sufficient for a current read out over a shunt resistor. The board is equipped with Serial Wire Debug (SWD) pins for programming, voltage measurement for both of the batteries, a 12 V power supply and a 3.3 V power supply. A 12 V Low Drop-Out (LDO) regulator is used which converts the 24 V of the combined batteries into 12 V . It has been chosen to convert the 24 V of both batteries instead of using the 12 V of a single battery so both batteries will be drained equally. From the 12 V bus, a 3.3 V LDO is used to create the voltage supply for the microcontroller. Each LDO is equipped with a status Light Emitting Diodes (LED) in order to indicate if the power supply is properly functioning.

The two switches are controlled with a half-bridge driver which is powered with the 12 V supply. Because now only two batteries are balanced, only one balancer block is needed, which consist of two MOSFETs and a single inductor. The LM5108 [33] has been chosen as half-bridge driver because it has the ability to individually control the switches, meaning that they do not have to be switched complementary. Also, it has shoot-through protection so it is never possible to have both MOSFETs on at the same time. This is an important safety measure because if this were the case, a short circuit occurs between the two batteries. It is acknowledged that a bootstrap circuit might not be the most suitable for all applications. Namely in applications where the upper switch is always meant to be on, but the lower switch does not have this problem. Considering that the choice is free to balance from one battery to the other or vice versa the bootstrap circuit should not give problems for the prototype testing. By choosing to balance from the lower battery to the upper battery, only the lower switch needs to be toggled and the desired tests can be performed. For the prototype this is a good and simple solution, in the final design different drivers have to be used. Schematic of the balancing part of the prototype can be seen in figure 20, the full schematic can be found in appendix B.

Currents with a peak up to 10 A will be switched at a frequency of about 80 kHz . In order to minimize Electromagnetic Compatibility (EMC) problems and not have these switching currents over the long cables connecting to the batteries, a Pi filter is placed at the battery connections point on the Printed Circuit Board (PCB). This way, the high-frequency currents are provided by the capacitors rather than directly form the batteries. In figure 20, the inductors L1, L2 and L4 have a higher complex impedance than the capacitors C25,26,29,30,31,32,27,28, making sure that the Alternating Currents (AC) are extracted from the capacitors.

Two shunt resistors are placed in-line with the switches Q1 and Q2, one for the upper side and one for the lower side. The INA240 Bidirectional Current sense amplifier is used to determine the current. The output of the INA240 is half of the operating voltage when no current is flowing through the shunt resistor and thus no differential input is supplied to the amplifier. The operating voltage is 3.3 V which means that the range in both directions is 1.65 V . Currents from 100 mA need to be sensed and maximum currents are expected to be 10 A . If the gain is set to 100 and the shunt resistor has a value of $1.5 \mathrm{~m} \Omega$ this means the voltage deviation will be between 15 mV and 1.5 V as can be seen in equations 13 and 14.

Voltage deviation [V]: $\quad I * R_{\text {sense }} *$ gain $=0.1 * 0.0015 * 100=15 \mathrm{mV}$
Voltage deviation [V]: $\quad I * R_{\text {sense }} *$ gain $=10 * 0.0015 * 100=1.5 \mathrm{~V}$

A 12-bit ADC provides a resolution of $0.8 \mathrm{mV} / \mathrm{bit}$ so with the chosen circuit parameters it is possible to detect all the currents desired to be monitored.

The results from the MATLAB model showed that $R_{D S_{o n}}, \mathrm{t}_{\text {Rise }}, \mathrm{t}_{\text {Fall }}$ and $\mathrm{Q}_{\mathrm{rr}}$ are important MOSFET parameter when it comes to minimizing the losses. Resulting in the choice for the Texas Instruments CSD18510Q5B N-Channel MOSFET. From the available components at the selected supplier it scored the best on the abovementioned criteria. The only downside is that the body diode has a large $\mathrm{V}_{\mathrm{F}}$ of 0.8 V . And this voltage drop determines largely the efficiency of the balancer. Therefore the choice has been made to place an extra Schottky diode in parallel with the body diode, RBR20BM40AFHTL [34] diode is used for this.

Other features of the prototype:

- 10 A fuses at the battery input terminals
- RX and TX pins for serial communication
- I2C communication header
- 4 x additional status LEDs
- Potentiometer to adjust the balancing current
- Jumper to set balancing direction
- $2 x$ jumper for additional settings
- Test points for: $12 \mathrm{~V}, 24 \mathrm{~V}$, PWM control signal and at both sides of the main inductor (L3)


Figure 20 Part of the schematic showing the buck-
boost converter system balancer

### 4.3 Board layout

The PCB consist of four copper layers: Copper_top, Copper_in1, Copper_in2 and Copper_bottom. Most traces are routed on the top and the bottom layer, this has been done intentionally to keep most of the traces accessible so they can be patched in case of an error. Copper layer in 1 and bottom contains the main ground plane, whereas layer Copper_in2 has a 3 V 3 plane. The high power flows go through the copper planes on the top layer. It is chosen to let them flow through the top layer because this provides better cooling than the inner layers because it is not enclosed. Besides that, the bottom and the top have thicker copper layers than the inner layers, therefore it has been chosen to have the high power flows go through the outer layers.

Figure 21 shows the 3D model of the board, the full PCB design can be found in appendix B. The microcontroller can be found on the left side of the board, away from the high frequency switching currents. Most tracks have a width of 0.2 mm , only several traces for the 12 V and 3.3 V power supply are thicker. All the high power paths for the balancer go through the power planes.


Figure 21 3D model of the PCB design of the system balancer

## Chapter 5

## Results and Discussion

This chapter shows the results of the modeling and simulations. It also shows the results of the prototype testing. The results are discussed and answer the research questions whether system level balancing is more beneficial than balancing on cell level for a given battery system and what efficiencies can be achieved and which parameters influence this. A case study shows what real life benefits the system level balancer can provide.

### 5.1 MATLAB results

Different input parameters have been set in the model in order to determine the significance of certain components / input values and the efficiency. The results of the model for system level balancing, where $\mathrm{VB} 1=\mathrm{VB} 2=13 \mathrm{~V}$, can be found in table 3 . The results for cell level balancing, where VB1 = $\mathrm{VB} 2=3.6 \mathrm{~V}$, can be seen in table 4 . The results show that there is a difference of more than $10 \%$ in efficiency between active balancing on system level and on cell level. Comparing the results of both tables also clearly shows the relationship between $t_{\text {off }}$ and the efficiency. With a higher efficiency (Table 3) the values of $t_{\text {on }}$ and $t_{\text {off }}$ lie closer to each other than with a lower efficiency (Table 4).

Table 3 Model input parameters for system level balancing (left) Model outputs (right)

| MODEL INPUT <br> system level | MODEL OUTPUT |
| :--- | :--- |
| $\mathrm{D}=0.3$ | $\mathrm{t}_{\mathrm{on}}=3.19 \mathrm{e}-06 \mathrm{~S}$ |
| $\mathrm{~F}=94 \mathrm{kHz}$ | $\mathrm{t}_{\text {off }}=3.07 \mathrm{e}-06 \mathrm{~S}$ |
| $\mathrm{VB} 1=\mathrm{VB} 2=13 \mathrm{~V}$ | $\mathrm{I}_{\text {peak }}=8.8 \mathrm{~A}$ |
| $\mathrm{~L}=4.7 \mathrm{e}-6 \mathrm{H}$ | Ibalance $=1.32 \mathrm{~A}$ |
| $R_{D S_{o n}}=1.8 \mathrm{e}-3$ | $c L o s s_{S 1}=0.0139 \mathrm{~W}$ |
| $\mathrm{Tr}=9 \mathrm{e}-9$ | $\operatorname{swLoss}_{S 1}=0.1934 \mathrm{~W}$ |
| $\mathrm{Tf}=3 \mathrm{e}-9$ | cLoss $_{D 2}=0.6414 \mathrm{~W}$ |
| $\mathrm{Q}=145 \mathrm{e}-9$ | LossL $=0.180 \mathrm{~W}$ |
| $\mathrm{R} 1=9.3 \mathrm{e}-3$ | TotalLosses $=1.0288 \mathrm{~W}$ |
| $\mathrm{RD}=0.001, \mathrm{~V}_{\mathrm{F}}=$ | Efficiency $\approx 94 \%$ |
| 0.5 |  |

Table 4 Model input parameters for cell level balancing (left) Model outputs (right)

| MODEL INPUT <br> cell level | MODEL OUTPUT |
| :--- | :--- |
| $\mathrm{D}=0.3$ | $\mathrm{t}_{\mathrm{on}}=3.19 \mathrm{e}-06 \mathrm{~S}$ |
| $\mathrm{~F}=94 \mathrm{kHz}$ | $\mathrm{t}_{\text {off }}=2.80 \mathrm{e}-06 \mathrm{~S}$ |
| $\mathrm{VB} 1=\mathrm{VB} 2=3.6 \mathrm{~V}$ | $\mathrm{I}_{\text {peak }}=2.44 \mathrm{~A}$ |
| $\mathrm{~L}=4.7 \mathrm{e}-6 \mathrm{H}$ | Ibalance $=0.37 \mathrm{~A}$ |
| $R_{D S_{o n}}=1.8 \mathrm{e}-3$ | cLoss $_{S 1}=0.0011 \mathrm{~W}$ |
| $\mathrm{Tr}=9 \mathrm{e}-9$ | $\operatorname{swLoss}_{S 1}=0.0503 \mathrm{~W}$ |
| $\mathrm{Tf}=3 \mathrm{e}-9$ | $\operatorname{cLoss}_{D 2}=0.1609 \mathrm{~W}$ |
| $\mathrm{Q} \mathrm{Qr}=145 \mathrm{e}-9$ | LossL$=0.043 \mathrm{~W}$ |
| $\mathrm{Rl}=9.3 \mathrm{e}-3$ | TotalLosses $=0.2550 \mathrm{~W}$ |
| $\mathrm{RD}=0.001, \mathrm{~V}_{\mathrm{F}}=$ <br> 0.5 | Efficiency $\approx 80 \%$ |

The results in table 3 give an approach of what the efficiency of the system level active balancer can be. However, this model does not take into account cable losses, parasitic behavior of the battery and other possible losses, so the actual efficiency will be lower. Other limitations to the model are that not all parameters that affect efficiency are taken into account. The rise and fall times of the switch are not taking into account, they have been taking into account by calculating the switching loss but the current is assumed to instantly have a free path as the switch is turned on. Also parameters like junction temperature are not taken into account and are presumed to be constant.

By observing the individual losses of the system compared to the total loss it is clear that the conduction losses of the diode is the most significant. This is because of the voltage drop over diode which causes the biggest losses in the system. Considering the small influence of the resistive losses, a simplified version of the model has been made, taking only into account the significant losses and approaching it as a linear system. This gives an approximated but fast approach of the efficiency of the system. The following equations describe the simplified model.

Efficiency [\%]:

$$
\begin{equation*}
\text { Efficiency }=\frac{P_{\text {out }}}{P_{\text {in }}}=\frac{V B 2 * \frac{t_{\text {off }} I_{\text {I }}}{2}}{V B 1 * \frac{t_{\text {on }}^{*} I_{P E A K}}{2}} \tag{15}
\end{equation*}
$$

Where

Peak current [A]:

$$
\begin{equation*}
I_{P E A K}=\frac{V B 1}{L} * D * T s \tag{16}
\end{equation*}
$$

Time off [s]:

$$
\begin{equation*}
t_{o f f}=t_{o n} * \frac{V B 1}{V B 2+V f} \tag{17}
\end{equation*}
$$

Substitution gives:
Efficiency [\%]:

$$
\begin{equation*}
\text { Efficiency }=\frac{V B 2}{V B 2+V f}=\frac{V B 2}{V B 1} * \frac{T_{o f f}}{T_{o n}} \tag{18}
\end{equation*}
$$

Efficiency system level [\%]: $\quad$ Efficiency SystemLevel $=\frac{13}{13+0.5}=96.3 \%$
Efficiency cell level [\%]: $\quad$ Efficiency $y_{\text {CellLevel }}=\frac{3.6}{3.6+0.5}=87 \%$
Equation 18 shows that the influence of the diode is measured with respect to VB2. When VB2 becomes smaller the system will be less efficient. This proves that the chosen topology is more efficient for system level balancing than for cell level balancing because of the differences in voltage levels. Also both efficiencies are now higher, this is because equation 18 does not take all the losses into account and therefore the efficiency appears to be slightly higher than in the MATLAB results. Filling in equation 18 shows an efficiency of $96.3 \%$ for system level balancing and $87 \%$ for cell level balancing.

Rewriting the equation shows that the ratio between $t_{\text {on }}$ and $t_{\text {off }}$ also provide information about the efficiency of the system. This is a handy characteristic because it are measurable values which will make it easier to validate the efficiency of the prototype.

### 5.2 Simulink results

The results of three switching schemes mentioned in chapter 3.2 , table 2 can be seen in figures 22 a , 22 b and 22c. The initial SoC of all battery modules have been set to $80 \%$, this way it is clear to see which battery increases and which one decreases. It also proves that the chosen method works independently of SoC or open circuit voltage and this shows that it is possible to balance in the flat region of LFP batteries.


Figure 22a VB3 (green) is charged with VB1 (red) VB2 (Blue) and VB4 (pink) stay the same


Figure 22b VB2 (blue) and VB4 (pink) are charged from both VB1 (red) and VB3 (green)


Figure 22c VB2 (blue) is double charged from both VB1 (red) and VB3 (green), VB4 (pink) stays the same

Also the amount of charge to be transported can be adjusted, which can be done by tuning the duty cycle. When a higher duty cycle (up to maximum 50\%) is used, more charge is redistributed and with a lower duty cycle less is redistributed. Figure 23a clearly illustrates this result. The control signal corresponding with VB1 and VB2 is set to $30 \%$ whereas the control signal corresponding with VB3


Figure 23a VB3 (green) charging VB4 (pink) with duty cycle of $30 \%$. VB1 (red) charging VB2 (blue) with duty cycle of $50 \%$


Figure 23b All batteries starting at a different SoC being balanced towards the same SoC.
and VB4 is set to $50 \%$. Figure 23b demonstrates how batteries with different SoC can be balanced towards each other. But it also shows that the balancing process continues even after the batteries are in balance. This is because this topology does not balance itself, unlike other methods which balance autonomously based on voltage levels. It is therefore important to keep track of the current SoC of all batteries and adjust the balancing process based on that status. When all the batteries are in balance all the switches should be turned off in order to stop the balancing process.

The simulations above show the flexibility of the balancer topology to shift around the charges in all different configurations. Next, more results will be shown of the efficiency.

The efficiency of the system is validated again with the Simulink model. This is because the MATLAB model does not take into account parasitic behaviour of the battery and other losses like cable losses. The simulation does take into account ohmic losses due to cables, connectors etc. These losses are estimated and represented ohmic loss resistors, since they are estimated the real life losses may still be different. Also the model does take into account certain aspects of the battery like internal resistance and the non-linear voltage vs SoC curve so it gives more realistic insight into the efficiency of the system. The setup can be seen in appendix A, only two batteries are used in this example. The current coming out of VB1 is measured, integrated over time and multiplied with the voltage of battery VB1, this is the energy input of the system. Subsequently, the current going in VB2 is measured and multiplied with the voltage of VB2 and then also integrated over time, this is the energy input. The output is divided by the input and multiplied by $100 \%$ in order to obtain the efficiency of the system. The results can be seen in table 5, showing that the efficiency is now $87.73 \%$ for system level balancing, which is lower than the efficiency in the MATLAB model as was expected. The same test is executed with two battery cells instead of whole batteries in order to show the difference. The efficiency for cell level balancing is $83.67 \%$ which is also lower than the MATLAB efficiency for cell level balancing. It must be noted that the results of the efficiency between system and cell level balancing differ less from each other in the Simulink model than in the MATLAB model. This could be because the voltage drop over the diode is dominant in the MATLAB model and this has more impact on the cell level balancer then on the system level balancer. Whereas in the Simulink model, other (parasitic) losses also play an important role in the total efficiency which affect both balancers more equally. Besides that, the ohmic resistances are lower in the cell level balancer because the cells are positioned closer to each other than the whole batteries which allows for shorter connections and thus, less ohmic resistances.

Table 5 Simulink results system level balancing
efficiency and cell level balancing efficiency

| Balancing type | Efficiency [\%] |
| :---: | :---: |
| System level | 87.73 |
| Cell level | 83.67 |

### 5.3 Prototype testing

The main goal of the prototype testing is to validate the core functioning of the balancing topology. Namely, the ability to move charge between two batteries independent of their voltage levels. Additional, a rough estimate will be given about the efficiency of the prototype but in order to get more exact results on the efficiency further testing is required.

The PCB was partly assembled upon delivery so the first step was to complete the assembly. The fully assembled PCB can be seen in figure 24.


Figure 24 Fully asembled system level active balancer PCB

### 5.3.1 Test plan

The test plan is set up in order to make the testing process run smoothly. It can be divided into multiple sections: Optical inspection and power levels testing, software testing and hardware testing.

## Optical inspection and \& power levels testing

First the board will be optically inspected in order to see if all the components are assembled properly and if no visible shorts can be detected. After that the board will be supplied with a voltage source with current limiting in order to test if the right voltages are present on the board and to see if there are no shorts or undesired opens.

## Software testing

The test plan for the software focuses first on being able to communicate with the microcontroller, the blink LED program will be uploaded and it can be confirmed with the onboard user LEDs. Once the communication is confirmed by the blink LED, the timers and PWM will be tested. The PWM input signal for the half bridge driver is available on one of the header pins so it is easy to see with an oscilloscope if the PWM signal is functioning correctly. It will be verified if the PWM signal has the right frequency and duty cycle.

## Hardware test plan

The most interesting part is the hardware testing. Here the actual movement of charge between two batteries will be tested. Two Nomada 12 V 105 Ah batteries are connected in series, they will first be connected to the board without using the switches. Just to confirm that all voltage levels are correct and no shorts exist. They are charged such that their voltages are equal. Then the PWM signal, with first a duty cycle of $10 \%$, is applied to the driver and the switches are activated, charge should now be transported from one battery to the other. In order to confirm this, Super B's Be in charge software will be used for this, it can read out all the statistics of the battery, including the incoming or outgoing current. Once the functioning is confirmed the duty cycle will be increased to $15 \%, 20 \%$ and $30 \%$. The currents will be monitored and a thermal camera is used to check in nothing will get too hot. With the duty cycle at $30 \%$ the currents will be the highest, this makes it easier to perform additional measurements on the prototype. The on-board shunt resistor will be measured to approximate the currents and also an estimate of the $\mathrm{t}_{\mathrm{on}}$ and $\mathrm{t}_{\text {off }}$ can be extracted from this, giving insight into the efficiency of the balancer. At last, the Pi filter will be tested, because the balancer will have high
switching currents up to 10 A with a frequency of about 80 kHz which will cause EMC problems if these are extracted directly from the battery. The filter will be tested by means of looking at the waveform of the outcoming current of one battery, to see if this is indeed the average balancing current and by looking at its ripple.

### 5.3.2 Setup

For the hardware testing the two batteries, referred to as Nomada 034 and Nomada 035, both have a battery voltage of 13.0 V . They are connected in series and both of them are protected with an extra 7.5 An in-line fuse. The PCB also contains two fuses right at the battery connectors but the in-line fuses are added as an extra safety measure to have the fuses as close to the battery as possible. Additionally, the battery terminals are taped with isolation tape to prevent accidental shorts. Of course also safety glasses and safety shoes are worn during the testing. The full setup can be seen in figure 25.


Figure 25 Showing the test setup with the prototype board, batteries and software monitoring
For the PWM signal the 16 -bit Timer 2 of the STM32 is used. It is configured with Prescaler value 0 (this value has a hidden +1 ), this generates a PWM signal with a frequency of 94 kHz . The Period value is 255 and the Pulse value is varied in order to generate the desired duty cycle, table 6 shows the pulse values with its corresponding duty cycle value.

Table 6 Varying pulse values with
their corresponding duty cycle

| Pulse | Duty cycle [\%] |
| :--- | :--- |
| 25 | 10 |
| 38 | 15 |
| 50 | 20 |
| 75 | 30 |

With the duty cycle set to $30 \%$ additional measurements will be executed. Therefore the MATLAB model is used to predict what the values for the (average) current, $\mathrm{t}_{\mathrm{on}}$ and $\mathrm{t}_{\text {off }}$ will be. The input values of the model can be seen in table 7 those are the exact variables that are applicable to the prototype. The output variables of the model can be seen in table 8 , they will later on be compared with the measured results to see if they align.

Table 7 Input parameters of MATLAB model corresponding with prototype parameters

| Input variable | Value |
| :--- | :--- |
| $\mathrm{VB} 1=\mathrm{VB} 2$ | 13.0 V |
| L | 4.7 uH |
| Frequency | 94 kHz |
| Duty cycle | 0.3 |
| $\mathrm{~V}_{\mathrm{F}}$ | 0.5 V |

Table 8 Output paramers of MATLAB model

| Output parameter | Value |
| :--- | :--- |
| $\mathrm{I}_{\text {peak }}$ | 8.8 A |
| $\mathrm{I}_{\text {balance }}$ (average current) | 1.32 A |
| $\mathrm{t}_{\text {on }}$ (switch conducting) | 3.19 us |
| $\mathrm{t}_{\text {off }}$ (diode conducting) | 3.07 us |

### 5.3.3 Measurement results

First the PWM signal is checked to see if it is indeed 94 kHz and if the duty cycle is correct. This is an important step because a wrong frequency, for example 1 kHz , leads to a higher $\mathrm{t}_{\mathrm{on}}$ time resulting $\mathrm{I}_{\text {peak }}$ to increase up to undesired high values. The duty cycle is first set to $30 \%$ the result can be seen in figure 26 . Then the duty cycle is set to $10 \%$ and the voltage over the inductor is measured as can be seen in figure 27.


Figure 26 PWM signal showing a duty cycle of $30 \%$ with frequency of 94 KHz


Figure 27 Showing first positive 13 V over the main inductor, consecutively negative 13 V

Figure 26 shows that the control signal is correct, debugging results of the control signal can be found in appendix B. Figure 27 shows that the switching scheme also works properly. Providing first a positive 13 V over the inductor, consecutively negative 13 V over the inductor. It is clear that there is still ringing of the inductor current. When the inductor current of a converter in DCM falls to zero this phenomenon occurs. The current ringing can be a source of additional losses and electromagnetic interferences and is therefore an undesired effect [36]. The RC snubber, which is present on the board, should reduce the current ringing. For the prototype the parameters of the snubber have been estimated. However, the best way to determine the snubber parameters is by executing oscillation frequency measurements and based on that derive the correct values to cancel the current ringing. This has not been done for the prototype and therefore not all the current ringing is supressed.

The results of the charge exchange from Nomada - 035 (N-035) to Nomada - 034 (N-034) with a duty cycle of $30 \%$ can be seen in figure 27 a and 27 b Here it clearly shows that the battery current from N035 is negative $(-1.5 \mathrm{~A})$ and $\mathrm{N}-034$ has a positive $(0,9 \mathrm{~A})$ battery current. Meaning that battery $\mathrm{N}-035$ is charging battery $\mathrm{N}-034$, this proves the core functioning of the prototype. Note that both currents differ in magnitude. This does not necessary all have to refer to losses in the system, it can also be caused by unprecise current measurement. Because the internal current measurement of the battery is designed to measure high currents, in the range up to hundreds of Amperes, and not in the range of hundreds of mA , which makes it unprecise with low currents. This is also why the Be in charge software could not provide battery current results for the test with a duty cycle of $10 \%$ because the current was too low for the battery to detect. Figure 28 shows the results of the thermal camera. The components that heat up the most are the 12 V LDO (which was expected) and the RC snubber circuit (which was not expected). The components that have been chosen for the RC snubber are of size 0805 which, afterwards, turned out to be too small. An improvement for a next design is to use bigger components for the snubber which easily solves this problem. There were further no alarming thermal


Figure 27a Showing outgoing current of 1.5 A from Nomada 034


Figure 27b Showing incoming current of 0.9 A from Nomada 035


Figure 28 Thermal camera showing temperature increase at snubber
measurements detected. The test was executed with the duty cycle set to $30 \%$ the results with duty cycle $15 \%$ and $20 \%$ can be found in Appendix B.

After the core functioning of the topology had been verified the currents were measured. This has been done by measuring the voltage over the $1.5 \mathrm{~m} \Omega$ shunt resistor at the discharging battery side. The measurements have been taken whilst the duty cycle was set to $30 \%$ so the results can be compared with the MATLAB output values in table 8. The results of the measurements can be seen in figure 29a and 29b.


Figure 29a Voltage measurement over $1.5 \mathrm{~m} \Omega$ resistance, showing a peak of 12.0 mV


Figure 29b Voltage measurement over $1.5 \mathrm{~m} \Omega$ resistance, showing a peak of 13.6 mV (Same measurement but zoomed out view)

The signals were rather noisy so extracting precise data from it was challenging. Both figures show the results of the same setup but multiple measurements have been taken because of the noisy signal. Additional measurements have shown results comparable with Figure 29a and 29b. The results of the voltage measurement and the corresponding currents can be seen in table 9. Figure 29a shows a voltage of 12.0 mV over the $1.5 \mathrm{~m} \Omega$ resistor which results in an inductor peak current of 8 A , figure 29 b shows a voltage of 13.6 mV which results in an $\mathrm{I}_{\text {peak }}$ of 9.1 A . According to the MATLAB model $\mathrm{I}_{\text {peak }}$ should be 8.8 A so the measurements show the currents as expected.

Table 9 measured peak voltage and corresponding outcoming peak currents

| Peak voltage measurement | Corresponding $\mathrm{I}_{\text {peak }}$ |
| :--- | :--- |
| 12.0 mV | 8 A |
| 13.6 mV | 9.1 A |

Next, $\mathrm{t}_{\mathrm{on}}$ and $\mathrm{t}_{\mathrm{off}}$ are measured. This is done by looking at the time where the inductor current is rising ( $\mathrm{t}_{\text {on }}$ ) and the time where the inductor current is falling ( $\mathrm{t}_{\text {off }}$ ). Two shunt resistors are on the PCB and they are measured separately, the combined result can be seen in figure 30a and 30b as the purple Math signal. The cursor in figure 30a shows a $\mathrm{t}_{\mathrm{on}}$ time of 3.12 us, figure 30b show a toff time of 2.24 us.


Figure 30a Green / pink showing the inverse voltage of the high side shunt, yellow showing the voltage over the low side shunt. Purple showing combined signal, representing the inductor current. Cursor shows $t_{o n}$


Figure 30b Green / pink showing the inverse voltage of the high side shunt, yellow showing the voltage over the low side shunt. Purple showing combined signal, representing the inductor current. Cursor shows toff

Using equation 18 gives a rough estimate of the efficiency. To gain more exact results of the efficiency additional and more precise testing is required.

Prototype efficiency [\%] $=\frac{13.0}{13.0} * \frac{2.24 u s}{3.12 u s} \approx 72 \%$ efficiency
At last the current filter is tested, it is also tested with the duty cycle at $30 \%$. The Pi filter should provide the AC currents for the converter, instead of pulling them directly from the battery. When the filter works properly only the DC average balancing current should be extracted as a constant current from the battery. To perform the measurement a $1 \Omega$ resistor is placed in series with the discharging battery, and the voltage over it is measured in order to determine the outgoing current, the setup can be seen in appendix B. First the oscilloscope is set to AC coupling to see the current ripple, the result can be seen in figure 31 .


Figure 31 Green line showing the battery current with a current ripple of 31.2 mA peak to peak. Other lines are irrelevant


Figure 32 Yello line showing the 1.32 A DC current drawn from the battery. Minor noice at the left side of the signal is visable.

The current ripple (the green sinusoidal waveform) can be read of from the cursor points and is 31.2 mV peak to peak. Because it is measured over a $1 \Omega$ resistor the current ripple is 31.2 mA peak to peak which is a good result, considering that the switching current has peaks up to 8.8 A . Now switching to DC coupling, the result can be seen in figure 32. According to the MATLAB results (table 8 ) the average current, and thus the balancing current, should be 1.32 A . The cursors in figure 32 show that that the outcoming current of the battery is indeed exactly 1.32 A . This means that the results show that the filter is functioning correctly.

Table 10 shows the results of all the output values according to the MATLAB model versus the values measured on the prototype board.

Table 10 Output variables of MATLAB model

| Parameter | MATLAB | Measurement |
| :--- | :--- | :--- |
| $\mathrm{I}_{\text {peak }}$ | 8.8 A | 8.6 A |
| Ibalance (average current) | 1.32 A | 1.32 A |
| $\mathrm{t}_{\text {on }}$ (switch conducting) | 3.19 us | 3.12 us |
| $\mathrm{t}_{\text {off }}$ (diode conducting) | 3.07 us | 2.24 us |
| Efficiency | $94 \%$ | $72 \%$ |
| Current ripple | - | 31.2 mA peak to peak |

### 5.4 Case study

This chapter provides insight in the benefits of the active system balancer if it were to be implemented in real life. Two case studies explain the advantages that can be gained.

### 5.4.1 Case study 1

A case study of a fully electric passenger canal cruise boat supplied with Nomia $12 \mathrm{~V}, 340 \mathrm{Ah}$ batteries. The total system consist of a 162 kWh battery system. From interviews with the company Super B it became clear that an imbalance of about $1 \%$ to $3 \%$ arises between the batteries over one month of time. So the imbalance increases over time and it will also get worse as the batteries get older. The assumption has been made that the average imbalance is $2 \%$, this means that after one month the imbalance is:

Imbalance [Wh]: $\quad 162000 * 0.02=3240 \mathrm{~Wh}$
If this imbalance is brought back in balance again with the passive balancers this would mean that all the excess energy would be thrown away. It is directly converted into heat and 11664 kJ of energy is released. All this energy is released in a small area inside the battery which causes the temperature to increase.

When the batteries are brought back in to balance with the active system level balancer there will be advantages on the efficiency of the system. With the results shown in chapter 5.3 the efficiency can reach $72 \%$, and this could be even higher if the balancer is improved. $72 \%$ of the excess energy would now be reused rather than thrown away.

Redistributed energy [Wh]: $\quad 3240 * 0.72=2332.8 \mathrm{~Wh}$
Meaning that more than 2.3 kWh can be saved and this is already in the range of capacity of one battery. So by active balancing instead of passive balancing almost the same usable battery capacity can be approached but with one battery less. One Nomia battery has a selling price of around $€ 4500$ [35] so it can lead to savings of initial system cost. It will become even more beneficial over time, because as the batteries grow older even larger imbalances will occur and thus the amount of energy that can be saved will be bigger. Figure 33 shows that with lower efficiencies energy still can be saved, it also shows that if the efficiency of the balancer is improved even more energy can be saved. Saving energy and begin able to have more useable battery capacity with the same amount of batteries also means saving weight. For example, in campervans this can be an important aspect because it is challenging to keep them under the 3500 kg weigh limit. So saving weight is also an important asset. Additionally, in electronic transportation where less weight means less energy required for the transport.

The Nomia 340 battery weights 33 kg , converting this into capacity per kg means $123 \mathrm{~Wh} / \mathrm{kg}$. Figure 34 shows the weight that can be saved over a efficiency range between $60 \%$ and $100 \%$.


Figure 33 Energy that can be saved over a range of efficiencies between $60 \%$ and $100 \%$


Figure 34 Weight that can be saved over a range of efficiencies between $60 \%$ and $100 \%$

Besides the advantages of gained efficiency, less heat production and saved weight there is also the advantage of the faster balancing with active balancing methods. For active balancing it is theoretically possible to balance with way higher balancing currents because of the higher efficiency which causes less heat to be generated. But, increasing the balancing current can also influence the losses. So if it is not necessary to balance with high currents it is desirable to still balance with lower balancing current. At the current situation with passive balancing, everything is balanced at the end of charge, meaning that sometimes high balancing currents are required. Case study 2 provides more insight in the gained balancing time.

### 5.4.1 Case study 2

In order to perform calculations on gained balancing time a fictive case will be studied. The situation consist of two $12 \mathrm{~V}, 340$ Ah batteries in series. They are situated in a campervan (or any other recreational vehicle or boat which is only used seasonally). The batteries are of mid-age so the imbalance that grows each month is $2 \%$. After seven months of not being used in the winter period the imbalance between the two batteries can grow to be $14 \%$, meaning a charge difference of 47.6 Ah. It is desired to balance the batteries as fast as possible. The maximum balancing current of the passive balancers on the BMS is 1.5 A . The active balancer can easily pump the balancing current up to 3 A , this can be even higher if right components are chosen for this.

Passive balancing (all the imbalance needs to be removed):

$$
\text { Balancing time }[\mathrm{h}]: \quad \quad \frac{\text { Imbalance }[\mathrm{Ah}]}{\text { Balancing current }[A]}=\frac{47.6}{1.5}=31.7 \text { hours }
$$

Active balancing ( $50 \%$ of the imbalance needs to be redistributed):
Balancing time $[\mathrm{h}]$ :

$$
\frac{\text { Imbalance }[\mathrm{Ah}]}{\text { Balancing current }[\mathrm{A}]}=\frac{23.8}{3}=7.9 \mathrm{hours}
$$

The results of both case studies have been combined in table 11, it clearly shows the advantages of active balancing on multiple aspects, assuming an efficiency for the active system level balancer of $72 \%$ and an imbalance of $2 \%$ per month.

Table 11 Comparing case study results of active balancing and passive balancing

|  | Passive | Active |
| :--- | :--- | :--- |
| Losses | 3240 Wh | 907.2 Wh |
| Heat | 11664 kJ | 3266 kJ |
| Weight | +26.3 kg | +7.37 kg |
| Time | 31.7 h | 7.9 h |

### 5.5 Cost estimation

The benefits of the active system level balancer become clear in chapter 5.4 but it also comes with disadvantages. The main disadvantages are the additional costs of the system. The Bill of Materials (BoM) of the prototype gives an idea of what the extra costs would be. Because the prototype is designed as a standalone system it consist many more components than would be necessary if the balancer is implemented on the existing BMS. Therefore a reduced BoM can be seen in table 12 which only shows the necessary components for the balancing process. Also an estimation of the extra board costs has been made. Merely the board had a price of $€ 6$ per piece, it is estimated that by implementing the balancer on the existing BMS only a fraction of the board will be larger or maybe this is not even necessary / possible considering that the board is situated inside the battery with limited space. The extra board costs are estimated as $€ 1$ and the additional required connector and cable are also estimated to be $€ 1$. The extra costs for the components can be seen in table 12 .

Table 12 Reduced BoM of system level active balancer prototype

| Comment | Designator | Quantity | Total price [ $¢$ ] |
| :---: | :---: | :---: | :---: |
| All resistors |  | 11 | 0.37 |
| All capacitors |  | 16 | 0.61 |
|  |  |  |  |
| Filter inductor | L4,L2,L1 | 3 | 1.75 |
| Main inductor | L3 | 1 | 0.93 |
|  |  |  |  |
| Status LED | D5,D2 | 2 | 0.34 |
| Balancer Diode | D4,D3 | 2 | 1.88 |
| MOSFET | Q2,Q1 | 2 | 4.55 |
| MOSFET <br> Driver | U4 | 1 | 0.91 |
|  |  |  |  |
| Extra board cost |  | Estimated price | 1 |
| Extra Cable 20 cm |  | Estimated price | 0.2 |
| Extra Connector |  | Estimated price | 0.8 |
|  |  | Total price [€] | 13.34 |


| Qty. | Unit Price | Ext. Price |
| :--- | :--- | :--- |
| $1+$ | US\$2.4469 | US\$ 2.45 |
| $10+$ | US\$2.1319 | US\$ 21.32 |
| $30+$ | US\$1.9346 | US\$ 58.04 |
| $100+$ | US\$1.7325 | US\$ 173.25 |
| $500+$ | US\$1.6419 | US\$ 820.95 |
| $1000+$ | US\$1.6021 | US\$ 1602.10 |

Figure 35 Different component prices for orders of different quantities

The table shows a strongly reduced BoM. This is because of the many functionalities that are already present on the current BMS. Fuses are already present, coulomb counting for current measurement is already happening as well as the microcontroller and power supply which are also already there. It is therefore not necessary to count these components as additional cost because they already exist. As can be seen, the total extra component costs would now be $€ 13.34$ in order to implement the active balancer on the existing BMS. But these prices are overestimated and can significantly be reduced. When designing the prototype, costs were not an issue so no attention has been paid to the prices of certain components. If the balancer were to be really implemented, cheaper components could be chosen to reduce the costs. Also there are now only five prototype PCBs ordered. In figure 35 it can be seen that the component price per piece is significantly higher than the price for more than 1000 pieces (which is more than $35 \%$ cheaper). Since the batteries are produced in large amounts it is possible to buy large amounts of each component which will decrease the price. Assuming that the proposed measures are taking, it is expected that the total price can drop down about $45 \%$, which would mean that the extra components cost would now only be $€ 7.34$. Note that the additional engineering costs have not been taking into account, because for the scope of this research it is not possible to provide a realistic approximation for this.

When this active balancing method would be applied to cell level balancing the additional cable and extra connector would not be necessary, saving $€ 1$. However there would be the need for a balancer block between all of the cells, so three balancer blocks are necessary to balance the four cells connected in series. And even though the components can be lower power components it would still be more expensive than the system level balancer. Assuming that the components would be an additional $10 \%$ cheaper than the system level balancer because of the lower voltage ratings, this gives:

Cell level additional costs $[€]: \quad((€ 13.34-€ 1) * 0.45) * 3=€ 16.66$
The calculation above shows that cell level balancing would cost an additional $€ 16.66$ per battery whereas for the system level balancer it would only cost an additional $€ 7.34$ per battery. This, amongst the efficiency differences answers the question if system level balancing is more beneficial than cell level balancing for the chosen topology.

## Chapter 6

## Conclusion

This research aimed to find a suitable method for actively balancing LFP batteries on system level, so in series connected battery packs $(12 \mathrm{~V})$ rather than in series connected battery cells ( 3.6 V ). The researched mainly focused on whether active balancing on system level is beneficial or not and what the possible advantages can be. An important topic throughout the study is that the balancer should be able to balance within the flat voltage region of LFP batteries.

The research questions have been answered as follows:
In which situations is active balancing desired and what are the advantages?
The research shows that active battery balancing can have major advantages over passive balancing and that it is an asset in different applications. Especially in situations where energy is scare and it is desired to have to optimal usable battery capacity. It also counts for situations where weight limits are critical like in spacecraft or airplanes. Also in electronic transportation active balancing can be an improvement because of reduced balancing times and less battery weight due to higher efficiencies.

What are the trade-offs involved in the implementation of various active balancing techniques for system level balancing and which technique is most suitable for this research?
Various active system level balancing techniques have been researched and the buck-boost converter based topology showed to be the best for this study. It has been chosen based on its good scores on modularity, economically feasibility and its ease of integration.

## What are the efficiencies that can be achieved, and what are the parameters that influence the efficiency?

Results of MATLAB models, simulations and prototype measurements showed that it is possible with the buck-boost converter topology to move charge between two batteries regardless of their voltage levels. It showed flexibility of transporting charges in various directions and the balancing currents for this could be controlled by adjusting the duty cycle, providing full control over the balancing process. The results throughout the research indicate that the efficiency lies in the range between $72 \%$ and $94 \%$. The study did not provide an exact efficiency of the balancer, additional measurements would be needed for this. The most significant loss in the system was caused by the voltage drop over diode, conducting during $\mathrm{t}_{\text {off. }}$.

Is system level balancing more beneficial than balancing on cell level for a given battery system? The impact of the voltage drop over the diode is measured with respect to the voltages of the batteries. The higher the battery voltage, the lower the significance of the loss of the diode will be, meaning that the buck-boost active balancer is more efficient for system level balancing than for cell level balancing. Besides, only one balancer block is required inside each battery if it were balanced on system level whereas for cell level balancing, a balancing block is required between all cells in the series string. For a 12 V battery this would mean 3 balancer blocks inside each battery. This also makes the balancer more financially attractive for system level balancing than for cell level balancing.

All results combined show many useful assets for implementing the system level balancer. The balancing time can be strongly reduced, down to $75 \%$. The total system efficiency is increased, less heat is produced during the balancing process and weight can be saved on the battery system. To implement the balancer only one additional cable for each battery is required, combined with a few additional components which can be implemented on the existing BMS.

## Chapter 7

## Future recommendations

The study on the active system level balancer looks promising, but additional measurements are required to obtain more accurate efficiency results. It should be further investigated what the realistic efficiencies of the system are and how this can be further improved.

As already suggested, it would be more efficient if the second switch of the converter is conducting during $\mathrm{t}_{\text {off }}$ rather than let the diode, which is known to be the source of the biggest losses in the system, conduct all the current. The first step in improving the efficiency would be to further research the options on how to implement this smarter switching scheme. Considering that the loss of the diode is measured relative to the battery voltage, it should also be researched if the balancer topology can provide increased efficiency results on batteries with even higher voltages.

Subsequently, other opportunities of the presence of a buck-boost converter inside each battery are recommended to be investigated. If the buck-boost converter balancer can have a multipurpose function it justifies the choice to implement the topology even more.

When using a single battery, so not connected in a series string. There is no use for using the buckboost converter as an active system level balancer. However, it might be useful if it is used merely as a buck-boost converter to adjust the output voltage of the battery. Or to change the incoming charging voltage of a battery charger. The possibilities for this should be further researched. Also it could potentially be used for State of Health $(\mathrm{SoH})$ estimation of the battery. A promising method to obtain a proper SoH estimation is by the use of Electrochemical Impedance Spectroscopy (EIS). It is a powerful tool for the characterization of the batteries SoH where a small AC signal is applied to the electrochemical cell and the response is measured. Form this response a SoH estimation can be made [37]. Here the buck-boost converter can come in as an useful asset, considering that it is able to generate the small AC signal. It could potentially be a promising feature but further research is required.

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## Appendix A

Appendix A provides additional company information and extra simulation models

## A-1: Super B

As earlier discussed, this research will be executed in cooperation with the company Super B [6]. Super B develops and manufactures high-end LFP batteries. They are developed to outperform leadacid batteries on the road, on the water and off-the-grid. The batteries offer a tremendous amount of energy in a small, lightweight and maintenance-free box that is robust safe and reliable. They also offer a range of accessories which can be connected to the batteries to simply make optimal use of the LFP batteries. Their goal is to become a leading player in first-class lithium batteries. They focus on quality and serving their clients in the best possible way.

Super B offers many battery models including a range of starter batteries which are mostly used in power sports. Another battery is the Epsilon (12V) series, which comes in three options of 90Ah, 100 Ah and 150Ah and they are widely used in recreational vehicles and leisure boats. The Nomia $(12 \mathrm{~V})$ battery comes in four options of $100 \mathrm{Ah}, 160 \mathrm{Ah}, 210 \mathrm{Ah}$, and 340 Ah they are used for the same purposes as the Epsilon but they are also used in commercial vessels, industry and for energy storage systems. The last battery that is offered is the Nomada (12V) which comes as a 105 Ah edition. It is a modular battery which is mostly used as a system battery rather than a stand-alone battery. Currently all Super B batteries have passive balancing systems.
"Super B is part of the Dutch clean energy solutions conglomerate Koolen Industries. As Koolen Industries, it is our mission to enable everyone to contribute to the energy transition. By using energy from the wind or the sun. By making sure it is there, whenever you need it. By providing you with an autonomous life, independent of the grid. Or by sharing and trading energy with others that want to contribute to a better world too. " [7]

## A-2: Battery model

Full battery model used in simulations. The figure below shows the model setup for simulating one battery cell. By adjusting the values for $\mathrm{V}_{\text {nom }}, \mathrm{V}_{\text {full }}$ and $\mathrm{V}_{\text {exp }}$ the battery model can represent complete battery packs.


## A-3: Simulink efficiency test setup

The figure below shows the setup of the efficiency test in Simulink. The results are shown in Chapter 5.2


## Appendix B

Appendix B provides additional information concerning the prototype. Including full design and test results.

## B-1: Prototype schematic

The figure below shows the full schematic of the prototype.


## B-2: PCB design

Copper top



Inner layer 2


Copper bottom


## B-3: PWM signal debugging

During the hardware testing the PWM signal first showed undesired behavior as can be seen in the figure below. By mistake a 100 nF capacitance was put in the signal line, causing the unwanted behavior.


By removing the capacitor the problem was easily solved, as can be seen in the figure below.


B-4: Test results current flowing from one battery to another, with different duty cycle and thus, different balancing currents.

Duty cycle $15 \%$


Duty cycle 20\%


Duty cycle 30\%


## B-5: Test setup

Setup showing how the average outgoing current of one battery is measured over a $1 \Omega$ resistor.


## B-6: Safety measures

Photos of me, executing measurements in the lab wearing safety glasses and safety shoes.


## Appendix C

## Appendix C presents the code of full MATLAB model

```
clear, clc
%% Circuit parameters
VB1 = 13;
VB2 = 13;
L=4.7e-6;
im=3;
```

$\mathrm{D}=0.3 ; \quad$ \% Duty cycle
$\mathrm{F}=94000$; $\quad$ \% Switching frequency $[\mathrm{Hz}]$
\% Voltage battery 1 [V]
\% Voltage battery 2 [V]
\% Inductance [H]
\% Imbalance between batteries [Ah]
\% \% Component parameters (for loss calculation)

## \%MOSFET

Rds on $=5 \mathrm{e}-3$
$\mathrm{Tr}=120 \mathrm{e}-9$;
\% ON resistance MOSFET [Ohm]
Tf $=120 \mathrm{e}-9$,
OSFET rise time [s]
$\mathrm{Tf}=74 \mathrm{e}-9$;
\% MOSFET fall time [s]
Qrr = 70e-9;
\% Reverse Recovery Charge [C]
\% add inductor values
$\mathrm{Rl}=163 \mathrm{e}-3$; $\quad$ \% Inductor resistance [ohm]
$\operatorname{LossL}=0.002$;
REDEXPERT
\% Diode
$\mathrm{RD}=0.001 ; \quad$ \% Diode conduction resistance [Ohm]
Vf $=0.3$;
\% Diode forward voltage drop [V]
\% \% Model calculations
$\mathrm{Ts}=1 / \mathrm{F} ; \quad$ \% Period time [s]
ton $=\mathrm{D} * \mathrm{Ts} ; \quad$ \% ON time switch [s]
time_on = $0: 1 \mathrm{e}-9:$ Ton;
i_switch $=($ VB1/(Rds_on+Rl) $) *\left(\left(1-\exp \left(-t i m e \_o n ~ *\left(\left(\left(R d s \_o n+R 1\right) / L\right)\right)\right)\right)\right)$;
Ipeak $=$ i_switch(end);
toff $=-(\mathrm{L} /(\mathrm{RD}+\mathrm{Rl})) * \log (-\mathrm{Ipeak} /((\mathrm{VB} 2+\mathrm{Vf}) /(\mathrm{RD}+\mathrm{Rl}))+1)$;
charging
time_off = ton : 1e-9 : (ton+toff); $\quad$ \% Time the diode is conducting
time_dead $=($ ton+toff $): 1 \mathrm{e}-6: \mathrm{Ts}$;
$\mathrm{t}=0: 1 \mathrm{e}-9: \mathrm{Ts}$;
i_diode $=\operatorname{Ipeak}-((\mathrm{VB} 2+\mathrm{Vf}) /(\mathrm{RD}+\mathrm{Rl})) *((1-\exp (-($ time_off-ton $) *(((\mathrm{RD}+\mathrm{Rl}) / \mathrm{L}))))) ; \%$ Current through the diode during toff
i_dead $=0$; $\quad$ \% Current during dead time
\%plot the currents
figure(1), clf
title('Inductor current: Iswitch, Idiode, Idead_time')
hold on
plot(time_on,i_switch, 'LineWidth',3)
plot(time_off,i_diode, 'LineWidth',3)
plot(time_dead,i_dead, 'LineWidth',3)
grid on
xlabel('Time [s]'), ylabel('Current [I]')
hold off

```
Ibalance = (trapz(time_on,(i_switch)))/Ts;
    % Average balancing current, based on current
out VB1 [A]
Btime = im / Ibalance; % Balancing time given imbalnce im [h]
%% ton losses MOSFET
% Conduction loss MOSFET
IS_rms = sqrt(trapz(time_on,(i_switch .* i_switch))/(Ts)); % RMS current through MOSFET [A]
aPCloss_mos = IS_rms * IS_rms * Rds_on; %[w] % Conduction losses MOSFET [W]
% Switching loss MOSFET
I_Trise = (VB1/(Rds_on+Rl))*((1-exp(-Tr *(((Rds_on+Rl)/L))))); % This current is used to calculate the rise
time losses
I_Tfall = Ipeak; % This current is used to calculate the fall time
losses
aPSWloss_mos = (0.5*Tr*I_Trise*F*VB1)+(0.5*Tf*I_Tfall*F*VB1)+(F*Qrr*VB1); % Switching losses of MOSFET [W]
%% Diode losses
% Conduction loss Diode
Pcld = Vf * i_diode + RD * (i_diode .* i_diode); % Diode conduction loss calculation using
forward voltage and internal resistance
aPloss_diode = 1/Ts * trapz((time_off-Ton),Pcld); % Total diode conduction loss [W]
% Switching loss Diode
swloss_diode = Qrr*F; % Diode switching loss [W]
%% Total losses
aTotalLoss = aPCloss_mos + aPSWloss_mos + aPloss_diode + swloss_diode + LossL; % Total losses [W]
aPin = (trapz(time_on,(i_switch * VB1)))/Ts; % Input power [W]
aPout = aPin - aTotalLoss; % Output power [W]
aEFFICIENCY = aPout/aPin; % Efficiency calculation [%]
%% Display vlaues
disp(Ton)
disp(Toff)
disp(Ipeak)
disp(Ibalance)
disp(Btime)
disp(aPCloss_mos)
disp(aPSWloss_mos)
disp(aPloss_diode)
disp(swloss_diode)
disp(aTotalLoss)
disp(aPin)
disp(aPout)
```

