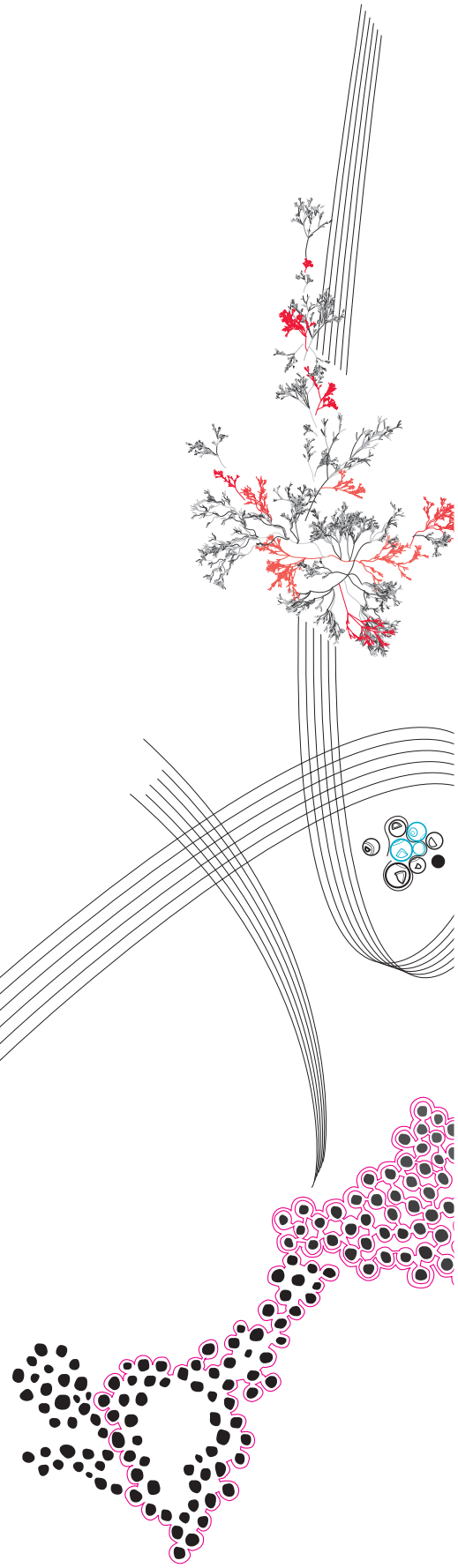


MSc Electrical Engineering
Thesis Report

Comparative Evaluation of Multilevel and Interleaved Voltage Source Inverters for Aerospace Applications

Thijmen Hoeksma

Supervisors:
prof.dr. T. Batista Soeiro
M.M. Naveed MSc

November, 2025

Department of Power Electronics
Faculty of Electrical Engineering,
Mathematics and Computer Science
University of Twente

UNIVERSITY OF TWENTE.

Contents

Abstract

The electrification of aircraft marks a pivotal advancement in the pursuit of sustainable aviation, offering substantial environmental and operational benefits. In conventional aircraft, the environmental control system is a major non-propulsive power consumer. In more electric aircraft (MEA), it is electrified using a high-speed motor compressor driven by a voltage source inverter (VSI). The VSI topology selection is a critical, multi-objective challenge as it directly dictates the system's efficiency, specific power ($\mathrm{kW\,kg^{-1}}$), power density ($\mathrm{kW\,L^{-1}}$), and total harmonic distortion (THD). However, existing topology comparisons are often inadequate, as they fail to benchmark complete systems within the unique aerospace context and its stringent DO-160G compliance requirements. This thesis addresses this gap by developing a framework to fairly compare VSI topologies at a system level to offer insight for topology selection.

Conventional and interleaved 2-level (2L) and 3-level (3L) VSI topologies are compared, including the neutral point clamped (NPC), active NPC (ANPC), and T-type variants. The framework is used for the design and selection of all critical subsystems, including all VSI components, heatsinks, and DO-160G compliant electromagnetic compatibility (EMC) filters. Interphase inductors are a key performance-defining component in interleaved topologies, so novel analytical expressions for peak and RMS circulation current were derived to inform their systematic design. This framework then evaluates the performance of each topology against the key metrics by sweeping design choices, including variations in switching frequency, number of parallel devices, and circulation current limits.

The framework was applied to a 20 kW aerospace compressor system, revealing there is no single 'best' topology. The selection depended on application priorities, particularly THD. The conventional 2L VSI was competitive in mass and volume, but its high voltage THD (76%) penalised efficiency by requiring high switching frequencies to meet low current THD. In contrast, the 3L VSI had 39% voltage THD, offering a superior trade-off by meeting THD limits at lower, more efficient switching frequencies. In particular, the T-type had the most balanced performance for this application. Interleaved VSIs consistently underperformed, as the mass, volume, and loss penalties of their interphase inductors outweighed any system-level filtering benefits.

This framework provides a reproducible method for quantitative topology benchmarking, highlighting non-obvious trade-offs and guiding aerospace inverter design.

Abbreviations

2L 2-level.

2LI 2-level interleaved.

3L 3-level.

3LI 3-level interleaved.

AC alternating current.

ANPC active neutral point clamped.

CM common-mode.

CSPI cooling system performance index.

DC direct current.

DM differential-mode.

ECS environmental control system.

EMC electromagnetic compatibility.

EMI electromagnetic interference.

ESR equivalent series resistance.

FOM figure of merit.

HV high voltage.

ISA international standard atmosphere model.

LISN line impedance stabilization network.

LV low voltage.

MEA more electric aircraft.

MPI mass performance index.

NPC neutral point clamped.

PCB printed circuit board.

PF power factor.

PWM pulse-width modulation.

RMS root mean square.

SF safety factor.

SMD surface-mounted device.

SVM space vector modulation.

THD total harmonic distortion.

VSI voltage source inverter.

Chapter 1

Introduction

In 2023, aviation accounted for 2.5% of global energy-related CO_2 emissions, and between 2000 and 2019 it grew faster than rail, road or shipping [1]. In 2019, the European Union (EU) launched the European Green Deal, which plans to make Europe climate-neutral by 2050 [2]. This has driven ambitious national targets, for example, the Dutch government mandates that by "2030 carbon emissions from aviation must be equal to 2005 levels. By 2050 they must be halved compared to 2005 levels. And by 2070 emissions must be reduced to zero [3]." However, currently aviation is not on track to meet these goals, as the efficiency improvements in aviation have not kept up with the growth and emissions are expected to grow rapidly through 2030 despite the efficiency gains [1]. To start reducing emissions, the sector must reduce emissions through operational improvements, airframe/engine efficiency, modal shifts where feasible, rapid scaling of sustainable aviation fuels, and electrification of onboard systems that provide measurable efficiency gains [1].

Aircraft in which the propulsion stays traditional but the hydraulic and pneumatic subsystems are replaced by electrically driven architectures are called MEA [4]. In conventional aircraft, the environmental control system (ECS) is a major non-propulsive power consumer [4]. In an MEA, this system is electrified using a high-speed motor compressor driven by a VSI [5]. The VSI is a key enabling component, and its design directly influences the overall system's performance and efficiency. This thesis focuses specifically on the VSIs for a 20 kW very-high-speed electric compressor for this ECS application. A simplified block diagram of the compressor system is shown in fig. 1.1. In this system, the VSI converts the direct current (DC) voltage into a three-phase alternating current (AC) voltage driving a motor that is part of a compressor stage.

Designing such a VSI for an aerospace application is a complex challenge. The complete system must comprise more than just the DC-AC inverter electronics. For instance, it must

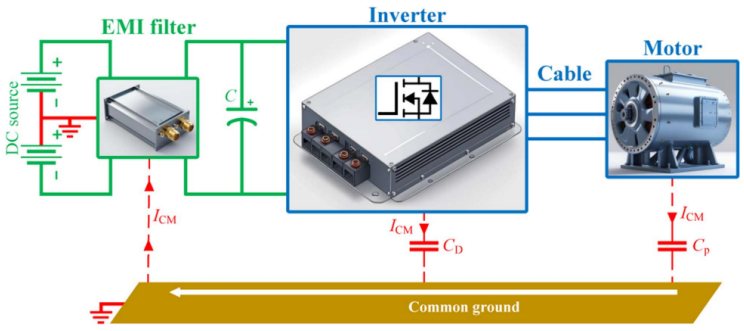


Figure 1.1: System overview, with the main common mode parasitics drawn [5].

include a cooling system, housing, EMC filter and protection (e.g. lightning, inrush). This complete system must then remain reliable under harsh environmental conditions (e.g., low pressure and a wide temperature range) while meeting stringent aerospace regulations, such as DO-160G [6]. The challenge, therefore, is not just selecting an inverter topology, but designing a complete and compliant system that can survive this environment.

There are multiple types of VSIs and each topology presents a different trade-off between the efficiency, common-mode (CM) voltage, specific power, EMC, power density, design complexity, thermal load, reliability and THD [5]. The conventional two-level H-bridge VSI is widely employed in motor drives due to its simplicity, high reliability, reduced number of switches and maturity [5]. However, they have larger voltage steps, which result in high CM voltage and steep voltage slopes ($\mathrm{d}v/\mathrm{d}t$) at the phase outputs. This can cause more electromagnetic interference (EMI), higher THD, and stress on motor windings [5]. Multilevel inverters can create smaller voltage steps, which improves output waveform quality and reduces harmonic content [7]. Furthermore, multilevel inverters sometimes have switches that require a lower blocking voltage, allowing the use of lower voltage-rated switches [5]. This, in combination with the possibility to use a lower switching frequency when the THD goal is constant, enables high efficiency designs. Another option is to interleave phase legs, where for one phase output, two or more single-phase legs are in parallel and driven out of phase. The outputs of the legs are combined via an interphase inductor. Interleaved inverters can offer benefits due to destructive interference at the input and output. This reduces the design requirements on the filter components [8].

The selection of a VSI for MEA applications is a complex, multi-objective optimisation problem with no single "best" solution. While advanced multilevel and interleaved topologies are known to offer superior output waveform quality compared to the conventional two-level VSI [5], their practical benefits in terms of specific power (kW/kg), power density (kW/L), and efficiency are not well-established for the aerospace context. Numerous surveys have documented the vast landscape of available topologies [7], [9], [10], highlighting the clear need for methodical comparisons. However, they lack either the specific aerospace environment or treat each inverter as just a set of switches, instead of a complete system in the correct environment. So to fairly compare inverter types, it requires designing all critical subsystems to meet the same stringent performance and regulatory targets (e.g., DO-160G). Only through this rigorous, system-level approach can the intricate trade-offs between efficiency, specific power, power density, and THD be accurately quantified.

This thesis addresses this gap by developing and applying a framework to benchmark and compare the performance of various complete systems using different VSIs topologies. It compares the complete systems based on efficiency, THD, specific power and power density. Through theoretical analysis and simulation, the study aims to evaluate the advantages and limitations of each topology, offering insights for selecting the most suitable VSI for aerospace applications. The main research questions are:

1. Which measures need to be taken to have a fair comparative analysis of voltage source inverters?
2. How to select the most suitable component sizes for each inverter?
3. What is the performance of each inverter for all key performance metrics?
4. How can the most suitable inverter topology for an aerospace application be selected?

To answer these research questions, this thesis will introduce all topologies under investigation in chapter 2. The working principles are explained along with the modulation

scheme used. For the interleaved inverters, a novel way to analytically estimate the peak circulation current is introduced. This forms the basis of the automated multi-stage design and optimisation framework of chapter 3, designed to ensure all designs meet the same set of requirements, have the most suitable components and can be compared fairly. Using this framework, multiple designs per inverter are created by changing the design choices. In chapter 4, the performance of each design is then evaluated and benchmarked against the key performance metrics: efficiency, specific power, power density, and THD. The performance data is synthesised into multi-objective trade-off analyses, including Pareto fronts and summary spider charts. This enables a discussion in chapter 5 of how the most suitable inverter type for an aerospace application can be selected. Chapter 5 also offers recommendations for future work and highlights key limitations of this work. Finally, chapter 6 provides the conclusions of the research.

Chapter 2

Inverter Topologies and Operating Principles

In order to perform the comparative analysis, the inverter topologies must be understood. To this end, the operating principles of various topologies under investigation are introduced in this chapter. Starting with the baseline 2L VSI and moving on to the 3L VSI and interleaved VSI. Key principles are also explained, such as the circulation current and the modulation schemes used. Finally, the chapter will define the system specifications for the 20 kW aerospace compressor system, to provide the basis for the subsequent design and analysis.

2.1 Conventional 2 Level Voltage Source Inverter

In fig. 2.1a, a single-phase leg of an H-bridge VSI is drawn. Each leg consists of two switches in series, where the midpoint is the phase output. Depending on which switch is turned on, the phase output to ground voltage (V_i where $i = [a, b, c]$) is either $+\frac{1}{2}V_{\mathrm{DC}}$ or $-\frac{1}{2}V_{\mathrm{DC}}$, making this a 2-level system. A 3-phase system uses three legs, where the phase output voltages are synthesised via space vector modulation (SVM) by varying on-times of the switches (see section 2.4). The MOSFETs need to block the full DC bus voltage, which is at most 884 V [6]. To ensure a margin from this voltage, 1200 V SiC MOSFETs were chosen, as this technology has the best FOM at this blocking voltage [11].

The DC-link capacitor (C_{DC}) is shared between all legs. It provides the high-frequency current, minimises the DC-link voltage ripple, is an energy buffer for sudden changes in power draw, absorbs regenerated energy and filters some of the differential-mode (DM) noise. This capacitor needs to handle the full DC input voltage and root mean square (RMS) current, with some safety factor.

2.2 Conventional 3 Level Voltage Source Inverters

Multilevel inverters have three or more output voltage levels. In this thesis, the focus is on the basic 3L VSIs to limit the scope. 3L VSIs introduce an intermediate voltage, so that the phase output voltage can be: $+\frac{1}{2}V_{\mathrm{DC}}$, 0 V or $-\frac{1}{2}V_{\mathrm{DC}}$. The benefit of the intermediate voltage is that a smaller voltage step can be taken, which reduces the THD [7]. It does require the main DC-link capacitor (C_{DC}) to be split into two series-per-level capacitances C_d, but these need only to block half the voltage each. Common multilevel topologies are listed in [7], but not all can be used. The main limiting factors are that only one DC input

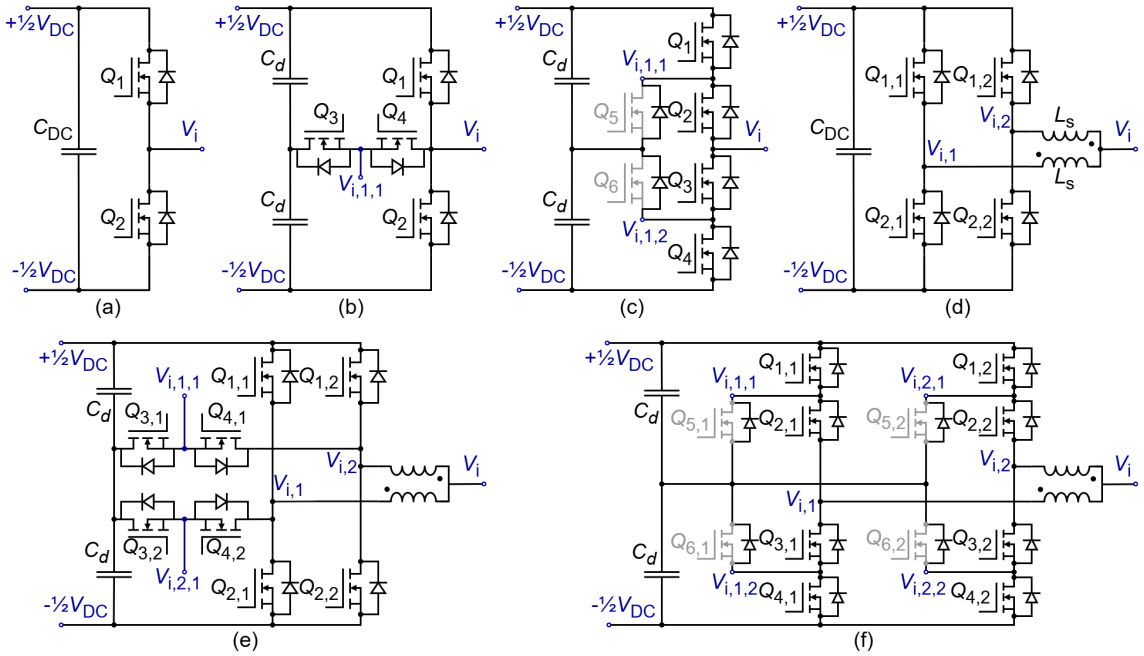


Figure 2.1: Single-phase legs of VSI topologies, drawn along with the (split) DC-link capacitor. (a) 2L H-bridge, (b) 3L T-type, (c) 3L neutral point clamped (NPC) and in gray active neutral point clamped (ANPC), (d) 2-level interleaved (2LI) H-bridge, (e) 3-level interleaved (3LI) T-type, (f) 3LI ANPC/NPC.

source is available and that the size and weight are limited. Three promising candidates are further investigated:

1. **T-type**. A single-phase leg is drawn in fig. 2.1b. It uses the same configuration as a 2L H-bridge, where it introduces a back-to-back MOSFET to connect the capacitor midpoint to the phase output. Turning the back-to-back MOSFET on and the others off creates the extra 0 V output level. The switches connecting the DC-bus need to block V_{DC} just like the H-bridge, but the back-to-back MOSFET only needs to block $\frac{1}{2}V_{\mathrm{DC}}$.

2. **NPC**. A single-phase leg is drawn in fig. 2.1c. It consists of four series switches and two clamping diodes connected to the DC midpoint. The extra 0 V output level is created by turning on the two inner switches and turning off the two outer switches. Through one of the diodes, the phase output is then connected to the capacitor midpoint (0 V). A key advantage is that each of the switches only needs to block $\frac{1}{2}V_{\mathrm{DC}}$, allowing for the selection of switches with a lower blocking voltage. These switches have a higher figure of merit (FOM) [11] and are thus more efficient. A disadvantage of this topology is that the losses are distributed unevenly across the switches [7].

3. **ANPC**. It is also drawn in fig. 2.1c, but it uses the grey MOSFETs instead of diodes for the clamping legs. The diodes are replaced to increase the efficiency and provide uniform switching losses [7].

These topologies have the disadvantage that they require a voltage balancing circuit [7]. This is a circuit that dynamically corrects voltage deviations at the DC midpoint, which is essential because an unbalanced voltage would exceed the blocking capabilities. The

blocking voltage of some of the devices is $\frac{1}{2}V_{\text{DC}}$, allowing 650 V devices to be used. To prevent variations from different semiconductor technologies and isolate the performance benefits of the topology change, SiC MOSFETs were used for both voltage levels.

In fig. 2.1, the floating node voltages are stated as $V_{i,h,k}$, where i is the phase, h states the inverter leg (with $h = 1$ if not interleaved), and k states the floating node number. The floating node voltages and phase output voltages (V_i) create CM noise, which is further explained in section B.2. Crucially, since topologies differ in the number and placement of these floating node voltages, their resulting CM noise spectrums are distinct, thus necessitating a unique filter for each topology.

2.3 Interleaved Voltage Source Inverters

Interleaving of VSIs is when two or more single-phase legs are used in parallel for one phase output. These additional legs are driven out of phase with the original legs. The 2LI VSI is drawn in fig. 2.1d, and the 3LI VSIs are drawn in fig. 2.1e and f. Directly connecting the phase outputs leads to short-circuits of the DC-link. So an interphase inductor is required to limit this current. This can be a coupled or uncoupled inductor at each leg output, where the connecting point is the new interleaved phase output. The coupled inductor solution is shown in fig. 2.1. A coupled inductor is preferred as it increases the inductance seen by the circulating current, and the load current does not saturate the core.

The benefit of interleaving is that it halves the RMS current through each leg, reducing the stress on the semiconductor devices and reducing the resistive losses. Interleaving also destructively interferes at some frequencies, and the specific frequencies that cancel differ between 2LI and 3LI. It always results in a reduction of the RMS current in the DC-link capacitor [12]. The peak current in the capacitor is unchanged, but the peaks occur for a shorter duration [12]. Thus, for interleaved inverters, a smaller DC-link capacitor can be chosen when ripple voltage or ripple current is the limiting factor.

2.3.1 Circulation Current

Circulating current (I_{cir}) is the undesired current that flows between the parallel-connected inverter legs in interleaved VSIs. It is created due to a voltage difference between the legs, where it does not contribute to the load current. I_{cir} should be limited as it decreases system efficiency, saturates the interphase inductor, and increases thermal stress of the DC-link capacitors and switches [13]. In chapter A, the peak circulation current ($\hat{I}_{\text{cir}}$) was derived for a 2LI and 3LI VSI using equivalent sequence SVM (for SVM see section 2.4). The peak circulation current in a 2LI and 3LI VSI is respectively:

$$\hat{I}_{\text{cir,2LI}} = \frac{V_{\text{DC}}}{4L_{\text{cir}}f_{\text{sw}}}; \qquad \hat{I}_{\text{cir,3LI}}(m) = \frac{V_{\text{DC}}}{8L_{\text{cir}}f_{\text{sw}}} \min\left(m\sqrt{3}, 1\right). \tag{2.1}$$

Here f_{sw} is the switching frequency, V_{DC} is the DC input voltage, $m \in [0, \frac{2}{\sqrt{3}}]$ is the modulation index and L_{cir} is the inductance seen by the circulation current. For a coupled inductor with a self-inductance L_{s} and coupling factor k, the circulation inductance is $L_{\text{cir}} = 2L_{\text{s}}(1 + k)$ (uncoupled inductors have the same equation but $k = 0$) [14]. eq. (2.1) assumes that the switching frequency is much greater than the modulated frequency (f_{ac}), e.g. $f_{\text{sw}} \gg f_{\text{ac}}$. For the 2LI, low ratios do not result in an error of $\hat{I}_{\text{cir,2L}}$. For the 3LI, low ratios exhibit significant errors. The exact error is stated in section A.3.2, practically using integer ratios of $\frac{f_{\text{sw}}}{f_{\text{ac}}} > 12$ the error is at most 18% and for $\frac{f_{\text{sw}}}{f_{\text{ac}}} > 21$ the error is at most 10%.

From eq. (2.1), it can be seen that the 3LI have half the $\hat{I}_{\text{cir}}$ compared to the 2LI for the worst case of $m \geq \frac{1}{\sqrt{3}}$. This is a significant benefit of using a 3LI, as the core saturation is linearly dependent on $\hat{I}_{\text{cir}}$ [15]. To reduce the circulation current, three methods can be used:

1. **Reducing V_{DC}**. This cannot be done in most cases, because V_{DC} is fixed by specification, such as the load requirements.

2. **Increasing f_{sw}**. This can be done, as f_{sw} is a design choice. However, it has practical limits, as a higher switching frequency results in higher switching losses, reducing efficiency.

3. **Increasing L_{cir}**. This can be achieved by increasing the L_{s} of the interphase inductor. This also has its limits, as it increases resistive losses in the wire due to the increase in turns, and it significantly increases the weight and volume of the inverter.

To effectively limit the circulation current, designers must increase L_{cir} and/or f_{sw}. This maintains system efficiency and prevents interphase inductor saturation, but it forces a trade-off against the negative impacts of higher switching losses, volume, and mass. More details about the design of the interphase inductor are provided in section C.5.

2.4 Modulation Scheme

A modulation scheme dictates the switching pattern of the VSI to synthesise a desired three-phase sinusoidal output waveform. Multiple modulation schemes can be used, such as sinusoidal pulse width modulation, third harmonic injection or SVM. SVM is used in this work for its better utilisation of DC-link voltage, reduced THD and straightforward digital implementation [16]. The core concept is explained in chapter A. The specific implementation details for the conventional and interleaved VSIs are presented below.

2.4.1 Conventional SVM Implementation

For the conventional VSIs, the PLECS SVM blocks for 2L and 3L topologies are used. Both blocks utilise a symmetrical, index-based SVM. This approach is well-suited as it centres the active vectors within the switching period, a method known to reduce the THD of the output waveforms [17]. The 3L version additionally includes a specific algorithm to ensure the DC-link neutral-point voltage remains balanced [17].

2.4.2 Interleaved SVM Implementation

When applying SVM to interleaved inverters, two main approaches exist.

- **Equivalent sequence SVM**. This method phase shifts the carrier signals of the individual inverters relative to each other, while sharing the same reference voltages. For two legs, it is shifted by 180°. The average of their per-leg phase voltages thus results in three distinct phase output voltage levels for the 2LI, effectively producing a 3L waveform. Similarly, the average phase voltage for the 3LI is a 5-level waveform. This approach maintains the simplicity of conventional SVM, while effectively creating higher levels. However, the resulting switching sequence is only an equivalent representation of some degrees of freedom inherent to true SVM [16].

- **True SVM**. Here, the two parallel inverter legs are explicitly treated as one converter, meaning a 3-level diagram is used for the 2LI VSI and a 5-level diagram for the 3LI VSI. The reference voltage vector is synthesised directly within the space vector diagram, where the switching states of both phase legs are coordinated to realise genuine voltage vectors. This method ensures that the average common-mode voltage difference between the two inverters is zero over each switching period, thereby eliminating net circulating currents. Furthermore, it allows for the implementation of both continuous and discontinuous pulse-width modulation (PWM) (DPWM) techniques, providing better control over switching losses, current ripple, and equivalent neutral-point balancing [16]. The trade-off is a higher implementation complexity, as accurate coordination and reference signal modification are required.

In this work, the equivalent sequence SVM approach is selected due to its simplicity and ease of implementation. It is realised by using two conventional SVM PLECS blocks and introducing a 180° phase shift to the carrier of the second block. Although the true SVM method would provide superior performance in terms of circulating current control and THD, its implementation complexity was considered beyond the practical scope of this study.

2.5 System Specifications

The VSIs are designed to drive a high-speed compressor for an aerospace application. This application, along with regulatory standards, defines a fixed set of system specifications that all designs in this thesis must meet. These specifications are detailed below and summarised in table 2.1.

2.5.1 Regulatory Constraints

The primary constraints are derived from the aerospace standard DO-160G [6]. The standard dictates the nominal input voltage (V_{DC}) of 540 V (derived from two 270 V supplies) and an operational range of 470-570 V. Additionally, the standard specifies a potential surge voltage of at most 884 V. Furthermore, it limits the conducted EMI by setting a frequency-dependent limit on the current spectrum. The standard's limit is 7% of the maximum current ($\approx 3.0\,\mathrm{A}$). To ensure compliance, a safety factor (SF) of 1.7 is applied, resulting in a stricter design target of $I_{\mathrm{pp}} \leq 1.8\,\mathrm{A}$. Furthermore, it sets the environment in which the heatsink system must operate, specifying an ambient temperature (T_{amb}) of $-55\,^{\circ}\mathrm{C}$ to $70\,^{\circ}\mathrm{C}$ and a pressure (P_{amb}) of 11.6 kPa to 101.32 kPa [6].

2.5.2 Load and Operational Requirements

The load is a 20 kW high-speed compressor (P_{L}) operating at a modulated frequency (f_{ac}) of 2 kHz. For simulation and analysis, the load is modelled with an inductance (L_{L}) of 170 µH and a resistance (R_{L}) of $3.45\,\Omega$ to represent the back-EMF. From the power and nominal voltage, the maximum input current (I_{DC}) is calculated to be 43.4 A, assuming a target efficiency (see eq. (C.1)).

2.5.3 Safety and Design Constraints

Several constraints are imposed for safety and design robustness. To limit leakage currents, the maximum CM capacitance ($C_{\mathrm{CM,max}}$) is a design choice set to 180 nF. This limit

applies to any added capacitance from the DC-link to the ground/chassis. The maximum temperature of the heatsink ($T_{\text{hs,max}}$) is set to 100 °C. This temperature is a key factor that determines which temperature class of components can be used. For a forced air cooling system, it must be set higher than the maximum ambient temperature ($T_{\text{amb,max}}$) of 70 °C, where a larger margin is an easier design but requires a more limited temperature class of components. The peak-to-peak input voltage ripple (V_{pp}) is limited to 1% of the V_{DC} (i.e. 5.4 V), to ensure DC-link stability and controllability.

Table 2.1: System specifications used for all inverters

Parameter	**Value**
Input voltage range	470-570 V
Nominal input voltage (V_{DC})	540 V
Maximum surge voltage	884 V
Input current (I_{DC})	0-43.4 A
Maximum input voltage ripple (V_{pp})	$0.01 V_{\text{DC}} = 5.4$ V
Maximum input current ripple (I_{pp})	$0.070 \frac{I_{\text{DC}}}{SF} \approx 1.8$ A
Load power draw (P_{L})	20 kW
Load inductance (L_{L})	170 µH
Load resistance (EMF imitator) (R_{L})	3.45 Ω
Modulated frequency (f_{ac})	2 kHz
Ambient temperature range (T_{amb})	-55-70 °C
Ambient pressure range (P_{amb})	11.6-101.32 kPa
Maximum heatsink temperature ($T_{\text{hs,max}}$)	100 °C
Maximum CM-to-ground capacitance ($C_{\text{CM,max}}$)	180 nF
Safety factor (SF)	1.7

Chapter 3

Design Framework

To ensure a fair and objective comparison between different inverter topologies, a systematic, multi-stage optimisation framework is employed. This automated process, detailed in fig. 3.1 and expanded upon in chapter C, ensures that every inverter design meets the same system specifications and constraints (e.g., P_{L}, V_{DC}, EMI limits) while being optimised for minimum mass and volume. The framework executes a sequential design flow, where the results from one stage are used as inputs for the next.

1. **DM filter stage:** The process begins with the DM filter. This stage performs a wide search by sweeping through a library of pre-defined DC-link inductors (L_{DC}) and DM capacitors (C_{DM}). For each pair, it performs a binary search to find the minimum DC-link capacitance (C_{DC}) required to meet three criteria: DM noise spectrum 6 dB below limit line, below maximum voltage ripple, and below maximum current ripple. From all valid designs, the algorithm selects the optimal one using a weighted normalised score ($score = 2\tilde{m} + \tilde{V}$) that heavily prioritises low mass, which is a key priority for the chosen aerospace compressor application.

2. **Interphase inductor stage:** For interleaved topologies, this stage calculates the required circulating current inductance (L_{s}). It then searches a pre-defined core and winding library to select the lightest physical inductor design that meets this requirement without saturating. This selected design also determines the equivalent filter inductance ($L_{\mathrm{f}} = \frac{1}{2}L_{\mathrm{s}}(1-k)$ [14]), which is the inductance seen by the phase leg output current.

3. **CM filter stage:** Using the components from the optimised DM filter and the interphase inductor's equivalent filter inductance, the CM filter is designed. This stage performs a binary search to find the minimum CM choke inductance (L_{CM}) that successfully attenuates the CM noise spectrum to at least 6 dB below the regulatory limit.

4. **Complete design and sizing:** This block gathers all the designed component values. It uses this to complete the design in the following steps:

   (a) **Design the heatsink:** First, a loss simulation is run to determine the total power dissipation under worst-case conditions. The loss value is then used to calculate the mass and volume of the forced-air cooling system, by using pre-determined mass and volume performance indices (mass performance index (MPI) and cooling system performance index (CSPI)).

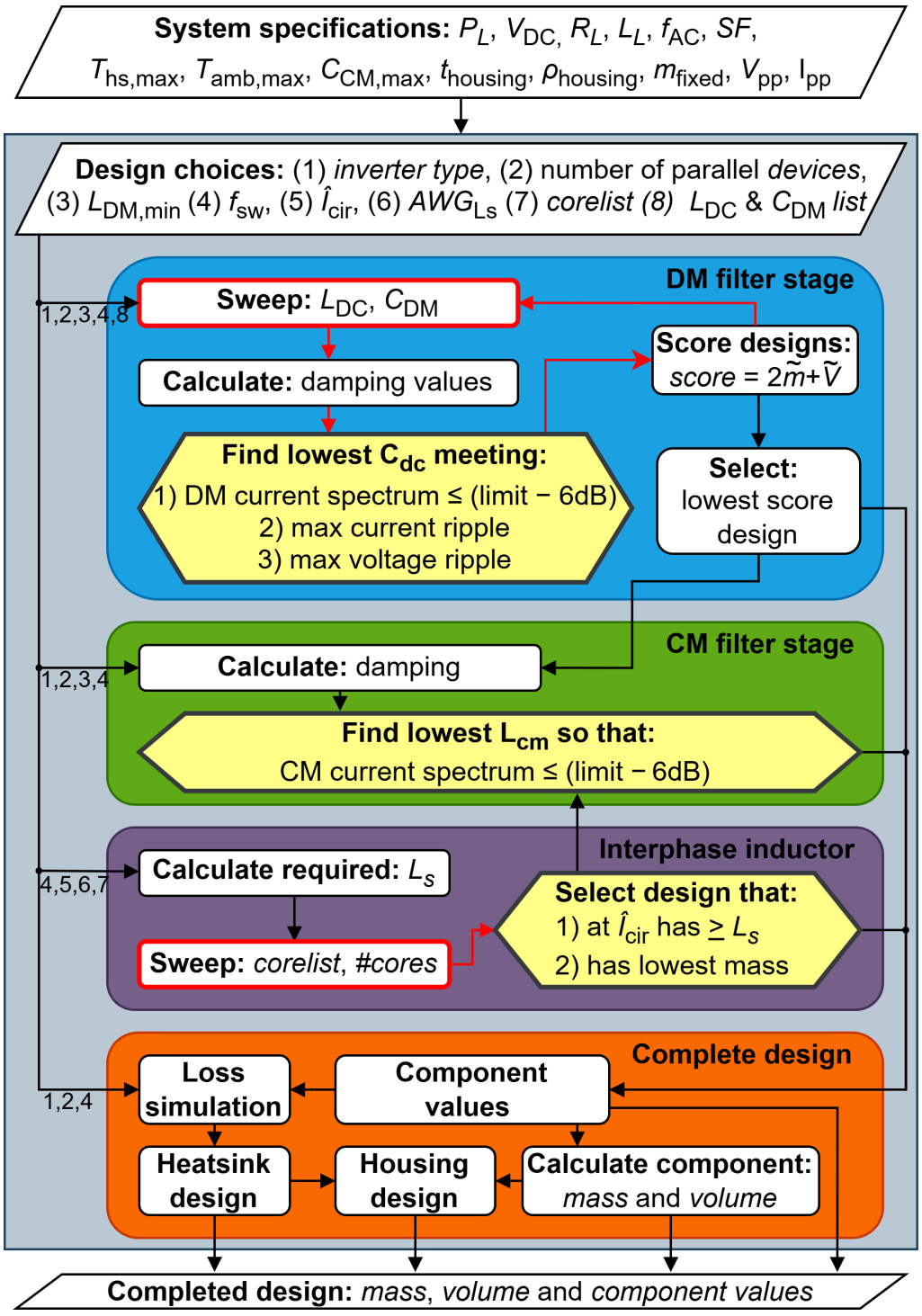


Figure 3.1: Multi-stage optimisation design flow for inverter design.

(b) **Calculate final mass/volume:** The framework calculates the size of the power printed circuit board (PCB), estimates the housing dimensions, and sums the mass and volume of all components (filters, heatsink, PCB, and other fixed-value parts) to produce the final inverter design.

The output of this framework is a complete inverter design with its total mass, volume, component values and simulated losses and THD, allowing for an objective comparison of different topologies.

To conduct the comparative evaluation presented in the next chapter, this framework was used to create a comprehensive design space by systematically sweeping a set of key design choices. While the system specifications are constant for all designs (as stated in table 2.1), the primary variables swept are:

- **Inverter topology:** The eight conventional and interleaved topologies under investigation.
- **Device count:** The total number of MOSFETs and diodes, ranging from 6 to 72.
- **Switching frequency:** Five levels: $\{24, 36, 48, 60, 72\}$kHz.
- **Peak circulating current:** For interleaved topologies, there are five peak circulating current levels from 10% to 50% of the RMS output current.
- **Inductor Wire Gauge:** Two options for the interphase inductor wire size: 7 AWG and 9 AWG.

By sweeping these parameters, a total of 780 unique and fairly comparable inverter designs were generated. For more details about the detailed design process and the components used, the reader is referred to chapter C. For more details about the simulation set-up, the reader is referred to chapter B. The performance of these designs is evaluated and benchmarked in the next chapter.

Chapter 4

Performance Evaluation

The 780 inverter designs created using the framework of chapter 3 are evaluated in this chapter. This evaluation is done for the four key performance metrics, efficiency, THD, mass and volume. The performance metrics are examined individually to find the impact of the design choices such as the topology, device count, switching frequency and wire thickness. Finally, a system-level comparison is performed using Pareto fronts and summary spider charts.

4.1 Efficiency and Power Loss

Efficiency is a critical performance metric for inverters, not only for the power saving, but also because it directly influences cooling requirements. In this section, the efficiency across the inverter types is analysed with respect to the design choices: switching frequency, number of parallel devices and interphase inductor design criteria. To start, a loss breakdown will be performed across the inverters. All results in this section are at 20 kW output power.

4.1.1 Loss Breakdown

In fig. 4.1, the losses are broken down per inverter type for the highest efficiency design. Comparing the interleaved versions against their conventional counterpart, it can be seen

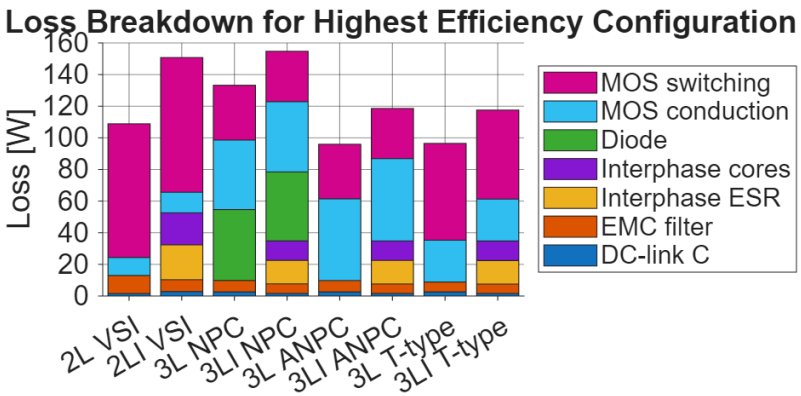


Figure 4.1: Loss breakdown by component for each inverter topology. Operating point: $P_{\text{out}} = 20\,\text{kW}$, $f_{\text{sw}} = 24\,\text{kHz}$, 72 devices total, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

that they have higher losses. These extra losses are roughly equal to the resistive losses and the core losses in the interphase inductors. Comparing the 3L VSI with the 2L inverter, the NPC has higher losses, mainly due to high diode losses. The ANPC and T-type have lower losses than the 2L VSI. This is not universally true, as it is dependent on switching frequency and device count. All the 3L VSI have lower switching losses, but also higher conduction losses. For NPC and ANPC, the switching losses are lower due to the lower voltage across the MOSFETs, whereas the conduction losses are higher as they now need to pass through two switches. For the 3L T-type compared to the 2L VSI, the only thing that is added is the back-to-back MOSFET to the neutral point. The back-to-back MOSFET has higher conduction losses but reduced switching losses, resulting in a net decrease in losses. Overall, interleaving increases total loss for equal device counts, and depending on configuration, not all 3L VSIs outperform the 2L VSI.

4.1.2 Effect of Switching Frequency

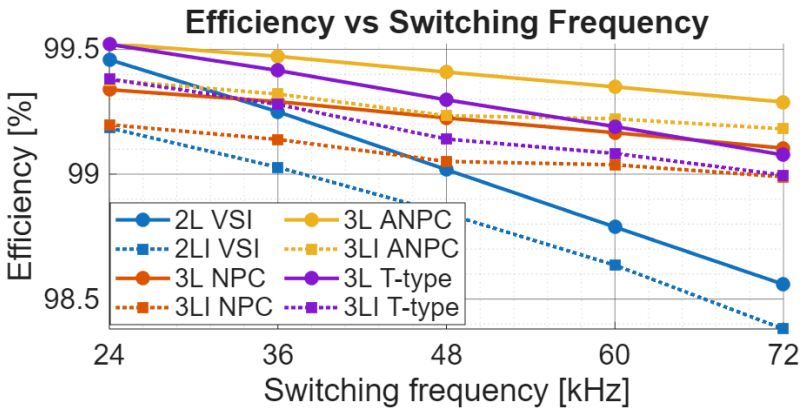


Figure 4.2: Efficiency versus switching frequency for all inverter topologies. Operating point: $P_{\text{out}} = 20\,\text{kW}$, 72 devices total, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

Figure 4.2 plots the efficiency versus switching frequency using a comparable configuration. The efficiency declines approximately linearly with switching frequency, where the conventional and interleaved 2L VSI decline more steeply than the multilevel inverters. This suggests that the switching losses in the 2L VSI grow quicker than in the 3L VSIs. The T-type inverter has a slope in between that of the ANPC/NPC and the 2L VSI, because only the neutral-point back-to-back pair sees reduced voltage, the line devices still switch near V_{DC}. The ANPC only shows significantly improved efficiency compared to the T-type at high switching frequencies, while at low switching frequencies they are roughly equal. Furthermore, the interleaved inverters have a slightly shallower decrease in efficiency than their conventional counterpart because the interphase inductors become smaller and thus more efficient at higher frequencies. Even so, the interleaved variants remain less efficient over the full frequency range.

These observations are consistent with fig. 4.3, which shows the exact breakdown of losses over switching frequency. The switching losses dominate the loss increase with switching frequency. The increase is largest for 2L, followed by T-type, and ANPC/NPC have the smallest increase. A small decrease in filter losses and interphase inductor losses can be observed, meaning that these components do improve within the switching frequency range.

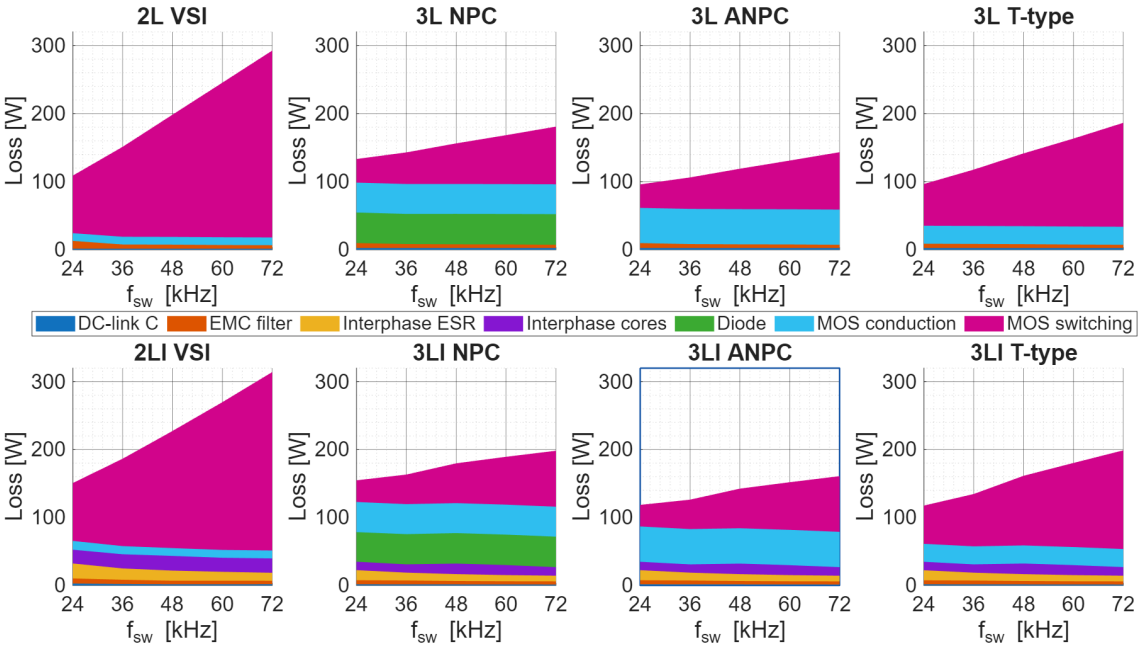


Figure 4.3: Total inverter loss breakdown versus switching frequency for each topology. Operating point: $P_{\text{out}} = 20\,\text{kW}$, 72 devices total, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

4.1.3 Effect of Device Count

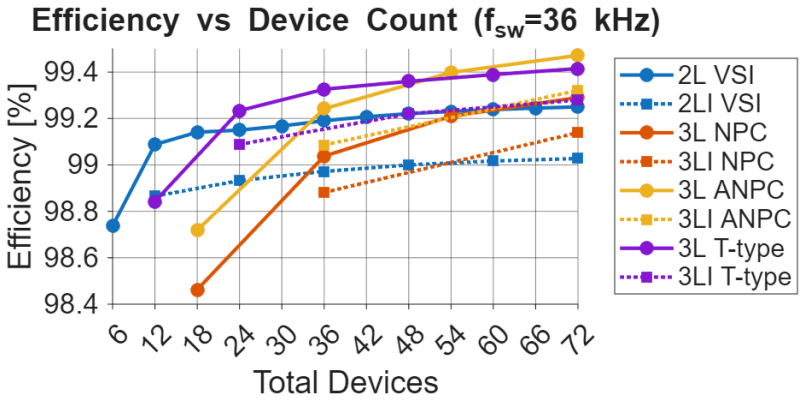


Figure 4.4: Efficiency versus total device count (MOSFETs + diodes) for all inverter topologies. Operating point: $P_{\text{out}} = 20\,\text{kW}$, $f_{\text{sw}} = 36\,\text{kHz}$, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

In fig. 4.4, the efficiency is plotted against the total device count, including MOSFETs and diodes. The total number of devices was increased up to a maximum of 72, with a step size that varies as each inverter type has a different base device count. The efficiency improves greatly for the first steps of the device count, and then the improvement per step decreases. The improvement in efficiency is mainly due to the decrease in conduction losses, which is inversely proportional to the number of parallel devices.

The total number of devices is directly related to the size of the power PCB. For a small power PCB footprint (6-12 devices), the conventional 2L VSI offers the best efficiency at the same switching frequency. The conventional T-type has the best efficiency at a low to

medium device count (12-48 devices) for the multilevel inverters, while the conventional ANPC is best at the very highest device count (54-72 devices).

Comparing the 2LI VSI at low device count to the conventional multilevel inverters, it can be seen that it is competitive in terms of efficiency. However, this is not universally true, as the switching losses in the 2LI grow more quickly than for the multilevel inverters, so at higher switching frequencies the performance of the 2LI will be worse. So, interleaving can be competitive at low device count in terms of efficiency. Among the interleaved options, the interleaved T-type is the best performing inverter under high and low device counts. But at the highest device count and high switching frequency, the interleaved ANPC is slightly more efficient.

4.1.4 Effect of Interphase Inductor

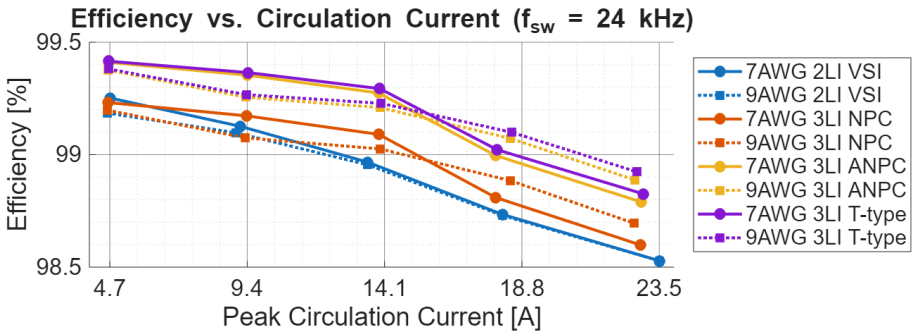


Figure 4.5: Efficiency versus peak simulated circulation current $\hat{I}_{\text{cir}}$ for interleaved topologies with two interphase inductor wire gauges (7 AWG and 9 AWG). Operating point: $P_{\text{out}} = 20\,\text{kW}$, $f_{\text{sw}} = 24\,\text{kHz}$, 72 devices total. Range shown: $\hat{I}_{\text{cir}} \approx 10\% - 50\%$ of $\hat{I}_{\text{out,RMS}}$.

The interphase inductor had three main design choices: the wire size, the core used and the maximum peak circulation current. In fig. 4.5, the efficiency versus simulated peak circulation current is plotted for two wire thicknesses. The RMS output current was 47 A, so the plotted circulation current is in the range of 10% to 50% of the RMS output current. The general trend is that more circulation current results in more losses. The exact decrease profile is primarily a combination of the peak-to-peak B-field, core volume and the equivalent series resistance (ESR) of the interphase inductor (for details see section B.3). When the peak circulation current goes from roughly 10% to 50% of the RMS output current, the efficiency drops by roughly 0.5-0.7%, where this is a critical effect in the high efficiency regime of around 99%.

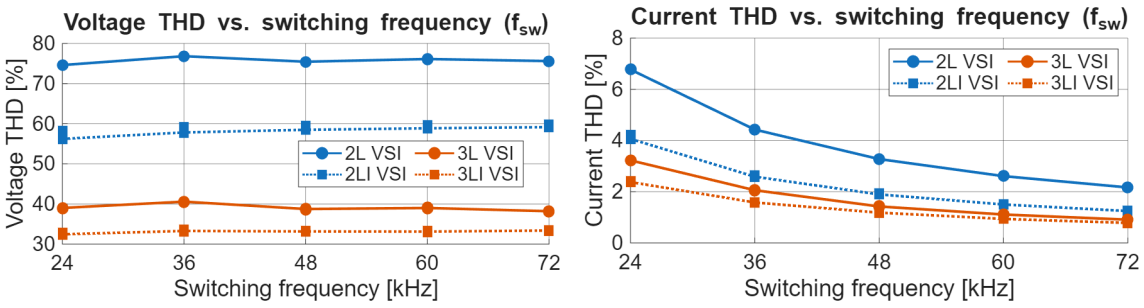
It can be seen that the thicker 7 AWG at a lower circulation current has a higher efficiency than the thinner 9 AWG wire, due to the lower ESR. However, at higher circulation currents, the interphase inductor with the thinner 9 AWG wire results in a higher efficiency. This is due to the 7 AWG wire requiring a larger core. This reduces the B-field but increases the core volume. The core losses for the same input conditions are proportional to $V_e \cdot B^c$, where V_e is the core volume, B the magnetic flux density in the core, and c is the Steinmetz material constant [15]. Even though B decreases for the 7 AWG wire, the larger V_e dominates and decreases the efficiency compared to the smaller 9 AWG wire inductor. Thus, choosing a thicker wire is not always the most efficient.

The simulated peak circulation current is not always equal to the predicted maximum, as seen from the variation in marker location around the predicted values. This is mainly dependent on the modulation index and ratio of f_{sw} to f_{ac} as explained in section A.3.2.

4.2 Total Harmonic Distortion (THD)

THD is an important figure of merit for inverters, as it increases motor losses. While output voltage THD is useful to compare modulation strategies and inverter topologies, its impact on the machine is indirect because voltage harmonics translate into loss primarily via the resulting harmonic currents. The voltage THD only affects the iron losses. The majority of the harmonic losses in the motor are proportional to the sum of squared harmonic currents in the stator and rotor [18]. This makes the current THD the best motor loss indicator. Accordingly, we evaluate both voltage and current THD, but emphasise current THD for performance comparisons.

4.2.1 THD versus Switching Frequency



(a) (b)

Figure 4.6: THD vs switching frequency. NPC, ANPC, and t-type are bundled under 3L, and their interleaved version under 3LI. All 780 designs are drawn, and the connecting line is drawn for the most efficient design. (a) Voltage THD, (b) current THD.

In fig. 4.6a, the phase output voltage THD is shown as a function of switching frequency. While small fluctuations with frequency are visible, no clear trend can be identified. What can be seen is that the modulation type used is the dominant factor. Averaged across all designs and switching frequencies, the THD levels are approximately 76% for the 2L VSI, 59% for the 2LI VSI, 39% for the 3L VSI and 33% for the 3LI VSI. This confirms that increasing the effective number of voltage levels reduces the THD, through the smaller steps available. Since the output voltage has no filtering component except for the interphase inductor, no significant change is expected with frequency.

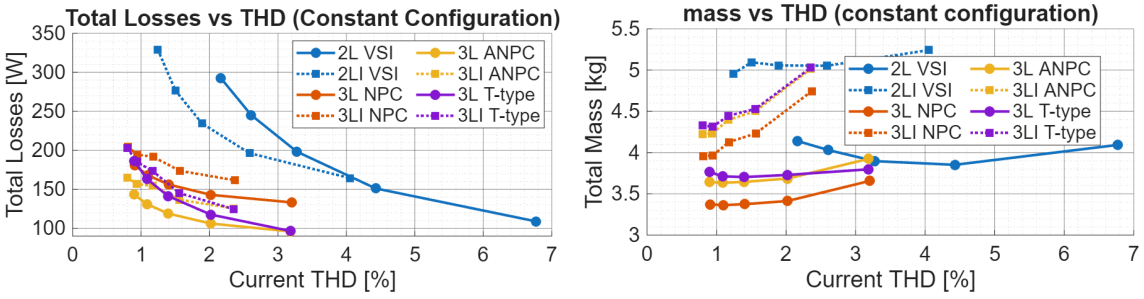
In fig. 4.6b, it can be seen that the order of the output current THD level is the same as for the voltage THD level. Moreover, the THD of the output current decreases for all inverter types with switching frequency. This is because the motor inductance has a filtering effect on the high-frequency current, so that higher switching frequencies are more effectively filtered. Consequently, a multilevel inverter can achieve the same THD at a lower switching frequency. For example the 3L compared to the 2L reduces the current THD at 36 kHz by 50%. For the 2L to have equal THD, it would require a little more than double the switching frequency of the 3L.

The interleaved compared to the conventional inverter has a lower THD. A 2LI VSI can create 3 levels, just like a 3L VSI. From fig. 4.6 it can be seen that the THD of the 2LI VSI is not equal to that of the 3L VSI. This is because equivalent SVM is used (see section 2.4). This is different from a true SVM modulation scheme, because it does not always apply the nearest voltage vectors. Thus, the voltages at the phase outputs differ from the ideal 3L case, thus leading to a higher THD. If the proposed method of [16] were

to be used, then the THD of the 2LI VSI would be roughly equal to that of the 3L VSI. This is because the output waveform generation is identical, but the interleaved inverter has a slightly reduced THD due to the filtering effect of L_{f}.

Furthermore, in fig. 4.6 all the 780 designs are plotted, from which it can be seen that the variance per group is small, meaning that the THD is only driven by the switching frequency. Only for the interleaved inverters is a small spread visible. This is due to the different interphase inductors used, where variations in equivalent filter inductance slightly affect the THD.

4.2.2 Relation between THD, Losses and Mass



(a) (b)

Figure 4.7: All inverter configurations use 72 devices and if applicable, an interphase inductor of 7 AWG that produces $\hat{I}_{\mathrm{cir}} = 4.7\,\mathrm{A}$. (a) current THD versus losses at 20 kW, (b) current THD versus mass.

Figure 4.7a compares current THD with total inverter losses under equal device count and interleaving conditions. The conventional and interleaved two-level topologies clearly form the least favourable cluster, requiring significantly higher losses to achieve a given THD. In contrast, conventional and interleaved three-level topologies occupy the desirable low-loss and low-THD region.

The 2LI VSI has reduced THD for the same losses, compared to the conventional 2L VSI. Whereas the opposite occurs for the 3LI case, where the interphase inductor losses outweigh the gains from the THD improvement. Thus, interleaving only offers a worthwhile trade-off for the 2LI VSI in terms of efficiency. Where THD of interleaving can be further reduced by implementing a true SVM scheme (see section 2.4).

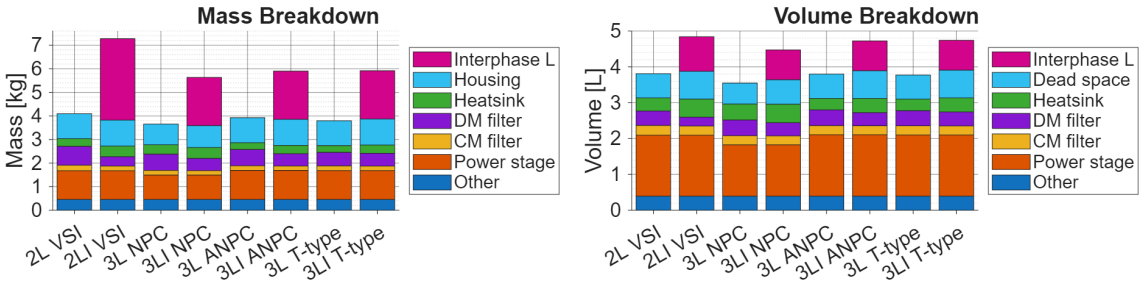
Figure 4.7b shows the THD versus the mass, for the same configuration. It can be seen that the conventional VSIs have the lowest mass for a given THD. The 3LI VSIs have a significantly smaller mass at lower THD values, due to the decrease in interphase inductor size. The 3L VSIs have a low mass, but at 3.3% THD it is equal to the 2L VSI, indicating that in terms of specific power the 2L can still be a good option. However, when looking back at fig. 4.7a, it can be seen that the losses of the 2L are almost double at 3.3% THD compared to the 3L ANPC. Still indicating a clear advantage of the conventional 3L VSIs.

Overall, a clear trade-off emerges: if higher THD is acceptable, the two-level inverter remains competitive in both mass and losses. However, for low-THD requirements, conventional three-level inverters outperform the other topologies in terms of both efficiency and mass. It is important to note that these results correspond to a specific configuration; selecting a design with fewer components could better leverage the inherent advantages of the conventional 2L VSI (see section 4.1.3).

4.3 Mass and Volume

Mass and volume, and their corresponding metrics of specific power (kW/kg) and power density (kW/L) are key metrics for aerospace inverters. In practice, the same design choices that influence the efficiency also influence the mass and volume: switching frequency, device paralleling, and interphase inductor design. This section evaluates how these choices affect the mass and volume.

4.3.1 Mass and Volume Breakdown



(a) (b)

Figure 4.8: Mass and volume breakdown by component for each inverter topology. Operating point: $P_{\text{out}} = 20\,\text{kW}$, $f_{\text{sw}} = 24\,\text{kHz}$, 72 devices total, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$. (a) Mass breakdown. (b) Volume breakdown.

In fig. 4.8a, the mass of the inverters has been split into the different components. From which it can be seen that the interphase inductors are the main reason for a large mass difference between the conventional and interleaved inverters. The interleaving did decrease the mass of the DM filter, but this did not outweigh the mass increase due to the interphase inductor.

For the breakdown of the volume in fig. 4.8b, it can also be seen that the main difference between the conventional and interleaved inverters comes from the interphase inductor. Due to the same configuration, the rest of the inverters are very similar, only the NPC has a slightly lower volume and mass due to diodes not requiring driving circuitry. Given that mass is a primary design constraint in aerospace, the following analysis will focus on mass, although the trends for volume are strongly correlated.

4.3.2 Effect of Switching Frequency

In fig. 4.9, the change of the system mass versus switching frequency can be seen. The overall trend is that the mass drops with switching frequency. This is mainly due to a decrease in required interphase inductance and EMC filter size. This decrease will not continue indefinitely, as seen for instance for the 2L VSI. This is because the growth in switching losses requires a larger heatsink, which at some point will increase the net system mass.

This effect can more clearly be seen when splitting all the losses separately as done in fig. 4.10. From which it is clear that the mass of the filter and interphase inductor drops while the heatsink mass grows. Furthermore, it can be seen that the DM filter decreases significantly with switching frequency, while the CM filter stays roughly constant. This is expected as increasing the switching frequency decreases the voltage and current ripple,

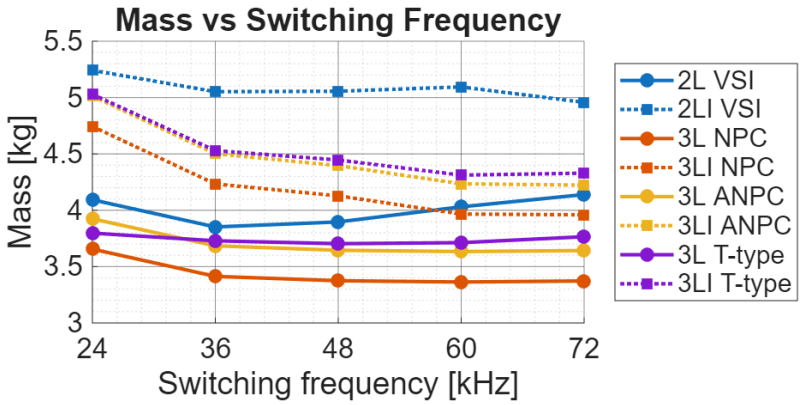


Figure 4.9: Total inverter mass breakdown versus switching frequency for each topology. Operating point: $P_{\text{out}} = 20\,\text{kW}$, 72 devices total, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

decreasing the requirement on the DC filter. While a higher switching frequency does not decrease the CM filter size, as the envelope of the CM noise is flat until the one over the rise/fall time of the MOSFETs [19]. So if the rise/fall time does not change, the CM noise envelope does not change, so no change in mass is expected. For the interleaved inverters, it can be seen that a higher switching frequency reduces the size of the interphase inductor. Which is expected as the required inductance is inversely proportional to the switching frequency ($\propto \frac{1}{f_{\text{sw}}}$). Where the drop in total mass is larger for the 3LI VSIs, as there the heatsink size does not grow as quickly as for the 2LI VSI.

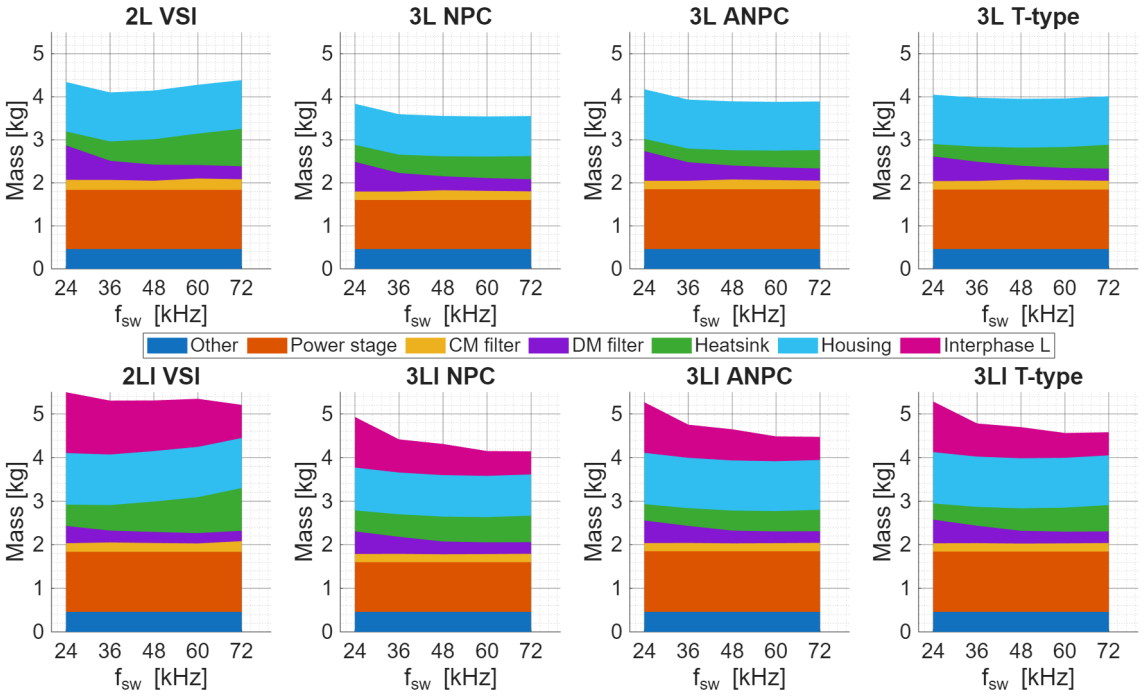


Figure 4.10: Total inverter mass breakdown versus switching frequency by component for each topology. Operating point: $P_{\text{out}} = 20\,\text{kW}$, 72 devices total, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

4.3.3 Effect of Device Count

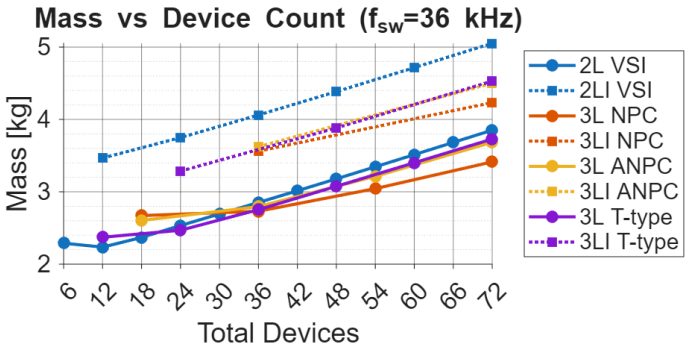


Figure 4.11: Total inverter mass versus total device count (MOSFETs + diodes) for all topologies. Operating point: $P_{\text{out}} = 20\,\text{kW}$, $f_{\text{sw}} = 36\,\text{kHz}$, and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

In fig. 4.11, the inverter mass is plotted against the total number of devices. A clear trend can be seen across all topologies, where more devices result in a higher mass. This change is driven by the extra mass of the devices, the extra PCB mass and the larger housing. Where the slopes depend on the topology, as for instance NPC require fewer gate drivers, thus it is also lighter.

An interesting effect can be seen for the 2L VSI at low device numbers. At the initial increase of devices, the total inverter mass decreases. This is due to the decrease in heatsink mass. This is closely linked to the initial efficiency gain seen in fig. 4.4. Initially, it has a large efficiency gain, after which the marginal gain per step decreases. The mass and volume of the heatsink are directly linked to the efficiency. So initially, the heatsink mass was larger than the additional mass of the devices. For the conventional multilevel inverters, it can be seen that the first step in device count resulted in only a small increase in mass, but a significant step in efficiency. For the interleaved inverters, this behaviour cannot be observed. Where this trade-off lies is dependent on the exact MOSFET selected, and then mainly on the on-resistance.

4.3.4 Effect of Interphase Inductors

When a larger peak circulation current is allowed, the required interphase inductance decreases. However, the mass of the interphase inductor is not only determined by the required inductance but also by the peak circulation current itself. As a higher circulation current increases the Amps per Turn ($I \cdot N$), which decreases the inductance coefficient (A_L) at that current. This then requires more turns to get the same inductance [15], which increases the weight. This can also be seen for the 7 AWG 2L VSI in fig. 4.12, where this decrease is mainly due to the three interphase inductors together decreasing in mass from 3.45 kg, to 2.13 kg. This was a special case as initially it needed to use 2 cores to get to the required inductance, where at 9.4 A it only required 1 core per inductor, greatly reducing the required mass. All other interphase inductors used only 1 core, so this change is not as large.

The 9 AWG 2L VSI combined interphase inductor mass goes from 1.40 kg at 4.7 A, to 1.17 kg at 9.4 A and 1.00 kg at 23.5 A. Thus, the decrease in mass of the interphase inductor alone is not significant, mainly due to the requirement to handle higher currents. Furthermore, due to the higher circulation current, the losses also increase as seen in fig. 4.5. This

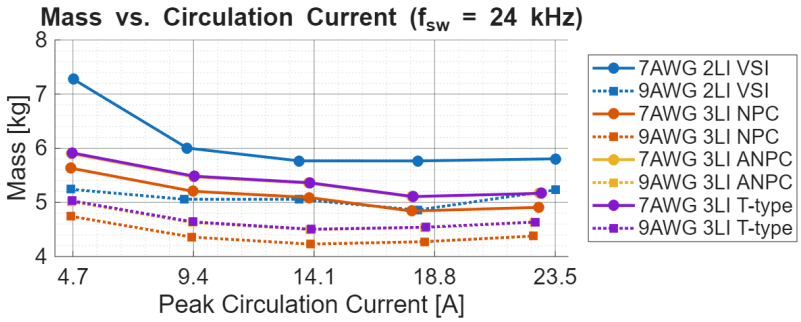


Figure 4.12: Total inverter mass versus peak circulation current for interleaved topologies with two interphase inductor wire gauges (7 AWG and 9 AWG). Operating point: $P_{\text{out}} = 20\,\text{kW}$, $f_{\text{sw}} = 24\,\text{kHz}$ and 72 devices total.

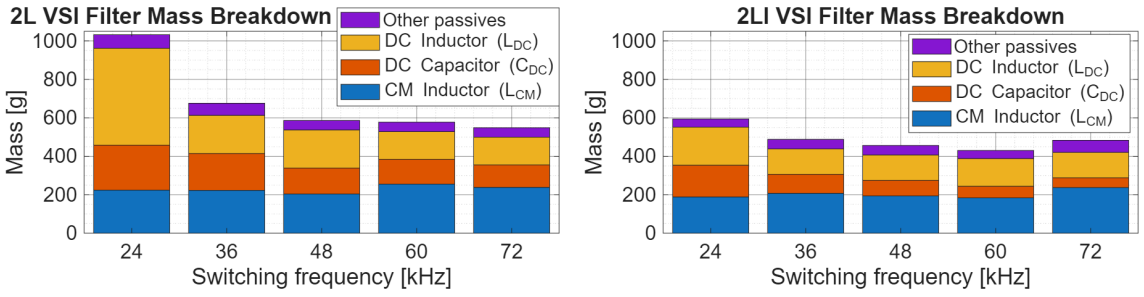
requires a larger heatsink, which adds more mass counteracting the small mass decrease in the interphase inductor. This complex interaction means simply minimising inductance doesn't guarantee minimum mass. A more effective way to reduce the interphase inductor size is to increase the switching frequency, as seen in fig. 4.10.

Comparing the mass of the 9 AWG with the 7 AWG designs in fig. 4.12, it can be seen that the mass is significantly less for the 9 AWG options. Neglecting the outlier where the number of cores changed, the average decrease in mass is 12%. While the difference in efficiency was not more than 0.1%, it was even more efficient in some conditions to have a smaller wire size (see section 4.1.4). This highlights that the interphase inductor design is a critical mass-versus-efficiency trade-off where simple component-level assumptions, such as a higher allowed circulating current always resulting in a lower system mass, are sometimes invalid. The optimal solution requires a system-level balance between the direct mass of the magnetic components and the total system losses, which are themselves dependent on design choices like circulating current and switching frequency.

4.3.5 EMC Filter Mass

DM Filter Effects

The change in CM and DM filter mass can be observed in fig. 4.13 for the 2L and 2LI VSI. The DM filter comprises mainly of the DC-link inductor and DC-link capacitor, where a decrease can be observed in DM filter size with switching frequency. This has two main



(a) (b)

Figure 4.13: Filter mass breakdown, where other passives include the CM and DM capacitors and damping. Operating point: 72 devices total and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$. (a) 2L VSI. (b) 2LI VSI.

reasons: first, for a higher switching frequency, the DM noise also moves to a higher frequency. This allows the cut-off frequency of the filter to also increase, reducing the size of the passive components. The second is that a higher switching frequency reduces the normalised voltage and current ripple [20], so for the same ripple requirement, the filter size can be smaller. This decrease in filter mass is not linear, as can be observed in fig. 4.13. Firstly, as component size and mass are not linear. Secondly, as the cut-off frequency (f_c) shift and component size change are also not linear, as for a second-order low pass filter: $L_{\mathrm{DC}}C_{\mathrm{DC}} \propto \frac{1}{4\pi^2 f_c^2}$.

When comparing the conventional and interleaved two-level DM filter mass, it can be observed that at 24 kHz the DM mass for the interleaved version is halved. While for the higher switching frequencies, this decrease is not as significant. This indicates that interleaving only offers a significant DM filter benefit if the DM noise is large, but it does always reduce DM filter size. This benefit of interleaving is also observed in the multilevel topologies, as shown by the consistently lower DM filter mass for the interleaved variants in fig. 4.10. However, the trend that interleaving only offers a significant DM filter benefit at low frequencies cannot be seen for the T-type. This might mean that the DM noise was not large enough or that this is not a general phenomenon.

CM Filter Effects

The CM filter is not expected to change with the switching frequency as discussed in section 4.3.2. However, a small fluctuation of L_{CM} can be seen in fig. 4.13, mainly due to the position of peaks relative to the limit line changing, which can lead to small fluctuations in the filtering needed. The CM filter is also not influenced by the interphase inductor, as the equivalent filter inductance at the output results in a low-pass filter where the cut-off frequency is not close enough to that of the filter to help attenuate the noise. The CM inductor is influenced by the size of the stray capacitance, which increases with the number of parallel devices. This extra attenuation needed by the filter can be approximated with [21],

$$\Delta H_{\mathrm{dB,\ CM}}(C_{\mathrm{s}}) \approx 20 \log_{10} \left(\frac{3C_{\mathrm{s}} + C_{\mathrm{output,CM}}}{C_{\mathrm{output,CM}}} \right). \tag{4.1}$$

Here C_{s} is the added stray ground-source capacitance of a single MOSFET and $C_{\mathrm{output,CM}}$ is the sum of the CM output capacitances (all capacitance at the right-hand side of the source in fig. B.4). This implies that for a linear increase of C_{s} with device count, the attenuation, and thus CM inductance (L_{CM}) also would grow linearly. In fig. 4.14 L_{CM} is plotted against the device count, where it is nearly linear as expected from eq. (4.1). However, it curves slightly as some of the ground-source capacitances are connected to the DC-link, which filters the noise. Thus, the simulation meets the theoretical and experimentally verified expectation of [21], which confirms that at least the change with device count is correctly captured in the model. Due to the use of a nanocrystalline core, the increase in CM inductance does not significantly add weight, as it often only requires a single extra turn, making the effect negligible for our setup.

Comparing the required L_{CM} for the conventional VSIs, it can be seen that the 2L requires significantly more inductance than the T-type, which requires slightly more than the NPC/ANPC. Furthermore, it can be observed from fig. 4.14 that interleaving also offers a benefit for the CM filter, as the interleaved topologies consistently require a lower CM inductance than their conventional counterparts.

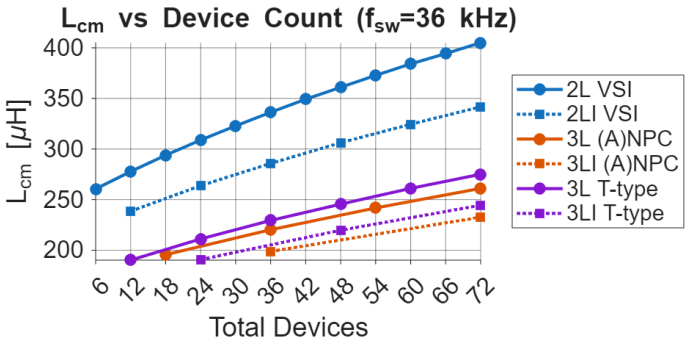


Figure 4.14: CM inductance relationship with the total number of devices. Operating point: $f_{\text{sw}} = 36\,\text{kHz}$ and if applicable, a 9 AWG interphase inductor inducing $\hat{I}_{\text{cir}} = 4.7\,\text{A} \approx 0.1\hat{I}_{\text{out,RMS}}$.

4.4 System Level Trade-Off Between Efficiency, Specific Power and THD

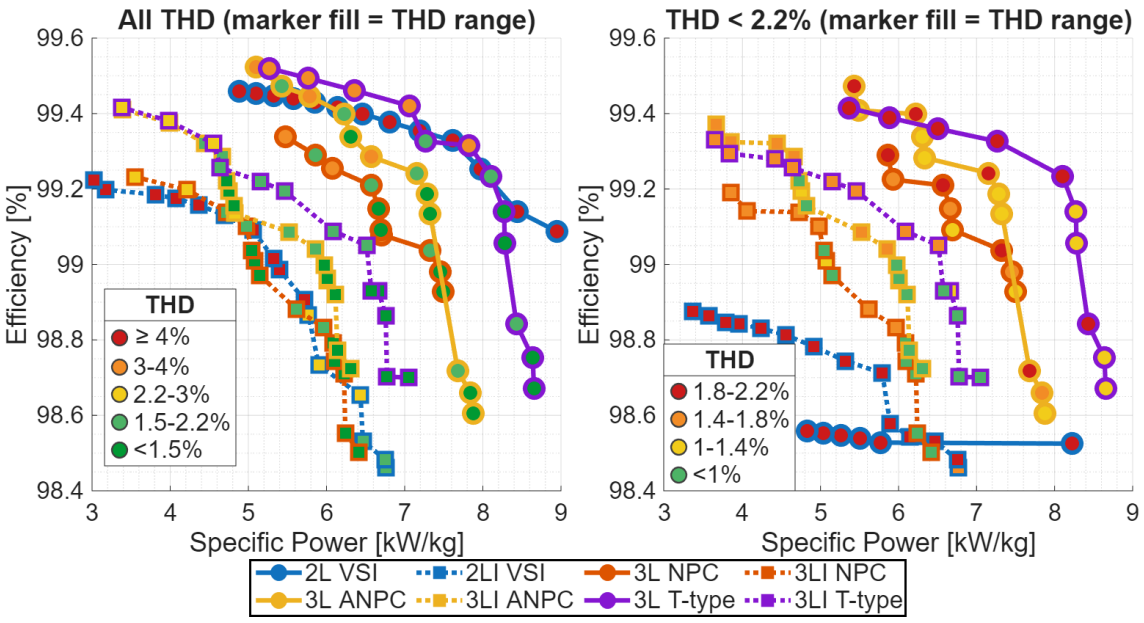


Figure 4.15: Pareto fronts of inverter designs in terms of efficiency versus specific power. Left, all designs, with marker fill indicating the corresponding THD range. Right, designs constrained to THD $\leq 2.2\%$, with marker fill denoting finer THD range.

In fig. 4.15, the Pareto front for inverter efficiency and specific power is shown across all topologies, where the marker fill identifies the THD range. For the unconstrained case on the left, the conventional inverters dominate over the interleaved inverters, mainly due to the interphase inductors. The 2L VSI is capable of reaching high specific power and high inverter efficiency, but it comes at the expense of increased THD, above 4%. In contrast, the 3L T-type and ANPC have high specific power with high efficiency at notably lower THD levels. The T-type can offer higher specific power than the ANPC when a drop in efficiency is permissible.

The right plot in fig. 4.15 applies a THD constraint of $\leq 2.2\%$, chosen to limit motor losses and ensure all inverter topologies can be fairly compared within a common operating

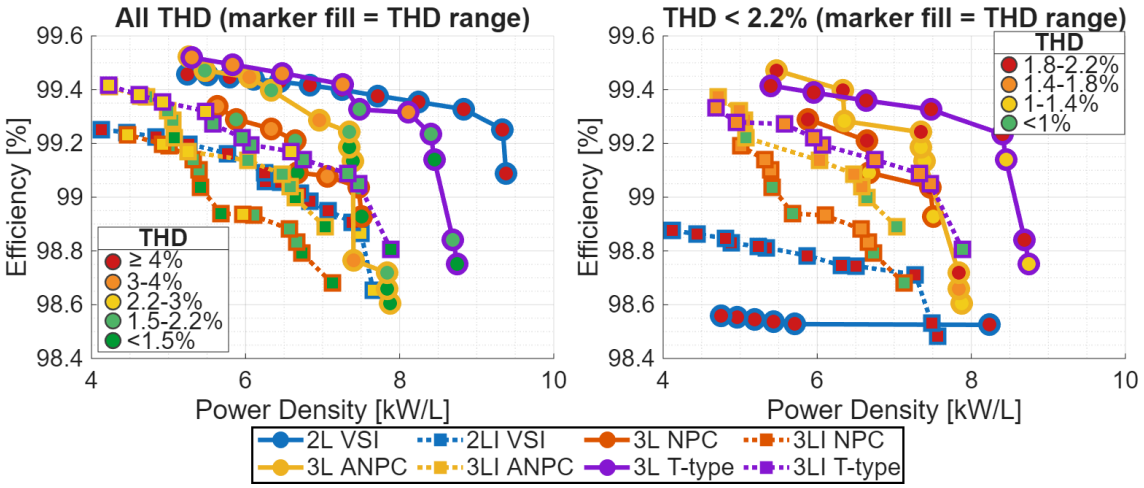


Figure 4.16: Pareto fronts of inverter designs in terms of efficiency versus power density. Left, all designs, with marker fill indicating the corresponding THD range. Right, designs constrained to THD $\leq 2.2\%$, with marker fill denoting finer THD range.

boundary. Under this constraint, the performance of the 2L VSI is strongly penalised, due to the higher required switching frequency, which reduces efficiency. The multilevel inverters still retained a high specific power and efficiency trade-off, where the T-type can offer a better specific power. However, the ANPC has lower switching losses growth (see fig. 4.3) and thus compared to the T-type can offer lower THD at the same performance.

As anticipated from the THD analysis in section 4.2, the interleaved inverters remain unable to compete with their conventional counterparts, except the 2LI VSI, which achieves improved efficiency for the same THD but only at the expense of reduced specific power.

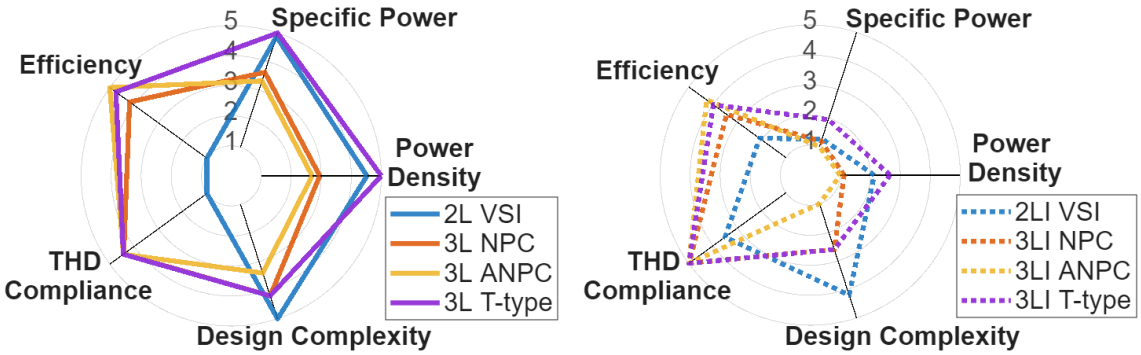
In fig. 4.16, the analysis is performed again, but now for the power density. While the overall trends are similar to the specific power analysis, the relative performance rankings between certain topologies have shifted. This is expected, as both are correlated. However, the 2L VSI shows the best power density possibility, with the caveat that when limiting the THD, it is heavily penalised again. The interleaved T-type inverter outperforms the conventional NPC for the power density efficiency trade-off.

Overall, figs. 4.15 and 4.16 highlight that once realistic THD limits are imposed, multilevel topologies, particularly the ANPC and T-type, consistently provide the best compromise between efficiency, specific power, power density and THD.

4.5 Overall Benchmarking

In fig. 4.17, the overall benchmarking of the investigated inverter topologies is visualised through a spider chart. A larger and more balanced shape indicates a superior overall performance profile. From this, the conventional 3L T-type is the superior choice. It gives the most balanced performance across all metrics. In contrast, the 2L VSI performs well in design complexity, power density and specific power, but its performance is undermined by a low efficiency and THD compliance. The efficiency of the 2L VSI was competitive when a low THD was not required (see fig. 4.15), so the 2L VSI is only a good solution when low THD is not required. The ANPC and NPC offer a less balanced performance than the T-type, but better than the 2L VSI.

When comparing the interleaved to the conventional inverters, it is apparent that their performance is lower, as their shapes are smaller. Where only for the THD compliance, do



(a) (b)

Figure 4.17: Performance comparison chart for a stringent THD requirement, (a) for the conventional inverters, (b) for the interleaved inverters. Raking system given in chapter E

they have a better performance than their conventional counterparts. This visually confirms the conclusion of the preceding sections, which concluded that generally the mass, volume, and loss penalties of the required interphase inductors outweigh the filtering benefits at a system level. For the interleaved inverters, the 3LI T-type offers the best trade-offs, but it does not compete against the conventional 3L T-type.

The spider chart analysis clearly indicates that the multilevel inverters can consistently outperform the two-level inverters and that the conventional inverters can consistently outperform the interleaved inverters.

Chapter 5

Discussion

5.1 Remarks and Observations

The outcome of this research has provided insight into how the most suitable inverter topology for an aerospace application can be selected, revealing that for the 20 kW compressor system, there is no single 'best' VSI. Rather, the application priorities play a significant role, and the interpretation of the results hinges on the 'efficiency cost' each VSI topology must pay to produce a low output current THD. For applications with stringent current THD requirements, 3L VSIs consistently and significantly outperform their 2L counterparts. Generating smaller voltage steps allows the 3L inverters to achieve lower voltage THD, reducing the switching frequency required to achieve a target current THD. This, in turn, reduces the switching losses, which leads to higher efficiency and a smaller, lighter heatsink. In contrast, the 2L VSI is forced to compensate for its larger output voltage steps by operating at close to double the switching frequency to meet the same low-THD target. Furthermore, the switching losses for the 2L VSI also grow faster with switching frequency, compared to the 3L VSIs, as shown in fig. 4.3.

Following this logic, it is expected that the interleaved inverters would outperform due to having more voltage levels and destructive interference, reducing the filtering requirements. This is where the system-level approach shows that the added interphase inductor mass is significantly more than the mass and volume reduction in the EMC filter (fig. 4.8). Furthermore, the efficiency loss inside the interphase inductor outweighs the efficiency gain from a lower switching frequency (fig. 4.7a). This conclusion is dependent on the interleaved modulation strategy. In particular, the performance of the 2LI VSI is negatively impacted by the use of equivalent SVM instead of true SVM [16]. If true SVM was implemented, the THD of the 2LI VSI would be equal to that of the 3L VSI, improving its performance. Even with this improved THD, it is unclear if the 2LI VSI could overcome the fundamental mass and loss penalties of its required interphase inductor. This highlights that the implementation can shift the performance metrics.

For the specific compressor application, the results demonstrate that for a fair comparison, component-level intuition can be misleading, and system-level trade-offs that account for the interaction between subsystems must be considered. For example, a counter-intuitive result from the system-level approach is that when initially adding devices to the 2L VSI, the total system mass decreases (fig. 4.11). While adding devices increases the component mass, the net system mass decreases because the resulting efficiency gain reduces the heatsink mass by a greater amount. Similarly, for several topologies, increasing the switching frequency eventually increased the total mass (fig. 4.9), as the reduction in passive component size was outweighed by the significant mass penalty of the larger heatsink

required to dissipate the higher switching losses. A final non-obvious trade-off was revealed in the design of the interphase inductor, where using a thicker, lower-resistance wire was found to be less efficient at high circulating currents (fig. 4.5). The assumption that lower resistance is always better was proven false, as the thicker wire required a larger magnetic core, and the resulting increase in core losses surpassed the savings in conduction losses. These findings prove the need for the system-level design framework, as only by evaluating the interactions between subsystems can these critical, non-obvious design trade-offs be revealed.

This thesis provides a method for selecting a suitable inverter topology for an aerospace application. The selection process starts with a rigorous definition of the application priorities. This includes which metrics are most important and in which order, be it minimising mass, maximising efficiency or a low THD limit. Only after these priorities are well established can the framework guide the selection process, where the result varies depending on the system specifications and design choices under investigation. The priorities for the 20 kW high-speed compressor application are, in order: a current THD limit of 2.2% (to limit motor losses), low mass, and high efficiency. For this application, the spider chart (fig. 4.17 and Pareto-fronts (fig. 4.15) provide a clear, visual tool for topology selection. In this case, the 3L topologies come out on top, with the T-type offering the best overall balance. However, if the application priorities were to change, the optimal topology would likely change as well. For instance, an application with relaxed THD and efficiency requirements, but very stringent volume requirements, might result in the 2L VSI being the most suitable inverter. As seen in Figure 4.16, it can offer the highest power density due to its compact PCB footprint. The ultimate value of this thesis lies not just in this specific result, but in demonstrating the capability of the system-level framework to produce clear, quantitative and reproducible comparisons.

5.2 Limitations

While the developed framework provides a robust basis for comparing inverter topologies, the research has several limitations that should be acknowledged:

- **Simplified EMI simulation models**. The EMI models used for the filter design were simplified to ensure computational feasibility. The approach separates the analysis of DM and CM noise, which does not fully account for mixed-mode emissions that occur in practice [22]. Furthermore, key parasitics such as the DC-link capacitor's stray inductance and parasitic capacitances were neglected. Including these effects would improve the model's accuracy and likely result in a larger EMC filter design that is more heavily dependent on the topology. Furthermore, the models rely on exact parasitic values, but these are heavily design dependent. Another potential cause of error is that the EMI spectrum has only been simulated at the nominal voltage and maximum current, and not the complete operating range. The change in voltage affects the noise generation, and the change in current affects the size of the inductors due to core saturation.

- **Suboptimal modulation for interleaved inverters**. This study employed an equivalent sequence SVM for the interleaved topologies due to its simpler implementation. This method does not achieve the same level of performance as a true SVM scheme, resulting in higher THD. Consequently, the performance of the interleaved topologies, particularly the 2LI VSI, may be understated in this comparison,

as a more advanced modulation strategy could improve their efficiency and waveform quality.

- **Subjectivity in the optimisation framework**. The framework's design selection was guided by criteria that, while systematic, included subjective elements. The $score = 2\tilde{m} + \tilde{V}$ metric applies an arbitrary 2:1 weighting to mass over volume, and key constraints like the 1% DC-link voltage ripple were self-imposed rather than derived from regulations. Consequently, the resulting "optimal" designs are tailored to these specific priorities, and a different weighting or set of constraints could lead to different conclusions, even though the comparative methodology remains fair.

- **Approximations in physical and mechanical modeling**. To manage the complexity of evaluating 780 unique designs, the physical realisation of components was approximated. The heatsink was sized using a generalised thermal performance model (CSPI/MPI) instead of a detailed thermo-fluid analysis, which may not accurately capture performance for all geometries. Similarly, the mass and volume of the power PCB, housing, and other components were based on estimates and idealised shapes, neglecting the detailed mechanical considerations of assembly, structural integrity, and manufacturability that would be required for a physical prototype.

- **Idealised system and loss modelling**. The simulation models for system performance included several idealisations. Key factors such as semiconductor dead time, the effect of gate driver resistance, and the need for active neutral-point balancing circuits for the NPC and ANPC topologies were not included in the loss calculations. These factors would introduce additional losses and affect the output waveform in a practical implementation, slightly reducing the reported efficiency figures.

5.3 Recommendations for Future Work

The findings and limitations of this thesis point to several promising avenues for future research that can build upon the established framework:

- **Advanced modulation schemes for interleaved topologies**. This study used a simplified modulation strategy for interleaved inverters. A critical next step is to implement and evaluate more advanced schemes, such as true SVM. This would likely reduce the circulating currents and significantly improve the THD of the interleaved topologies, potentially making the 2LI VSI competitive with 3L inverters and providing a more definitive assessment of its viability. This also holds for the conventional inverters, as there are other PWM techniques that can reduce CM voltage, efficiency or THD [5].

- **Hybrid time-frequency domain EMI simulation**. To overcome the trade-off between accuracy and simulation speed, future work should focus on developing a hybrid EMI modelling approach. This would involve using time-domain simulations to accurately characterise the high-frequency noise sources generated by the switching devices, and then applying this data to a frequency-domain model of the system. Which can accurately predict the required filter sizing. This method would enable a more accurate and computationally efficient EMC filter design.

- **Motor loss model**. Currently, the THD is used as an indicator for motor losses. Having a motor loss model would allow for a direct quantification of how the inverter impacts motor losses, providing a more complete view of the system-level trade-offs.

- **Expansion of the comparative framework**. The developed framework can be expanded to provide an even more comprehensive comparison. This includes investigating higher levels to see if the performance benefits continue to scale. As well as additional types of inverters to identify additional well-performing VSI topologies. The evaluation performed with the framework should also comprise an analysis across the operating range. Furthermore, the framework should be extended to include other critical aerospace performance metrics such as reliability, cost and fault tolerance.

- **Evaluation of alternative component technologies**. This research focused on SiC-MOSFETs, film capacitors and specific core materials (Edge and nanocrystalline). The framework could be used to evaluate the system-level impact of emerging component technologies. Where Gallium Nitride (GaN) devices can reduce switching losses, their use is possible due to the lower required blocking voltage of high level VSI. Investigating alternative magnetic core and capacitor technologies might yield further reductions in the mass and volume of passive components and possible different inverter trade-offs.

- **Hardware prototyping and experimental validation**. The ultimate validation of this simulation-based research is the construction of a hardware prototype. Building and testing one of the Pareto-optimal designs can provide experimental data to verify the accuracy of the efficiency, THD, EMI, and thermal models, confirming the conclusions drawn in this thesis.

- **Expand analytical modelling within the framework.** This work's framework was limited by computationally intensive time-domain simulations for EMI and losses. A key future step would be to develop and validate fast analytical models to replace these simulation blocks. This would drastically reduce computation time, enabling a far greater design space exploration (e.g., sweeping more components or finer frequency steps) and offering more immediate feedback on design choices.

Chapter 6

Conclusion

This thesis addressed the gap in VSI system-level evaluation for aerospace applications, specifically focused on a 20 kW high-speed compressor system. It developed and applied a system-level optimisation framework. Enabling the comparison to go beyond a theoretical topology analysis and delivering a quantitative analysis of the real-world trade-offs between efficiency, specific power, power density and THD. This was done to answer the four main research questions, with the key findings summarised below.

1. **Which measures need to be taken to have a fair comparative analysis of the inverters?** A fair comparison of VSI topologies is possible due to the development of an automated, multi-stage design and optimisation framework. This framework required three main principles. The first is that each inverter is treated as a complete system. This means that the mass, volume and loss of all critical subsystems (e.g. EMC filter, heatsink, housing) are included. Secondly, it requires that all designs meet the same set of system specifications. This includes regulatory constraints (DO-160G), operating requirements (e.g. 20 kW compressor) and design constraints (e.g. maximum temperature, ripple). Lastly, it requires that the design process steps and methods be the same for all designs.

2. **How to select the most suitable component sizes for each inverter?** This thesis sets out a methodology for component selection, rather than a set of single "best" components. The "most suitable" components are thus identified by the optimisation framework, which systematically sweeps the design choices. The selection is based on analytical equations and simulations. A novel equation of the required interphase inductance based on the maximum circulation inductance was used in this framework.

3. **What is the performance of each inverter for all key performance metrics?** Figure 4.17 summarises each inverter performance across design complexity, efficiency, THD, specific power and power density. Providing clear insights into the strengths and weaknesses of each topology.

    - **2L VSI.** This topology is only competitive if high THD is acceptable. As its voltage THD is high (76% on average), forcing a high switching frequency for a low current THD, leading to a substantial efficiency penalty.
    - **3L VSIs (T-type, ANPC, NPC).** These offer the best balanced performance. This is because they can generate smaller output voltage steps, resulting in a lower voltage THD (39% on average). This enables much lower switching frequencies, improving the efficiency. This gives them the best trade-off between

the key metrics, where the T-type in particular shows the best overall performance.

- **Interleaved VSIs (2LI, 3LI).** These topologies consistently underperform. The significant extra mass, volume and loss that comes from the interphase inductor outweigh the filtering benefits at a system level.

4. **How can the most suitable inverter topology for an aerospace application be selected?** The 'most suitable' inverter is not a fixed choice, but changes with application priorities. This thesis demonstrates that the selection must be made through a system-level, multi-objective trade-off analysis, for which the design framework and tools (e.g., Pareto fronts and summary charts) were created.

While the optimisation framework enables a comprehensive analysis, its limitations, detailed in section 5.2, must be considered. The performance of the interleaved topologies, for instance, is underestimated due to the use of equivalent SVM instead of true SVM. Similarly, the EMI models were simplified to achieve computational feasibility. These limitations can be addressed with the recommendations outlined in section 5.3. These include implementing more advanced modulation schemes to fairly compare interleaved VSIs, developing a hybrid time-frequency domain EMI simulation to reduce the simulation time, testing actual hardware to validate the results and expanding the framework to incorporate motor losses, reliability and cost.

To conclude, this thesis addressed the critical gap in VSI system-level evaluation for aerospace applications. While the results demonstrate that 3L VSIs offer a superior, well-balanced performance for the aerospace high-speed compressor, the primary contribution of this research is the design and optimisation framework that enabled this analysis. This framework provides a robust and reproducible methodology that moves the field beyond theoretical topology comparisons by delivering a quantitative analysis of system-level trade-offs. It ultimately enables engineers to make quantitative design decisions that are directly aligned with the application priorities.

Bibliography

[1] T. Lombardo, *Aviation - iea*, 2025. [Online]. Available: https://www.iea.org/energy-system/transport/aviation.

[2] E. Commission, *Reducing emissions from aviation*, 2025. [Online]. Available: https://climate.ec.europa.eu/eu-action/transport-decarbonisation/reducing-emissions-aviation_en.

[3] Government of the Netherlands. "Aviation policy." Accessed: 2025-10-31. [Online]. Available: https://www.government.nl/topics/aviation/aviation-policy.

[4] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-board microgrids for the more electric aircraft—technology review," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5588–5599, 2019. DOI: 10.1109/TIE.2018.2881951.

[5] M. M. Naveed, M. S. Shah, N. Moonen, M. Gerber, and T. B. Soeiro, "Advancing high-frequency inverter design in more electric aircraft: Challenges and research perspectives," *IEEE Open Journal of the Industrial Electronics Society*, vol. 6, pp. 1423–1447, 2025. DOI: 10.1109/OJIES.2025.3597042.

[6] Radio Technical Commission for Aeronautics (RTCA), "Environmental conditions and test procedures for airborne equipment (do-160g)," RTCA, Inc., Washington, DC, USA, Tech. Rep. DO-160G, 2010, Includes Change 1 (2014).

[7] S. Munawar, M. S. Iqbal, M. Adnan, M. Ali Akbar, and A. Bermak, "Multilevel inverters design, topologies, and applications: Research issues, current, and future directions," *IEEE Access*, vol. 12, pp. 149 320–149 350, 2024. DOI: 10.1109/ACCESS.2024.3472752.

[8] X. Zhang, D. Boroyevich, and R. Burgos, "Design and integration of interphase inductors for interleaved three phase voltage-source-inverters in dc-fed motor drive systems," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 2626–2631. DOI: 10.1109/IPEC.2014.6869960.

[9] S. Choudhury, M. Bajaj, T. Dash, S. Kamel, and F. Jurado, "Multilevel inverter: A survey on classical and advanced topologies, control schemes, applications to power system and future prospects," *Energies*, vol. 14, no. 18, 2021, ISSN: 1996-1073. DOI: 10.3390/en14185773. [Online]. Available: https://www.mdpi.com/1996-1073/14/18/5773.

[10] J. A. Anderson, L. Schrittwieser, M. Leibl, and J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," in *2017 IEEE International Telecommunications Energy Conference (INTELEC)*, 2017, pp. 456–463. DOI: 10.1109/INTLEC.2017.8214178.

[11] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020. DOI: 10.1109/OJPEL.2020.3018220.

[12] A. Bali, X. Zhang, A. Bose, K. S. Haran, and A. Stillwell, "A 7-level interleaved hybrid active neutral point clamped converter for high-frequency low-inductance motors," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 561–566. DOI: 10.1109/APEC48139.2024.10509087.

[13] H.-W. Choi and K.-B. Lee, "Reduction method of circulating current in parallel three-level inverters using modified discontinuous pulse-width modulation based on interleaving scheme," *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 2322–2333, 2024. DOI: 10.1109/TPEL.2023.3327945.

[14] B. Evstatiev, *Mutually coupled inductors: Coupling coefficient; power and energy of mutually coupled inductors; analysis of circuits with mutually coupled inductor*, Lecture notes, Theory of Electrical Engineering, University of Ruse, Accessed: 2025-11-06. [Online]. Available: https://www.uni-ruse.bg/disciplines/TE/Lecture%20notes/Lectures%20notes%20Mutually%20coupled%20inductors.pdf.

[15] N. Mohan, T. Underland, and W. Robbins, *Power electronics Converters, Applications and Design*, Second. New York: Wiley, 1995.

[16] K. Shukla and R. Maheshwari, "A generalized method to generate carrier-based 3l pwm techniques using two parallel interleaved 2l vsis," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 6, pp. 4177–4188, 2019. DOI: 10.1109/TIE.2018.2860523.

[17] Plexim GmbH, *Plecs user manual, version 4.9*, 4.9, Accessed: 2025-10-31, Zurich, Switzerland: Plexim GmbH, 2024. [Online]. Available: https://www.plexim.com/sites/default/files/plecsmanual.pdf.

[18] C. Debruyne, B. Corne, P. Sergeant, J. Desmet, and L. Vandevelde, "Evaluation of the additional loss due to supply voltage distortion in relation to induction motor efficiency rating," in *2015 IEEE International Electric Machines & Drives Conference (IEMDC)*, 2015, pp. 1881–1887. DOI: 10.1109/IEMDC.2015.7409321.

[19] C. R. Paul, *Introduction to Electromagnetic Compatibility*, 2nd ed. Wiley-Interscience, 2006, ISBN: 9780471755005.

[20] P. Dahono, Y. Sato, and T. Kataoka, "Analysis and minimization of ripple components of input current and voltage of pwm inverters," *IEEE Transactions on Industry Applications*, vol. 32, no. 4, pp. 945–950, 1996. DOI: 10.1109/28.511653.

[21] T. Hoeksma, "A comparative study of the effect of thermal management on emc on an existing inverter," MSc Electrical Engineering Internship Report, University of Twente, 2025.

[22] F. A. Kharanaq, A. Emadi, and B. Bilgin, "Modeling of conducted emissions for emi analysis of power converters: State-of-the-art review," *IEEE Access*, vol. 8, pp. 189 313–189 325, 2020. DOI: 10.1109/ACCESS.2020.3031693.

[23] G. A. Raducu, "Control of grid side inverter in a b2b configuration for wind turbine applications," Master's thesis, Aalborg University, Aalborg, Denmark, 2008. [Online]. Available: https://projekter.aau.dk/projekter/files/17642356/PED10.pdf.

[24] L. Ran, S. Gokani, J. Clare, K. Bradley, and C. Christopoulos, "Conducted electromagnetic emissions in induction motor drive systems. ii. frequency domain models," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 768–776, 1998. DOI: 10.1109/63.704154.

[25] Q. Liu, W. Shen, F. Wang, D. Boroyevich, V. Stefanovic, and M. Arpilliere, "Experimental evaluation of igbts for characterizing and modeling conducted emi emission in pwm inverters," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 4, 2003, 1951–1956 vol.4. DOI: 10.1109/PESC.2003.1217751.

[26] Q. Liu, F. Wang, and D. Boroyevich, "Modular-terminal-behavioral (mtb) model for characterizing switching module conducted emi generation in converter systems," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1804–1814, 2006. DOI: 10.1109/TPEL.2006.882903.

[27] A. C. Baisden, D. Boroyevich, and F. Wang, "Generalized terminal modeling of electromagnetic interference," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 2068–2079, 2010. DOI: 10.1109/TIA.2010.2058836.

[28] G. Grandi, D. Casadei, and U. Reggiani, "Common- and differential-mode hf current components in ac motors supplied by voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 16–24, 2004. DOI: 10.1109/TPEL.2003.820564.

[29] L. Wang, C. Ngai-Man Ho, F. Canales, and J. Jatskevich, "High-frequency modeling of the long-cable-fed induction motor drive system using tlm approach for predicting overvoltage transients," *IEEE Transactions on Power Electronics*, vol. 25, no. 10, pp. 2653–2664, 2010. DOI: 10.1109/TPEL.2010.2047027.

[30] L. Ran, S. Gokani, J. Clare, K. Bradley, and C. Christopoulos, "Conducted electromagnetic emissions in induction motor drive systems. i. time domain analysis and identification of dominant modes," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 757–767, 1998. DOI: 10.1109/63.704152.

[31] H. H. Sathler, B. Cougo, J.-P. Carayon, F. Costa, and D. Labrousse, "Modeling of common-mode voltage source for multilevel inverter topologies," in *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–3. DOI: 10.1109/EMCEUROPE48519.2020.9245681.

[32] R. Erickson, "Optimal single resistors damping of input filters," in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, vol. 2, 1999, 1073–1079 vol.2. DOI: 10.1109/APEC.1999.750502.

[33] Magnetics, Inc., "Edge® powder cores – technical bulletin," Magnetics, Inc., Pittsburgh, PA, USA, Technical Bulletin, 2023, Accessed: 2025-10-27. [Online]. Available: https://www.mag-inc.com/Media/Magnetics/File-Library/Product%20Literature/Powder%20Core%20Literature/Magnetics-Edge-Powder-Cores-Bulletin-2023-EN.pdf.

[34] Magnetics, Inc. "Common mode filter design tools and general information." Accessed: 2025-10-27, Magnetics, Inc. [Online]. Available: https://designtools.mag-inc.com/commonmode/.

[35] Vishay Intertechnology, Inc., "Mkp1848c dc-link – metallized polypropylene dc-link film capacitor, technical datasheet (doc. no. 26015, rev. 09-aug-2023)," Vishay Intertechnology, Inc., Datasheet 26015, 2023, Accessed: 2025-10-27. [Online]. Available: https://www.vishay.com/docs/26015/mkp1848cdclink.pdf.

[36] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, "Ac/dc/ac pwm converter with reduced energy storage in the dc link," *IEEE Transactions on Industry Applications*, vol. 31, no. 2, pp. 287–292, 1995. DOI: 10.1109/28.370275.

[37] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proceedings of the 2005 International Conference on Power Electronics, Intelligent Motion, Power Quality (PCIM Europe 2005)*, 2005, pp. 608–619.

[38] U. Drofenik and J. W. Kolar, "Analyzing the theoretical limits of forced air-cooling by employing advanced composite materials with thermal conductivities $>$ 400w/mk," in *4th International Conference on Integrated Power Systems*, 2006, pp. 1–6.

[39] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded-fin heat sink," *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 509–520, 2015. DOI: 10.1109/TIA.2014.2336977.

[40] U. Drofenik and J. W. Kolar, "Sub-optimum design of a forced air cooled heat sink for simple manufacturing," in *2007 Power Conversion Conference - Nagoya*, 2007, pp. 1189–1194. DOI: 10.1109/PCCON.2007.373116.

[41] M. Cavcar, "The international standard atmosphere (isa)," Anadolu University, Tech. Rep., 2000, Accessed: 2025-10-27. [Online]. Available: http://fisicaatmo.at.fcen.uba.ar/practicas/ISAweb.pdf.

[42] Orion Fans. "How to select the right fan for your application." Accessed: 2025-10-27. [Online]. Available: https://orionfans.com/how-to-select-the-right-fan-for-your-application/.

[43] G. Verkerk, *BiNaS: Handbook for the Natural Sciences and Mathematics*, 6th edition. Groningen, Netherlands: Noordhoff Uitgevers, 2015. [Online]. Available: https://www.jeltad.com/binas.pdf.

[44] Wikipedia contributors. "Fr-4." Accessed: 2025-10-27. [Online]. Available: https://en.wikipedia.org/wiki/FR-4.

Appendix A

Circulation Current

Circulating current (I_{cir}) is the undesired current that flows between the parallel-connected inverter legs in interleaved VSIs. It is created due to a voltage difference between the legs, where it does not contribute to the load current. I_{cir} poses a significant challenge in the design and operation of interleaved VSIs, impacting system efficiency, mass, volume and saturating the interphase inductor core. This chapter presents an analytical derivation of these currents based on the equivalent SVM technique established in chapter 2. The resulting peak circulation current ($\hat{I}_{\text{cir}}$) and RMS circulation current ($I_{\text{cir,RMS}}$) expressions are formulated as a function of the modulation index (m). To simplify the analysis and create a theoretical baseline, this derivation makes a few assumptions. First of all, it assumes ideal converter operation, neglecting non-idealities such as dead time, switching delays, and component voltage drops. The ratio between the fundamental output frequency (f_{ac}) and the switching frequency (f_{sw}) is assumed to be infinite. Finally, the interleaving angle is assumed to be 180°.

A.1 Derivation of Circulation Current for Two-Level (2L)

A.1.1 Circulation Current in a 2LI VSI

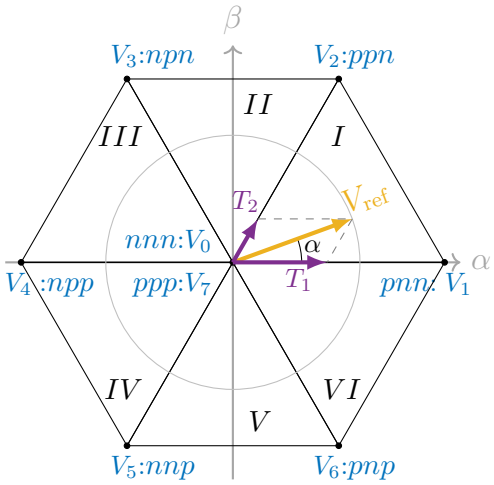


Figure A.1: 2L SVM diagram.

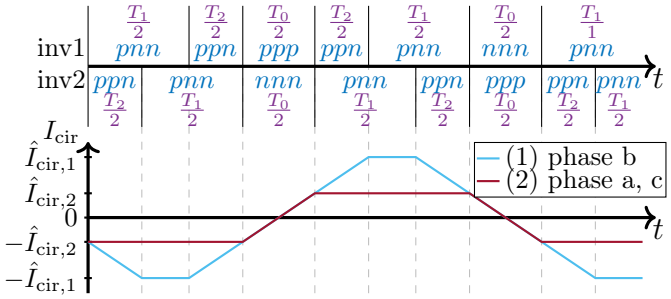


Figure A.2: Timing and resulting circulation current of 2LI VSI at $\alpha = 20°$, $m = 0.8$ and $\varphi = 180°$.

In this section, the circulation current in a 2LI VSI using equivalent SVM is presented. Figure A.1 shows the SVM diagram for a 2L configuration. Each of the corners of the hexagon is a large vector (V_1 to V_6), and in the middle, there are two zero vectors (V_0, V_7). The three-letter code states which switch is turned on per phase, p is used for the top switch closed, and n is used for the bottom switch closed. The reference vector V_{ref} rotates with the modulated frequency through the diagram, where the two adjacent large vectors and the zero vectors are used within a switching period to synthesise the desired reference vector. The duty cycles of these vectors are calculated based on the instantaneous position of the reference vector within the hexagonal space vector diagram and can be found as [23]:

$$T_0 = T_{\text{sw}} \left(1 - \frac{\sqrt{3}}{2} m \cos\left(\frac{(2n-1)\pi}{6} - \alpha\right)\right) \tag{A.1}$$

$$T_1 = \frac{\sqrt{3}}{2} m T_{\text{sw}} \sin\left(\frac{n\pi}{3} - \alpha\right) \tag{A.2}$$

$$T_2 = \frac{\sqrt{3}}{2} m T_{\text{sw}} \sin\left(\alpha - \frac{(n-1)\pi}{3}\right) \tag{A.3}$$

$$T_{\text{sw}} = T_0 + T_1 + T_2 \tag{A.4}$$

$$m = \frac{V_{\text{ref}}}{\frac{1}{2} V_{\text{DC}}} \tag{A.5}$$

Here α is the angle (in radians) of the reference vector, $n \in \{1, 2, 3, 4, 5, 6\}$ is the sector in which the reference vector points, and m is the modulation index. T_0 is the time per switching cycle spent equally between the zero voltage vectors V_0 and V_7. T_1 is the time spent on the large voltage vector in the current sector with the smallest angle of α, and T_2 is the time spent on the largest angle. For example, in sector 1, T_1 is the time spent on V_1 and T_2 on V_2.

In fig. A.2, a timing scheme and resulting circulation current are shown for a stationary voltage vector in sector 1. At the top, the switching states are shown for both legs, along with their application time. Below, the resulting circulation current waveform is shown. For each phase, a difference in switching states results in a voltage over the interphase inductor (for inv1|inv2: $p|n \rightarrow V_{\text{DC}}$, $n|p \rightarrow -V_{\text{DC}}$). In fig. A.2, it can be seen that for phases a and c, the change in circulation current only occurs during T_0, as otherwise the voltage over the inductor is zero. Where it goes from 0 A to the peak current ($\hat{I}_{\text{cir},2}$) in $\frac{1}{4}T_o$. Thus, for these two phases at any point in the sector, the peak circulation current

Table A.1: 2-level lookup table per sector for the peak circulation current equation, governing which phase.

sector (n)	**Phase $\hat{I}_{\mathbf{cir,2}}$** eq. (A.6)	**Phase $\hat{I}_{\mathbf{cir,1}}$** eq. (A.7)
1	a, c	b
2	b, c	a
3	a, b	c
4	a, c	b
5	b, c	a
6	a, b	c

can be calculated as:

$$\hat{I}_{\text{cir},2}(m,\alpha) = \frac{1}{L_{\text{cir}}}\int_0^{\frac{1}{4}T_0} V_{\text{DC}}\text{dt} = \frac{V_{\text{DC}}}{L_{\text{cir}}}\frac{T_0}{4}. \tag{A.6}$$

The peak current for phase b ($\hat{I}_{\text{cir},1}$) can be found from the time where the voltage over the coupled inductor is V_{DC}, which is $\frac{1}{2}T_0 + \min(T_1, T_2)$. Over this time, the circulation current goes from peak to peak. Thus, the peak circulation current can be found as:

$$\hat{I}_{\text{cir},1}(m,\alpha) = \frac{V_{\text{DC}}}{L_{\text{cir}}}\left(\frac{T_0}{4} + \frac{1}{2}\min(T_1, T_2)\right). \tag{A.7}$$

This waveform is not unique to sector 1. The only difference between sectors is which phase has the large peak amplitude ($\hat{I}_{\text{cir},1}$ of eq. (A.7)) and which two have the lower peak amplitude ($\hat{I}_{\text{cir},2}$). table A.1 shows per sector which phase corresponds to which equation. With this information, the maximum circulation current is known at any point in the SVM diagram, assuming a near infinite ratio between f_{sw} and f_{ac}.

A.1.2 Maximum Circulation Current in the 2LI VSI

The peak circulation current over the full range of $\alpha \in [0, 2\pi]$ can be found by investigating only the first sector, as the waveform is symmetric per sector. First, the maximum of $\hat{I}_{\text{cir},2}(m,\alpha)$ of eq. (A.6) is investigated. In sector 1, $\hat{I}_{\text{cir},2}(m,\alpha)$ is maximised for $\max(T_0)$, this occurs when $\cos\left(\frac{(2n-1)\pi}{6} - \alpha\right)$ is minimized. This in turn occurs at the boundaries $\alpha = [0, \frac{\pi}{3}]$, filling this into eq. (A.6) and substituting eq. (A.1) yields the maximum $\hat{I}_{\text{cir},2}$:

$$\hat{I}_{\text{cir},2}(m) = \frac{V_{\text{DC}}T_{\text{sw}}}{4L_{\text{cir}}}(1 - \frac{3}{4}m). \tag{A.8}$$

For $m = 0$ this phase circulation current maximum is maximised, equaling $\frac{V_{\text{DC}}T_{\text{sw}}}{4L_{\text{cir}}}$, for higher m it decreases until 0 A for $m = \frac{4}{3}$.

Next the maximum value of $\hat{I}_{\text{cir},1}(m,\alpha)$ of eq. (A.7) is investigated. $\hat{I}_{\text{cir},1}(m,\alpha)$ is maximised when $\min(T_1, T_2)$ is maximised, which occurs when $T_1 = T_2$ at $\alpha = \frac{\pi}{6}$. At that angle this part of the equation: $\frac{1}{4}T_0 + \frac{1}{2}\min(T_1, T_2)$ simplifies into $\frac{1}{4}T_{\text{sw}}$. Note that this does not depend on the modulation index. Sustituting this maximisation into eq. (A.7) yields the maximum $\hat{I}_{\text{cir},1}$:

$$\boxed{\hat{I}_{\text{cir,2L}} = \hat{I}_{\text{cir},1} = \frac{V_{\text{DC}}T_{\text{sw}}}{4L_{\text{cir}}}} \tag{A.9}$$

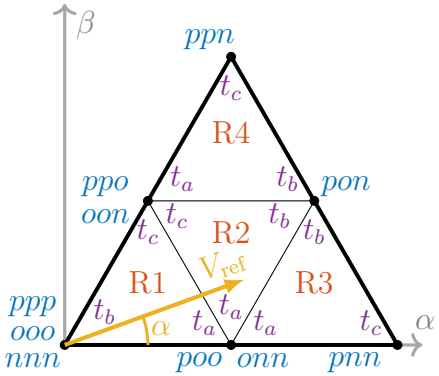


Figure A.3: Sector 1 of a 3-level SVM diagram.

Region	t_a	t_b	t_c
R1	$T_{\text{sw}}\left[m\sqrt{3}\sin\left(\frac{\pi}{3}-\alpha\right)\right]$	$T_{\text{sw}}\left[1-m\sqrt{3}\sin\left(\frac{\pi}{3}+\alpha\right)\right]$	$T_{\text{sw}}\left[m\sqrt{3}\sin(\alpha)\right]$
R2	$T_{\text{sw}}\left[1-m\sqrt{3}\sin(\alpha)\right]$	$T_{\text{sw}}\left[m\sqrt{3}\sin\left(\frac{\pi}{3}+\alpha\right)-1\right]$	$T_{\text{sw}}\left[1-m\sqrt{3}\sin\left(\frac{\pi}{3}-\alpha\right)\right]$
R3	$T_{\text{sw}}\left[2-m\sqrt{3}\sin\left(\frac{\pi}{3}+\alpha\right)\right]$	$T_{\text{sw}}\left[m\sqrt{3}\sin(\alpha)\right]$	$T_{\text{sw}}\left[m\sqrt{3}\sin\left(\frac{\pi}{3}-\alpha\right)-1\right]$
R4	$T_{\text{sw}}\left[2-m\sqrt{3}\sin\left(\frac{\pi}{3}+\alpha\right)\right]$	$T_{\text{sw}}\left[m\sqrt{3}\sin\left(\frac{\pi}{3}-\alpha\right)\right]$	$T_{\text{sw}}\left[m\sqrt{3}\sin(\alpha)-1\right]$

Table A.2: Applying time of the voltage vectors in sector 1 [23].

Both eqs. (A.8) and (A.9) have the same maximum value across the complete modulation index. However, eq. (A.8) decreases with modulation index, while eq. (A.9) remains constant at the peak value. Thus, when considering the complete modulated cycle, the maximum circulation current is equal to eq. (A.9), which is independent of modulation index.

A.2 Derivation of Circulation Current for Three-Level (3L)

A.2.1 Circulation Current in a 3LI VSI

The circulation current can also be derived for a 3LI VSI, where the circulation current is symmetric in all sectors. Furthermore, the circulation current is symmetric around the middle of the sector, so that we only need to analyse $\alpha \in [0, \frac{\pi}{6}]$. In fig. A.3, the first sector of a 3L SVM diagram is drawn, with the applying time per voltage vector indicated with t_a, t_b and t_c. table A.2 lists the application times for all four regions.

Regions 1 (R1) and 2 (R2) result in identical circulation current waveforms, for equal applying times, as seen in fig. A.4. Which phase corresponds to which waveform is again expressed in table A.1. For waveform (2), the peak circulation current can be found as:

$$\hat{I}_{\text{cir,R1/2,(2)}} = \frac{1}{L_{\text{cir}}} \int_0^{\frac{t_a+t_c}{4}} \frac{V_{\text{DC}}}{2} \mathrm{d}t = \frac{V_{\text{DC}}}{2L_{\text{cir}}} \cdot \frac{t_a+t_c}{4} \tag{A.10}$$

For waveform (1), it has an identical peak circulating current as proven below:

$$\hat{I}_{\text{cir,R1/2,(1)}} = \frac{V_{\text{DC}}}{L_{\text{cir}}} \left(\int_0^{\frac{\max(t_a,t_c)-\min(t_a,t_c)}{4}} \frac{1}{2} \mathrm{d}t + \int_0^{\frac{\min(t_a,t_c)}{4}} \mathrm{d}t \right) \tag{A.11}$$

$$= \frac{V_{\text{DC}}}{L_{\text{cir}}} \cdot \frac{\max(t_a,t_c) + min(t_a,t_c)}{8} = \frac{V_{\text{DC}}}{2L_{\text{cir}}} \cdot \frac{t_a+t_c}{4} \tag{A.12}$$

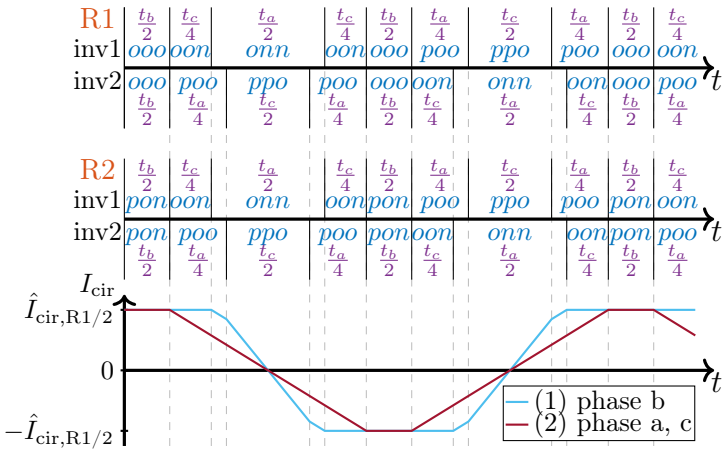


Figure A.4: States of the two inverter legs in sector 1, region 1 and 2 for fixed applying times. With the resulting circulation current waveform.

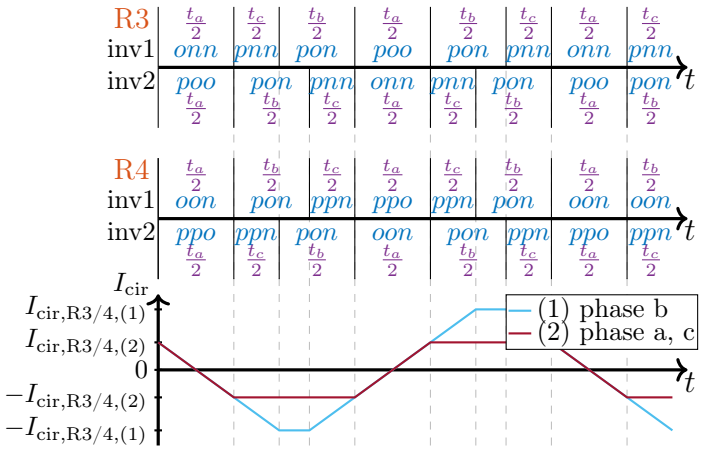


Figure A.5: States of the two inverter legs in sector 1, region 3 and 4 for fixed applying times. With the resulting circulation current waveform.

Regions 3 (R3) and 4 (R4) also result in the same waveform for equal applying times as seen in fig. A.5. However, waveforms (1) and (2) have different peak values, and which phase which waveform corresponds to is stated in table A.1. Using the timings stated in fig. A.5, the peak circulation current for waveform (1) in region 3 or 4 ($\hat{I}_{\text{cir,R}/4,(1)}$) can be derived as:

$$\hat{I}_{\text{cir,R3}/4,(1)}(m,\alpha) = \frac{V_{\text{DC}}}{2L_{\text{cir}}}\left(\frac{1}{4}t_a + \frac{1}{2}\min\left(t_b, t_c\right)\right) \tag{A.13}$$

For waveform (2), the peak circulation current in region 3 or 4 can similarly be derived as:

$$\hat{I}_{\text{cir,R3}/4,(2)}(m,\alpha) = \frac{V_{\text{DC}}}{2L_{\text{cir}}}\left(\frac{1}{4}t_a\right) \tag{A.14}$$

A.2.2 Maximum Circulation Current in 3LI VSI

For region 1 only, waveform (1) needs to be considered as it is always larger than waveform (2) because the applying times are non-negative. The maximum circulation current in region 1 ($\hat{I}_{\text{cir, R1}/2}(m)$) occurs when $\alpha = \frac{\pi}{6}$, as then $\min(t_b, t_c)$ is maximised. Substituting the equations from table A.2 into eq. (A.10) at $\alpha = \frac{\pi}{6}$ yields the maximum of:

$$\hat{I}_{\text{cir,R1}/2}\left(m, \frac{\pi}{6}\right) = \frac{V_{\text{DC}}T_{\text{sw}}}{8L_{\text{cir}}}m\sqrt{3} \tag{A.15}$$

When m increases beyond $\frac{1}{\sqrt{3}}$, $\alpha = \frac{\pi}{6}$ is no longer a valid value. If traversing the border between R1 and R2, t_b is zero and $t_a + t_c = T_{\text{sw}}$. So, a more general equation for R1 can be derived as:

$$\hat{I}_{\text{cir,R1}/2}(m) = \frac{V_{\text{DC}}T_{\text{sw}}}{8L_{\text{cir}}}\min\left(1, m\sqrt{3}\right) \tag{A.16}$$

For region 2, the time where $t_a + t_c$ is maximised is along the borders of R1, R3 and R4. Along the border of R1-R2, the peak circulation current value matches that of R1, given by $\frac{V_{\text{DC}}T_{\text{sw}}}{8L_{\text{cir}}}$. The border of R2-R3 and R2-R4 gives identical circulation current for a given m. Hence, analysis is confined to the R2-R3 border, spanning from $m = \frac{2}{3}, \alpha = 0\pi$ until $m = \frac{2}{\sqrt{3}}, \alpha = \frac{1}{6}\pi$. The α that corresponds to this border is given by:

$$\alpha_{\text{R2-R3}}(m) = \frac{\pi}{6}\frac{m - \frac{2}{3}}{\frac{2}{\sqrt{3}} - \frac{2}{3}}. \tag{A.17}$$

The circulation current in R2 is expressed as

$$I_{\text{cir,R2}}(m,\alpha) = \frac{V_{\text{DC}}T_{\text{sw}}}{8L_{\text{cir}}}\left(\sin\left(\frac{\pi}{3} - \alpha\right) + 1 - m\sqrt{3}\sin(\alpha)\right). \tag{A.18}$$

Substituting $\alpha_{\text{R2-R3}}(m)$ into the expression and simplifying yields the maximum circulating current in R2:

$$\hat{I}_{\text{cir,R2}}(m) = \frac{V_{\text{DC}}T_{\text{sw}}}{8L_{\text{cir}}} \cdot \begin{cases} 1, & m \in [\frac{1}{\sqrt{3}}, \frac{2}{3}] \\ 2 - m\sqrt{3} \cdot \cos\left(\frac{(m-\frac{2}{3})\pi\sqrt{3}}{4(3-\sqrt{3})} - \frac{\pi}{6}\right), & m \in [\frac{2}{3}, \frac{2}{\sqrt{3}}] \end{cases} \tag{A.19}$$

For regions 3 and 4, the resulting maximum circulation current is equal due to the symmetry. For R3 eq. (A.13) is always larger than eq. (A.14), where eq. (A.13) is maximimized when $t_b = t_c$. These applying times from table A.2 are equal when:

$$\sin(\alpha) - \sin\left(\frac{\pi}{3} - \alpha\right) = -\frac{1}{m\sqrt{3}}. \tag{A.20}$$

Solving this for α gives $\alpha_{\max}$, which is the angle at which the circulation current inside R3 is maximised:

$$\alpha_{\max}(m) = \frac{\pi}{6} + \arcsin\left(-\frac{1}{2m\sqrt{3}}\right). \tag{A.21}$$

Substituting $\alpha_{\max}$ into the applying times (table A.2) and substituting that into eq. (A.13) yields the maximum circulation current in R3 and R4:

$$\hat{I}_{\text{cir,R3/4}} = \frac{V_{\text{DC}} T_{\text{sw}}}{8 L_{\text{cir}}}. \tag{A.22}$$

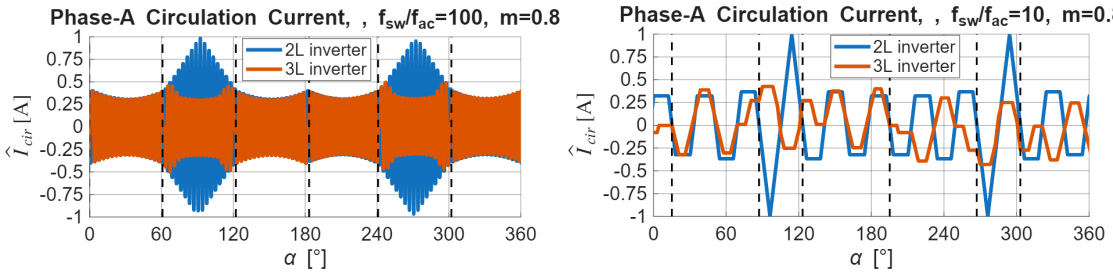
From this, it can be noted that at $\alpha_{\max}$ the peak circulation current is not dependent on modulation index.

Equations (A.15), (A.19) and (A.22) give the maximum circulation current inside the different regions of the SVM diagram. Where combining these equations, the maximum circulation current inside the SVM diagram for $m \in [0, \frac{2}{\sqrt{3}}]$ can be found as:

$$\boxed{\hat{I}_{\text{cir,3L}}(m) = \frac{V_{\text{DC}} T_{\text{sw}}}{8 L_{\text{cir}}} \min\left(m\sqrt{3}, 1\right)} \tag{A.23}$$

A.3 Verification of the Analytical Formulas

A.3.1 Waveform Verification



(a) (b)

Figure A.6: Simulated circulation current waveform for one modulated period, $m = 0.8$ and a constant ratio of $L_{\text{cir}} = \frac{V_{\text{DC}}}{4 f_{\text{sw}}}$. Where the vertical black line indicates the sector boundary used by the PLECS block. (a) for $\frac{f_{\text{sw}}}{f_{\text{ac}}} = 100$. (b) $\frac{f_{\text{sw}}}{f_{\text{ac}}} = 10$.

Using the PLECS SVM blocks and phase-shifting one carrier by 180°, an equivalent SVM modulator is created. This drives an ideal interleaved H-bridge and NPC inverter with an ideal coupled inductor, from which the circulation current waveforms are plotted in fig. A.6. The preceding analysis assumed that f_{sw} was significantly larger than f_{ac}, which holds for fig. A.6a. For the 2L, the peak is in the middle of the sector with the amplitude equal to the predicted value in eq. (A.9) without any error. For the 3L, the waveform follows

the predicted maximum circulation current envelope closely, and the maximum values also align with eq. (A.23) with an error less than 1%. When looking at the transitions between regions, there is a small transient waveform that is not zero. This induces a minor error for the 3L as the complete waveform in that sector is shifting up/down.

When decreasing the ratio to 10, as in fig. A.6b, the waveform maximum no longer follows the predicted envelope. This is because for 1 sector, there is only time for $\frac{10}{6} \approx 1.66$ waveform. This can also be seen by the sector boundary used by the PLECS block, where they now no longer align with the real sector borders at intervals of 60°. As in the PLECS block, timing is discretised to the switching period, and only an integer number of switching cycles can be applied per sector. Thus, leaving some sectors with 2 states and some only with 1. This creates a waveform that is no longer well-defined by the previously created framework. The 2L $\hat{I}_{\text{cir}}$ still has the same maximum peak as defined in eq. (A.9), without error. The 3L $\hat{I}_{\text{cir}}$ at this modulation index is now overpredicted by eq. (A.23), by 15%.

A.3.2 Peak Circulation Current Verification

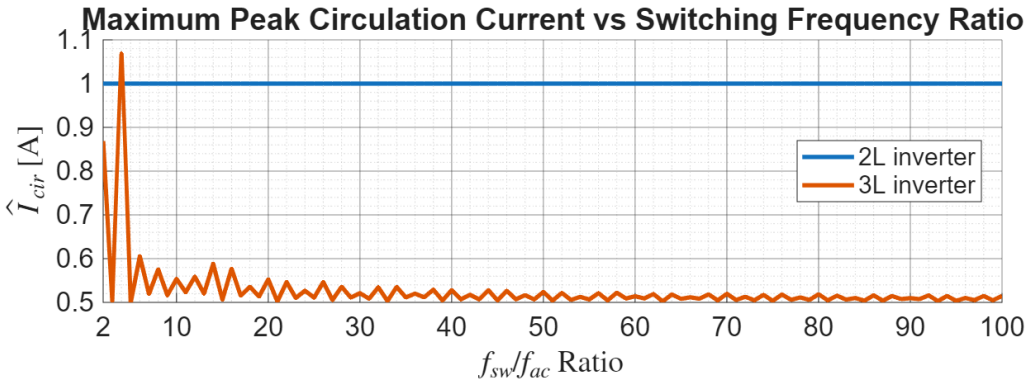


Figure A.7: The peak simulated circulation current vs integer ratios of $\frac{f_{\text{sw}}}{f_{\text{ac}}}$, where the ratio $L_{\text{cir}} = \frac{V_{\text{DC}}}{4 f_{\text{sw}}}$ is constant and the maximum is in the full range of $m \in [0, \frac{2}{\sqrt{3}}]$.

The assumption that the ratio $\frac{f_{\text{sw}}}{f_{\text{ac}}} = \infty$ is unachievable for a real application, so fig. A.7 shows the $\hat{I}_{\text{cir}}$ for different ratios. From this, it can be seen that the 2L has the exact level predicted (1 A) by eq. (A.9) for any ratio. Thus eq. (A.9) is also a good prediction of $\hat{I}_{\text{cir}}$ for all ratios. For the 3L, a deviation can be seen from the expected value (0.5 A), where the error envelope decreases with an increase in the ratio (for the reason see section A.3.1). It does not go below the calculated maximum, where for some higher ratios starting at 15 and then continuing in steps of 6, it is equal to the maximum calculated by eq. (A.23). In this thesis, the lowest ratio used is 12 and for ratios of 12 and higher, the maximum error is 18% if only an integer ratio is used. Note that if non-integer ratio's are used this error can increase to 75% for ratio's larger than 12. Where then the main error is at ratio's near $15 + 6\mathbb{N}$, where the integer ratio has no error.

In fig. A.8 $\hat{I}_{\text{cir}}$ is plotted for different ratios of $\frac{f_{\text{sw}}}{f_{\text{ac}}}$ against m. It can be seen that at a ratio of 10, the 2L follows the prediction of eq. (A.9) without error. The 3L $\hat{I}_{\text{cir}}$ follows the prediction of eq. (A.23) for the ratio $\frac{f_{\text{sw}}}{f_{\text{ac}}} = 1000$. As shown in the previous plot, the 3L deviates from the calculated maximum when decreasing this ratio. It does follow the general trend of first increasing until $m = \frac{1}{\sqrt{3}}$ and then having a plateau. The plateau region has the largest error, both positive and negative. For a ratio of 10, an undershoot occurs at higher m because, to reach the maximum in region 3 or 4, a very specific angle

needs to be reached. When going quickly through the region, this specific angle is skipped, and the maximum is not reached.

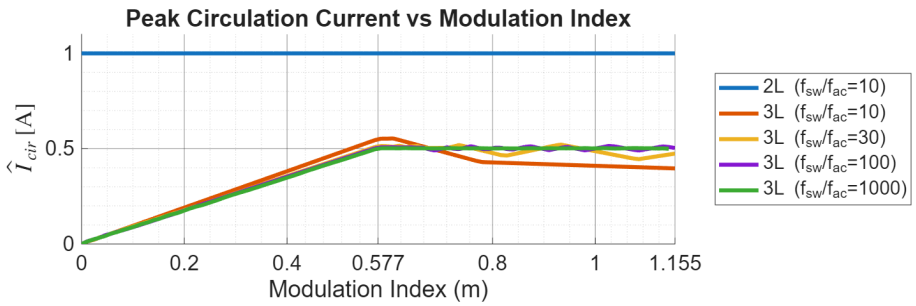


Figure A.8: Peak simulated circulation current, for different $\frac{f_{\text{sw}}}{f_{\text{ac}}}$ ratios, while keeping $L_{\text{cir}} = \frac{V_{\text{DC}}}{4f_{\text{sw}}}$ constant.

Appendix B

Simulation Setup

In the optimisation framework, several simulations are run to estimate component sizes and evaluate performance. This chapter explains the simulation techniques used for noise (DM and CM), efficiency, and THD.

B.1 DM Noise Simulation

"High frequency parasitic elements of the drive system, including the stray capacitor within the motor winding or between two conductors, the nonlinear capacitance of switching devices, the stray inductance of the DM link capacitor, busbar impedance and reverse recovery current of diodes all contribute to DM EMI emission generation during switching transients" [22]. There are several approaches to simulate DM noise in power converters [22]. One classical option is the frequency-domain modelling method [24], which uses equivalent circuits to represent DM noise sources and propagation paths in inverter-fed drives. More generally, simulation strategies include behavioural black-box modelling, such as the Thevenin Equivalent Frequency Source Model (TEFSM) [25], Modular Terminal Behavioral (MTB) models [26], and General Terminal Modeling (GTM) [27], which simplify converters into equivalent sources and impedances for fast EMI prediction. Another route is time-domain switching simulations, where the inverter operation is modelled directly, and a current spectrum analyser can be imitated to get the DM noise spectrum [28] [22].

B.1.1 Time Domain DM Modelling Approach

In this work, the time-domain approach was selected because 2L, multilevel and interleaved DM noise models are not well compared. Thus, the time-domain approach gives a straightforward and fair way of studying how different inverter configurations influence DM noise generation and propagation.

This method, however, has clear limitations. The small time steps needed to capture high-frequency conducted emissions make the simulations slow. In PLECS there are further restrictions: not all transients are represented, the stray inductance of the DC-link capacitor cannot be included due to state-space discontinuity issues, and adding all parasitics quickly increases the simulation time to a level where parametric sweeps are no longer feasible. Similar drawbacks of detailed time-domain modelling are also pointed out in the literature [22], where it is shown that although this approach is accurate, it becomes slow and computationally heavy when too many parasitics are added.

To deal with this, the DM model was simplified so that the main mechanisms of EMI generation are still captured while the simulations remain manageable. The model used

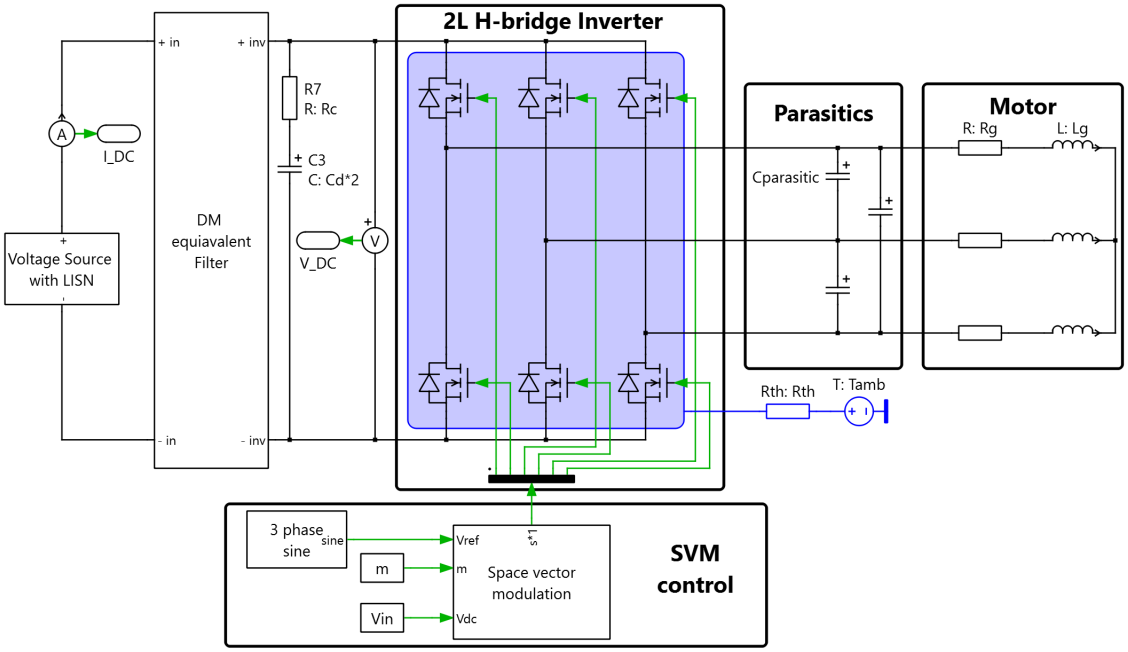


Figure B.1: PLECS simulation schematic for the 2L VSI, where the current after the voltage source and voltage over the DC-link capacitor are exported to MATLAB.

here includes the LISN, EMC filter, DC-link capacitor with ESR, power switches, equivalent interphase parasitic capacitance, and a simplified motor model. In this way, simplified lumped models can still provide useful EMI information at much lower computational cost, especially when the goal is not to calculate exact filter values but to get an indication of the required parameters and how they change with different design choices. The PLECS simulation schematic is shown in fig. B.1 for the 2L VSI configuration, and the equivalent DM filter circuit can be seen in fig. C.2. Some parasitics that are thus neglected, such as the DC-link capacitor equivalent inductance, MOSFET drain source capacitance and cable inductance. The shown parasitic capacitance is a lumped capacitance containing:

$$C_{\text{parasitic}} = C_{\text{board}} + C_{\text{g1}} + C_{\text{i}} + C_{\text{c}}/4 + C_{\text{s}}/2 \tag{B.1}$$

Where C_{board} is the interphase capacitance of the PCB, C_{g1} is the motor input capacitance as defined in [29], C_i is cable-to-cable capacitance, C_{c} is the cable to shield capacitance and C_{s} is the sum of the source-to-ground capacitance of the MOSFETs whose source is connected to the phase output.

However, the simulation time was too limited when using the parasitic capacitors, so these were set to zero. To see the impact of this assumption, the spectrums with and without the parasitic capacitors are modelled in section B.1.3. The values used for this verification simulation are based loosely on the data from [21] and are presented in table B.1.

The PLECS model works by inputting a constant modulation index and letting the inverter settle for 0.01 s and then measuring the input current and capacitor voltage for 6 cycles of the modulated frequency. In MATLAB, these time domain signals are post-processed to produce the peak-to-peak voltage ripple, peak-to-peak current ripple and the current spectrum. The PLECS simulation can be started with MATLAB code, so a sweep of filter component values and modulation indices can be performed.

Table B.1: List of CM and DM parasitic components, based on the value of [21].

Component	Symbol	Value
Cathode/source-to-ground capacitance	C_{device}	93 pF
Phase-to-phase PCB capacitance	C_{board}	400 pF
Per-phase PCB to ground capacitance	C_{e}	20 pF
Per-phase cable-to-cable capacitance	C_{i}	20 pF
Per-phase cable-to-shield capacitance	C_{c}	135 pF
Per phase motor input to ground capacitance	C_{g1}	240 pF
Per phase motor midpoint to ground capacitance	C_{g2}	120 pF
Per-phase cable inductance	L_c	2 µH
Shield inductance	L_{shield}	1 µH

B.1.2 From Time Signal to Current Spectrum

Starting from the simulated DC-link current $i_{\text{DC}}(t)$, the algorithm produces a 1 kHz resolution–bandwidth (RBW) spectrum in dBµA through six successive operations.

First, the transient interval $t < t_{\text{settle}}$ is discarded and the remaining waveform is uniformly re-sampled at f_{s} for a measurement window of length t_{meas}, giving $N = \lfloor f_{\text{s}} t_{\text{meas}} \rceil$ samples $i[n]$ $(n = 0, \ldots, N-1)$; this ensures evenly spaced data required by the fast Fourier transform (FFT).

Second, the DC component is removed (via MATLAB `detrend`) to eliminate the large zero-frequency bin that would otherwise dominate the low-frequency spectrum and obscure the conducted-emission harmonics. A Hann window $w[n]$ (MATLAB `hann`) is then applied to mitigate spectral leakage; the Hann window is chosen because it offers a good compromise between main-lobe width and side-lobe suppression, making it suitable for general-purpose spectral analysis where both frequency resolution and dynamic range matter.

Third, we select the FFT length N_{FFT} so that the frequency-bin spacing satisfies

$$\Delta f \;=\; \frac{f_{\text{s}}}{N_{\text{FFT}}} \;\le\; \frac{\text{RBW}}{10} \;=\; 100\,\text{Hz}. \tag{B.2}$$

Ten bins per RBW are used to ensure that the subsequent integration over 1 kHz accurately emulates a spectrum analyser's intermediate-frequency (IF) filter without discretisation artefacts or loss of narrow spectral lines.

Fourth, we compute the windowed FFT with zero-padding to N_{FFT} and obtain a one-sided power spectral density (PSD) $S_{ii}^{(1)}[k]$ in A^2/Hz at frequencies $f_{\text{k}} = k\,\Delta f$ using standard MATLAB periodogram steps (window power normalization and one-sided scaling).

Fifth, to emulate the compliance receiver's 1 kHz rectangular IF filter, we integrate $K = \text{round}(\text{RBW}/\Delta f) \approx 10$ adjacent PSD bins via convolution with a rectangular kernel and scale by Δf to convert spectral density (A^2/Hz) into mean-square current (A^2) within each 1 kHz cell. This step is essential because DO-160 limits are defined for the integrated power over a finite resolution bandwidth, not for per-hertz density. The result is $P_{\text{RBW}}[k]$ in A^2.

Sixth, we convert to root-mean-square (RMS) current and then to logarithmic units as required by RTCA DO-160G:

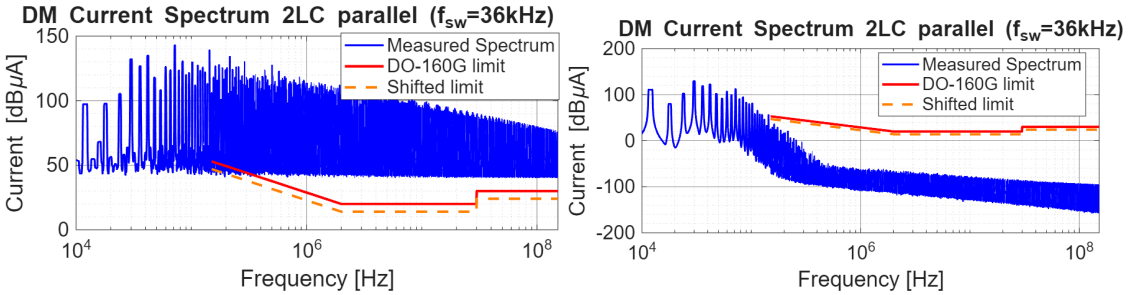
$$I_{\text{RBW}}[k] = \sqrt{P_{\text{RBW}}[k]}, \qquad I_{\text{dB}\mu\text{A}}[k] = 20\log_{10}\!\left(\frac{I_{\text{RBW}}[k]}{1\ \mu\text{A}}\right). \tag{B.3}$$

We then restrict the analysis to the DO-160 conducted-emission band $f_{\mathrm{lo}} = 150\,\mathrm{kHz}$ to $f_{\mathrm{hi}} = 152\,\mathrm{MHz}$ (and $f_{\mathrm{k}} \leq f_{\mathrm{eval,max}}$). The limit line of the DO-160 is compared linearly at each frequency bins $\{f_{\mathrm{k}}\}$, and the margin is calculated as:

$$M(f_{\mathrm{k}}) = I_{\mathrm{dB}\mu\mathrm{A}}[k] - L(f_{\mathrm{k}}). \tag{B.4}$$

A positive margin indicates emissions above the limit. The worst-case margin $M_{\mathrm{worst}} = \max_k M(f_{\mathrm{k}})$ and its frequency f_{worst} summarise whether the design meets, equals, or exceeds the DO-160G conducted-emission mask. This is used to guide the filter-design optimisation, requiring a minimum of 6 dB margin for a filter to pass.

B.1.3 DM Noise Simulation Spectrums



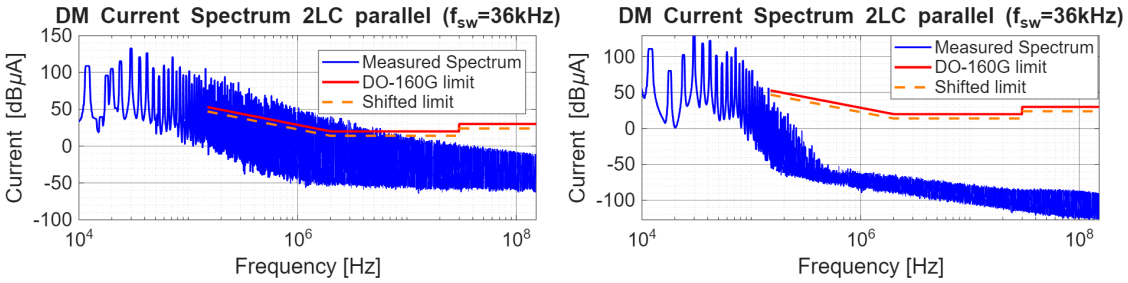
(a) (b)

Figure B.2: The simulated DM spectrum for a 2L VSI at $f_{\mathrm{sw}} = 36\,\mathrm{kHz}$, no parallel devices and no parasitics. (a) No filter, (b) the optimised DM filter.

In fig. B.2a, the DM current spectrum is shown for a 2L VSI with no DM filter (also no DC-link capacitor), but including the line impedance stabilization network (LISN). The LISNs connected to each line will already form a low-pass filter with a cut-off frequency of: $f_c = \frac{1}{2\pi\sqrt{5\cdot10^{-6}\cdot0.1\cdot10^{-6}}} \approx 225\,\mathrm{kHz}$. The spectrum shows that damping is required to push it below the limit line. Using the filter design of the optimisation procedure of section C.3, the spectrum was attenuated, as shown in fig. B.2b. The spectrum now falls under the limit line, where the margin is the lowest near the start of the limit line. Since the $-6\,\mathrm{dB}$ limit was not the only design criterion, the spectrum is below the limit line. The steep decrease stops around 400 kHz due to the current spectrum emulator setup. This is just the noise floor and not the real spectrum.

The spectra of fig. B.2 were created without the parasitic capacitance. In fig. B.3, the MOSFET output capacitance C_{oss}, parasitic phase-to-phase capacitance $C_{\mathrm{parasitic}}$ are included. Comparing the unfiltered spectrums, it can be seen that the one with parasitics has a steeper attenuation. This did not result in the filtered response having more attenuation, as the margin to the limit line is similar. This goes against the experimentally verified model of [21], which predicted that adding more $C_{\mathrm{parasitic}}$ results in more DM noise. Specifically for adding more ground-source capacitance (C_{s}) (e.g. adding more MOSFETs in parallel), it predicts the noise will increase in accordance with eq. (B.5). So this model does not correctly capture the influence of the parasitics.

$$\Delta H_{\mathrm{dB,\,DM}}(C_{\mathrm{s}}) \approx 20\log_{10}\left(\frac{C_{\mathrm{s}} + C_{\mathrm{parasitic}}}{C_{\mathrm{parasitic}}}\right). \tag{B.5}$$



(a) (b)

Figure B.3: The simulated DM spectrum for a 2L VSI at $f_{\text{sw}} = 36\,\text{kHz}$, no parallel devices and with $C_{\text{parasitic}}$. (a) No filter, (b) the optimised DM filter.

B.2 CM Noise Simulation

For the CM analysis, the model proposed by L. Ran et al. [30] was used, where the expansion of the model for multilevel and interleaved inverters was used from [31]. This model includes the dominant parasitic capacitances that define the CM current paths in inverter-fed motor drives, such as the capacitance between the motor winding and the frame, between the power module baseplate and the heatsink, and between the cables and ground. These elements are the main contributors to CM noise propagation in such systems [30].

Other modelling approaches for CM noise have been discussed in [22]. Behavioural models, such as the modular terminal behavioural (MTB) models [26], and general terminal modelling (GTM) [27], simplify the converter into equivalent sources and impedances. They are straightforward to implement and computationally efficient, but require parameter extraction from measurements and provide little information about the internal generation mechanisms. This makes them impractical for this investigation. Detailed physics-based models aim to include all parasitic elements and switching dynamics, offering high accuracy and flexibility, but at the cost of significantly increased complexity and simulation time [22]. Frequency-domain approaches, such as those described in [30] and [31], model the converter and its parasitics using equivalent circuits, allowing fast prediction of CM emissions when the noise sources and propagation paths are well understood.

B.2.1 Time Domain CM Noise Modelling Approach

The model of [31] was chosen here because it captures the main physical mechanisms of CM current flow and can easily be adopted for the different inverter types used. This approach models the inverter as an equivalent CM circuit driven by one or more equivalent voltage sources. For a standard 2L VSI, the circuit is simplified to a single CM voltage source ($V_{\text{CM}}(t)$) that represents the creation of the CM noise. This noise flows through the stray CM equivalent capacitances connected to the VSI input and output.

The benefit of this model is that it can easily be adopted to multilevel and interleaved topologies by defining floating nodes. In Figure 2.1, these have been stated as $V_{i,h,k}$, representing any node not directly connected to the phase output. These nodes also encounter high dv/dt and are coupled via stray capacitances to the ground, also creating CM noise. The model of [31] accounts for this by introducing an additional voltage source ($V_{\text{CM-s}}$) that accounts for the contributions of these noise sources.

Figure B.4 shows the CM equivalent circuit, where the simplified CM filter can be found in fig. C.3. To the output of V_{CM}, the CM equivalent phase-to-ground circuit is

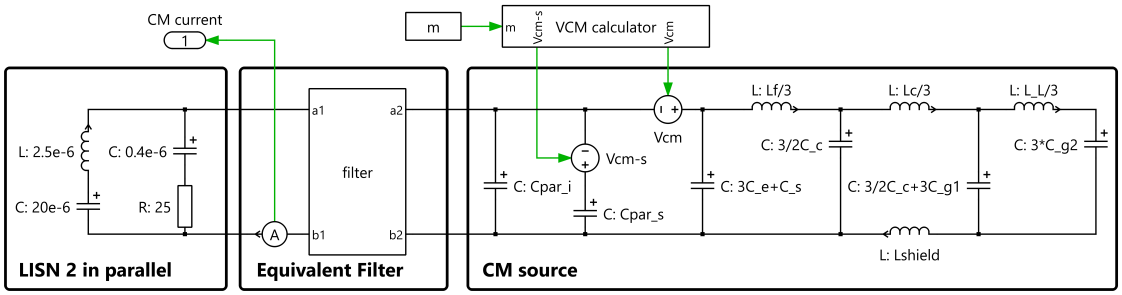


Figure B.4: CM equivalent simulation schematic for all VSIs.

shown. The component values and physical meaning can be found in table B.1. Besides those constant parasitic components, there are also some components that change with the inverter type and the number of parallel devices. C_{s} is the sum of all the cathode/source-to-ground capacitances (C_{device}) connected to any phase output. $C_{\mathrm{par,i}}$ is the sum of all the cathode/source-to-ground capacitances connected to the DC-link. $C_{\mathrm{par,s}}$ is the sum of all the floating cathode/source-to-ground capacitances.

The Common-Mode Voltage

The common-mode (CM) voltage, V_{CM}, can be expressed directly in terms of the three phase-to-ground voltages V_i, where $i = a, b, c$. Under balanced conditions, Kirchhoff's current law enforces $i_a + i_b + i_c = 0$, leading to the well-known expression [15]:

$$V_{\mathrm{CM}}(t) = \frac{1}{3}\big(V_a(t) + V_b(t) + V_c(t)\big). \tag{B.6}$$

This relation is universal: it holds for 2L, interleaved, and multilevel inverter topologies. The differences lie only in how the phase voltages are synthesised from the internal node voltages of the converter. For a 2L leg, each phase only has one node directly connected to the phase output, which leads to the standard expression of eq. (B.6).

In interleaved topologies, each phase consists of N_{legs} parallel inverter legs. There are N_{legs} voltage levels per phase output. The inverter leg voltage is now denoted as follows: $V_{i,h}$, where i denotes the phase and h the leg. The CM voltage is still the average of the phase output voltages, so [31]:

$$V_{\mathrm{CM}}(t) = \frac{1}{3N_{\mathrm{legs}}} \sum_{i=a,b,c} \sum_{h=1}^{N_{\mathrm{legs}}} V_{i,h}(t). \tag{B.7}$$

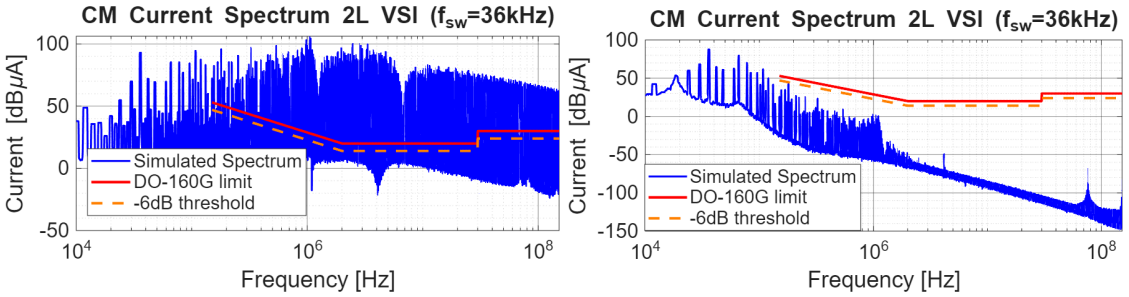
For the 2L VSI, all MOSFETs were connected at one side to the DC-link and the other side to the phase outputs. However, in multilevel converters, the MOSFETs are not per se connected to the DC-link and phase output. They can also be connected to an intermediate point (e.g., clamped junctions in NPC or the back-to-back MOSFET middle points for T-type). These nodes couple to ground through stray capacitances and thus act as supplementary CM voltage sources. Therefore, the total CM excitation of a multilevel inverter is the superposition of:

1. The averaged phase output voltage $V_{\mathrm{CM}}(t)$, given in eq. (B.6)
2. The supplementary averaged floating nodes voltage $V_{\text{CM-s}}(t)$

The voltages at the nodes can be expressed as $V_{i,h,k}$ (as seen in fig. 2.1), where i denotes the phase, h the leg and k the floating node. Note that the node connected to the phase output is not part of k. The supplementary CM source can be written as the average of all floating node voltages, [31]

$$V_{\text{CM-s}}(t) = \frac{1}{3N_{\text{legs}}N_{\text{nodes}}} \sum_{i=a,b,c} \sum_{h=1}^{N_{\text{legs}}} \sum_{k=1}^{N_{\text{nodes}}} V_{i,h,k}(t). \tag{B.8}$$

B.2.2 CM Noise Simulation Spectrums



(a) (b)

Figure B.5: The simulated CM spectrum for a 2L VSI at $f_{\text{sw}} = 36\,\text{kHz}$. (a) No filter, (b) the optimised CM filter.

The simulated CM spectrum for the 2L VSI with and without the CM filter can be seen in fig. B.5. For the case with no filter, it can be seen that the spectrum is above the limit line for the complete frequency range. When implementing the proposed filter and optimisation procedure of section C.4, the spectrum decreases below the limit line by more than 6 dB for the complete range. The peaks nearest the start of the limit line have the smallest margin. This is true for all other spectra, where, when changing the switching frequency, the location of the peaks changes, which causes a small fluctuation in the required attenuation. This can both increase and decrease the needed attenuation.

The chosen current spectrum emulator does not have a higher resolution bandwidth after 30 MHz. Including this increases the amplitude of the peaks after this frequency. It is not implemented due to the large margin, making it unlikely that there is a peak reaching the limit line. Thus, it was omitted to reduce simulation complexity while not compromising the accuracy.

B.3 Efficiency and Loss Simulation

The losses in the inverter are evaluated using PLECS, as this enables the use of the exact MOSFET models. The model is the same as for the DM noise simulation, seen in fig. B.1. To have a reproducible result, it is important to simulate for equal temperatures. Therefore, all thermal resistances are set to zero and all temperatures are forced to be 100 °C. The inverter output power is controlled with a PID loop, where it takes the output power as the input, compares this to the reference output power and outputs the modulation index. If needed, the output power setpoint can be swept slowly to do a loss sweep. The loss simulation measures these main loss components:

- **Input filter:** the main losses in the input filter are in the ESR of the CM and DC inductors. To increase the simulation speed, the negligible components can be removed, so the CM capacitors with their damping are removed.
- **DC-link capacitor:** has a small loss in its ESR.
- **Inverter legs:** the main losses in the inverter legs are in the MOSFETs and diodes. For this, the exact models can be used in PLECS. Where PLECS has a built-in conduction and switching loss calculator.
- **Interphase inductor:** the main losses are the resistive and core losses. The resistive losses are directly found by the power loss in the ESR, but the skin effect losses are neglected. The core losses are found by exporting the simulated time domain circulation current is $I_{\text{cir}}(t) = \frac{1}{2}\left(I_{\text{leg},1}(t) - I_{\text{leg},2}(t)\right)$. Assuming a linear core and no saturation, then the magnetic flux density (B) in the core can be calculated as [15]:

  $$B(t) = \frac{N\mu_0\mu_{\text{r}}I_{\text{cir}}(t)}{L_{\text{e}}} \tag{B.9}$$

  From this time domain magnetic flux density, the core loss can be found directly using the generalised Steinmetz (iGSE) equation. Where this thesis instead uses the classical Steinmetz equation due to easier implementation using [15]. It uses the peak magnetic flux B_{pk} (sometimes called B_{ac}), which is half of the flux swing. As the time domain has many flux swings, the B_{pk} is calculated for each swing. From which the power loss per unit volume (P_v) is calculated, and that is averaged over time for all swings. Below the equation for P_v is given [15],

  $$P_v = aB_{\text{pk}}^b f^c \tag{B.10}$$

  Here, a, b, c are the Steinmetz parameters found in the datasheet of the cores, and f is the per-segment frequency of the swing. Using the core volume data and multiplying this by the number of cores, we find the total core loss as $P_{\text{core}} = P_v(V_e \cdot \#cores)$ [15].

The simulation is run for every design, as part of the design process, see fig. 3.1. The simulation is run for 0.5 s and the data from the last 0.1 s is used and averaged for all loss components.

This simulation has some key simplifications that influence the loss results. The first is that no dead time is used, which would increase the switching losses [15]. Omitting the ground-source capacitance underestimates the switching losses [21]. No cable, trace, or busbar resistance was included, underestimating the resistive losses. Lastly, power consumption by the auxiliary circuits (safety, logic, neutral-point balancing, and drivers) is not included.

B.3.1 THD

During the power loss simulation, the phase current and voltage waveforms are also captured. These waveforms are then post-processed to calculate the THD relative to the modulated frequency.

Appendix C

Design Methodology and Optimization Framework

To compare inverter topologies in a fair and transparent way, a systematic design process is required. This process must ensure that every inverter meets the same requirements and that design trade-offs are evaluated on an equal basis. For this purpose, a structured multi-stage design framework is applied. The framework standardises the procedure by dividing it into clear stages: DM filter, CM filter, interphase inductor, power stage PCB, heatsink, and housing. Each stage is parameterised so that component sizing and selection follow consistent criteria and regulatory constraints. In this way, the resulting inverter designs can be compared objectively in terms of performance, weight, and volume.

C.1 MOSFET and Diode Selection

C.1.1 MOSFET

The MOSFET selection has a large influence on the efficiency performance of the VSI. The topologies have MOSFETs with different blocking voltages. The performance of MOSFETs increases when the blocking voltage requirement is reduced. Thus, it is chosen to use different MOSFETs for the two blocking voltage requirements of 1200 V and 650 V.

In [11], the device FOM of different MOSFET types is compared along with their extended FOM when applied in different VSIs. From their FOM plot, it can be seen that for 1200 V blocking voltage, SiC MOSFETs are the only option. For the 650 V blocking voltage, multiple technologies are available, where GaN only has a marginally better FOM than SiC. To isolate the performance gains from the topology change and prevent variations from different semiconductor technologies or manufacturers, it is chosen to use SiC MOSFETs from a single manufacturer (Wolfspeed) for both voltage levels.

The catalogue of Wolfspeed was surveyed, and the $C3M0016120K$ and $C3M0015065K$ were selected for the 1200 V and 650 V blocking voltage, respectively. These were selected as they offered the lowest on-resistance for their respective blocking voltage. These feature Kelvin source connections, which reduce the current dependence of the switching losses [11] compared to standard 3-pin MOSFETs. A Kelvin source pin is a second pin connected to the source of the MOSFET, which is dedicated to the gate driver.

C.1.2 Diode

The clamping diodes in the NPC topology are a critical component influencing VSI efficiency. Standard p-n diodes were avoided due to their significant reverse recovery charge.

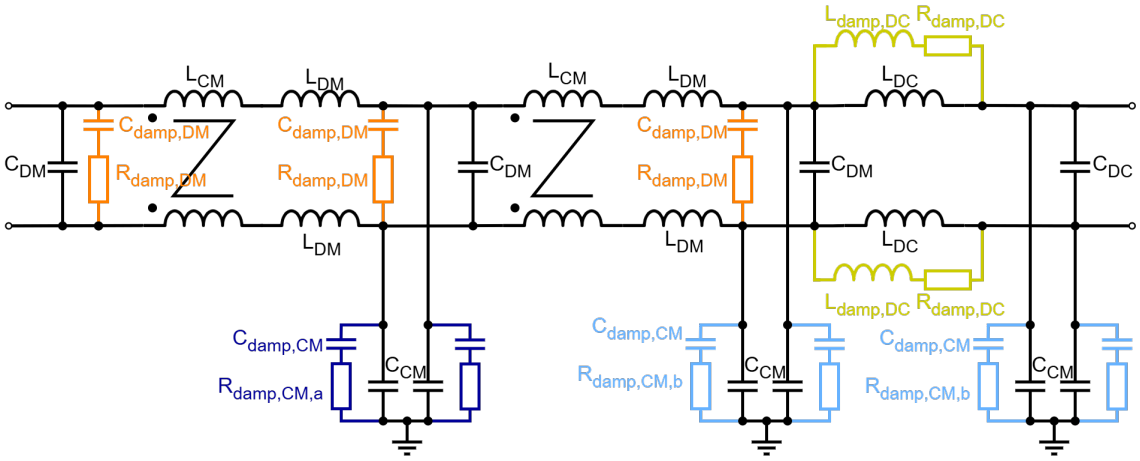


Figure C.1: EMC input filter, with the different damping components coloured.

During switching, this charge is pulled through the main MOSFETs as they turn on, creating a large current spike that dramatically increases their turn-on switching losses. SiC Schottky diodes, which have a very small Qrr, were selected to eliminate this loss mechanism. The catalogue of Wolfspeed was surveyed, and the $E3D30065D$ was selected. It can handle the current peaks and offers the required 650 V blocking voltage.

C.2 Filter Design

To meet the EMC conducted emissions regulations, the inverter requires an input filter. The required attenuation depends on factors such as inverter topology, switching frequency, and parasitic elements. To allow fair comparison across inverter types, each design must include a filter tuned to provide an equivalent level of compliance.

Because it is very challenging to accurately simulate DM and CM noise simultaneously, the design problem is separated into the DM and CM filter design. The CM filter design uses the DM filter results for the design process. The CM and DM spectra are each required to lie at least 6 dB below the limit lines. This margin accounts for the possibility that the two components could add coherently in measurement, even though in practice they are often partially uncorrelated.

"In a three-phase motor drive, the switched system is not symmetric with respect to the input power mains (or LISN) during the switching transitions. This leads to mixed-mode EMI emissions" [22]. Thus, while splitting it into CM and DM noise provides a structured design method, it does not fully capture mixed-mode emissions. Furthermore, not all parasitic components are included in the models, which reduces the accuracy of the models. This means the filter design is not the exact value for a prototype, but a consistent framework across inverter types to assess trends and design trade-offs.

The implemented filter, shown in fig. C.1, consists of a two-stage CM section cascaded with a single DM stage. Both stages also influence the opposite noise type, providing additional cross-attenuation. A two-stage CM configuration was selected because, under the given design constraints, it consistently provides lower mass than a one-stage solution. Damping networks are included to limit resonance peaks and to mitigate excessive DC-link capacitor currents during susceptibility tests [32].

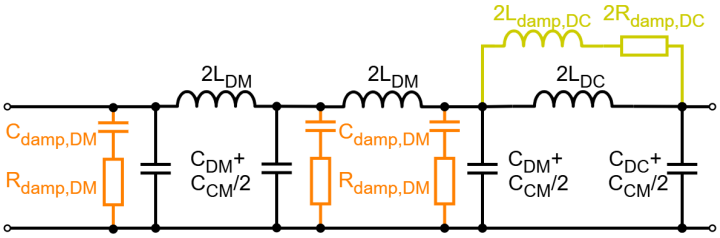


Figure C.2: DM equivalent filter, with the different damping components coloured.

C.3 DM Filter Stage

The DM filter has two main tasks: limit the current and voltage ripple at the DC-link, and filter the DM noise below the conducted emissions limit line. The DM filter equivalent circuit of fig. C.1 can be seen in fig. C.2. From this, it can be seen that it is equivalently a seventh-order filter, where the leakage inductance of the CM choke (L_{DM}) is used as part of the DM filter. This leaves the design of the DM capacitors (C_{DM}), DC-link inductor (L_{DC}), DC-link capacitor (C_{DC}) and their corresponding damping circuits. In this section, how to design these components is presented.

C.3.1 DM Filter Component Selection

Before deriving the electrical values of the components, a framework must be established for how each component is physically realised. Where the focus is on the selection of the materials (e.g., core and dielectric types) and the physical design considerations (e.g., wire gauge and core geometry) needed to create a component of a given inductance or capacitance. To estimate the weight, volume and electrical properties of any potential filter design.

Inductor Selection (L_{DC} and $L_{\mathrm{damp,DC}}$)

The design of the DC-link inductor (L_{DC}) is primarily driven by the need to handle the full DC current without saturating. This section outlines the selection of materials and the physical design process for realising an inductor, once its required inductance value is known. It needs to do this under the full DC-current, temperature range and for the worst specified tolerance. The maximum current for our system specifications (see table 2.1) is,

$$\hat{I}_{\mathrm{DC}} = \frac{P_{\mathrm{out}}}{\eta_{\mathrm{min}} V_{\mathrm{in,min}}} = \frac{20000}{0.98 \cdot 470} \approx 43.4\,\mathrm{A}. \tag{C.1}$$

This current will saturate most (ungapped) high-permeability cores, so powder cores are used in this work. There are many types of powder cores, but for this thesis, Edge cores of Magnetics are used. The benefit of Edge is that it has a high DC bias tolerance, low core losses, is size efficient, has a usable frequency of 20 MHz, ±1% across the temperature range, has high saturation flux and light if used at high currents [33].

There are multiple shapes in which the inductor can be made, but an E-core is used as it provides shielding from the generated field and is easier to cool. The wire wound inside the core must be able to carry 43.4 A, so 8 AWG was used. This was based on the recommendation of the manufacturer of [34]:

$$\text{wire size} = -4.31 \ln\left(\frac{1.889 \cdot \hat{I}_{\mathrm{DC}}}{C_d}\right) = -4.31 \ln\left(\frac{1.889 \cdot 43.4}{500}\right) \approx 8\mathrm{AWG} \approx 8.37\,\mathrm{mm}^2.$$

(C.2)

Where C_d is the current density in A/cm^2, where 800 A/cm^2 is aggressive and 400 A/cm^2 is conservative [34]. A current density in between these two bounds of 500 A/cm^2 is chosen, which results in a wire thickness of 8 AWG. For the design, the lightest possible design was selected for each inductance value, taking into account a maximum winding factor of 80%. 13 different DC inductors have been designed in the range from 0.6µH to 155µH.

For the damping inductor ($L_{\text{damp,DC}}$), a stock inductor can be used due to the low current rating. Where the exact maximum is dependent on the ratio of the ESR of the main DC-link inductor and the DC damping resistor ($R_{\text{damp,DC}}$), but it is assumed to be at most 1 A. For this, most stock inductors in the inductance range of interest can achieve close mass and volumes. So a volume of 1 cm^3 and a weight of 2.5 g is used regardless of the $L_{\text{damp,DC}}$ value.

Capacitor Selection (C_{DM} and C_{DC})

The capacitor must operate over a wide range of temperatures, where the operating temperature affects the capacitance and dissipation factor. Therefore, it is chosen to work with polypropylene film capacitors, specifically the "MKP1848C" series from Vishay [35]. This specific type has a capacitance increase for low temperature by up to 3% of the room temperature value and a decrease for high temperature of −5%. This can be used for all capacitors present in the DM equivalent filter. Where the DC-link capacitor is split into two series capacitors for the 3L converters. The inverter can see at most 884 V at the DC bus [6], so a blocking voltage of 1000 V is required and 600 V for the two series capacitors of the 3L converters.

The design requires a smooth and unbiased capacitance in increments of 1 µF. For this, a linear model is used to estimate capacitor mass and volume. This approach avoids the performance discontinuities and skewed results that would arise from selecting specific, discrete components from the "MKP1848C" catalogue. Based on an analysis of the catalogue data, the model uses the following specific mass and volume approximations per voltage class:

- 1000 V **rating:** 3 g/µF and 3.1 cm^3/µF.
- 600 V **rating:** 2 g/µF and 2.0 cm^3/µF.

Since the DC-link of the 3L VSIs is composed of two series capacitors, achieving an equivalent capacitance of C_{DC} requires two capacitors of $2C_{\text{DC}}$ each. Therefore, the total mass and volume contribution of the DC-link capacitor bank is calculated using four times the specific values of the 600 V units. C_{DM} is designed in the range of 1-6 µF, these discrete values are available in the 1000 V catalogue so will directly be used.

The required C_{DC} value is determined by five requirements:

1. **DM current spectrum at the inverter DC input:** should be below the DO-160G limit lines [6], with a margin of at least 6dB. The current spectrum is not maximised for all inverter types at a specific modulation index, so it needs to have a 6 dB margin for the full operating range.
2. **Maximum peak-to-peak voltage ripple over the DC-link capacitor:** is limited to ensure stable inverter modulation and prevent output voltage distortion. It is a system specification which is not directly limited by the regulations. For this thesis, the peak-to-peak voltage ripple across the DC-link must not exceed 1% of the nominal DC voltage (5.4 V).

3. **Maximum peak-to-peak current ripple:** is limited in the DO-160G to 7% of the maximum DC input current, e.g. $0.07\hat{I}_{\mathrm{DC}} \approx 2.86\,\mathrm{A}$. As this is a hard limit, it should include a SF (see table 2.1), thus it should be limited to: $I_{\mathrm{pp,DC}} \leq \frac{0.07}{SF}\hat{I}_{\mathrm{DC}} = \frac{0.07}{1.7} \cdot 43.4 = 1.8\,\mathrm{A}$.

4. *Energy buffer:* the DC-link capacitor must act as a local energy source, capable of supplying transient load power steps ($P_{\mathrm{step}}^{\mathrm{req}}$) with a maximum voltage drop ($\Delta V_{\mathrm{DC}}^{\mathrm{req}}$) for the step period ($T_{\mathrm{step}}$). Dependent on the step shape, it can be found as [36]:

$$C_{\mathrm{DC}} \geq \begin{cases} \frac{\Delta P_{\mathrm{step}}^{\mathrm{req}} T_{\mathrm{step}}}{2V_{\mathrm{DC}} \Delta V_{\mathrm{DC}}^{\mathrm{req}}}, & \text{triangular response} \\ \frac{\Delta P_{\mathrm{step}}^{\mathrm{req}} T_{\mathrm{step}}}{V_{\mathrm{DC}} \Delta V_{\mathrm{DC}}^{\mathrm{req}}}, & \text{step response} \end{cases} \tag{C.3}$$

5. *Regenerative energy absorption:* during events such as regenerative braking of the motor, C_{DC} must be sized to absorb regenerative energy from the motor during braking events without exceeding the maximum voltage rise limits stipulated by DO-160G [6].

The optimisation procedure will find the minimum C_{DC} value that simultaneously satisfies the three primary constraints: DM noise attenuation, DC-link voltage ripple, and DC-link current ripple. While energy buffering and regenerative energy absorption are critical functions of a DC-link capacitor in a complete drive system, they are considered outside the scope of this comparative analysis. This is because their sizing is highly dependent on application-specific parameters, such as motor inertia and transient load profiles, which are not defined in this generalised study. By focusing on the three requirements that are highly dependent on the inverter design, the framework ensures a fair comparison based on the intrinsic performance of the topologies themselves.

Resistors Selection (R_{damp})

For the damping networks, standard surface-mounted device (SMD) resistors are used. Since the mass and volume of SMD resistors are primarily determined by their package size rather than their resistance value, a constant mass of 2.5 g and volume of $1\,\mathrm{cm}^3$ are assumed for each resistor in the optimisation framework. The final selected resistance value for the SMD component accounts for the ESR of the corresponding inductor or capacitor to achieve the total required damping resistance. This also holds for the damping resistors of the CM filter.

C.3.2 Optimised Damping of the DM filter

Damping is crucial for several reasons: it suppresses resonances, prevents destabilisation of feedback loops, and avoids excessive capacitor currents during conducted susceptibility tests [32]. In the DM filter equivalent circuit of fig. C.2, the DM damping circuits (orange) and the DC-link damping circuits (green) are visible. An RL parallel damping (green) circuit is chosen for the DC-link stage, as an RC damping parallel with C_{DC} would require a large damping capacitor. This would be significantly larger than the RL damping, as the inductor does not require a large current rating, so it can be a small stock inductor. Parallel RL damping is not possible for the first two stages, as this would bypass the CM choke in the CM equivalent circuit. So, an RC shunt damping is required. The design can significantly increase the filter's size and cost. Hence, the damping must be designed efficiently, which can be done by following the approach of [32].

RC Damping (orange):

The DM damping capacitor is chosen as $C_{\text{damp,DM}} = \frac{1}{2}C_{\text{DM}}$, as this satisfies for all designs the requirement of "$C_{\text{damp,DC}}$ should have an impedance magnitude that is sufficiently less than $R_{\text{damp,DM}}$ at the filter resonant frequency" [32]. It offers a good trade-off between damping versus capacitor size. From [32], it can be found that the optimum Q factor in this case is:

$$Q_{\text{opt}} = \frac{R_{\text{opt}}}{R_0} = \sqrt{\frac{(2 + \frac{C_{\text{damp,DM}}}{C_{\text{DM}}})(4 + 3\frac{C_{\text{damp,DM}}}{C_{\text{DM}}})}{2(\frac{C_{\text{damp,DM}}}{C_{\text{DM}}})^2(4 + \frac{C_{\text{damp,DM}}}{C_{\text{DM}}})}} = \sqrt{\frac{55}{9}}. \tag{C.4}$$

Here $R_0 = \sqrt{\frac{L_{\text{DM}}/2}{C_{\text{DM}}}}$. When using the optimum damping R_{opt} for the $R_{\text{damp,DM}}$ this can also be rewritten into:

$$R_{\text{damp,DM}} = R_{\text{opt}} = R_0\sqrt{\frac{55}{9}} = \sqrt{\frac{L_{\text{DM}}}{2C_{\text{DM}}}}\sqrt{\frac{55}{9}}. \tag{C.5}$$

Thus the $R_{\text{damp,DM}}$ can be found directly from the values of L_{DM} and C_{DM}. The high-frequency attenuation is not affected by the choice of $C_{\text{damp,DM}}$ [32].

RL Damping Networks (green):

The DC damping inductor is chosen as $L_{\text{damp,DC}} = \frac{1}{2}L_{\text{DC}}$. This offers a good trade-off between degradation of HF filter attenuation and damping. In [32], an optimisation procedure is laid out to get the optimal ratio based on the maximum allowable output impedance. However, it is chosen to keep the ratio constant to have the same degradation of HF for all filter designs, which makes the comparison more fair. From [32], it can be found that the optimum Q factor in this case is:

$$Q_{\text{opt}} = \frac{R_{\text{opt}}}{R_0} = \sqrt{\frac{\frac{L_{\text{damp,DC}}}{L_{\text{DC}}}(3 + 4\frac{L_{\text{damp,DC}}}{L_{\text{DC}}})(1 + 2\frac{L_{\text{damp,DC}}}{L_{\text{DC}}})}{2(1 + 4\frac{L_{\text{damp,DC}}}{L_{\text{DC}}})}} = \sqrt{\frac{5}{6}}. \tag{C.6}$$

Here $R_0 = \sqrt{\frac{L_{\text{DC}}/2}{C_{\text{DC}}}}$. When using the optimum damping R_{opt} for the $R_{\text{damp,DC}}$ this can also be rewritten into:

$$R_{\text{damp,DC}} = R_{\text{opt}} = R_0\sqrt{\frac{5}{6}} = \sqrt{\frac{L_{\text{DC}}}{2C_{\text{DC}}}}\sqrt{\frac{5}{6}}. \tag{C.7}$$

Thus the $R_{\text{damp,DC}}$ can be found directly from the values of L_{DC} and C_{DC}. This filter type degrades the high-frequency attenuation of the filter, where "the high-frequency asymptote of the filter transfer function is increased from $1/\omega^2\frac{L_{\text{DC}}}{2}C_{\text{DC}}$ to $1/\omega^2\frac{L_{\text{DC}}//L_{\text{damp,DC}}}{2}C_{\text{DC}}$" [32].

C.3.3 DM Filter Sizing Procedure

The DM filter design procedure seen in the blue box in fig. 3.1 is used to find the DM filter components that minimise the mass and volume, while satisfying the requirements. It is a multi-stage framework, where order is important. The DM filter results are required by two other design blocks, so it is done first. The design procedure has system specifications (see table 2.1) that are kept constant for all designs to ensure fair comparison and design choices that can vary between designs. For the DM filter design the following design choices can be made:

- **Inverter type:** Are the eight VSI under investigation, where only one can be selected per design.
- **Number of parallel devices:** Can be set for all active devices (including the diodes), from no parallel devices to a maximum of 72 devices total. Where the maximum number of parallel devices is different per inverter type.
- **Minimum $L_{\mathbf{DM}}$:** Is the minimum L_{DM} that can result from the design of the DM filter stage. This can be predicted, but a constant conservative minimum for our design is 1 µH. As L_{CM} is not smaller than 150 µH for the created designs. Thus, with a high coupling of 0.99 and taking some margin 1 µH was set, and this is not varied, although it could be done.
- **Switching frequency ($f_{\mathbf{sw}}$):** Can be set as any frequency. For this thesis, the following values are considered: $f_{\mathrm{sw}} = \{24, 36, 48, 60, 72\}$kHz.
- **List of $L_{\mathbf{DC}}$ and $C_{\mathbf{DC}}$:** are the components that can be considered for the DM filter design as specified in section C.3.1. This range can be limited, for instance, if it is known that a design requires more damping than a previous design, all smaller L_{DC} values compared to that design can be skipped.

The core of the DM filter design is a nested search algorithm, as illustrated in fig. 3.1. The algorithm sweeps through every possible combination of L_{DC} and C_{DM}. This creates a broad search space of passive filter configurations to be evaluated. For each pair, the minimum C_{DC} should be found that meets the design requirements listed in section C.3.1. To do this, a binary search is used for the range of $C_{\mathrm{DC}} \in [1, 500]$µF. Where, if it passes all the requirements, the value is decreased and otherwise increased. Until the C_{DC} is known with a resolution of 1 µF. If no value of C_{DC} within the predefined range can meet the requirements, the initial (L_{DC}, C_{DM}) combination is deemed invalid and is discarded from the list of potential solutions. During this search, each tested value of C_{DC} and its corresponding damping network is simulated for multiple modulation indices ($m = \{0.1, 0.4, 0.57735, 0.8, 1.0\}$), using the method set out in section B.1.

After the nested loops are complete, the algorithm has a list of all valid filter designs, each defined by a unique set of L_{DC}, C_{DM} and $C_{\mathrm{DC,min}}$. The final step is to select the single best design from this list. Each valid design's total mass and volume are calculated and then normalised against the minimums found across the entire sweep. A final score is computed using the formula:

$$score = 2\tilde{m} + \tilde{V} = 2\frac{m}{m_{\mathrm{min}}} + \frac{V}{V_{\mathrm{min}}}. \tag{C.8}$$

where $\tilde{m}$ and $\tilde{V}$ are the normalized mass and volume, respectively. Mass is weighted twice as heavily as volume, reflecting its higher priority in aerospace applications. The design that achieves the lowest score is selected as the optimal DM filter for the given inverter configuration.

C.4 CM Filter Stage

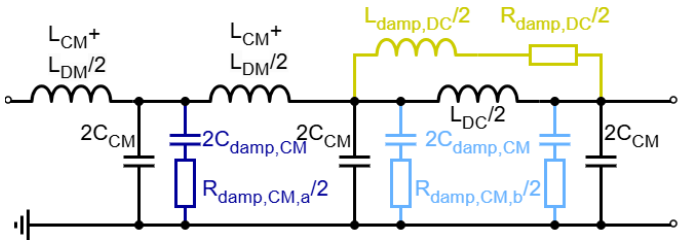


Figure C.3: CM equivalent filter, with the different damping components coloured.

The CM filter needs to attenuate the CM noise generated by the VSI below the limit line. The CM equivalent circuit of fig. C.1 can be seen in fig. C.3. From this, it can be seen that it is a sixth-order filter where the DC inductor (L_{DC}) with its damping is part of the CM filter. For this reason, the CM filter design needs to be done after the DM filter design. This leaves the design of the CM choke (L_{CM}), CM capacitor (C_{CM}) and their corresponding damping circuits. In this section, how to design these components is presented.

C.4.1 CM Filter Component Selection

As for the DM filter design, the physical CM components need to be pre-selected.

CM Choke Selection (L_{CM})

The CM choke is designed using toroidal nanocrystalline cores from Magnetics Inc. due to their high permeability, which allows for high inductance with minimal size and mass. A key advantage of the CM choke topology is the inherent cancellation of DC magnetic flux, as the 43.4 A load current flows through the two windings in opposite directions. This prevents core saturation, meaning the physical design is driven primarily by achieving the target inductance with the required 8 AWG wire gauge (see eq. (C.2)).

To create a realistic component library, a MATLAB script was developed to find the theoretical minimum-mass design for any required inductance by simulating all winding configurations for every core in the manufacturer's catalogue. The results of this process are shown as the stepped curves in fig. C.4. To use this data within the continuous optimisation framework, a conservative upper-bound linear model was fitted to the data. This ensures that any component selected by the algorithm is guaranteed to be physically realisable. The resulting linear approximations for the choke's ESR, mass, and volume as a function of its CM equivalent inductance (L_{CM} in µH) are:

1. $R_{\text{ESR,CM}} = 0.0010 \cdot L_{\text{CM}} + 0.2728$ in mΩ.
2. $m_{\text{Lcm}} = 0.1673 \cdot L_{\text{CM}} + 29.0042$ in g.
3. $V_{\text{Lcm}} = 0.000122 \cdot L_{\text{CM}} + 0.031624$ in L.

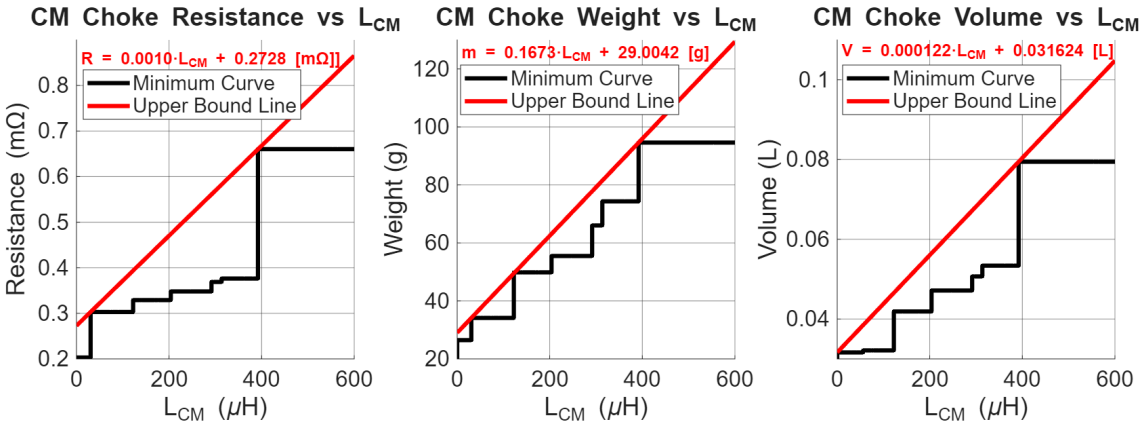


Figure C.4: Theoretical minimum weight CM choke designs with the corresponding resistance, weight and volume. An upper bound linear line shows the used approximation.

CM Capacitor Selection (C_{CM})

For the C_{CM}, a larger capacitance offers better filtering. However, the total value of line-to-ground capacitance must be limited to $C_{\mathrm{CM,max}}$ stated in table 2.1. This is primarily due to safety considerations related to leakage currents. The capacitors create a path for a small AC leakage current to flow to the equipment's chassis, and excessive leakage current can pose an electric shock hazard [19].

Although DO-160G does not specify a direct limit on CM capacitance for aerospace applications, the principle of limiting leakage current remains critical. For this framework, an upper bound of 180 nF is set for the total CM capacitance. This value is distributed across the 6 CM and damping capacitors with the ratio $C_{\mathrm{CM}} = 2C_{\mathrm{damp,CM}}$, i.e. $C_{\mathrm{CM}} = 20\,\mathrm{nF}$ and $C_{\mathrm{damp,CM}} = 10\,\mathrm{nF}$. SMD ceramic capacitors are used, as these are fixed across all designs, a constant weight and volume of 5.7 g and $0.666\,\mathrm{cm}^3$ are used.

C.4.2 Optimised Damping of the CM Filter

Effective damping is required for the CM filter for the same reasons as for the DM filter: to suppress resonances and ensure stability. The CM equivalent circuit of fig. C.3 shows that each stage requires its own damping network. Due to the difference in inductance, two different damping networks are required. An RC series damping topology is used for both stages as it provides a compact and effective solution.

The design of these damping networks follows the same optimal Q-factor approach used for the DM filter, as detailed in [32]. The damping capacitor is chosen as $C_{\mathrm{damp,CM}} = \frac{1}{2}C_{\mathrm{CM}}$, which results in an optimal Q-factor of $Q_{\mathrm{opt}} = \sqrt{55/9}$ (see eq. (C.4)). The required damping resistance for each stage can then be calculated directly.

- **CM choke damping (dark blue):** The first two stage damping circuit is responsible for damping the filter comprising the CM choke, which consists of the main CM choke (L_{CM}) and the leakage inductance of the CM choke ($\frac{1}{2}L_{\mathrm{DM}}$). Note that in the equivalent circuit, the damping resistance is halved. Thus, requiring double the resistance, so the optimal damping resistance is:

$$R_{\mathrm{damp,CM,a}} = 2R_0Q_{\mathrm{opt}} = 2R_0\sqrt{\frac{55}{9}} = 2\sqrt{\frac{L_{\mathrm{CM}} + \frac{1}{2}L_{\mathrm{DM}}}{2C_{\mathrm{CM}}}}\sqrt{\frac{55}{9}}. \tag{C.9}$$

- DC inductor damping (light blue): Similarly, the second damping circuit is responsible for damping the filter comprising the DC inductor in parallel with its damping inductance ($\frac{1}{2}L_{\mathrm{DC}}//\frac{1}{2}L_{\mathrm{damp,DC}}$). The optimal resistance for this network is:

$$R_{\mathrm{damp,CM,b}} = 2R_0Q_{\mathrm{opt}} = 2R_0\sqrt{\frac{55}{9}} = 2\sqrt{\frac{\frac{1}{2}\frac{L_{\mathrm{damp,DC}}\cdot L_{\mathrm{DC}}}{L_{\mathrm{damp,DC}}+L_{\mathrm{DC}}}}{2C_{\mathrm{CM}}}}\sqrt{\frac{55}{9}}. \tag{C.10}$$

C.4.3 CM Filter Sizing Procedure

The CM filter design procedure, shown in the green box in fig. 3.1, is used to find the CM filter components that minimise mass and volume while satisfying the regulatory requirements. This stage follows the DM filter design, receiving the completed DM filter as a fixed input. As with the preceding stage, the procedure uses the fixed system specifications (see table 2.1) and a set of variable design choices. For the CM filter design, the design choices are: inverter type, number of parallel devices, $L_{\mathrm{DM,min}}$ and switching frequency. It also receives the filter inductance of the interphase inductor.

The sizing process begins by calculating the required damping components for the search range, using eqs. (C.9) and (C.10). Next, a binary search is performed over the range of $L_{\mathrm{CM}} \in [1, 1000]$µH to find the minimum required inductance. For each tested L_{CM} value, the system is simulated across multiple modulation indices, $m = \{0.1, 0.2, .., 0.57735, .., 1\}$, using the method detailed in section B.2. The resulting CM current spectrum is then evaluated against the single pass/fail criterion, where the entire spectrum must be at least 6 dB below the DO-160G limit line for all tested modulation indices. Based on the pass/fail result, the search interval is halved, and the process continues until the required inductance is known with a resolution of 1 µH. The lowest inductance value found that satisfies the criterion is then selected as the final design.

C.5 Interphase Inductor Design

Table C.1: Equivalent inductance and resistance for coupled and uncoupled interphase inductors [14].

Inductor type	$\boldsymbol{L_{\mathrm{cir}}}$	$\boldsymbol{L_{\mathrm{f}}}$	$\boldsymbol{R_{\mathrm{cir}}}$	$\boldsymbol{R_{\mathrm{f}}}$
Coupled	$2L_{\mathrm{s}}(1+k)$	$\frac{1}{2}L_{\mathrm{s}}(1-k)$	$2R_{\mathrm{s}}$	$\frac{1}{2}R_{\mathrm{s}}$
Uncoupled	$2L_{\mathrm{s}}$	$\frac{1}{2}L_{\mathrm{s}}$	$2R_{\mathrm{s}}$	$\frac{1}{2}R_{\mathrm{s}}$

The interleaved inverter types require an interphase inductor to limit the circulating current. This inductor can be coupled or uncoupled. A coupled inductor benefits from extra inductance seen by the circulating current (L_{cir}) compared to an uncoupled inductor for equal self-inductance (L_{s}), as seen in table C.1. Where $k \in [0, 1]$ denotes the magnetic coupling factor between the windings. The equivalent filter inductance (L_{f}) is seen by the inverter output before the load. From table C.1 it can be seen that for a coupled inductor, this is smaller than for an uncoupled inductor. This reduces the high-frequency filtering of the CM noise (as L_{f} forms a low-pass filter in the coupling path in fig. B.4). If it is large, the required CM filter could be reduced [8]. However, the coupled inductor has the benefit that the flux due to the output current cancels inside the core. Thus, the magnetic core can be smaller and lighter for the coupled inductor than for two uncoupled inductors. So from now on, only a coupled interphase inductor (interphase transformer) is used.

C.5.1 Design Requirements and Sizing Equations

Interphase Inductance Lower Bound to Limit the Circulation Current

The circulation current should be limited to reduce the losses, reduce the voltage ripple and protect the semiconductors and diodes from overcurrent. Rewriting eq. (A.9) and eq. (A.23) for the L_{cir} yields the expression for the minimum required circulation inductance:

$$L_{\text{cir,2LI}} \geq \frac{V_{\text{DC}}}{4 f_{\text{sw}} \hat{I}_{\text{cir}}^{\text{req}}}; \quad L_{\text{cir,3LI}} \geq \frac{V_{\text{DC}}}{8 f_{\text{sw}} \hat{I}_{\text{cir}}^{\text{req}}} \min(m_{\text{max}}\sqrt{3}, 1). \tag{C.11}$$

Here $\hat{I}_{\text{cir}}^{\text{req}}$ is the required maximum peak circulation current and m_{max} maximum modulation index to meet the maximum output power. From this, it can be seen that for a 3LI VSI for any m, the minimum L_{cir} is at least half the size of that of a 2LI VSI. This is an intrinsic benefit of interleaving a multilevel inverter. For most practical designs, it can be assumed that $m > \frac{1}{\sqrt{3}} \approx 0.577$. Thus requiring twice as large an interphase inductor for a 2LI compared to a 3LI VSI.

$\hat{I}_{\text{cir}}^{\text{req}}$ can be determined based on:

- **Available current margin:** The maximum current of the MOSFETs and diodes, with some safety factor, should not be surpassed with the addition of the circulation current. Thus, the absolute maximum the circulation can be is dependent on this margin. Having more parallel devices can increase this margin nearly indefinitely. This gives the smallest possible L_{cir} value that could be used. This comes at the downside of higher losses, increased DC link current and voltage ripple, increased EMI generation through an increase of $\mathrm{d}i/\mathrm{d}t$ and high magnetic flux density (B). A high B-field requires a large core to prevent saturation, meaning that the decrease in size and mass does not continue indefinitely with a decrease of L_{cir}
- **User defined maximum:** There is a trade-off between lower losses and a smaller inverter size. However, this is not a linear trade-off, as a smaller $\hat{I}_{\text{cir}}^{\text{req}}$ reduces the core size needed, and a larger core allows for more turns, creating more inductance more easily. This trade-off is mainly dependent on the core material chosen, devices and wire size.

Interphase Inductance Upper Bound to Ensure Power Delivery

The equivalent filter inductance L_{f} sets an upper limit on the size of the interphase inductor. This is because the L_{f} is part of the output seen by the inverter and thus changes the power factor (PF) and thereby how much real power can be delivered to the load (P_{L}), without exceeding the maximum modulation index m_{max}. The power in the load can be calculated by eq. (C.12), where I_{o} is the RMS output current given by eq. (C.13) [20]. Assuming a lossless system so that $I_{\text{DC}} = \frac{P_{\text{in}}}{V_{\text{DC}}} = \frac{P_{\text{o}}}{V_{\text{DC}}}$, where P_{o} is the output power. The output power can also be written in terms of the load power by $P_{\text{o}} = \frac{P_{\text{L}}(R_{\text{L}}+R_{\text{f}})}{R_{\text{L}}}$, where R_{f} is the equivalent filter resistance of the interphase inductor being half the winding resistance (R_{s}). Using this and substituting eq. (C.13) into eq. (C.12) and rewriting for $\cos(\theta)$ gives

eq. (C.14).

$$P_{\mathrm{L}} = 3I_{\mathrm{o}}^2 R_{\mathrm{L}} \tag{C.12}$$

$$I_{\mathrm{o}} = \frac{2\sqrt{2}}{3} \frac{I_{\mathrm{DC}}}{m\cos(\theta)} \tag{C.13}$$

$$\cos(\theta) = \sqrt{\frac{8(R_{\mathrm{L}} + R_{\mathrm{f}})^2 P_{\mathrm{L}}}{3m^2 V_{\mathrm{DC}}^2 R_{\mathrm{L}}}} \tag{C.14}$$

The PF of the complete output can be calculated with eq. (C.15). Setting eqs. (C.14) and (C.15) equal and rewriting for L_{f} gives eq. (C.16). Which gives the maximum equivalent filter inductance to deliver the desired load power P_{L} given a maximum modulation index $m_{\max}$.

$$\cos(\theta) = \frac{R_{\mathrm{L}} + R_{\mathrm{f}}}{\sqrt{(R_{\mathrm{L}} + R_{\mathrm{f}})^2 + \omega_{\mathrm{AC}}^2 (L_{\mathrm{L}} + L_{\mathrm{f}})^2}} \tag{C.15}$$

$$L_{\mathrm{f}} < \frac{R_{\mathrm{f}} + R_{\mathrm{L}}}{2\pi f_{\mathrm{AC}}} \sqrt{\frac{3m_{\max}^2 V_{\mathrm{DC}}^2 R_{\mathrm{L}}}{8P_{\mathrm{L}}(R_{\mathrm{L}} + R_{\mathrm{f}})^2} - 1} - L_{\mathrm{L}} \tag{C.16}$$

In our case for $m_{\max} = 1$, $P_{\mathrm{L}} = 20\mathrm{kW}$ and $R_{\mathrm{f}} = 0.5R_{\mathrm{s}} = 2\mathrm{m}\Omega$, $L_{\mathrm{f}} < 40\mu\mathrm{H}$. Assuming a coupling factor of $k = 0.96$ gives a maximum self-inductance of $L_{\mathrm{s}} < \frac{2L_{\mathrm{f}}}{1-k} = 2.00\,\mathrm{mH}$.

C.5.2 Component Selection and Modelling

As the interphase inductor has a significant $\hat{I}_{\mathrm{cir}}$, inducing a large flux in the core, nanocrystalline cannot be used. For the same reasons as for the DC inductor, Edge is also a good core material to use in this situation. MPP can also be a good option, but it will saturate more quickly than Edge, which becomes a problem for the higher circulation currents we also investigate. To facilitate an easier comparison between designs, the same material should be used. Therefore, Edge was chosen for all the designs. Edge is available in toroidal cores and E-cores. In this thesis, toroidal cores were selected as they are available in a higher permeability core. A permeability of $\mu_{\mathrm{r}} = 90$ was selected as it is a good trade-off between saturation and inductance per turn for the given situation. To compensate for the decreased cooling capabilities of toroidal cores, the number of cores is kept at one unless not possible otherwise.

The trade-off between efficiency and weight/mass is investigated by designing for five different $\hat{I}_{\mathrm{cir}}^{\mathrm{req}}$ values: {10%,20%,30%,40%,50%} of the RMS output current, corresponding to $\hat{I}_{\mathrm{cir}} = \{4.7, 9.4, 14.1, 18.8, 23.5\}\mathrm{A}$. A 9 AWG wire was initially selected. To evaluate the trade-off between conduction losses and inductor mass, a thicker 7 AWG wire is also investigated. The thicker wire has a lower ESR but results in a heavier and larger component

For each combination of $\hat{I}_{\mathrm{cir}}$, f_{sw} and wire size, a new interphase inductor needs to be designed. This is because the interphase inductor needs to have the specified inductance at the specified circulation current. As a higher current saturates the core quicker, it is not fair to reuse the same design for all circulation currents. A larger wire size limits the maximum number of turns, while a change in f_{sw} changes the required inductance (see eq. (C.11)). The designed cores all stay below a winding factor of 50%.

C.5.3 Interphase Inductor Sizing Procedure

The final selection of the interphase inductor follows the direct process illustrated in the purple box of the design flowchart (fig. 3.1). The procedure ensures the lightest possible component that meets the performance requirements is chosen.

First, for each unique design configuration defined by the chosen wire size, f_{sw} and $\hat{I}_{\text{cir}}^{\text{req}}$, the minimum necessary self-inductance (L_s) is calculated using eq. (C.11).

Next, for each core in the core list, all winding configurations for every core are evaluated. Only if the largest core cannot meet the inductance requirement is the number of cores incremented. The evaluation is at $\hat{I}_{\text{cir}}$ and assuming the worst tolerance. The final selected interphase inductor is the lightest out of all the possibilities that have more or equal to the required L_s.

C.6 Heatsink Design

The goal of the heatsink design is not to have the most optimal solution for every heatsink design, but rather to characterise the mass and volume based on the required thermal resistance. The heatsink can use either passive cooling, forced convection cooling or liquid cooling. Liquid cooling is not available in all aircraft, and passive cooling cannot achieve a low enough thermal resistance for a competitive mass/volume. Thus, forced convection cooling is used, using one or more fans blowing over a heatsink with multiple fins. Drofenik et al. [37], [38], [39], [40] investigate the theoretical converter power density limits for forced convection cooling. This method involves modelling the thermal and fluid dynamics numerically to find an operating point where the fan's pressure curve intersects with the heatsink's impedance curve. This theoretical model will be used as the basis of the heatsink design. Since the goal is not to design the theoretical limit, but rather to have a heatsink that is fair in comparison. The global heatsink trend will be approximated into performance metrics based on the required thermal resistance.

C.6.1 System Requirements and Component Selection

The designed inverter needs to fulfil the requirements of the DO-160G chapter 4, where it falls in category D2. For this category, the inverter operates in an environment equal to the outside, where it goes from sea level to 15.2 km. This means that it operates at an air pressure of 11.6 kPa to 101.32 kPa and has a temperature range of −55 °C to 70 °C [6]. It is described in the DO-160G that it needs to operate in this full range. However, this is an unrealistic criterion as at 15.2 km temperatures of 70 °C are 125 °C above the international standard atmosphere model (ISA) [41], which is unrealistic. For a more realistic approach, ISA+35 °C is used, combined with the ground point that remains 70 °C at 101.32 kPa. This results in two critical design points: (−20 °C, 11.6 kPa) and (70 °C, 101.32 kPa).

Ram air could be used for forced convection, but fans are used instead, as their behaviour is well-documented. Centrifugal and axial fans can both be used, where centrifugal fans have the benefit of higher static pressure, which could be beneficial in our situation [42]. However, axial fans are more readily available in various sizes and are easier to arrange side-by-side for modularity. Due to these practical advantages, an axial fan is selected for this study.

The specific fan chosen is the THD0612VE-00, a high-performance 60 mm axial fan. It is rated for an operating temperature range of −40 °C to 70 °C and at sea level has the operating curve as seen in fig. C.5. It is important to note that the fan's lower temperature

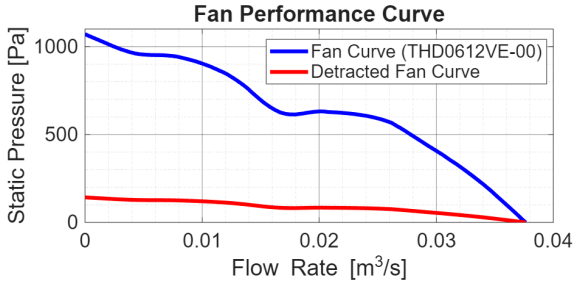


Figure C.5: THD0612VE-00 operating curve, with the derated curve at 15.2 km altitude.

limit of −40 °C does not meet the full −55 °C requirement from the DO-160G standard, representing a known limitation in this component selection.

A critical aspect of the design is de-rating the fan's performance for the high-altitude, low-density environment. Fan performance curves are specified at sea-level standard conditions. At altitude, the air density (ρ) decreases significantly, which reduces the fan's ability to generate pressure (P). Air density is calculated using the ideal gas law: $\rho = \frac{P}{RT}$ [43], where R is the specific gas constant and T the temperature. To find the de-rating factor, the density at the high-altitude condition is compared to the sea-level reference density:

$$\frac{\rho_{\text{alt}}}{\rho_0} = \frac{P_{\text{alt}}/T_{\text{alt}}}{P_0/T_0} = \frac{11.6/253.15}{101.32/293.15} \approx 0.133 \tag{C.17}$$

So at altitude, the density ratio $\frac{\rho_{\text{alt}}}{\rho_0} \approx 0.133$ implies the fan can deliver roughly 13.3% of its sea-level rated static pressure (neglecting Reynolds-number effects and assuming unchanged speed and geometry). This significant performance reduction can be seen in fig. C.5.

C.6.2 Heatsink Sizing and Optimisation Procedure

An extruded-fin heatsink can be seen in fig. C.6a, where it also has some length L. The fan is placed in front of the base plate, but in front of the fins. The heatsink design is governed by several geometric and manufacturing constraints, based on the analysis in [37] and practical considerations:

- **Fixed geometry:** To ensure mechanical stability, enable thermal heat spreading and allow the use of screw holes, the base plate thickness is fixed at $d = 10\,\text{mm}$. No air duct will be used in the basic design, so the fin height is fixed at the fan height ($c = 60\,\text{mm}$). The heatsink width (b) is set to a multiple of the fan width.
- **Base plate area (A_{hs}):** The base plate must be large enough to mount the power PCB and all power inductors, e.g. $A_{\text{heatsink}} = A_{\text{pcb}} + 2A_{\text{Lcm}} + 2A_{\text{Ldc}} + 3A_{\text{Ls}}$. Combined with the width b, the length L can be calculated from the area.
- **Manufacturing limits:** For manufacturability, a minimum fin thickness of $t = 1\,\text{mm}$ and a minimum channel spacing of $s = 1\,\text{mm}$ are enforced.
- **Optimisation variables:** With these constraints, the primary variables for the thermal optimisation are the number of fins (n) and the channel width-to-pitch ratio ($k = \frac{s}{b/n}$) [37].

The design of the forced-air cooled heatsink follows the optimisation procedure set out in [39]. The overall layout of this process can be seen in fig. C.6b. The procedure begins

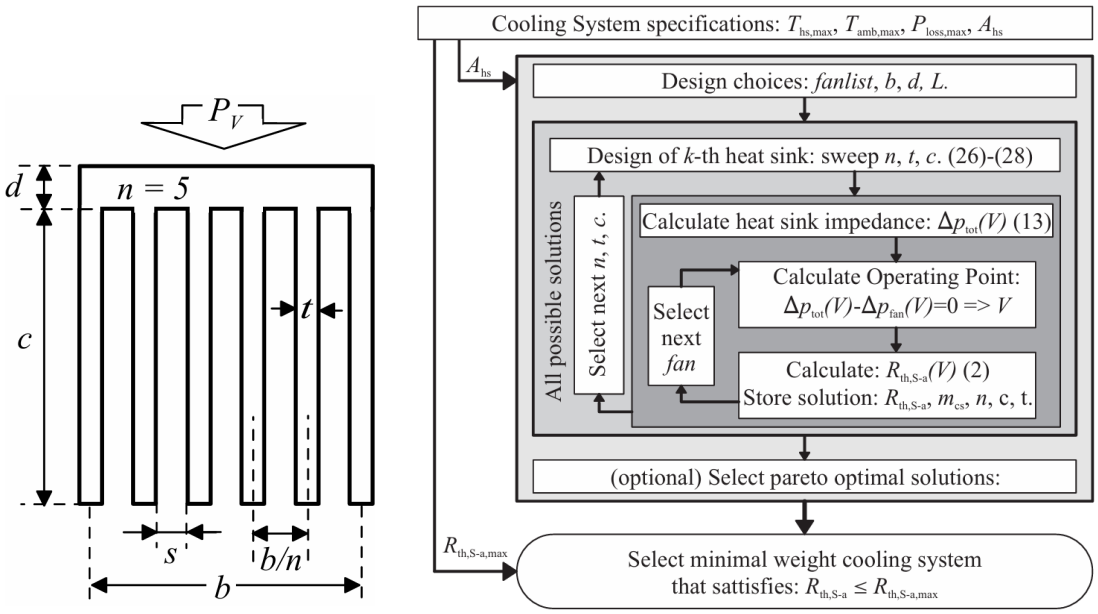


Figure C.6: (a) Geometry of the fan, with six fins and five channels [37]. (b) Minimum weight forced air cooling system optimisation procedure [39]

by defining the physical constraints of the heatsink and then executes a parametric sweep to find the configuration with the minimum mass for a required thermal resistance. For a detailed explanation, the reader is referred to [39]. The parametric sweep is implemented in a MATLAB script, which automates the search for the optimal fin geometry. Based on the design choices from above, the design follows these steps:

1. **Design of k-th heat sink: sweep n, t, c:** The script iterates through a range of possible numbers of fins (n) and, for each n, sweeps through a range of channel width-to-pitch ratios (k).

2. **Calculate heat sink impedance:** For each potential geometry, the heatsink's airflow impedance curve ($\Delta p_{\text{tot}}(\dot{V})$) is analytically calculated using the models for pressure drop in channels, as described in [37], [40].

3. **Calculate operating point:** The fan's actual operating point is found by numerically solving for the intersection where the heatsink's impedance equals the fan's de-rated pressure curve ($\Delta p_{\text{tot}}(\dot{V}) - \Delta p_{\text{fan}}(\dot{V}) = 0$). This yields the actual airflow rate ($\dot{V}$) for that specific geometry.

4. **Calculate performance and store solution:** Using the calculated airflow rate, the total thermal resistance ($R_{\text{th,S-a}}$) is calculated. Simultaneously, the total cooling system mass (m_{cs}) and volume (V_{cs}) for that geometry are computed. All relevant parameters ($R_{\text{th,S-a}}$, m_{cs}, V_{cs}, n, k, etc.) are then stored as a complete solution for that design point.

This entire process is repeated for all geometries and for the two critical environmental conditions. The final geometry is selected as the configuration that yields the minimum mass while satisfying the required thermal resistance ($R_{\text{th,S-a}} \leq R_{\text{th,S-a,max}}$) for the worst-case high-altitude condition.

C.6.3 Generalized Heatsink Results

Using the framework described in the previous section, a reference heatsink design is created to establish generalised performance metrics. The design is based on an aluminum heatsink ($\lambda_{\mathrm{Al}} = 210\,\mathrm{W\,m^{-1}\,K^{-1}}$) for a representative power loss of $P_{\mathrm{loss,max}} = 300\,\mathrm{W}$. The maximum allowable heatsink surface temperature is set to $T_{\mathrm{hs,max}} = 100\,^{\circ}\mathrm{C}$. The required thermal resistance ($R_{\mathrm{th,req}}$) is then calculated for the two critical environmental conditions:

$$R_{\mathrm{th,req}} = \frac{T_{\mathrm{hs,max}} - T_{\mathrm{amb,max}}}{P_{\mathrm{loss,max}}} \tag{C.18}$$

For the high-altitude condition ($T_{\mathrm{amb,alt}} = -20\,^{\circ}\mathrm{C}$), it requires $R_{\mathrm{th,req,alt}} \leq 0.4\,\mathrm{K\,W^{-1}}$. For the sea-level condition ($T_{\mathrm{amb,sea}} = 70\,^{\circ}\mathrm{C}$), it requires $R_{\mathrm{th,req,sea}} \leq 0.1\,\mathrm{K\,W^{-1}}$. The design is optimised to meet the more challenging high-altitude requirement. However, for some of the heatsink designs, it does not pass the thermal requirement for the sea-level conditions. These heatsinks are thus also removed from the options.

The optimisation procedure yields a minimum-mass heatsink design that satisfies these conditions. From this specific design, the performance indices for both environments can be determined. The CSPI is found to be:

$$CSPI = \frac{1}{R_{\mathrm{th}} \cdot V_{\mathrm{hs}}} \approx \begin{cases} 2.5\,\mathrm{W\,K^{-1}\,L^{-1}} & \text{at high altitude } (-20\,^{\circ}\mathrm{C}, 11.6\,\mathrm{kPa}) \\ 7.0\,\mathrm{W\,K^{-1}\,L^{-1}} & \text{at sea level } (70\,^{\circ}\mathrm{C}, 101.32\,\mathrm{kPa}) \end{cases} \tag{C.19}$$

Similarly, the MPI is found to be:

$$MPI = \frac{1}{R_{\mathrm{th}} \cdot m_{\mathrm{hs}}} \approx \begin{cases} 2.8\,\mathrm{W\,K^{-1}\,kg^{-1}} & \text{at high altitude } (-20\,^{\circ}\mathrm{C}, 11.6\,\mathrm{kPa}) \\ 7.5\,\mathrm{W\,K^{-1}\,kg^{-1}} & \text{at sea level } (70\,^{\circ}\mathrm{C}, 101.32\,\mathrm{kPa}) \end{cases} \tag{C.20}$$

This design was made for a few different power loss points, and the performance indices are within $0.2\,\mathrm{W\,K^{-1}\,kg^{-1}}$ and $0.2\,\mathrm{W\,K^{-1}\,L^{-1}}$. Thus, by using these performance indices to estimate the mass and volume of any heatsink based on the thermal resistance, a powerful simplification for the main optimisation framework is created. Where the indices for the high-altitude condition are used for the mass and volume estimation:

$$m_{\mathrm{hs}} = \frac{1}{R_{\mathrm{th,req}} \cdot MPI_{\mathrm{alt}}} = \frac{P_{\mathrm{loss}}}{(T_{\mathrm{hs,max}} - T_{\mathrm{amb,alt}}) \cdot MPI_{\mathrm{alt}}} \tag{C.21}$$

$$V_{\mathrm{hs}} = \frac{1}{R_{\mathrm{th,req}} \cdot CSPI_{\mathrm{alt}}} = \frac{P_{\mathrm{loss}}}{(T_{\mathrm{hs,max}} - T_{\mathrm{amb,alt}}) \cdot CSPI_{\mathrm{alt}}} \tag{C.22}$$

For the design process as seen in fig. 3.1, the inverter losses (P_{loss}) are simulated at the maximum output power P_{L} and at $100\,^{\circ}\mathrm{C}$ heatsink temperature. The maximum heatsink temperature ($T_{\mathrm{hs,max}}$) and maximum ambient temperature at altitude ($T_{\mathrm{amb,max}}$) are system specifications. Together, these parameters can be filled into eqs. (C.21) and (C.22) to find the mass and the volume. Using the CSPI and MPI at altitude. This method allows for a rapid yet fair estimation of the heatsink's contribution to the total inverter mass and volume for every design considered in this thesis.

C.7 Power PCB Design

The power PCB contains the MOSFETs, diodes, MOSFET drivers, isolated supplies, and isolated communication chips. Underneath the power PCB, the heatsink is placed to cool

all components. This low thermal path is deemed beneficial for this thesis, so it is assumed that a cut-out is made for each MOSFET/diode with some margin inside the PCB.

To approximate the PCBs size and mass, we first define three variables based on the topology and their physical properties.

- a: the total number of power devices (i.e., all MOSFETs and diodes). Each device has a TO-247 package. Per a, when accounting for clearance, this results in a footprint of $5.44\,\mathrm{cm}^2$ (with a $4.62\,\mathrm{cm}^2$ PCB cut-out) and a mass of 6 g.
- b: the total number of MOSFETs, where each requires a separate gate driver. Per b, each driver and its associated passive components are assumed to occupy an area twice that of a power device (i.e., $2 \cdot 5.44\,\mathrm{cm}^2 = 10.88\,\mathrm{cm}^2$) and have a mass of 6 g.
- c: the number of distinct isolation levels required for the gate drivers. Per c, it requires its own isolated supply and communication. This is estimated to require $3\,\mathrm{cm}^2$ of area and 6 g of mass per level. A fixed base mass of 20 g is also assumed for the main low-voltage supply.

Furthermore, it is assumed that the PCB has 30% of empty area. Thus, the total area including cut-outs of the power PCB is approximated as:

$$A_{\mathrm{pcb}} = 1.3((a + 2b) \cdot 5.44 + 3c) \qquad [\mathrm{cm}^2] \tag{C.23}$$

For the volume, we assume the PCB needs a 10 mm clearance above the components and the board itself has a standard height of 1.57 mm. As the board is mounted on the heatsink, this gives a total populated height of 11.57 mm (1.157 cm). The total populated volume is therefore:

$$V_{\mathrm{pcb}} = A_{\mathrm{pcb}} \cdot 1.157 \quad [\mathrm{cm}^3] \tag{C.24}$$

The total mass of the PCB is the sum of the component masses and the board mass. The component mass is derived from the bulleted list:

$$m_{\mathrm{components}} = 6(a + b + c) + 20 \quad [\mathrm{g}] \tag{C.25}$$

The board mass is calculated from its physical volume (total area minus cut-outs, times board thickness) and the $2.0\,\mathrm{g/cm}^3$ density of FR4 [44].

$$m_{\mathrm{board}} = (A_{\mathrm{pcb}} - (a \cdot 4.62)) \cdot 0.157 \cdot 2.0 \quad [\mathrm{g}] \tag{C.26}$$

The final PCB mass is the sum of these two parts:

$$m_{\mathrm{pcb}} = m_{\mathrm{components}} + m_{\mathrm{board}} \tag{C.27}$$

C.8 Other Components

In addition to the design-dependent parts, several fixed components contribute constant weight and volume, summarised in table C.2. These values are based on conservative assumptions and simplified estimates.

For lightning protection, two clamping diodes are placed before and after the filter. A device such as the *AK3-430C-Y* (2.7 g, $6\,\mathrm{cm}^3$ each) is assumed, leading to a total of 11 g and $24\,\mathrm{cm}^3$. Inrush protection is realised with two MOSFETs in series with resistors and two bypass MOSFETs, mirrored for positive and negative DC input, yielding 4 MOSFETs

Table C.2: Estimated fixed components

Component	Weight	Volume
Lighting protection	11 g	24 cm^3
Inrush protection	48 g	44 cm^3
Control PCB	200 g	150 cm^3
Connectors	100 g	75 cm^3 inside housing 75 cm^3 outside housing
LV EMI filter	100 g	25 cm^3
Total	459 g	318 cm^3 inside housing 75 cm^3 outside housing

and 2 resistors (all TO-247). Since the MOSFETs require only simple drivers, the occupied volume is taken equal to the MOSFETs themselves rather than doubled as in section C.7. The resulting total is 48 g and 44 cm^3.

The inverter control is handled by a dedicated PCB containing an FPGA, low voltage (LV) power supply, communication drivers, DC ride-through capacitive bank, connectors, storage, and hardware safety logic. This board is approximated at 200 g and 150 cm^3. Three connectors are required: one for the three-phase output, one for the high voltage (HV) input, and one for LV supply and signals. Their combined contribution is 100 g and 150 cm^3, of which only half the volume (75 cm^3) is considered inside the housing. Finally, a EMI filter for the LV electronics is included to ensure regulatory compliance. Although not designed in detail, it is estimated at 100 g and 25 cm^3 (see table C.2).

Altogether, the fixed contributions amount to 459 g and 318 cm^3 inside the housing, with an additional 75 cm^3 outside (table C.2).

C.9 Housing Design

The housing should act as a shield for the EMI and to protect the inverter from the environment, where in some cases it also needs to be pressurised. The bottom side of the housing is the heatsink, whose area is determined in section C.6.2. Since the goal is to see the general effect that the mass of the housing has, the housing itself will be a simple rectangular box.

The total internal volume of the housing is calculated throughout the design flow in fig. 3.1. The housing should be able to fit all the components, where it is assumed that it has a 30% unused space. Using the width and length of the heatsink and total internal volume, the height of the housing can be determined. The housing is made from aluminium with a wall thickness of $t_{\text{housing}} = 2\,\text{mm}$. From this, the mass and complete inverter volume can be calculated. The total volume now includes the external side of the connectors, heatsink size and housing size, including the wall thickness.

Appendix D

RMS Circulation Current In 2LI VSI

Using the equations from chapter A and assuming that $\frac{f_{\text{sw}}}{f_{\text{ac}}} = \infty$, the RMS circulation current can be derived. This can be done for both 2L and 3L, but it is only shown here for the 2L, as for the 3L it would deviate too much to be useful. This is because the waveform for the 3L is not well defined by the equations of chapter A when the ratio of $\frac{f_{\text{sw}}}{f_{\text{ac}}}$ is in the realistic range.

The first step is to derive the RMS current of the waveforms in fig. A.2. Both waveforms are piecewise-linear trapezoidal shapes, consisting of alternating flat (plateau) and ramp (linear) segments and are symmetric around the zero-current axis. Each period contains two plateaus at $\pm\hat{I}_{\text{cir}}$ lasting for a total time of $2T_p$, and two linear ramps (from 0 to $\pm\hat{I}_{\text{cir}}$ and back) lasting a total of $2T_r$, leading to a full period $T_{\text{sw}} = 2T_p + 2T_r$. For the plateau region, the RMS current value is equal to $\hat{I}_{\text{cir}}$ and for the ramp it is equal to $\frac{1}{\sqrt{3}}\hat{I}_{\text{cir}}$. Using this, the RMS circulation current over one period is expressed as

$$I_{\text{RMS}} = \sqrt{\frac{1}{T_{\text{sw}}}\left(2\hat{I}_{\text{cir}}^2 T_p + \frac{2}{3}\hat{I}_{\text{cir}}^2 T_r\right)} = \hat{I}_{\text{cir}}\sqrt{\frac{T_p + \frac{T_r}{3}}{T_p + T_r}}. \tag{D.1}$$

The plateau and ramp times can be found from fig. A.2 for waveform (1) $T_p = \frac{T_1}{2} - \frac{T_2}{2}$ and $T_r = \frac{T_0}{2} + \frac{T_2}{2}$. For waveform (2), $T_p = \frac{T_1}{2} + \frac{T_2}{2}$ and $T_r = \frac{T_0}{2}$. Due to the symmetry of space vector modulation (SVM), it is sufficient to evaluate the current waveform over the interval $0 \leq \alpha \leq \frac{\pi}{6}$. To obtain the average RMS current over the full SVM cycle, eq. (D.1) is squared, integrated over the range $\alpha \in [0, \frac{\pi}{6}]$, and normalised. Substituting the expressions for T_p and T_r, the resulting sector-averaged RMS currents are:

$$I_{\text{cir,RMS,1}}(m) = \sqrt{\frac{6}{\pi}\int_0^{\frac{\pi}{6}} \hat{I}_{\text{cir,1}}^2(m,\alpha)\frac{T_1 + \frac{1}{3}T_0 - \frac{2}{3}T_2}{T_1 + T_0}\mathrm{d}\alpha} \tag{D.2}$$

$$I_{\text{cir,RMS,2}}(m) = \sqrt{\frac{6}{\pi}\int_0^{\frac{\pi}{6}} \hat{I}_{\text{cir,2}}^2(m,\alpha)\frac{T_1 + T_2 + \frac{1}{3}T_0}{T_0 + T_1 + T_2}\mathrm{d}\alpha} \tag{D.3}$$

Due to the symmetry of the space vector modulation (SVM) scheme over one full fundamental cycle ($\alpha \in [0, 2\pi]$), the circulating current waveform can be decomposed into repeating segments of waveform (1) and waveform (2). Specifically, within the full 2π range, $I_{\text{cir,RMS,1}}$ occurs 4 times, while $I_{\text{cir,RMS,2}}$ occurs 8 times. As the RMS value is computed over the full cycle, the total RMS value is given by:

$$I_{\text{cir,RMS}}(m) = \sqrt{\frac{1}{12}\left(4I_{\text{cir,RMS,1}}^2(m) + 8I_{\text{cir,RMS,2}}^2(m)\right)} \tag{D.4}$$

This expression captures the full-cycle RMS current. Filling in eqs. (D.2) and (D.3) and eq. (A.1)-A.3 gives an equation that is hard to solve. Therefore, it is chosen to compute the result using MATLAB and perform a third-order polynomial fit. This results in the following 2L RMS circulation current expression:

$$I_{\text{cir,RMS,2L}}(m) = \frac{V_{\text{DC}}}{4L_{\text{cir}}f_{\text{sw}}}\left(0.232m^3 - 0.530m^2 + 0.036m + 0.575\right) \tag{D.5}$$

Appendix E

The Spider Chart Ranking System

To summarise the trade-offs across all inverter topologies, a spider chart ranking was created. All scores were normalised on a 1-5 scale, where 5 denotes the best performance observed within the design space. The scoring procedure for each axis is described below.

- **Efficiency:** The 95^{th} percentile efficiency of all operating points with THD $\leq 2.2\%$ was used to ensure outliers did not dominate. Scores were linearly scaled between the lowest and highest values observed.
- **Specific Power:** The 95^{th} percentile of the specific power values was taken from all designs where THD $\leq 2.2\%$ and the efficiency is within 0.5% of the most efficient design for that topology. This ensures that only realistic high-performance designs are considered, avoiding bias from inefficient outliers while still capturing the best-performing region.
- **Power Density:** The 95^{th} percentile of the power density values was taken from all designs where THD $\leq 2.2\%$ and the efficiency was within 0.5% of the most efficient design for that topology. This approach ensures that the values used to represent power density reflect realistic, high-performance operating points. Extremely inefficient but compact designs were therefore excluded, avoiding a distorted ranking while still rewarding top-performing configurations.
- **THD Compliance Ease:** The average voltage THD over the switching frequency range was selected as the metric, as this directly reflects the inherent ability of a topology to produce low-distortion waveforms. Lower THD corresponds to a higher score. Where it is normalised based on the minimum and maximum average voltage THD.
- **Design Complexity:** Only the number of controlled switches was considered (diodes excluded). Topologies with fewer active devices received higher scores. Scores were normalised between the minimum (the 2L VSI) and maximum (the 3LI ANPC).

Appendix F

AI statement

During the preparation of this work, I used the following AI tools:

- **ChatGPT-5 and Claude Sonnet 4.5** to create the Matlab code that performs the PLECS sweeps and plots the data. After using these tools, I thoroughly reviewed and edited the code as needed, taking full responsibility for the final outcome.
- **ChatGPT-4.1** for helping to derive the circulation current equation. While using this tool, I thoroughly reviewed and corrected the derivation where needed, taking full responsibility for the final outcome.
- **Abacus deep agent** was used to review the thesisd and help write the discussion. After using this tool, I thoroughly reviewed the feedback and implemented it where deemed valid, taking full responsibility for the final outcome.
- **ChatGPT-5 and Gemini 2.5 Pro** were used to help with the writing of the thesis text. This included: thesis layout, writing parts of the subsection text, giving feedback on written text, interpreting results, looking for missing parts and mistakes. After using these tools, I thoroughly reviewed the suggestions and text as needed, taking full responsibility for the final outcome.
- **Grammarly** was used to check for grammar and spelling mistakes. After using this tool, I thoroughly reviewed and edited the suggestions and text as needed, taking full responsibility for the final outcome.