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Design of a sub-1V Bandgap Reference in FinFET Technology

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MSc. Thesis

July 2009

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Report number: 067.3267

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Abstract

The minimum feature size in CMOS technology decreases with newer generations to enable higher packing densities and higher speed of operation. As transistor dimensions become smaller and smaller the fundamental limiting factors of conventional CMOS are coming closer. One of the candidates to replace the conventional bulk technology is FinFET technology.

One of the analog circuits that need to be implemented is the bandgap voltage reference circuit. The original bandgap reference outputs a voltage around the bandgap of a diode: 1.2V, independent of temperature. For implementations in the newer (low-voltage) CMOS processes the supply voltage is lower than this reference voltage which makes it impossible to use the conventional bandgap reference circuits. However, some solutions are known to implement bandgap reference circuits at low voltages, but all require a large total resistor value.

In FinFET technology it is difficult to implement resistors and diodes. In this master assignment, an averaging bandgap reference structure is proposed to implement a low-supply voltage bandgap reference circuit in FinFET technology. The resistors that are typically required in known low-voltage bandgap references are replaced by a PTAT voltage source and a triode resistor. The PTAT voltage is made by cascaded voltage followers, with build-in PTAT offsets.

To make the triode resistor accurate over large voltage swings both a N-type and a P-type FinFET are used. These triode transistors need to be biased with a supply independent voltage.

The output voltage is the average of a CTAT and a PTAT voltage, using two stages of transimpedance amplifiers.

The simulated (layout) performance is:

$$V_{ref} = 565\text{mV}$$

$$\text{Sigma } V_{ref} = 0.42\%$$

$$\text{Area} = 0,084 \text{ mm}^2$$

$$V_{dd} > 0.85\text{V}$$

The designed circuit is layouted, and is currently in fabrication in a 32 nm FinFET process at IMEC.

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Preface

Chapter 1

Introduction

An example of an analog circuit implementation to be investigated in SOI FinFET technology is a reference circuit. The most widely used implementation for a voltage reference with a low temperature coefficient is a band-gap voltage reference. When properly designed, the circuit's output is a voltage that is somewhat higher than the material bandgap at 0K (for main-stream CMOS processes this is $V_{ref} = 1.220V$) and independent of temperature.

The operation principle of bandgap voltage references is the following: two quantities having opposite temperature coefficients are added with proper weighting; the result is a zero temperature coefficient reference. This means that a negative and a positive temperature coefficient have to be identified. A diode can produce both. The voltage difference between two diodes caused by unequal current densities is a PTAT (Proportional To Absolute Temperature) voltage. The diode voltage itself is complementary to absolute temperature (CTAT). Usually resistors are used in an OPAMP structure to achieve proper weighting; these cannot be made accurately in a SOI FinFET technology. Such an implementation will give a reference voltage that is around 1.2V.

The principle can be simplified into a simple block diagram as shown in figure 1.1.

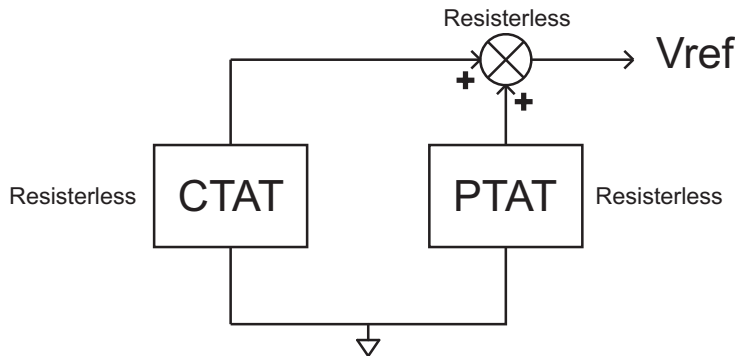


Figure 1.1: The blockdiagram of the main bandgap reference principle

Three blocks that have to be made: a voltage with a negative temperature coefficient (CTAT), a voltage with a positive temperature coefficient (PTAT)

and an adding circuit. To be able to make these in FinFET technology, these blocks preferably do not contain resistors. Also, the reference voltage needs to be lower than 1.2V, since the supply voltage is only 1V.

1.1 Problem definition

A problem for the integration of a bandgap reference in today's sub-micron CMOS technologies is that the supply voltage is lower than 1.2V, which is the reference voltage of the standard bandgap reference (see figure 1.2). Hence a low supply-voltage bandgap reference is needed.

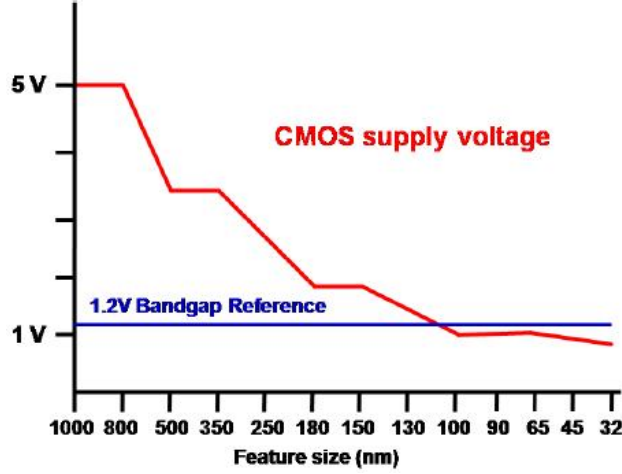


Figure 1.2: CMOS supply voltage as function of feature size

Another problem is that in FinFET technology it is difficult to make resistors, because there is no high-resistive layer (large area resistor needed). Diodes cannot be made by using source-well junctions, because there are no wells in our SOI FinFET process (a replacement of the source-well junctions is found in the lubistor (gated diode)).

FinFET technology properties are examined in section 1.2. The standard bandgap reference is reviewed in section 1.3. Various low-voltage bandgap reference topologies are considered in chapter 1.4. A thesis outline is given in section 1.5.

1.2 Fundamental limiting factors of the Mosfet

As the dimensions of the mosfet are decreasing also the control over the channel decreases. As a result the side effects will become more dominant [1], [2]. Some resulting problems are listed below:

- An important short channel effect is Drain-Induced-Barrier Lowering (DIBL). DIBL becomes more prominent as the length of the device is reduced. With higher drain voltage the depletion width between the drain and body increases in size and extends under the gate. As a result, the rest of the channel becomes more attractive for electrons. In other words, the potential energy barrier for electrons in the channel is lowered: the threshold voltage decreases.
- To keep short channel effects under control the gate oxide thickness is reduced (to ensure that the gate has more control over the channel than the drain). The thinner oxide layer decreases the energy barrier between the gate and the channel and therefore it is easier for electrons to tunnel through the insulator layer. Gate tunnelling can be avoided by using insulators with a higher dielectric constant: the so-called high-k materials, which increases the barrier between the gate and the channel.
- Another problem is that the threshold voltage is influenced more by doping fluctuations. As the gate length reduces the relative fluctuation in doping concentration becomes larger, because less doped ions are in the channel. So a small fluctuations in dopants will have a relatively large effect on the threshold voltage.

These problems become larger when the CMOS dimensions are shrinking. Therefore it is investigated how these problems can be solved. Some of the possibilities to postpone the fundamental limiting factors are not preferable, because they cannot be used in standard CMOS technology. Also some different device structures are proposed; one is to use a double gate. This is one of the options that can be used with others (for example high-K dielectric). To make a double gate structure various 3D rotations are possible: the planar device, the vertical (pillar) device and the FinFET as shown in figure 1.3 [3].

The planar device structure is closest to the MOSFET. The difference with the MOSFET is that there is a second gate below the channel. The electrons still flow parallel with the surface, but the additional gate provides extra control. A problem with this structure is the alignment of the gates, because the lower gate is masked by other layers. It can be done by using a sacrificial layer, but that requires additional steps. Creating the gates separately is simpler, but may lead to asymmetry and therefore increased overlap resistance, increased short channel effects and larger off-state leak currents. This problem can be solved by rotating the structure to its side. Now the gates are not masked by other layers. Another advantage of these vertical devices is the smaller wafer area that is needed. The disadvantage of the vertical MOSFET is that the gates are still separate pieces. Another disadvantage is that now the drain or source is masked. The easiest double gate structure to make, using standard CMOS processing, is the FinFET.

An advantage of the FinFET is that it eliminates the need of channel doping,

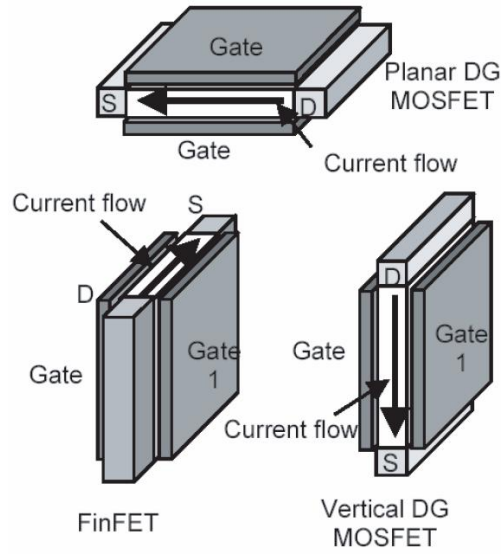


Figure 1.3: Planar, vertical and FinFET architectures

thereby reducing parametric spread due to dopant fluctuations and reducing junction leakage due to high electric fields. The reduction of leakage currents enables a steeper subthreshold slope and therefore lowers the power consumption (mainly of digital circuits). Besides the reduction of the leakage currents the multigate topology of the FinFET also increases the current of the device with a factor two. A disadvantage of the smaller dimensions of the fin and the undoped channel is the increasing source/drain resistance.

The crucial geometric device dimensions for the FinFET are (shown in figure 1.4):

L_{gate} = Gate length, the length of the gate metal.

W_{fin} = Width of the fin, the distance between the gate oxides of the two gates.

H_{fin} = Height of the fin, the distance between the buried oxide and the top gate oxide.

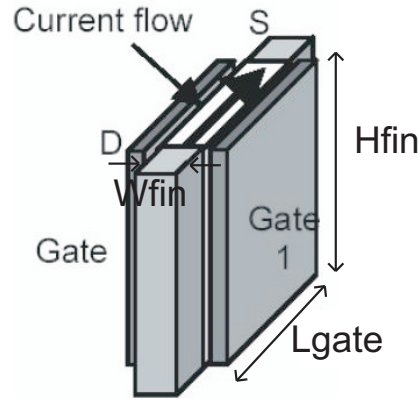


Figure 1.4: The FinFET device dimensions

1.3 Standard bandgap reference

As was already mentioned a bandgap voltage reference adds two quantities with opposite temperature coefficients with proper weighting; the result is a zero temperature coefficient. The voltage difference between two diodes caused by unequal current densities is used to generate a Proportional To Absolute Temperature voltage (positive contribution with increasing temperature). The voltage across a single diode itself is complementary to absolute temperature. A simple bandgap voltage reference circuit is shown in Figure 1.5 [4].

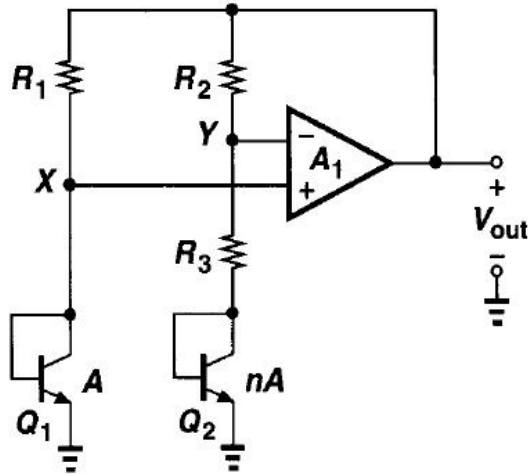


Figure 1.5: Symbolical circuit of a bandgap reference

The output of the OPAMP is temperature independent if the negative and the positive temperature coefficients are balanced. First these temperature coefficients are derived.

1.3.1 Negative temperature coefficient

The forward (base emitter) voltage of a pn-junction diode exhibits a negative temperature coefficient. To get an expression for this temperature coefficient the equation for the diode current is rewritten.

$$\begin{aligned}
 I_C &= I_{C,0} T^\eta e^{\left(\frac{q(V_{be} - V_{gap,0})}{K_b T}\right)} \\
 I_C &= I_s \exp \frac{qV_{be}}{K_b T} \\
 V_{be} &= \frac{K_b T}{q} \ln \left(\frac{I_C(T)}{I_{C,0} T^\eta} \right) + V_{gap,0}
 \end{aligned} \tag{1.1}$$

with:

$I_{C,0}$ a process and size-dependent constant;

$$I_s = I_{C,0} T^\eta e^{\left(\frac{q(-V_{gap,0})}{K_b T}\right)}$$

$\eta \approx 4$ a mobility-related constant;

T the temperature in K;

$V_{gap,0}$ the bandgap extrapolated to T=0K.

To find the temperature coefficient the derivative of the V_{be} to temperature has to be taken (for this $\frac{q}{K_b T}$ is rewritten as V_T).

$$\frac{\partial V_{be, V_T}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \left(\frac{I_c}{I_s} \right) - \frac{V_t}{I_s} \frac{\partial I_s}{\partial T} \tag{1.2}$$

with:

$$\frac{\partial I_s}{\partial T} = \mu_0 K_b (\eta) T^{\eta-1} e^{\left(\frac{-V_g}{K_b T}\right)} - \mu_0 K_b T^\eta \left(\frac{-V_g}{K_b T^2} \right) e^{\left(\frac{-V_g}{K_b T}\right)} \tag{1.3}$$

and

$$\frac{V_t}{I_s} = \frac{V_T}{\mu_0 k T^\eta e^{\left(\frac{-V_g}{K_b T}\right)}} \tag{1.4}$$

Substituting these in in equation 1.2 gives:

$$\begin{aligned}
 \frac{\partial V_{be, V_T}}{\partial T} &= \frac{\partial V_T}{\partial T} \ln \left(\frac{I_c}{I_s} \right) - \eta \frac{V_T}{T} + V_T \left(\frac{V_g}{K_b T} \right) \\
 &= \frac{V_{be} - \eta V_T - \frac{V_g}{q}}{T}
 \end{aligned} \tag{1.5}$$

1.3.2 Positive temperature coefficient

The voltage with a positive temperature coefficient is typically derived from a voltage difference between two diodes caused by unequal current densities. These unequal current densities can be forced in two ways; the current through the equal diodes can be different, or the diode area of the two diodes can be different. This is schematically shown in figure 1.6.

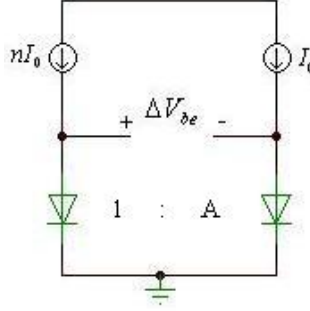


Figure 1.6: Simplified bandgap reference

The diode voltage difference is:

$$\begin{aligned}
 \Delta V_{diode} &= V_{be1} - V_{be2} \\
 &= V_T \ln\left(\frac{nI_0}{I_{s1}}\right) - V_T \ln\left(\frac{I_0}{AI_{s2}}\right) \\
 &= V_T \left\{ \ln(nI_0 - I_{s1}) - \ln(I_0 - AI_{s2}) \right\} \\
 &= V_T \ln\left(\frac{AnI_{s2}}{I_{s1}}\right)
 \end{aligned} \tag{1.6}$$

with n the current density ratio and A the diode area ratio.

To find the temperature coefficient the derivative of the V_{be} to temperature has to be taken.

$$\frac{\partial V_{be}}{\partial T} = \frac{K_b}{q} \ln(nA) \tag{1.7}$$

1.3.3 Reference voltage

When the temperature coefficients are known, an equation can be derived for the reference voltage (for the standard bandgap topology using resistors, see figure 1.1):

$$\begin{aligned}
 V_{out} &= I(R_2 + R_3) + \frac{K_b T}{q} \ln\left(\frac{I_C(T)}{I_{C,0} T^\eta}\right) + V_{gap,0} \\
 &= I(R_2 + R_3) + V_{diode2}
 \end{aligned} \tag{1.8}$$

The diode current is:

$$I = \frac{\frac{K_b T}{q} \ln(An)}{R_3} \tag{1.9}$$

This gives for the output voltage:

$$V_{out} = \frac{K_b T}{q} \ln(An) \frac{(R_2 + R_3)}{R_3} + V_{diode2} \tag{1.10}$$

In equation (1.10) the first term is PTAT, while the second is CTAT. To make the reference voltage temperature independent the weighting should be chosen properly:

$$\frac{\partial V_{diode}}{\partial T} \frac{R_2 + R_3}{R_3} = - \frac{\partial V_{vt}}{\partial T} \tag{1.11}$$

Substituting equation 1.7 and equation 1.5 yields:

$$\frac{R_2}{R_3} = - \frac{\frac{V_{diode} - \eta V_T - \frac{V_g}{q} + \frac{K_b}{q} \ln(An)}{T}}{\frac{K_b}{q} \ln(An)} \quad (1.12)$$

This simple bandgap reference cannot be implemented in FinFET technology because of two reasons. Firstly for its implementation three resistors are needed. For low power operation these need to be high ohmic. In FinFET technology these are difficult to make, because only metal(lic) gates are available to make resistors. This means no area efficient high-ohmic resistors can be made.

Secondly the reference voltage is higher than the supply voltage.

It can be concluded that a low-voltage bandgap reference topology needs to be found. In literature, low-voltage references can be found. Some are discussed in the next section.

1.4 Bandgap reference topologies / Solution proposal

Standard bandgap reference topologies need a supply voltage that is higher than the 1V supply that is available in the FinFET process. To be able to operate bandgap references at a supply voltage lower than the material bandgap, the bandgap reference circuits must have an output voltage lower than the silicon material bandgap voltage.

Associated with implementation in SOI FinFET technology include the use of high ohmic resistors and diodes; these cannot be made accurately in a SOI FinFET process.

In the next sections some architectures that use low supply voltages and also some circuits that do not require high-accuracy resistors are explored. A low voltage bandgap reference topology is chosen in section 1.5; which also gives the outline of the thesis.

1.4.1 Current domain bandgap reference

The bandgap reference topology proposed by Banba [5] is one of the most widely applied approaches to create good sub-1V bandgap reference circuits. A disadvantage of this approach is that it uses a number of matched high-ohmic resistors that take a significant die area for low power reference circuits. In FinFET technology this is even a larger problem because only metal(lic) gates can be used to make resistors.

The principle of Banba is that instead of voltages, currents are added. This is done by using the additional resistors. A PTAT current (I_{2a}) and a CTAT current (I_{2b} and I_{1b}) are added. This gives a current that is independent of temperature (I_2). The circuit is shown in figure 1.7.

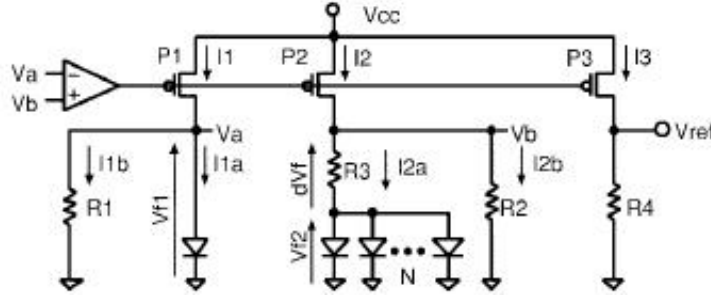


Figure 1.7: resistor subdivision bandgap reference

In the bandgap reference of Banba the two extra resistors are equal:

$$R_1 = R_2 \quad (1.13)$$

Due to the feedback loop around the OPAMP the voltages V_a and V_b are the same.

$$V_a = V_b \quad (1.14)$$

Also the transistors p1, p2 and p3 are the same:

$$I_1 = I_2 = I_3 \quad (1.15)$$

The PTAT current I_{2a} is known:

$$I_{2a} = I_{PTAT} = \frac{dV_f}{R_3} \quad (1.16)$$

with the voltage difference over the diode:

$$dV_f = V_{f1} - V_{f2} = \frac{K_b T}{q} \ln(N) \quad (1.17)$$

Also the CTAT current is known:

$$I_{2b} = I_{CTAT} = \frac{V_a}{R_2} \quad (1.18)$$

It follows that the current I_2 consists of I_{2a} (PTAT current) and I_{2b} (a CTAT current). By choosing the resistors correctly, a temperature independent

current can be generated. This current is then copied to the third branch which generates a reference voltage:

$$V_{ref} = R_4 \left(\frac{V_a}{R_2} + \frac{dV_f}{R_3} \right) \quad (1.19)$$

The disadvantage of this circuit is the use of additional high ohmic resistors. These can be made in FinFET technology, but only metal(lic) gates are available to make resistors. This means no area efficient high ohmic resistors can be made.

What is interesting in this bandgap reference circuit is the idea to mirror a current (the added PTAT current and CTAT current) to an extra resistor to generate the reference voltage.

1.4.2 Multi stage bandgap reference

One idea to eliminate the most high-ohmic resistor is found in the solution of Annema [7].

In conventional bandgap references (shown in figure 1.8), a PTAT voltage across a resistor compensates the negative temperature dependency of the voltage on a diode. For low power consumption, the current through the diodes must be small. This means that the resistors will be quite large. Note that the upper resistor is substantially larger than the lower ($N \approx 10$). Since these resistors need to be matched, the upper resistor will be physically large as well. If this resistor can be removed the occupied area will be substantially smaller.

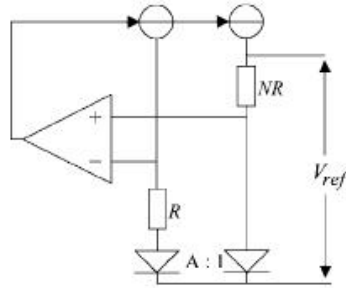


Figure 1.8: Typical CMOS bandgap reference

Elimination of the upper resistor can be done by replacing this resistor by cascaded voltage followers, with built-in PTAT offset voltages. The negative temperature coefficient of the voltage on the diode is then compensated by this offset voltage (the circuit is shown in figure 1.9). The leftmost part of this bandgap reference is similar to the conventional bandgap circuit. The only function of this block is to bias the diodes.

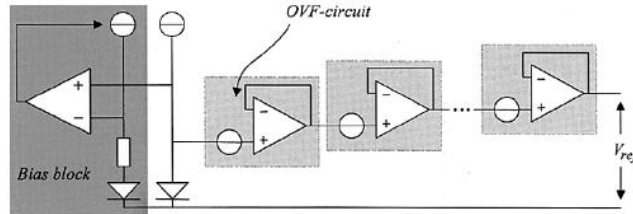


Figure 1.9: Principle of multistage bandgap reference

The cascaded voltage follower creates a PTAT voltage offset between the input and the output. An implementation of the voltage follower is shown in figure 1.10. In this circuit an intentional "size mismatch" in the differential pair and/or in the current mirror can be used to make unequal current densities in two subthreshold Mosfets.

For this the differential pair needs to have an exponential behavior:

$$I = I_0 e^{\frac{qV}{k_b T}} \quad (1.20)$$

In CMOS this can be done using DTMOST's as these have a diode like exponential transfer. For one cascaded voltage follower the output voltage is:

$$V_{out} = V_{in} + \frac{K_b T}{q} \ln\left(\frac{L_1}{W_1} \frac{W_2}{L_2} \frac{1}{M}\right) \quad (1.21)$$

With M the gain off the current mirror. When using this the reference voltage will be around 1.2V, as will a normal bandgap reference.

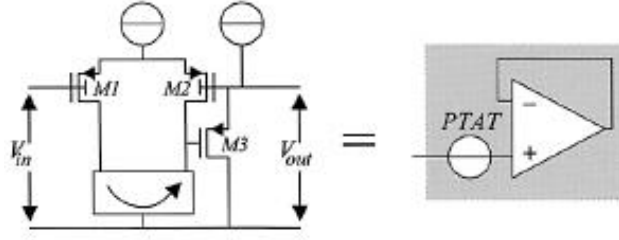


Figure 1.10: Schematic of the PTAT cascaded voltage follower circuit

The advantage of this topology is the reduced influence of the opamp error to the reference voltage. In the standard bandgap this opamp error is amplified by the resistor factor ($\frac{R_2}{R_3}$ in figure 1.5).

The advantage of this circuit is the reduction of the resistor dimensions. In CMOS DTMOST's are used to generate a PTAT voltage. In FinFET technology the sub-threshold behavior of a transistor has an exponential character and therefore this topology can work in FinFET technology as well. Another advantage is the reduced opamp error.

A disadvantage of the multistage bandgap reference is the high reference voltage, which is still 1.23V: this is above the supply voltage of FinFET technology.

1.4.3 Averaging bandgap reference

Another approach is to use weighted averaging. Instead of summing a PTAT and a CTAT voltage, they are averaged. Yielding a temperature independent voltage of 0.6V [6]. The averaging bandgap is shown in figure 1.11.

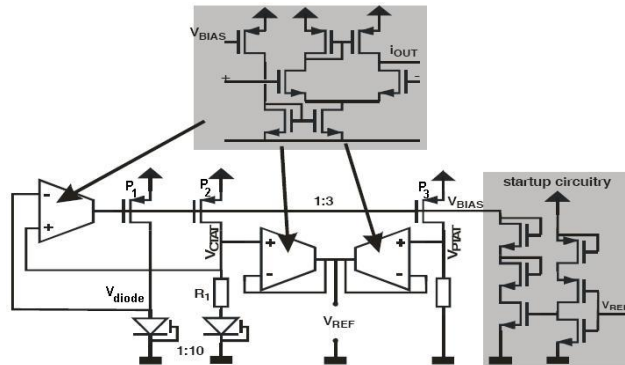


Figure 1.11: The sub-1-V bandgap circuit in 32 nm FinFET technology

The voltages V_{diode} and V_{CTAT} are the same because of the feedback loop around the opamp.

$$V_{diode} = V_{CTAT} \quad (1.22)$$

Because of this also the currents in transistors p1, p2 and p3 are the same (the current mirror gain is one).

$$I_1 = I_2 = I_3 \quad (1.23)$$

The V_{CTAT} is derived by the voltage over a diode.

$$V_{diode} = \frac{K_b T}{q} \ln\left(\frac{I_c}{I_{c,0} T^n}\right) + V_{gap,0} \quad (1.24)$$

The positive temperature coefficient is the difference between the diode voltages of the two diodes operating at different current densities. This gives a positive temperature coefficient of:

$$dV_f = V_{f1} - V_{f2} = \frac{K_b T}{q} \ln(N) \quad (1.25)$$

This PTAT voltage is then converted to a current with a resistor (R_1). This PTAT current is then copied to the third branch.

The averaging of the PTAT and CTAT signal is done using matched OTAs (operational transimpedance amplifier). These are used in such a way that OTA non-linearity is canceled.

The reference voltage is expressed by the following equation:

$$V_{ref} = \frac{g_{m_{left}}}{g_{m_{left}} + g_{m_{right}}} V_{ctat} + \frac{g_{m_{right}}}{g_{m_{left}} + g_{m_{right}}} V_{ptat} \quad (1.26)$$

When two identical OTAs are used gm_{left} and gm_{right} are equal and hence the output voltage is about 0.6V.

The advantage of this bandgap reference circuit is that it is similar to the traditional bandgap reference and contains just two resistors, which do not need to be so high ohmic. This is also the disadvantage of this circuit, because the two resistors need to be matched. Another advantage is that this circuit can operate at a low supply voltage.

1.5 Thesis outline

The principle of the averaging bandgap reference is used as the main principle for the bandgap reference in this project, which can be simplified into a simple block diagram as shown in figure 1.12.

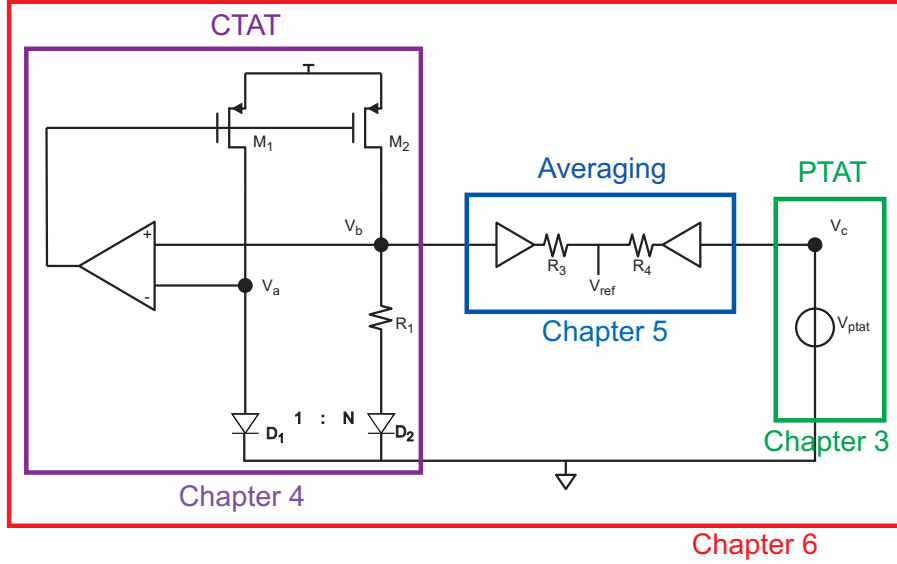


Figure 1.12: The averaging bandgap reference topology with chapter index

For all sub-blocks it is important that no high precision resistors and no high ohmic are used. Some other relevant target properties of the bandgap reference circuit that have to be taken into account are listed below:

$$V_{ref} \approx 0.6V$$

$$\sigma_{vref} = 0.5\%$$

$$\text{PSRR (Power Supply Rejection Ratio)} = 40dB.$$

The PTAT voltage is made by cascaded voltage followers, with build-in PTAT offsets (see section 1.4.3); the design of this PTAT stage is shown in chapter 2.

The CTAT sub-block uses a triode resistor for R_1 . To make this triode resistor accurate over larger voltage swings both, a N-type and a P-type FinFET are used. These triode resistor need to be biased with a voltage that is independent of the supply voltage (see chapter ??).

The averaging of the CTAT and the PTAT voltage is done using two stages of transimpedance amplifiers (see chapter 4).

The simulation results of the complete bandgap reference as well as the layout are presented in Chapter 5.

Finally in the conclusion the results of all chapters are summarized, and recommendations for future research are listed.

PTAT voltage generator

In an averaging bandgap reference circuit in SOI FinFET technology resistors have to be eliminated, because these are not easily realized in SOI FinFET technology (metal gates). Therefore, it is not possible to have resistor-based amplification of the PTAT signal. A solution for the PTAT side may be found in summing a number of small PTAT voltages instead of amplifying it to the required level. In this case the PTAT voltage can be completely independent of the rest of the circuitry.

2.1 Insensitivity to resistance variation

In conventional topologies, the PTAT voltage is generated on the CTAT side and then amplified. The resistor in the PTAT circuit can be replaced by separate PTAT voltage reference. It needs to be investigated what the error on the reference voltage due to mismatch will be. Both the conventional solution and the solution that uses a separate PTAT voltage reference are examined. The schematics of an averaging bandgap reference and of the circuit with resistor R_2 replaced by a (PTAT) voltage source are shown in figure 2.1

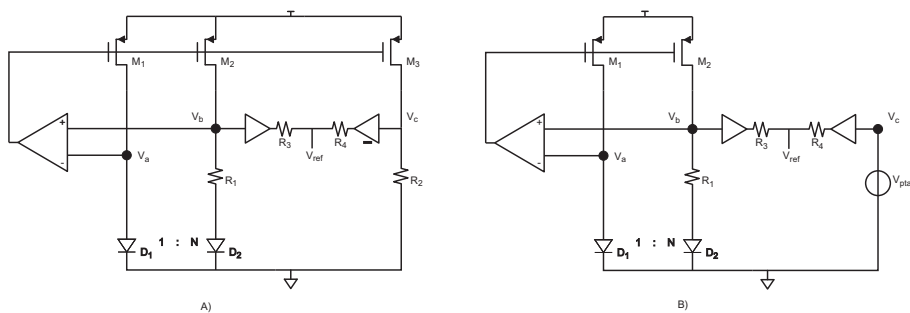


Figure 2.1: The schematic of an averaging bandgap reference: a) the conventional averaging bandgap reference circuit and b) the averaging bandgap circuit, with R_2 replaced by a (PTAT) voltage source

On-chip resistors substantially spread batch-to-batch and vary over temperature. Resistance variation gives an error in the current through the diodes.

$$I_{ptat} = \frac{\frac{K_b T}{q} \ln(n)}{R_1} \quad (2.1)$$

$$\Delta I_{ptat} = \frac{K_b T}{q} \ln(n) \frac{\Delta R_1}{R_1^2}$$

The total error on the reference voltage consists of the PTAT voltage error and the CTAT voltage error.

$$\Delta V_{ref} = \frac{1}{2}(\Delta V_{ctat} + \Delta V_{ptat}) \quad (2.2)$$

This equation is used in the next sections to calculate the batch-to-batch variation and the temperature variation.

2.1.1 Batch-to-batch variation

First the effect of batch-to-batch variation of the traditional averaging bandgap reference is examined. The influence of current error on the PTAT voltage is given by:

$$\frac{\partial V_{ptat}}{\partial I_{ptat}} = R_2 \quad (2.3)$$

The PTAT voltage changes due to a deviation in resistors R_1 and R_2 :

$$\Delta V_{ptat} = -\frac{K_b T}{q} \ln(nA) \frac{\Delta R_1}{R_1^2} R_2 + \frac{K_b T}{q} \ln(nA) \frac{\Delta R_2}{R_1} \quad (2.4)$$

When the resistors are matched it is seen that both contributions are equal.

$$\frac{\Delta R_1}{R_1} = \frac{\Delta R_2}{R_2} \rightarrow \frac{\Delta R_2}{R_1} = \frac{\Delta R_1}{R_1^2} R_2 \quad (2.5)$$

For the CTAT voltage error the following equation is derived:

$$\begin{aligned} \Delta V_{ctat} &= \frac{\partial \frac{K_b T}{q} \ln\left(\frac{I_c}{I_{c0}}\right) + V_{gap}}{\partial I} \Delta I \\ &= \frac{K_b T}{q} \frac{\Delta I}{I_c} \end{aligned} \quad (2.6)$$

The total error due to batch-to-batch variation is:

$$\Delta V_{ref} = \frac{1}{2} \left(\frac{K_b T}{q} \frac{\Delta I}{I_c} \right) \quad (2.7)$$

For the averaging bandgap reference with the PTAT source the same can be done. The influence of a current error on the PTAT voltage then is:

$$\frac{\partial V_{ptat}}{\partial I_{ptat}} = 0 \quad (2.8)$$

In the PTAT voltage source implementation, the PTAT voltage is not influenced by the current variation at all, because the current is not used on the PTAT side of the circuit. It is thus seen that batch-to-batch resistance variation has no influence on the PTAT voltage for both circuits.

The CTAT circuit of this bandgap reference is the same as in the traditional averaging bandgap reference circuit and therefore, also in the CTAT circuit the variation is the same.

2.1.2 Temperature variation

The negative temperature coefficient error due to variation in R_1 is:

$$\Delta V_{CTAT} = \frac{\partial V_{CTAT,error}}{\partial R_1} \frac{\partial R_1}{\partial T} \Delta T \quad (2.9)$$

With an approximation of the resistor including linear temperature dependencies:

$$R = R_0 + \alpha(T - T_0) \quad (2.10)$$

the temperature variation of the CTAT voltage is (derivation in appendix A.1):

$$\Delta V_{CTAT} = \frac{\partial V_{CTAT,error}}{\partial R_1} \frac{\partial R_1}{\partial T} \Delta T = -\frac{K_b T_0}{q} \alpha \Delta T \quad (2.11)$$

It is seen that the temperature dependence of the resistor influences the negative temperature coefficient. This change is linear with temperature and therefore in the design of the negative temperature coefficient it can be compensated. Note that this only holds when the temperature dependence of the resistor is (more or less) linear.

In the standard averaging bandgap reference circuit this is different, because there the resistors are matched and therefore the temperature variation in the resistors are canceled.

With the effects of batch-to-batch variation and temperature variation of resistors known, it can be concluded that in theory it is possible to replace one resistor by a PTAT voltage reference. What has to be taken into account is that the temperature coefficient of the CTAT voltage and the absolute CTAT voltage slightly changes.

2.2 Cascaded PTAT voltages

The PTAT voltage is generated by cascading a number of voltage followers with a build in offset voltage [7], see figure 2.2.

The cascaded voltage follower creates a PTAT voltage offset between the input and the output. This offset can be made by using an intentional "size mismatch" in the differential pair and/or a non-unity mirror gain to make an offset voltage. For this offset voltage to be PTAT the differential pair needs to have an exponential behavior. One stage gives an output voltage of:

$$I = I_0 \frac{W}{L} e^{\frac{qV}{K_b T}} \quad (2.12)$$

$$V_{out} = V_{in} + \frac{K_b T}{q} \ln(NK)$$

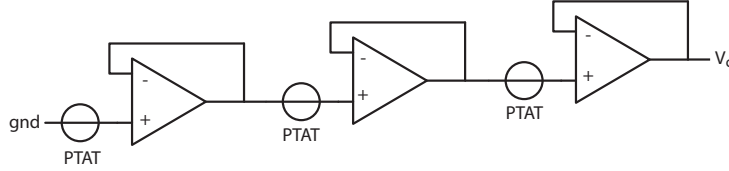


Figure 2.2: The cascading of the voltage followers

where N is the "size mismatch" in the differential pair and K the gain of the current mirror.

A possible implementation of the voltage follower is shown in figure 2.3.

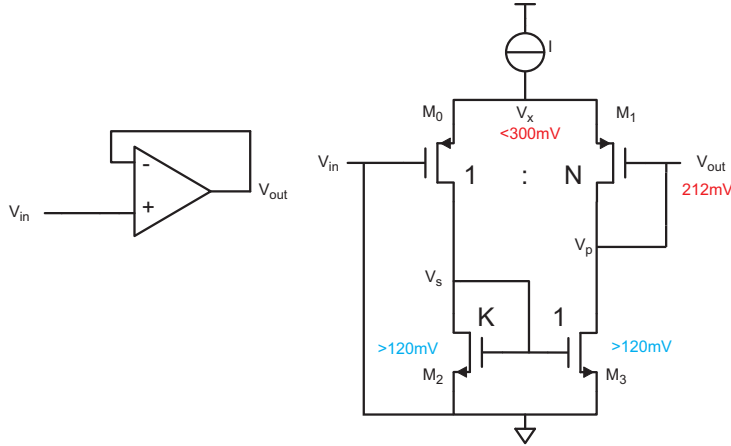


Figure 2.3: The PTAT voltage circuit with in blue the low temperature voltages and in red the high temperature voltages

Now some conditions for the voltage follower are given.

- The positive temperature coefficient needs to be equal to the negative temperature coefficient.

$$\begin{aligned}
 M \frac{K_b}{q} \ln(NK) &= \frac{\partial V_{CTAT}}{\partial T} \\
 &= \frac{V_{be} - 2.5 \frac{K_b T}{q} - E_g}{T} \\
 NK &= e^{\frac{\frac{\partial V_{CTAT}}{\partial T}}{\frac{K_b}{q} M}}
 \end{aligned} \tag{2.13}$$

In this equation M is the number of voltage follower stages and N is $\frac{L_1}{W_1} \frac{W_2}{L_2}$. W_1 , L_1 , W_2 and L_2 are the dimensions of the differential pair transistors.

- The differential pair needs to operate in subthreshold; therefore the gate source voltage of these transistors needs to be lower then the threshold voltage.

$$V_{gs,diff} < V_{thp} \tag{2.14}$$

- All transistors need to be in saturation: the drain source voltage of each transistor must be larger than approximately $3 \frac{K_b T}{q}$. This means that the output voltage swing is limited; the drain source voltage of the current mirror needs to be larger then $V_{ds,sat}$. Also the drain source voltage of the differential pair needs to be larger the $V_{ds,sat}$. Therefore the output voltage of a single stage, given in figure 2.3, must satisfy:

$$V_x - V_{ds,sat} > V_{out} > \frac{3K_b T}{q} \tag{2.15}$$

The proposed schematic of figure 2.3 has voltage headroom problems. When the the PTAT cascaded voltage followers are connected in stead of the resistor (see figure 2.1b), the input of the first stage will be ground. At low temperatures (-40^0C), the drain-source voltage of the current mirror needs to be larger than approximately $120mV$, to be in strong inversion (if the voltage is lower, the transfer of the current mirror has a large error). The drain of the current mirror is connected directly to the output, at low temperature the output voltage is therefore $\geq 120mV$. From this the minimum positive temperature coefficient can be calculated: $120mV/233K = 0.51mV/K$. At high temperature (140^0C) the output voltage will then minimally be $212mV$. At this temperature, the voltage node V_x must be smaller than the threshold voltage ($300mV$) (only for the first stage, because the input is ground). This means that the drain-source voltage of the right transistor of the differential pair will be smaller than $100mV$: it operates in triode (all voltages are shown in figure 2.3).

Also, since the input voltage is $0V$, the voltage on node V_x will be no higher than the threshold voltage. For the drain-source voltage of the input transistor to be high enough (so that it is not in triode) the current mirror transistor needs to be biased in the deep sub-threshold region. This is highly undesired because

it requires very large transistors for matching. Furthermore, any voltage error between the transistors will lead to a significant error in the transfer. Concluding, it can be stated that there is insufficient voltage headroom at the input side of the PTAT voltage source if the input of the first PTAT stage is ground.

Both problems can be solved by placing a voltage source at the input and between the output and the drain of M1. This is schematically shown in figure 2.4.

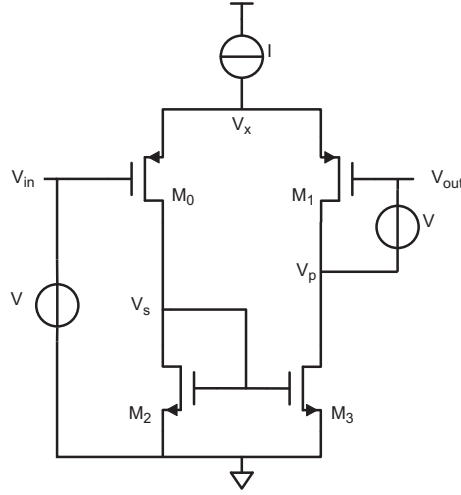


Figure 2.4: One PTAT voltage circuit with the added voltage sources

The voltage source at the output can be made by placing an additional n-FinFET. This FinFET has to be placed so that the threshold voltage is not added (no extra temperature coefficient in the already small voltage headroom). This is done by connecting the gate of the additional n-FinFET to the drain of M1, the output voltage is disconnected from V_p . Therefore, it has a smaller temperature coefficient. This is shown in figure 2.5. The voltage at the gate of the added transistor can be adjusted to an appropriate value (almost equal to the voltage at the gate of the current mirror).

The voltage headroom problem on the output side of the PTAT stage is solved; there is still the second headroom problem at the input side of the PTAT stage. For the circuit to work, the voltage at node V_x has to be larger than $V_s + V_{dssat}$ with the condition that V_s has to be larger than the threshold voltage. Because of this condition the voltage V_x has to be at least 0.5V at -40°C ($V_{thn}(-40) + V_{ds,sat}(-40)$). This means that the input voltage ($V_{in} = V_x - V_{thp}$) has to exceed 0.02V at -40°C . Also with this circuit, the input can not be connected to ground; a voltage source is needed. This voltage has to be subtracted later in the circuit; this circuit is described in section 2.3.

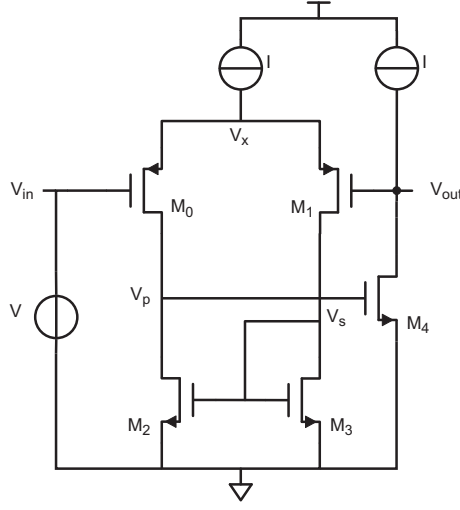


Figure 2.5: Implementation of the added voltage sources

2.2.1 Stability

Because of parasitic capacitances, a single PTAT stage may become instable. A simplified model of the circuit is shown in figure 2.6. It can be seen that there are two gm-C sections that each give 90 degrees of phase shift. Therefore the circuit is unstable or has little phase margin. This instability problem can be solved by placing a miller capacitor (large area consumption in CMOS). This is shown in the lower right part of figure 2.6. The first gm stage still has a phase shift of 90 degrees, but the second stage has not. The first pole is lowered and the second will move to a higher frequency [4].

The main principle of this pole splitting with miller compensation can be understood by assuming that the gain in the second stage is large.

The capacitance seen at node V_a is: $(1 + A_2)C_m$; due to the negative amplification, $(A+1)$ times the input voltage is on the capacitor C_m . This means that the current will be $(A+1)$ times that of $\frac{V}{j\omega C_m}$. This means the first pole will shift downward to:

$$\frac{1}{(C_1 + (1 + A_2)C_m)R_{out1}} \quad (2.16)$$

Except for very low frequencies this pole gives a 90° phase shift.

For the second pole also the assumption that the gain in the second stage is large is used. This means that all current flows through the miller capacitor: the capacitor from the first stage (C_1) can be neglected. By applying a voltage on the output it can be seen that the voltage on node V_a is equal to this output voltage. Therefore the output resistance is equal to $\frac{1}{gm_2}$

Therefore the second pole will move to:

$$\frac{C_{out}}{gm_2}$$

A solution to the instability problem is thus found by placing a capacitor over transistor M4.

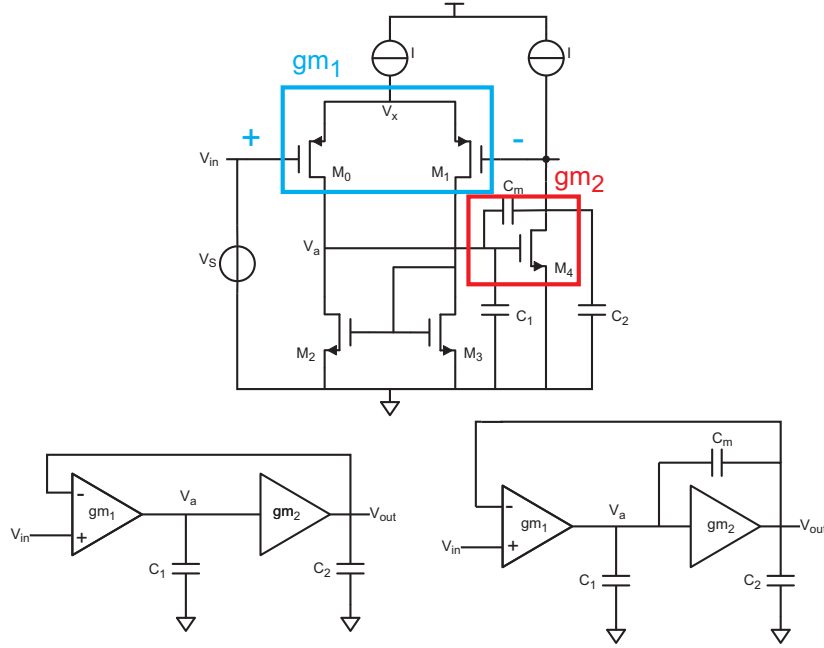


Figure 2.6: The unstable ptat voltage source. The upper shows the ptat voltage source circuit; lower left: an equivalent model lower right: solution with the miller feedback capacitor

For this solution of the PTAT circuit, however, an other instability problem was found. The circuit is susceptible to (relaxation) oscillations due to channel charge re-location. For normal operation an equation for the output voltage can be derived from the small signal equivalent circuit (see appendix A.3):

$$v_{out} = -v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \frac{(k+1)}{j\omega C} \quad (2.17)$$

It can be seen that for normal operation the PTAT voltage source is stable (a rising input voltage causes the output voltage to decrease). On the other hand when charge relocation is taken into account the voltage source becomes unstable.

When the output voltage becomes lower, the gate-source voltage of M_1 will reach the threshold voltage. At this point in time the channel charge is accumulated and a positive current is flowing into the device. This effect can be modeled as a current source with the sign opposite to the ordinary small signal equivalent. (when the voltage on the gate decreases the current flowing from the discharging of the channel increases). So when the channel discharging effect becomes larger then the normal current the effective gm changes sign. Therefore the output voltage equation changes to:

$$v_{out} = v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \frac{(k+1)}{j\omega C} \quad (2.18)$$

This behavior results in a positive feedback mechanism: it behaves as a relaxation oscillator. A solution to this problem is found by making two paths

from the sub-threshold FinFET to the output. This is done with additional current mirrors which copy the currents of the differential pair directly to the output. Therefore the PTAT stage contains just one (effective) gm stage with a capacitive load. All intermediate stages in the circuit have no gain and have their poles at a high frequency. This means that there is little phase-shift in the intermediate stages and the total gain of the circuit is lower (more stable). The final PTAT voltage circuit is shown in figure 5.17.

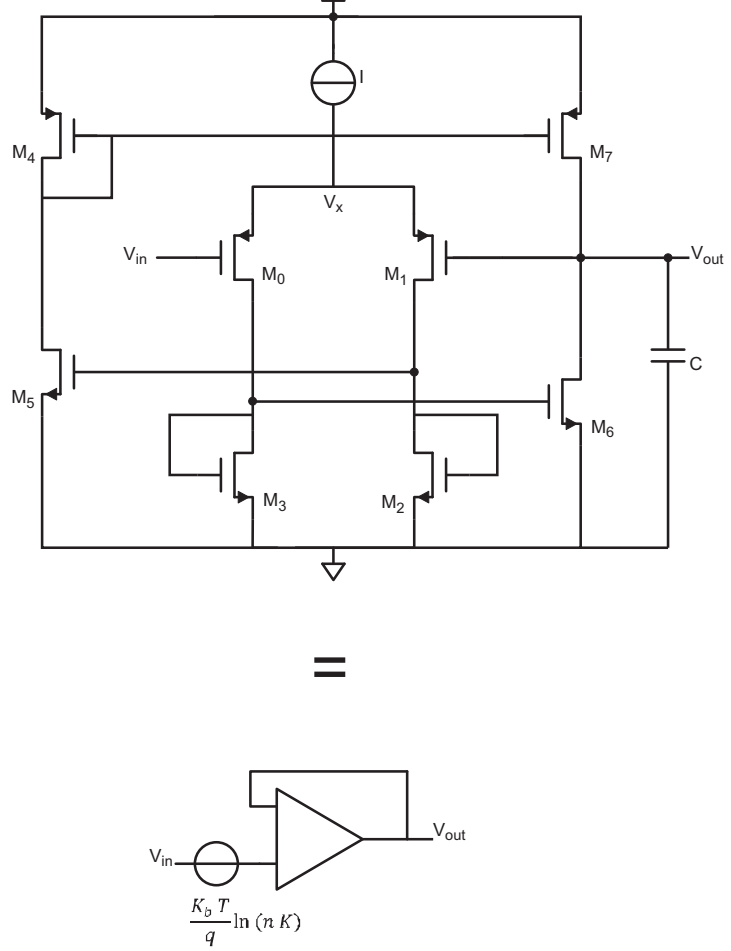


Figure 2.7: The final design of the PTAT voltage circuit

In this circuit the "size mismatch" of the differential pair is realized by choosing the width of M_1 N times larger than M_0 and the non-unity mirror gain will be made by choosing the width of M_3 k times M_2 .

2.3 Add and subtract circuit

The input of the first stage of the PTAT voltage source cannot be connected to ground. Therefore a voltage has to be added and later in the circuit subtracted. The input voltage must have the following limitations:

$$0.08V < V_{add} < 0.4V \quad (2.19)$$

The lower limit is the voltage that is needed to have enough voltage headroom in the input branch of the PTAT voltage circuit. The higher limit comes from the voltage at node V_x ; this needs to be lower than approximately 0.9V to have enough voltage room for the current source. Therefore it has to be investigated what the temperature coefficient of the added voltage can be and after how many stages the voltage is subtracted. Another important issue is that the added and the subtracted value have to be equal (a small difference will introduce an error in the reference voltage).

The voltage at the input of the first PTAT voltage stage can either have a positive or a negative temperature coefficient or it can be temperature independent. It is undesirable to have a positive temperature coefficient voltage source referenced to the supply voltage, because then the circuit will be dependent on the supply. Referring it to ground is difficult, because this voltage can not easily be connected to the gate (source voltage constant) of a n-FinFET (then the current will increase too much for high temperatures). When a negative temperature dependent voltage source is added, the output voltage of the second stage will be too high at low temperature. The added voltage must then be subtracted after the first stage. When this is done the input voltage of the second stage will be too low at low temperatures.

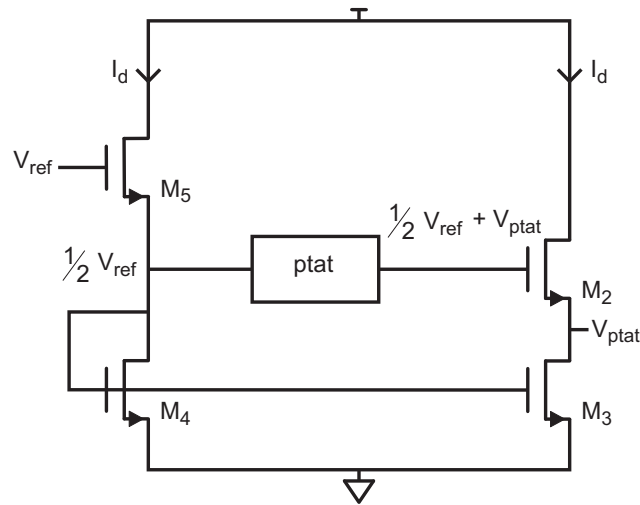
A solution to this problem is to use a temperature independent voltage source. A temperature independent voltage can be made by using the reference (output) voltage. Connecting the reference voltage directly to the input is not possible, this voltage is too high ($0.08V < V_{add} < 0.4V$); the voltage at node V_x needs to be lower than approximately 0.9V. Therefore the reference voltage is divided by two.

By using part of the reference voltage to bias the PTAT circuit a feedback loop is made. Therefore it has to be checked whether the circuit will start up. The lower limit of the PTAT voltage is 0.08V; the worst case reference voltage has to be higher than this voltage. The worst case is when the PTAT output voltage is still zero and the CTAT voltage will be (at low temperature) 0.37V; the reference voltage is then half of this ($V_{ref} = 0.5(V_{PTAT} + V_{CTAT})$) and the input to the PTAT voltage is half the reference voltage ($V_{in,PTAT} = 0.5V_{ref} = 0.09V$). This means that the reference voltage will be higher than the required input voltage of the PTAT; the PTAT will start-up. The reference voltage can thus be used as an input voltage of the PTAT circuit.

Next the subtract circuit has to be placed. Therefore the number of PTAT stages need to be known. A PTAT circuit with only one stage is not possible, because a voltage has to be added to the input; the output voltage will then be above the supply voltage. A PTAT voltage with two stages is also not possible; when the input voltage is subtracted after the first stage this voltage is too low

A PTAT voltage circuit with three and four stages are feasible to make. More than five stages is not usefull; it only increases power consumption and device sizes (mismatch).

The implementation of the add subtract circuit is shown in figure 2.8. The voltage divider is implemented (of the reference voltage) by cascoding two equal FinFETs (M4 and M5). These transistors are designed in such a way that they carry a certain current that is within reasonable bounds over temperature. This current is then copied with M3 to the second branch. If all transistors are chosen equal ($V_{gs,5} = V_{gs,4} = V_{gs,3} = V_{gs,2} = 1/2V_{ref}$) the currents through both branches is the same. This way, the gate of M2 has a voltage of $\frac{1}{2}V_{ref} + V_{PTAT}$. At the source of M2 the voltage is the PTAT voltage. The voltages in the add subtract circuit are shown in table 2.1.



Due to the large threshold variation over temperature, all FinFETs will be in subthreshold at low temperature and in strong inversion at high temperature (see table below). For M3, this gives the condition that when the FinFET is in strong inversion, the drain voltage should exceed $3 \frac{K_b T}{q}$. Therefore the input voltage can only be subtracted when this condition is met.

	-40 degrees	140 degrees
V_{ref}	0.6V	0.6V
V_{gs5}	0.3V	0.3V
V_{thn}	0.45V	0.28V
$\frac{3K_bT}{q}$	60mV	107mV

Table 2.1: Voltages in the add and subtract circuit

2.4 Design of a single stage

In the previous sections some design criteria of a single PTAT section and the add/subtract circuit are derived. Attention can now be paid to optimize the design of one PTAT stage. The circuit is optimized to low power consumption and a small area. This can be done using noise calculations and mismatch calculations.

2.4.1 Mismatch

Device mismatch can be modeled by a threshold voltage mismatch. This is shown in equation 2.20:

$$\sigma_{Vth} = \frac{A_{Vth}}{\sqrt{WL}} \quad (2.20)$$

The mismatch (referred to the output) of the differential pair ($\sigma_{Vth,out,d}$) and the current mirror ($\sigma_{Vth,out,c}$) is:

$$\sigma_{Vth,out}^2 = \sigma_{Vth,out,c}^2 + \sigma_{Vth,out,d}^2 \quad (2.21)$$

The output voltage mismatch due to device mismatch in the differential pair is:

$$\sigma_{Vth,out,d} = \sqrt{\left(\frac{A_{Vth}}{\sqrt{W_0L_0}}\right)^2 + \left(\frac{A_{Vth}}{\sqrt{W_1L_1}}\right)^2} \quad (2.22)$$

Note that the current density in M0 must be N times larger then in M1. This is done by taking W1 $\sqrt{N}$ times W0 and L0 $\sqrt{N}$ times L1. This way the current density ratio is n, but both devices have an equal contribution to the mismatch (equal areas). The total output voltage mismatch due to device mismatch in the differential pair is then:

$$\sigma_{Vth,out,d} = \sqrt{2} \left(\frac{A_{Vth}}{\sqrt{W_0L_0}} \right)^2 \quad (2.23)$$

Using a small signal equivalent circuit, the output referred voltage due to device mismatch in the current mirror is calculated. This is shown for M3 in figure 2.9.

From the figure an expression for the mismatch on one side of the current mirror is given:

$$\sigma_{Vth,out,c} = -\frac{gm_0 + gm_1}{gm_0gm_1} \frac{gm_3gm_2}{gm_2 + gm_3} \sigma_{Vth} \quad (2.24)$$

For the other side the mismatch transfer is the same. Note that the current ratio in the branches differs, there is a device ratio in the current mirror (k).

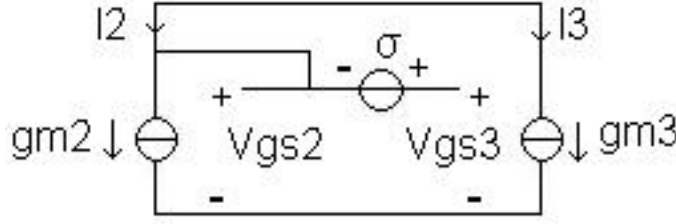


Figure 2.9: Small signal circuit of the effect of mismatch on one side of the current mirror

Therefore, the total expression of the (referred to output) mismatch of the current mirror is:

$$\sigma_{V_{th,out},c} = \sqrt{\left(\frac{1}{k} + 1\right)} \frac{gm_0 + gm_1}{gm_0 gm_1} \frac{gm_3 gm_2}{gm_2 + gm_3} \sigma_{V_{th}} \quad (2.25)$$

Note that $gm_2 = \sqrt{k} gm_3$ and $gm_0 = k gm_1$ (subthreshold). Rewriting this (see appendix A.4.1) so that it can be expressed with area gives:

$$\sigma_{V_{th,out},c} = \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{\sqrt{2}}{40} \frac{A_{V_{th}}}{V_{gt} \sqrt{W_3 L_3}} \quad (2.26)$$

Summing individual contributions:

$$\begin{aligned} \sigma_{V_{th,out}}^2 &= \sigma_{V_{th,out},c}^2 + \sigma_{V_{th,out},d}^2 \\ &= \left(\frac{k+1}{k}\right) \frac{(1+k)^2}{(1+\sqrt{k})^2} \frac{1}{k} \frac{2}{40^2} \frac{A_{V_{th}}^2}{V_{gt}^2 W_3 L_3} + \sqrt{2} \frac{A_{V_{th}}^2}{W_0 L_0} \end{aligned} \quad (2.27)$$

Since there are M PTAT stages cascaded, the total variance of the PTAT voltage is M times the mismatch error shown in equation 2.27. It can be seen that when the number of sections (M) is smaller the $\sigma_{V_{th,out}}$ per section can be higher and still have the same total mismatch. This means that the size of the FinFETs can be chosen smaller (taking into account that the width and length proportion as well as the minimum possible width and length have to be taken into account). So for the area it is better to take less sections (taking into account that you still have to make $M \ln(nk) = 0.6V$).

Rewriting equation 2.27 gives the total required (active) area of one PTAT voltage stage as a function of k (the device ratio in the current mirror). Optimizing for k and n yields:

$$A_{tot} = \frac{\sqrt{2} A_{V_{th}}^2}{\left(\sigma_{V_{th,out}}^2 - \left(\frac{k+1}{k}\right) \frac{k^2+2k+1}{k+2\sqrt{k}+1} \frac{1}{k} \frac{2}{40^2 V_{gt}^2} \frac{A_{V_{th}}^2}{A_3}\right)} + A_3 \quad (2.28)$$

The required area should be minimized; the derivation is found in appendix A.4.1.

The following optimum is found:

$$k = 1.803442406$$

$$N = 112.5625079$$

For a given output voltage mismatch, the required size (area) of all transistors is known. The aspect ratio of the transistors (W/L) is determined by noise calculations. Figure 2.10 shows the required area as a function of the tolerated mismatch. It is seen that when a larger sigma is allowed then the total area will decrease drastically.

For the required area it has to be taken into account that in this plot the

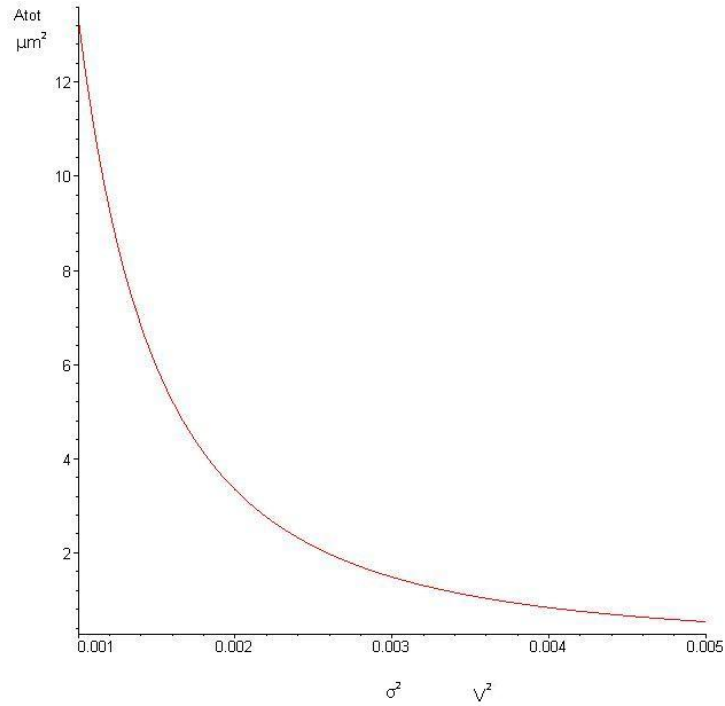


Figure 2.10: Total required area of one section versus the output voltage mismatch of the PTAT stage

mismatch versus area of one PTAT stage is plotted.

2.4.2 Noise

The noise generated by the PTAT voltage circuit is calculated, by summing individual noise contributions of each FinFET. The total noise in one section of the PTAT voltage is shown in equation 2.29 (see appendix A.5.):

$$\begin{aligned} V_{noise,tot}^2 &= V_{noise,m0}^2 + V_{noise,m1}^2 + V_{noise,m2}^2 + V_{noise,m3}^2 \\ &= \left(\frac{I_{noise,m0}}{gm_0} \right)^2 + \left(\frac{I_{noise,m1}}{gm_1} \right)^2 + \left(\frac{I_{noise,m2}}{kgm_1} \right)^2 + \left(\frac{I_{noise,m3}}{gm_1} \right)^2 \end{aligned} \quad (2.29)$$

This equation holds for both the flicker noise and the thermal noise. Thermal noise is used to optimize the PTAT circuit.

The thermal noise density of a single (long channel device) is given:

$$I_{noise}^2 = \frac{8}{3} K_b T g m \quad (2.30)$$

The total thermal noise density is:

$$V_{noise,tot}^2 = \frac{8}{3} K_b T \left(\frac{gm_0}{gm_0^2} + \frac{gm_1}{gm_1^2} + \frac{gm_2}{k^2 gm_1^2} + \frac{gm_3}{gm_1^2} \right) \quad (2.31)$$

Rewriting:

$$V_{noise,tot}^2 = \frac{8}{3} K_b T \frac{1}{40I_3} \left(\frac{1}{K} + 1 \right) \left(1 + \frac{\sqrt{2k_n \frac{W_3}{L_3}}}{40\sqrt{I_3}} \right) \quad (2.32)$$

Integrating the noise density over a certain frequency range yields the effective noise. It is not known what the bandwidth is; it is assumed that this is 1 GHz. The standard deviation is thus expressed by the following equation:

$$\sigma_{vn}^2 = \int_0^{1GHz} V_{noise,tot}^2 df \quad (2.33)$$

Rewriting (2.33) yields an expression for the minimum I_3 as a function of the noise bandwidth:

$$I_3 = f \frac{8KT}{120\sigma^2} \left(\left(\frac{1}{K} + 1 \right) \left(1 + \frac{2}{40V_{gt3}} \right) \right) \quad (2.34)$$

Note that $I_2 = KI_3$.

2.4.3 Device dimensions

Now that the currents and k and N are known, the device dimensions (aspect ratios) can be calculated. Note that the differential pair is in sub-threshold and the current mirror in saturation (for the sub-threshold slope of a p-FinFET the simulated curves are curve fitted):

$$\begin{aligned} I_d &= \frac{W}{L} I_{d0} 10^{-10^{-at+b} \frac{qV_{gs}}{K_b T}} \\ &= k_n \frac{W}{L} (V_{gs} - V_{th})^2 \end{aligned} \quad (2.35)$$

where T is the temperature in degrees Celsius. For this the sub-threshold parameters a and b also need to be known; these are determined by measurements ($a = 1.7510^{-3}$ and $b = 1.14$ see appendix A.2).

2.5 Summary

The design criteria of this chapter are given in the schematic of the add subtract circuit with one PTAT voltage stage shown in figure 2.11.

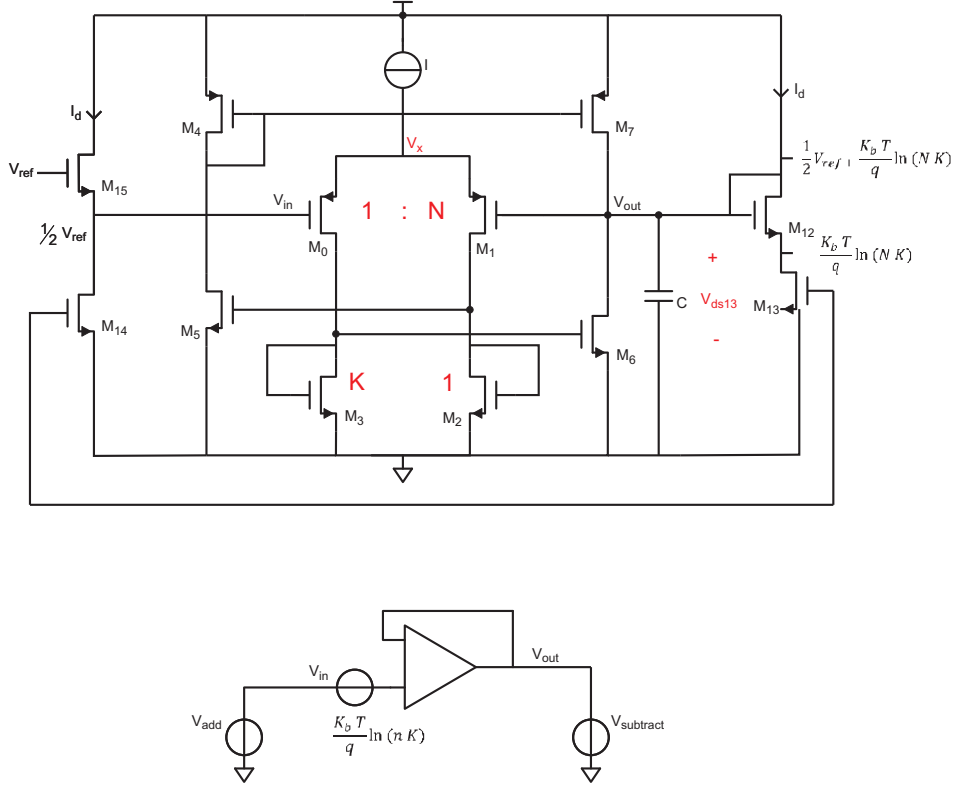


Figure 2.11: The schematic of a PTAT source with the add and subtract circuit (grey)

The PTAT voltage temperature coefficient is made by an intentional "size mismatch" in the differential pair and a non-unity mirror gain. The total offset voltage temperature coefficient must be equal to the negative temperature coefficient. Which is approximately -1.8mV/K (from measurements). For four stages the "size mismatch" in the differential pair and the non-unity mirror gain (see figure 5.17) can be calculated:

$$M \frac{K_b}{q} \ln(NK) = -NTC \quad (2.36)$$

$$NK = e^{\frac{-NTC}{M \frac{K_b}{q}}}$$

The differential pair must be biased in sub-threshold:

- $V_{gs,diff} < V_{th,p}$ (operate in sub-threshold)

Attention need to be paid to:

- $V_{gs,cm} > V_{th,n}$ (operate in strong inversion)
- $V_{ds,m0} \& V_{ds,m1} \& V_{ds,m3} > V_{ds,sat}$.
- $V_{ds,m13} > V_{ds,sat}$.

Chapter 3

The CTAT voltage generator

In the previous chapter the PTAT voltage circuit was designed. This chapter deals with the CTAT voltage circuit. The schematic of a conventional CTAT voltage generator is shown in figure 3.1.

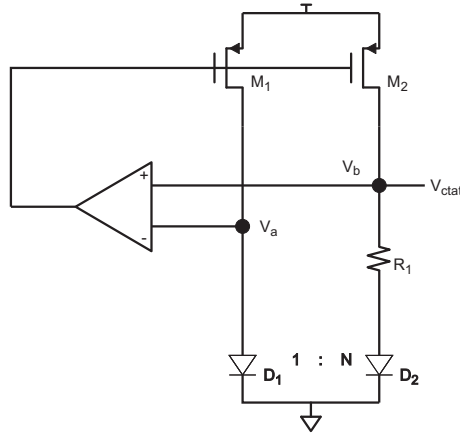


Figure 3.1: The schematic of the NTAT voltage generator

The CTAT voltage can be expressed as:

$$V_{ctat} = \frac{K_b T}{q} \ln\left(\frac{I}{I_{c0}}\right) + V_{gap} \quad (3.1)$$

with

$$I_{ptat} = \frac{\frac{K_b T}{q} \ln(n)}{R_1} \quad (3.2)$$

The temperature coefficient is:

$$\frac{\partial V_{be}}{\partial T} = \frac{V_{be} - (4 + m) \frac{K_b T}{q} - V_g}{T} \quad (3.3)$$

with $E_g = 1.12\text{eV}$ and $m = 1.5$

The target diode voltage is approximately 0.58V at 50 °C so the temperature

coefficient is approximately -1.85mV/K .

In the conventional CTAT circuit a resistor is used. In SOI FinFET technology the use of high ohmic resistors is not possible; these cannot be made accurately in a SOI FinFET process. Therefore this chapter describes a CTAT voltage circuit without resistors. This is done by replacing the resistor with a triode FinFET. For this replacement it is important to know the sensitivity to resistance variation of the CTAT voltage.

It was seen (in section 2.1) that a batch-to-batch resistance variation gives a change in the current through the diodes.

$$\Delta I_{ptat} = \frac{K_b T}{q} \ln(n) \frac{\Delta R_1}{R_1^2} \quad (3.4)$$

Taking this into account it is seen that the resistor can not vary too much (batch-to-batch and over temperature) because this will influence the CTAT voltage (the absolute value of the CTAT voltage changes with the natural logarithmic of this current).

3.1 Triode FinFET resistance

A resistance can be made by using the triode resistance of a FinFET. To use the triode resistance two conditions have to be met:

- The sensitivity to resistance variation of the CTAT voltage has to be low
- The drain source voltage has to be much smaller then the gate overdrive voltage

First the sensitivity to resistance variation of the CTAT voltage is examined. For this both the temperature variation and the batch-to-batch variation are taken into account.

For the batch-to-batch variaton the deviation in resistance causes the current through the diode to differ and therefore also the CTAT voltage differs from batch-to-batch. The output voltage is then:

$$V_{ctat} = V_d + \frac{K_b T}{q} \ln(n) \quad (3.5)$$

with:

$$V_d = \frac{K_b T}{q} \ln\left(\frac{\frac{K_b T}{q} \ln(n)}{I_{d0} R}\right) \quad (3.6)$$

The error due to batch-to-batch variation then is:

$$\begin{aligned} \Delta V_{ctat} &= \frac{\partial V_{ctat}}{\partial R} \Delta R \\ &= -\frac{K_b T}{q} \frac{\Delta R}{R} \end{aligned} \quad (3.7)$$

It is seen that the batch-to-batch error has the same effect on the CTAT voltage as temperature variation of the resistor itself. The batch-to-batch variation of a FinFET in triode is approximately 30%; this implies that the error voltage will be smaller than 1mV. Therefore, the triode-resistance can be used in the CTAT circuit.

Over temperature, it is seen that the resistance variation changes the current through the diode. The resulting voltage error is shown in equation 3.8:

$$V_{error} = \Delta I \frac{1}{gm_2} \quad (3.8)$$

with:

$$\begin{aligned} \Delta I &= \frac{\partial I_d}{\partial R} \Delta R \\ gm_2 &= I_d \frac{q}{K_b T} \\ I_d &= \frac{\frac{K_b T}{q} \ln(n)}{R} \end{aligned} \quad (3.9)$$

were n is the current ratio. Yields:

$$V_{error} = -\frac{K_b T}{q} \frac{\Delta R}{R} \quad (3.10)$$

When the resistance variation over temperature and the resistance value are known, the error voltage can be calculated.

The error due to the temperature variation is a lot larger, because also the threshold voltage changes over temperature.

$$I_d = \frac{\frac{K_b T}{q} \ln(n)}{R} \quad (3.11)$$

$$R_{on,x} = \frac{1}{2k \frac{W}{L} (V_{gs,x} - V_{th})}$$

This can be reduced by making a resistor by using the on-resistance of a n-FinFET and a p-FinFET in parallel (see figure 3.2). This results in a more constant resistance over a larger drain source voltage range.

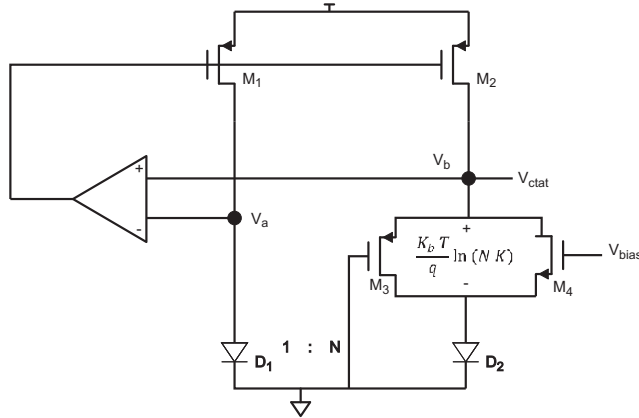


Figure 3.2: The replacement of the resistor by the on-resistance of a n-FinFET and a p-FinFET in parallel

To use the on-resistance of the p-FinFET and the n-FinFET the drain source value has to be much smaller than the gate overdrive voltage. The drain source voltage is rather small:

$$V_{ds} = V_{R1} = \frac{K_b T}{q} \ln(n) \approx 50mV \quad (3.12)$$

The absolute value at the ctat output voltage (V_{ctat}) is around 0.6V at room temperature. To have the p-FinFET in the triode region the gate voltage need to be low. This terminal can be connected to ground. The n-FinFET needs to be biased with a voltage higher than $V_{thn} + V_{ds} + V_s$. The worst case is approximately 0.9 V at low temperatures (the threshold voltage is highest). Connecting it to the supply is not an option because then the power supply rejection ratio (PSRR) will be low. When only a p-FinFET is used the resistance

will change too much over temperature. This means that a voltage reference circuit needs to be made with a voltage equal or larger than 0.9V.

The total on-resistance of the p-FinFET together with the n-FinFET is:

$$R_{tot} = \frac{1}{R_{on,n} + R_{on,p}} \quad (3.13)$$

with:

$$R_{on,x} = \frac{1}{2k \frac{W}{L} (V_{gs,x} - V_{th})} \quad (3.14)$$

The required total resistance can be calculated:

$$R = \frac{\frac{K_b T}{q} \ln(n)}{I} \quad (3.15)$$

For a near constant resistance the size ratio of the n-FinFET and the p-FinFET needs to be chosen correctly.

3.2 Triode resistor bias reference

Making a constant 0.9V reference voltage in a technology where the supply is 1V is difficult. In this work, the reference (output) voltage of the total circuit is multiplied by a factor 3/2 to get a stable voltage of 0.9V. This is done using multiple cascoded diode connected n-FinFETs (similar to the add/subtract circuit in the PTAT circuit, see section 2.3). The problem with this approach is that a current mirror has to be used above the cascoded FinFETs. This current mirror would then have only 0.1V drain source voltage; this is too low for high temperatures.

The implemented circuit uses an OPAMP is seen in figure 3.3. The OPAMP is used to adjust the current through the cascoded FinFETs. By using this OPAMP the previous described triode FinFET problem is eliminated (low drain source voltage on M_0). The positive input of the opamp will (almost) be equal to the negative one in a feedback situation, which means that the gate voltage of FinFET M_2 is equal to the reference voltage. By using a cascode of three equal diode connected n-FinFETs the voltage V_{SW} will be 0.9V. The transistors M_1 , M_2 and M_3 are equal and should be chosen in such a way that they carry a certain current that is within reasonable bounds over temperature.

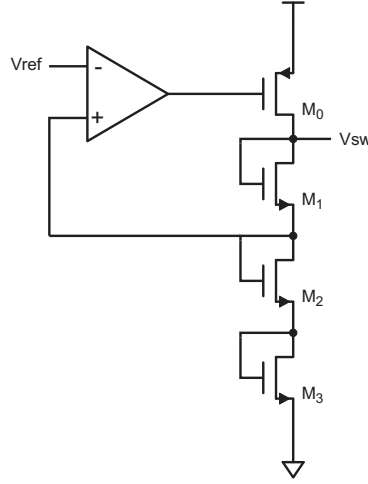


Figure 3.3: The 0.9V reference voltage circuit

Also the stability has to be verified, because the reference (output) voltage is used to make a 0.9V reference voltage that is used in the CTAT stage and therefore influences the reference voltage.

The loop gain is (the loop is cut at V_{ref} , with $V_{ref,i}$ the voltage on the node at the beginning of the loop and $V_{ref,o}$ at the end of the loop):

$$A_{loop} = \frac{\partial V_{ref,o}}{\partial V_{ctat}} \frac{\partial V_{ctat}}{\partial R_1} \frac{\partial R_1}{\partial V_{SW}} \frac{\partial V_{SW}}{\partial V_{ref,i}} \quad (3.16)$$

with

$$\begin{aligned}
\frac{\partial V_{ref,o}}{\partial V_{ctat}} &= \frac{1}{2} \\
\frac{\partial V_{ctat}}{\partial R_1} &= -\frac{K_b T}{q} \frac{1}{R_1} \\
\frac{\partial R_1}{\partial V_{SW}} &= R_1^2 k_n \frac{W_n}{L_n} \\
\frac{\partial V_{SW}}{\partial V_{ref,i}} &= \frac{3}{2}
\end{aligned} \tag{3.17}$$

Substituting this in equation 3.16:

$$\frac{1}{2} \frac{\partial V_{ctat}}{\partial R_1} \frac{\partial R_1}{\partial V_{ref}} = -\frac{3}{4} \frac{K_b T}{q} R_1 k_n \frac{W_n}{L_n} \tag{3.18}$$

Note that the gain of the 0.9V reference circuit multiplies the reference voltage with 3/2. The loop gain will be largest at high temperature; at low temperature the pFinFET dominates the total resistance. With $R_1 \approx 50\text{k}\Omega$ and $\frac{W_n}{L_n} \approx \frac{0.5}{9}$ this evaluates to a gain which is much smaller than 1 (0.013). This means that the circuit is stable.

A disadvantage of solving this problem with the OPAMP is limited bandwidth. For higher frequencies this circuit will not work properly; there will no longer be gain in the circuit (the circuit must be stable) which means the OPAMP no longer corrects errors in the output voltage. This lowers the PSSR performance at high frequencies. This can be a problem when on chip circuitry gives distortion, for example on the supply voltage.

3.3 Design of the OPAMP circuit

In the CTAT circuit as well as in the 0.9V reference voltage circuit an opamp is used. Before a design for the OPAMP in the CTAT circuit can be proposed the total required gain (in the OPAMP and the current mirrors) is evaluated. It is necessary to have a small difference between the two inputs of the opamp (V_{in}) because this leads to an error in the CTAT voltage. This is shown in equation 3.22 (see figure 3.4).

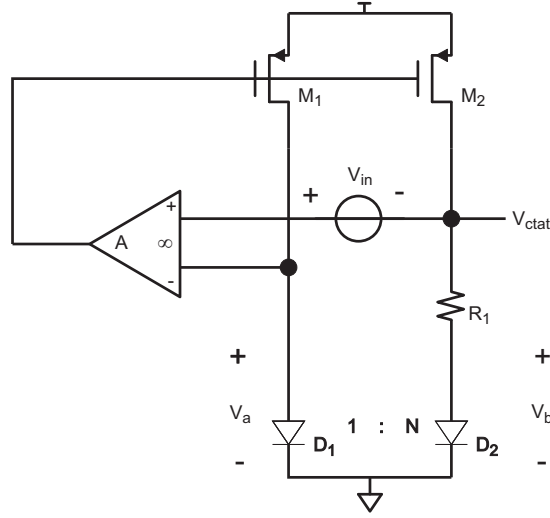


Figure 3.4: The ctat voltage circuit with opamp input voltage

$$V_{ctat} = V_b + IR_1 \quad (3.19)$$

with:

$$I = \frac{V_a - V_b - V_{in}}{R_1} \quad (3.20)$$

$$V_a - V_b = \frac{K_b T}{q} \ln(n)$$

Substituting:

$$\begin{aligned} V_{ctat} &= \frac{K_b T}{q} \ln\left(\frac{I}{I_{c0} n}\right) + \frac{\frac{K_b T}{q} \ln(n) - V_{in}}{R_1} \\ &= \frac{K_b T}{q} \ln\left(\frac{\frac{K_b T}{q} \ln(n) - V_{in}}{R_1 I_{c0}}\right) - V_{in} \end{aligned} \quad (3.21)$$

The error on the CTAT voltage due to the OPAMP input voltage is:

$$\begin{aligned} \frac{\partial V_{ctat}}{\partial V_{in}} &= -1 - \frac{K_b T}{q} \frac{R_1 I_{c0}}{\frac{K_b T}{q} \ln(n)} \frac{1}{R_1 I_{c0}} \\ &= -1 - \frac{1}{\ln(n)} \end{aligned} \quad (3.22)$$

With $n = 8$, the transfer of the OPAMP input voltage to the CTAT output is -1.48.

Note that the current mirror (in combination with the OPAMP) is designed in such a way that the input voltage of the OPAMP (with limited gain) is zero at a certain nominal temperature (T_0).

$$\begin{aligned} V_{in} &= \frac{\Delta I}{gm} \\ gm &= gm_1 A \\ \Delta I &= \frac{\frac{K_b T}{q} \ln(n)}{R} - \frac{\frac{K_b T_0}{q} \ln(n)}{R} \end{aligned} \quad (3.23)$$

ΔI is the current variation (PTAT) in the diodes of the CTAT circuit with respect to the current at temperature T_0 .

Yields:

$$gm_1 A = \frac{(T - T_0) \frac{k}{q} \ln(n)}{R V_{in}} \quad (3.24)$$

For $n = 8$, $I = 1\mu A$ ($R = \frac{kT \ln n}{I} \approx 52k\Omega$ at room temperature) the total gain must exceed 2.2 mS. The error in V_{ctat} is chosen smaller than 0.2mV ($V_{in} = 0.135mV$) so that the error is less than a tenth of a degree.

From the calculation can be seen that not a very large gain is required. This means that a single stage OPAMP is sufficient. The circuit of the OPAMP is shown in figure 3.5. In the circuit the current source will be made by a nFinFET biased by a reference voltage from the CTAT circuit. This configuration will require a start-up circuit, because the OPAMP will have a stable situation at ground.

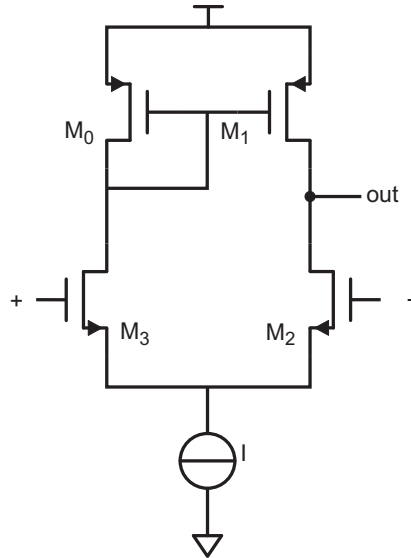


Figure 3.5: The circuit of the OPAMP

In the CTAT circuit and in the 0.9V reference circuit the same OPAMP can be used. The CTAT circuit has an (common mode level) input voltage dependent on temperature between approximately 0.4 and 0.7V. This is possible with the proposed OPAMP. Therefore the same OPAMP can be used in the 0.9V reference circuit; this common mode input level is equal to the reference voltage (approximately 0.6V).

3.4 CTAT diodes

Two diodes are used in the CTAT circuit. For matching it is better to make a square of all the diodes in layout. Therefore the diode ratio, n , should be 3, 8, 15 etc. When n is larger, a larger resistive value needs to be used for the same current. It can be seen that the voltage difference of the diodes scales with the natural logarithm of n therefore, a large n means more area is needed, but it does not decrease the resistor size by much. N is chosen 8.

Because there is no bulk diode in a SOI process the bulk diode can not be used. An idea is to use the sub-threshold slope of a FinFET instead of an actual diode, an other possibility is to use a gated PIN diode.

A disadvantage of using subthreshold FinFETs is that the gate source voltage needs to be lower then the threshold voltage (lower then 0.3V for a nFinFET at low temperature). The sub-threshold FinFET is diode connected so this means that the CTAT voltage will maximally be 0.3V (1 sub-threshold FinFET is used). This is a disadvantage because it is difficult to use in the averaging part of the circuit.

Therefore the diodes will be made by gated pin diodes.

3.4.1 Gated PIN diode

A PIN diode is a diode with a wide, lightly/ undoped intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. The gated pin diode can be simply made by using a FinFET (a FinFET has a PIP or NIN structure). The difference with the FinFET is that one drain/source is p-doped and the other is n-doped (shown in figure 3.6).

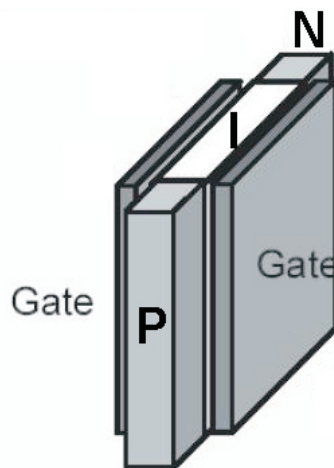


Figure 3.6: A FinFET as a gated PIN diode

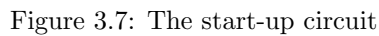
In the intrinsic region a depletion region with charge carriers from the "p" and "n" regions is formed. When the diode is forward biased the depletion region size decreases (electrons flow from the n area towards the p and holes visa versa).

In the design the gate of the gated PIN diode is floating. When the gate is grounded there can be leak currents that influence the diode characteristic on the other hand when the gate is connected to the anode the depletion region is influenced.

A measurement of Salsa 2 gated diode is shown in figure B.1 in appendix B.2.

In the figure the measured I-V curves are shown for different diode sizes. For all measurement the gate is floating.

The opamp in the CTAT section uses a current-source that is buffered from a voltage made in the CTAT circuit itself, it has to have a start-up circuit. The start-up circuit has to make sure that when the CTAT voltage is low, a current will flow through the diodes that increases the diode voltages so the opamp will work.


$$V_{gate,M3} = I_{M6} R_{triode,m6} \quad (3.25)$$

The total CTAT circuit is shown in figure 3.8.

Chapter 4

The buffer

The last part that needs to be designed are the output buffers. For these buffers it is important that they have a high input resistance, so that the isolation between the CTAT, the PTAT and the reference voltage is high. It is also important that the buffers are matched so that the CTAT and PTAT side are added and divided symmetrically. This is done using matched OTAs (operational transimpedance amplifier). These OTA's can be seen as a buffer in series with an output resistance (shown in figure 4.1 b.). The buffer makes sure that no current can flow into the CTAT or PTAT line; the CTAT and PTAT voltages are separated. The resistances should be matched so that the temperature dependence of the CTAT and PTAT are weighed correctly.

The reference voltage is expressed by the following equation:

$$V_{ref} = \frac{gm_{left}}{gm_{left} + gm_{right}} V_{ctat} + \frac{gm_{right}}{gm_{left} + gm_{right}} V_{ptat} \quad (4.1)$$

When two identical OTAs are used gm_{left} and gm_{right} are equal and hence the output voltage is about 0.6V (average of CTAT and PTAT).

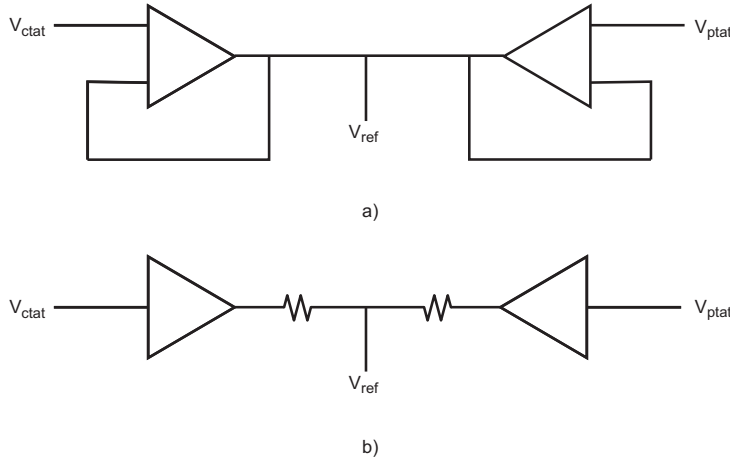


Figure 4.1: The circuit of the buffers

4.1 Solution exploration

For the design of the buffers it is important to know if the realization with the differential pair can handle voltage differences between the CTAT and the PTAT voltage.

The voltages of the PTAT and the CTAT are around 0.6V at 50 °C. With a temperature coefficient of approximately 1.8mV/K, at a temperature of 140 degrees, the CTAT voltage is approximately 0.42V and the PTAT voltage is 0.76V. The threshold voltage for a n-FinFET is approximately 0.25V at this temperature. At -40 °C the CTAT and PTAT values are reversed; the PTAT voltage is approximately 0.42V and the CTAT voltage is 0.76V. The threshold voltage is then approximately 0.35V. With the circuit in figure 4.1, two problems can be identified:

- Because of large voltage differences over the inputs of the differential pairs (at low and high temperatures), the current ratios in the differential pair will be high. This will give a large error on the reference voltage, because the current can flow from one OTA to the other.
- At low and high temperatures the drain-source voltage on the current sources in the two buffers will be different. Because the CTAT voltage is small and the threshold voltage is high the current source of the CTAT buffer will be in triode while the PTAT current source will still work properly. Therefore the buffers are not matched.

The current ratios in the differential pair can be described. When two OTAs are connected together the current can flow from one OTA to the other. This is schematically shown in figure 4.2.

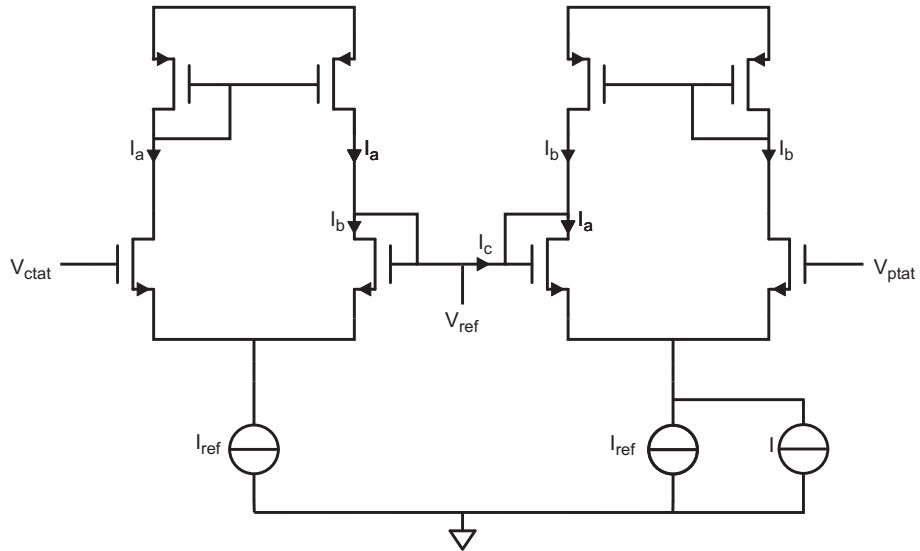


Figure 4.2: The circuit of the buffer with the different currents

What is known is that the current I_{ref} is equal to the sum of the currents in the differential pair.

$$I_{ref} = I_a + I_b$$

The current that flows from one OTA to the other is:

$$I_c = I_b - I_a$$

First, the error on the reference voltage due to a variation in the tail current (I_{ref}) of one stage is derived by using the small-signal equivalent circuit (see appendix C.1):

$$\frac{V_{ref}}{dI} = \frac{1}{2} \frac{gm_0 + gm_1}{gm_0 gm_1} \quad (4.2)$$

This is the output resistance of one buffer section. One buffer can thus be represented by the resistance which loads the other buffer.

The currents in the differential pair are a ratio of the current source (I_{ref}):

$$\begin{aligned} I_a &= (1 - \alpha)I_{ref} \\ I_b &= \alpha I_{ref} \end{aligned} \quad (4.3)$$

When α is equal to half, both branches carry equal currents. The limits are α is zero (all current is in I_a) or α is one (all current is in I_b).

For the error on the reference voltage, it is seen that when α is equal to a half (the differential pair is in balance) there is no error at the output. When most current is in one branch ($\lim_{\alpha \rightarrow 0}$ and $\lim_{\alpha \rightarrow 1}$) the error becomes very large. This gives:

$$\begin{aligned} \frac{V_{ref}}{dI} &= \frac{\sqrt{\alpha I_{ref}} - \sqrt{(1 - \alpha)I_{ref}}}{4\sqrt{2k_n}\sqrt{\alpha I_{ref}}\sqrt{(1 - \alpha)I_{ref}}} \\ &= \frac{1}{\sqrt{2k_n I_{ref}}} \frac{1 - \sqrt{\frac{1}{\alpha} - 1}}{4\sqrt{(1 - \alpha)}} \end{aligned} \quad (4.4)$$

The previous given problems have a contradiction; in the proposed schematic the drain-source voltage of the current source should be low. This way, there is more voltage headroom for the differential pair (which means the current ratio I_a/I_b is low). On the other hand, when the drain-source voltage of the current source is low, the current mirrors will not match very well. In practice, there is no suitable operating condition that yields small errors. This problem can be solved by decreasing the voltage step on the input of the buffer by using more buffer stages in series.

4.2 Buffer in series

Placing two OTAs in series yields a circuit with a buffer between each resistor (see figure 4.3a). Because of this, no current can flow through R_1 and R_4 and therefore the voltage after the first OTA stage is equal to the voltage before R_1 and therefore, this still works as a buffer with only one OTA stage.

To solve this a current path must be created. This is done by placing an OTA in a feedback loop (see figure 4.4). The reference voltage is then expressed by the following equation:

$$V_{ref} = \frac{R_1 R_2}{R_1 + R_2 + R_3 + R_4} V_{ctat} + \frac{R_3 R_4}{R_1 + R_2 + R_3 + R_4} V_{ptat} \quad (4.5)$$

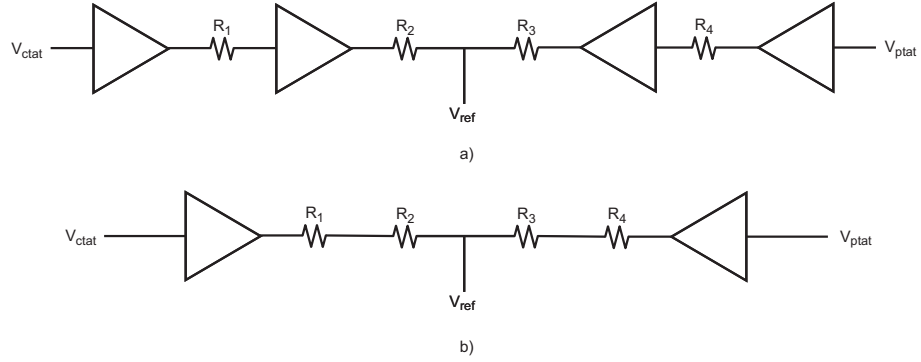


Figure 4.3: The simplification of the final buffer implementation: upper the series connected OTAs, lower the wanted configuration

The final block schematic of the buffer with two stages of OTAs is seen in figure 4.4.

In this setup, the voltage difference on the inputs of the OTA's is halved ($\frac{1}{2}(V_{ptat} - V_{ref})$). Therefore the current ratio in the buffer will be smaller and also the error to the reference voltage will be smaller.

When the CTAT voltage is small and the threshold voltage is high (at low temperatures) the current source of the CTAT outer buffer will be in triode while the PTAT current source operates in saturation. Therefore the outer buffers are not matched very well. For the inner buffers this problem is less significant, because the (common mode) voltage range on the inputs of the differential pair will be smaller; the current sources will always be in saturation. It is difficult to make the currents of the current sources in the outer buffers equal. A solution is making the drain source voltage of the current sources equal. By doing this, it is not relevant whether the drain-source voltage is very; it is only important that they are matched.

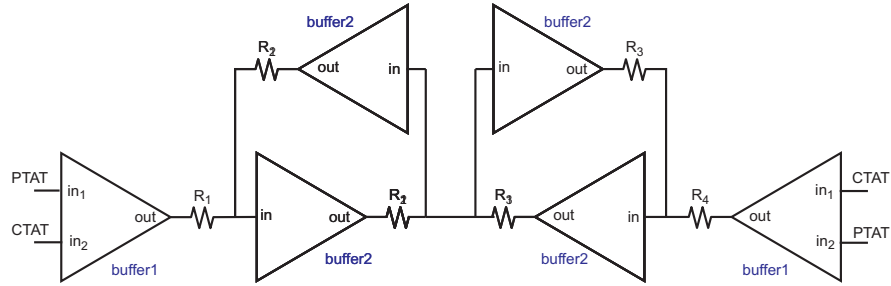


Figure 4.4: The block circuit of the final buffer implementation

4.3 Buffer implementation

The drain source voltages of the current sources are made equal by adding an additional differential pair. In this solution it is important that the extra differential pair matches the differential pair to the other ones. This holds for

the dimensions as well as the gate voltages. In figure 5.5 the implementation with the extra differential pair is shown.

In the figure, the gates of the differential pairs are connected as should be on the outer buffer on the PTAT side.

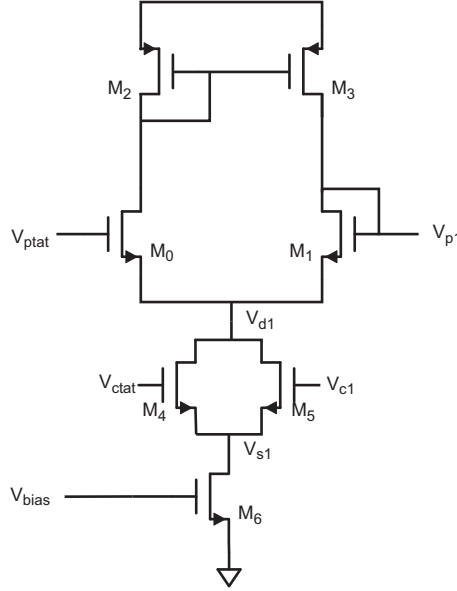


Figure 4.5: The new circuit of the buffers

When the temperature is 50°C the CTAT, the PTAT and the reference voltage are all 0.6V . In this case the top differential pairs of the outer buffers are in strong inversion. The lower differential pairs will be in triode (the drain source voltage is lower than the overdrive voltage); for this situation the nodes V_d and the V_{s1} voltages are almost equal.

When the voltage at the input(PTAT) of the buffer is lowered (low temperature) also the voltage at node V_s will be lower. In this case the CTAT voltage will be high. The FinFETs of the lower differential pair is in triode and V_d will become almost equal to V_{s1} (it will follow the voltage of V_d).

On the other hand, when the PTAT the voltage increases (high temperature), the voltage at node V_{s1} will be higher. Since the FinFET of the lower differential pair is connected to the opposite temperature coefficient (the CTAT voltage will decrease) the lower differential pair will go in saturation. Because this differential pair is equal to the other buffer, the voltage V_s will be equal to the voltage of V_d of the other buffer. Since V_d and V_s will be almost equal (on the CTAT side) both current sources have nearly the same drain-source voltage.

As was already shown in equation 5.3, the mismatch in the current source will influence the reference voltage. The mismatch is therefore used to determine transistor sizes in the buffer. To determine the total output referred

mismatch, the mismatch of the separate components are summed. The equation for the reference voltage variation due to a current variation in I_{ref} is:

$$\frac{V_{ref}}{dI} = \frac{1}{\sqrt{2k_n I_{ref}}} \frac{1 - \sqrt{\frac{1}{\alpha} - 1}}{4\sqrt{(1 - \alpha)}} \quad (4.6)$$

To calculate the mismatch for each component the current variation due to it's error has to be determined (see appendix C.1). For the current mirror this is:

$$\sigma_{currentmirror} = \frac{gm_0 + gm_1}{4gm_0gm_1} \frac{1}{\sqrt{2k_n I_{ref}}} \frac{1 - \sqrt{\frac{1}{\alpha} - 1}}{4\sqrt{(1 - \alpha)}} \frac{A_{vth}}{\sqrt{W_3 L_3}} \quad (4.7)$$

For the differential pair this is:

$$\sigma_{differentialpair} = \sqrt{2} \frac{A_{vth}}{\sqrt{W_0 L_0}} \quad (4.8)$$

4.4 Summary

The circuit of one side of the buffer is given in figure 4.6.

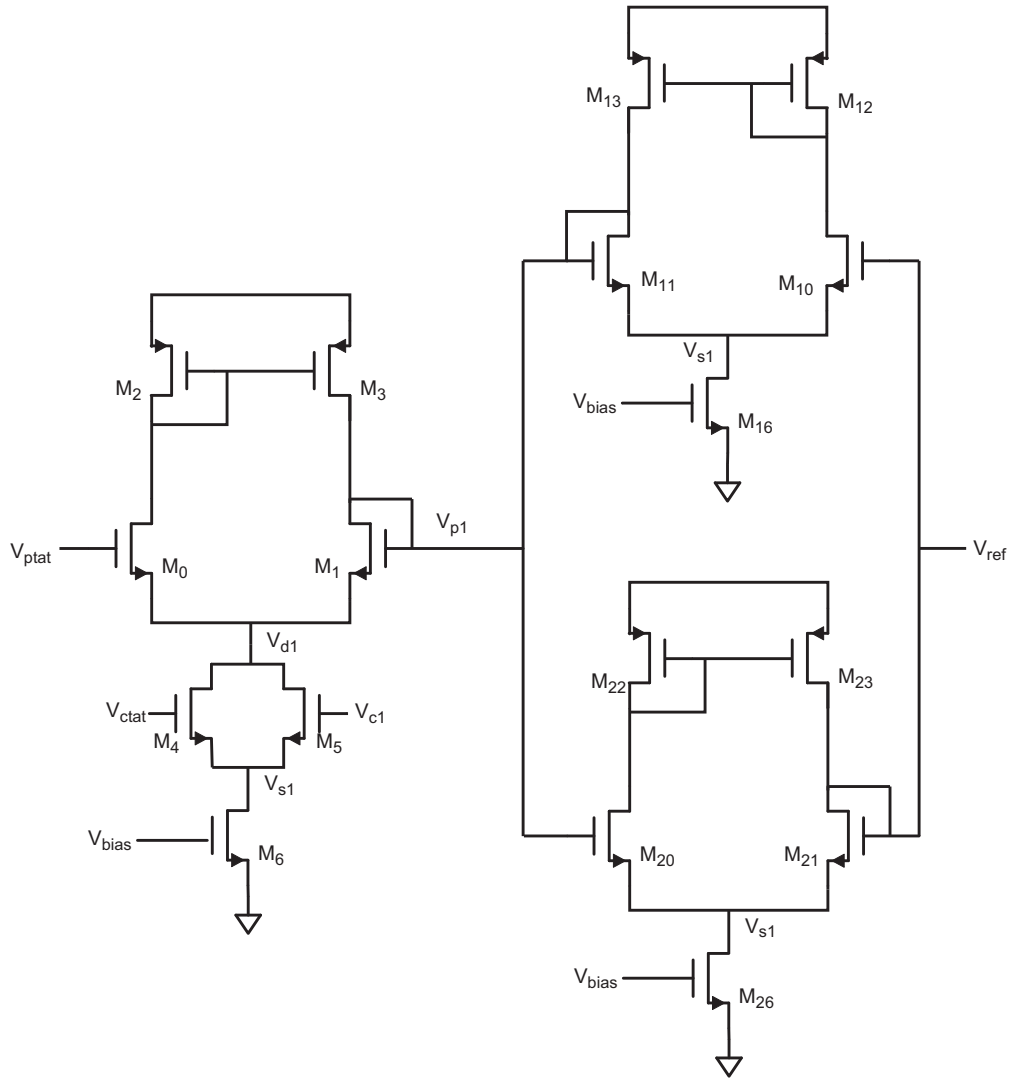


Figure 4.6: The circuit of one side of the buffer

Chapter 5

Simulations of the complete bandgap reference

Simulation are done on the total bandgap reference; to verify if the designed resistorless bandgap reference meets the targets. The following simulations were done:

- 5.1 Temperature sweep
 - The total bandgap reference
 - The PTAT voltage circuit
 - The buffer circuit
- 5.2 Stability analysis (applying steps on different nodes)
- 5.3 Power Supply Rejection Ratio
- 5.4 Mismatch

The targets are shown in section 1.5.

5.1 Temperature sweep

Measurements on gated diodes are done to verify what temperature coefficient a diode has (see figure B.2) in appendix B.2.

The actual diode voltage is approximately 0.58V at 50 °C so the temperature coefficient is approximately -1.85mV/K.

The negative temperature coefficient can be calculated with:

$$\frac{\partial V_{be}}{\partial T} = \frac{V_{be} - (4 + m) \frac{K_b T}{q} - V_g}{T} \quad (5.1)$$

with $E_g = 1.12\text{eV}$ and $m = 1.5$

This equation gives the correct temperature coefficient. The positive temperature coefficient must have the opposite temperature coefficient.

It is seen from a transient temperature sweep that the designed bandgap reference has an almost constant output voltage (Vref) as a function of temperature. When taking a closer look it is seen that the reference voltage still has a small slope (figure 5.1). This can be derived from the fact that there are no good diode models in the FinFET library.

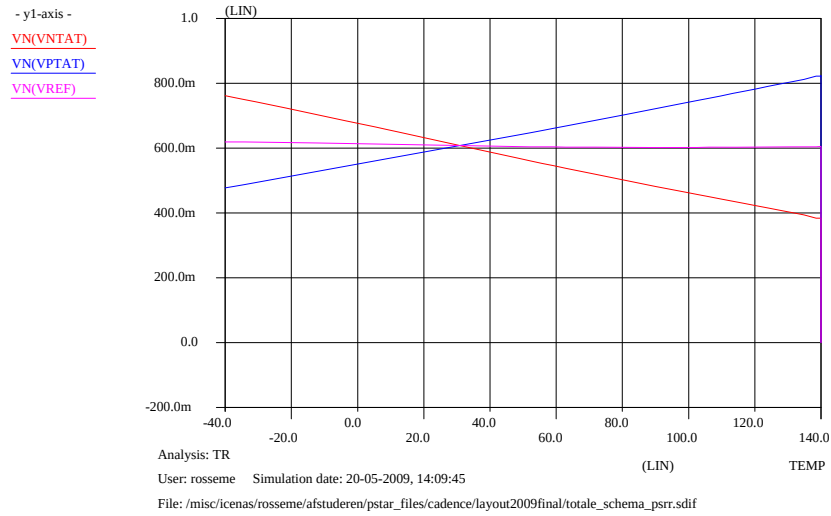


Figure 5.1: The result of the CTAT voltage, PTAT voltage and reference voltage sweep over temperature

In the simulation it is seen that the negative temperature coefficient is larger, approximately -2mV/K, while the positive temperature coefficient is approximately 1.85mV/K.

The total PTAT circuit appears to be working properly. Another simulation is done to verify if all PTAT stages as well as the add and subtract circuit are working properly.

5.1.1 PTAT

In the design four stages are used to generate a PTAT voltage there is also an add and subtract circuit. Shown in figure 5.2.

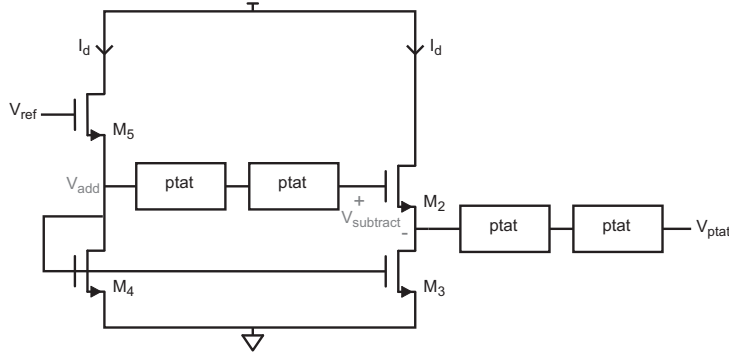


Figure 5.2: The PTAT voltage stages and the add subtract circuit with the plotted voltages

In figure 5.3 the output voltage of the different stages are plotted.

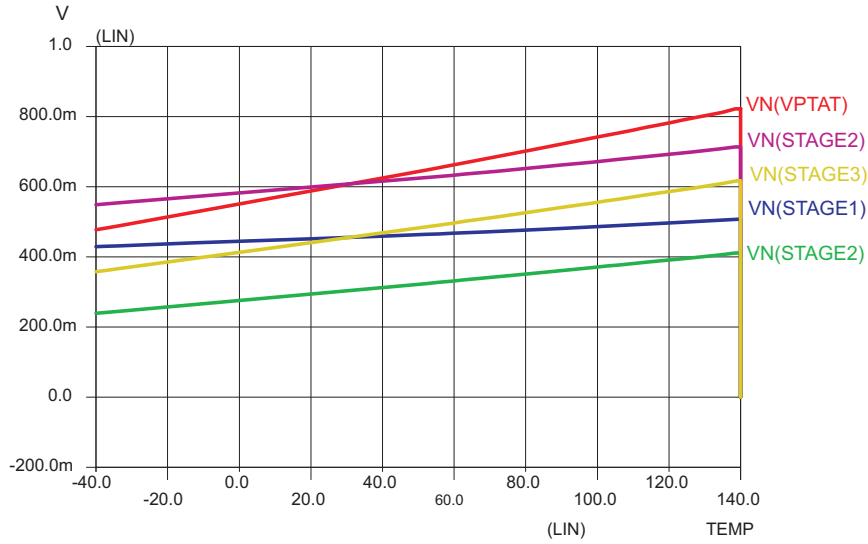


Figure 5.3: The result the different PTAT stages

The simulated and the expected temperature coefficients of the different stages are shown in table 5.1.

Therefore can be concluded that all PTAT stages work correctly.

	Temp Coeff simulated (mV/K)	Temp Coeff expected (mV/K)
stage1	0.444	0.462
stage2	0.890	0.924
stage3	1.33	1.386
stage4	1.88	1.85

Table 5.1: The temperature coefficients of the different stages

The added and subtracted voltages are shown in figure 5.4. The curve seems to have a strange shape. This is because the CTAT temperature coefficient is somewhat different then wanted. This gives the slope in the reference voltage that is used as the input of the add/subtract circuit.

Apart from the slope it is seen that the added voltage ($V_N(V_{in})$) and the subtracted voltage ($V_{subtract}$) are equal and are equal to half the reference voltage ($half_vref$). The add subtract circuit with the voltages is shown in figure 5.2.

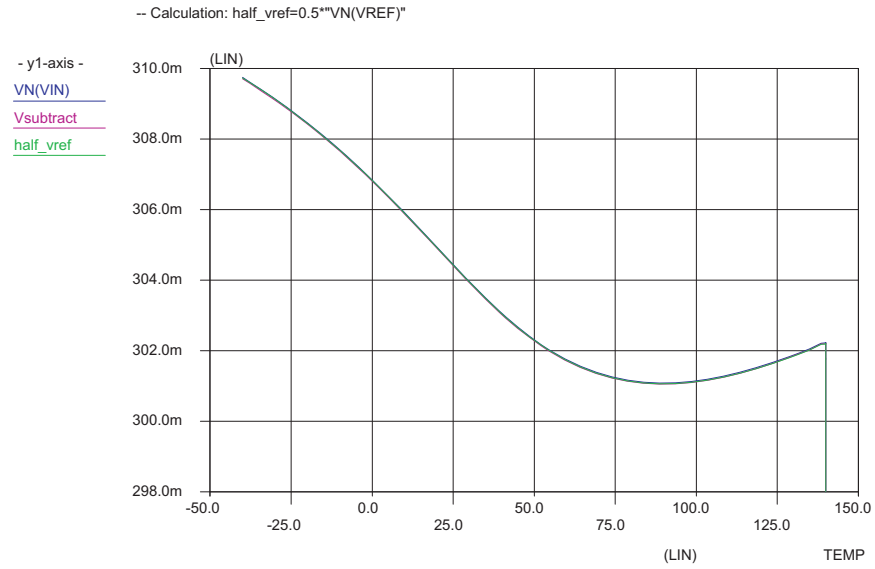
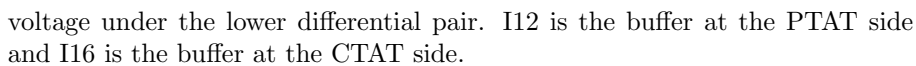


Figure 5.4: The added voltage and the subtracted voltage

The inner and outer buffers are simulated separately. The outer buffer stage has a larger input output voltage difference and therefore an extra differential pair is used. The simulation result for the outer buffer is shown in figure 5.6. For the buffer it is important that the currents of the current sources are approximately the same. This means that the voltage over the current sources in the buffer has to be approximately the same.

The circuit of the outer buffer is shown in figure 5.5).



At high temperature the voltage V_d will rise. Since all differential pairs are equal the REFERENCE voltage will be almost equal to the V_d voltage of the outer buffer with the low V_d voltage. This is also seen in the simulation.

It is seen that this error is about 5mV. This means the voltage over the current sources of the outer buffers are nearly equal. What is more important is that the currents in the outer buffers are equal. The current in the current sources are plotted in figure 5.8. In this figure I1 is the current of the current source in the outer buffer at the CTAT side and I22 is the current in the buffer at the PTAT side. For low temperatures the currents are approximately the

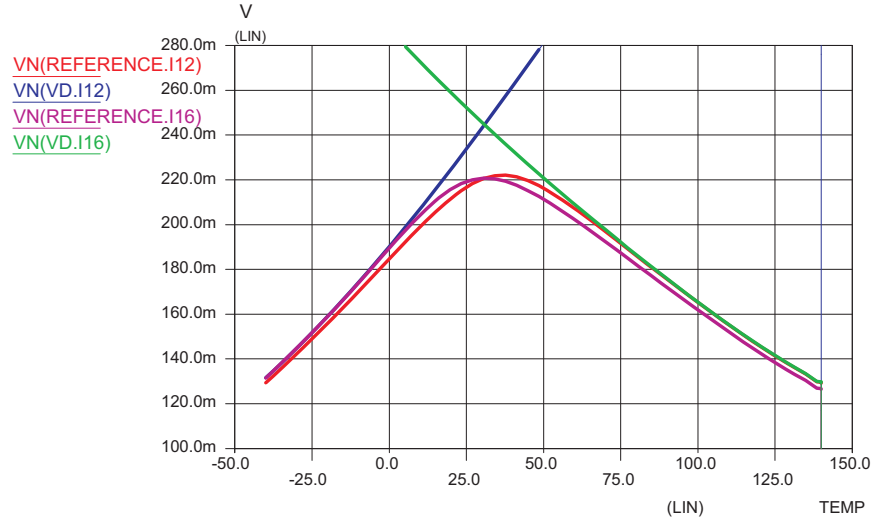


Figure 5.6: The simulation result of the outer buffer stages

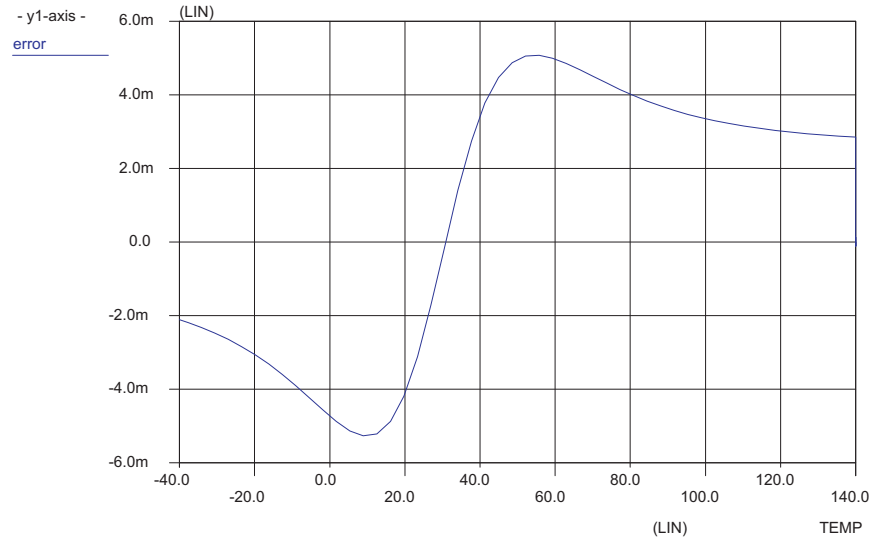


Figure 5.7: The voltage difference in the voltage over the current source of the outer buffers

same. For high temperature the error is largest (160nA). This current difference will lead to mismatch in the buffers and therefore the error in the bandgap reference's output is expected to be high at higher temperatures).

For the inner buffers the current source voltage problem is smaller, because the voltage range at the inputs of the differential pair is smaller. Therefore

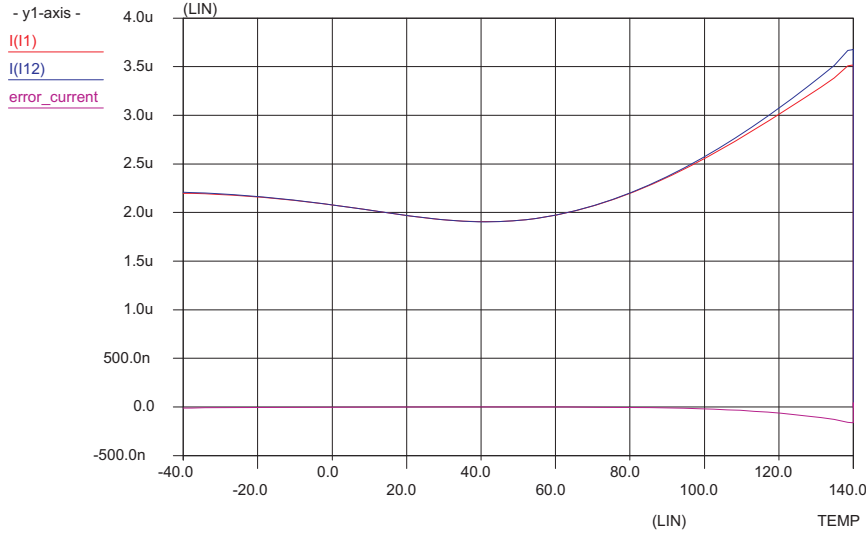


Figure 5.8: The currents of the current sources of the outer buffers

the current sources will always be in saturation. The simulation result of the voltage over the current source of the inner buffers is shown in figure 5.9.

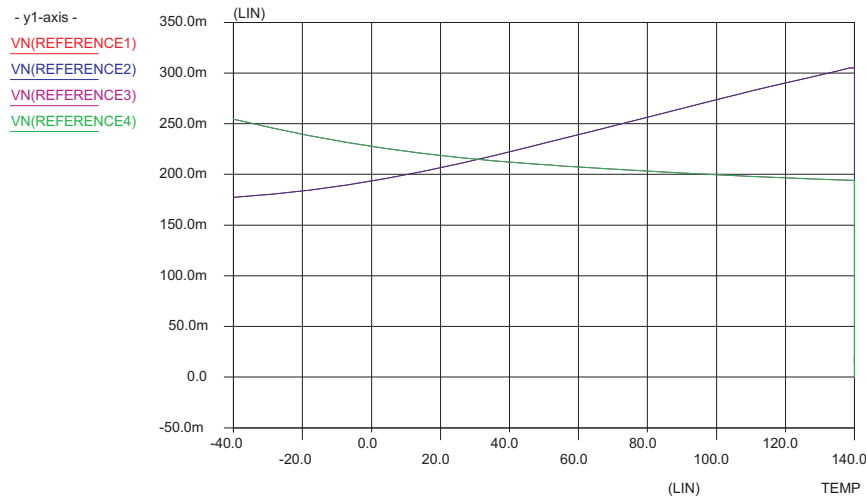


Figure 5.9: The voltage difference in the voltage over the current source of the inner buffers

In this figure it is seen that both buffers at the PTAT side (REFERENCE1 and REFERENCE2) and both buffers at the PTAT side (REFERENCE3 and REFERENCE4) have equal voltages. The voltage difference at the current sources in the inner buffers is a lot larger than is at the outer buffers, while the

current difference is smaller. The currents of the current sources are plotted in figure 5.10. I_6 and I_9 are the currents of the current sources of the inner buffers at the PTAT side while I_{14} and I_{17} are the currents of the current sources of the inner buffers at the CTAT side.

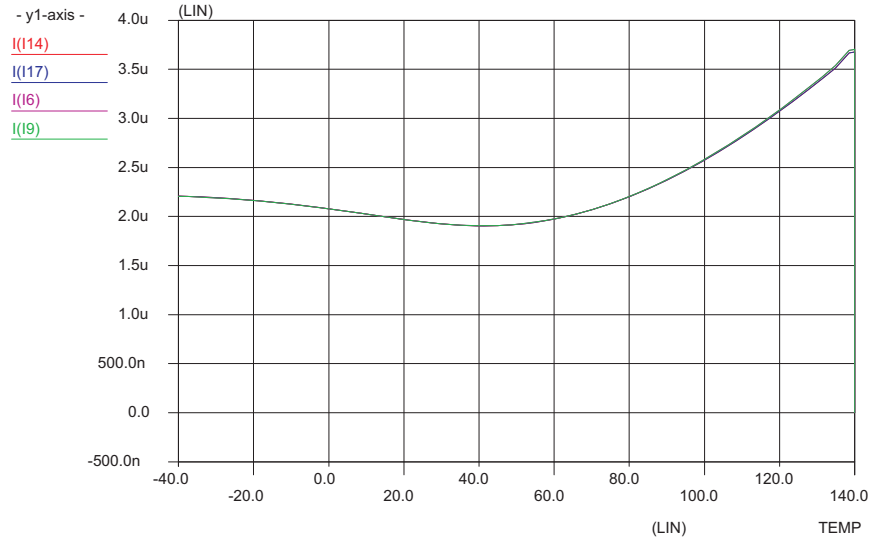


Figure 5.10: The current in the current sources of the inner buffers

From this simulation it is seen that the inner buffers indeed have a lot smaller current difference, while the voltage difference was larger. The largest current difference is at high temperature and is 27nA.

5.2 Stability analysis

A lot of problems were found doing simulations with the current FinFET models. For example the threshold voltage of the model could not be adapted (non convergence), no low temperature simulations and also no AC simulations could be done. Therefore it is assumed that the model is not so accurate.

To test the stability of the bandgap reference steps on different nodes in the circuit are applied. By applying a step on the supply voltage an instability is found (see figure 5.11).

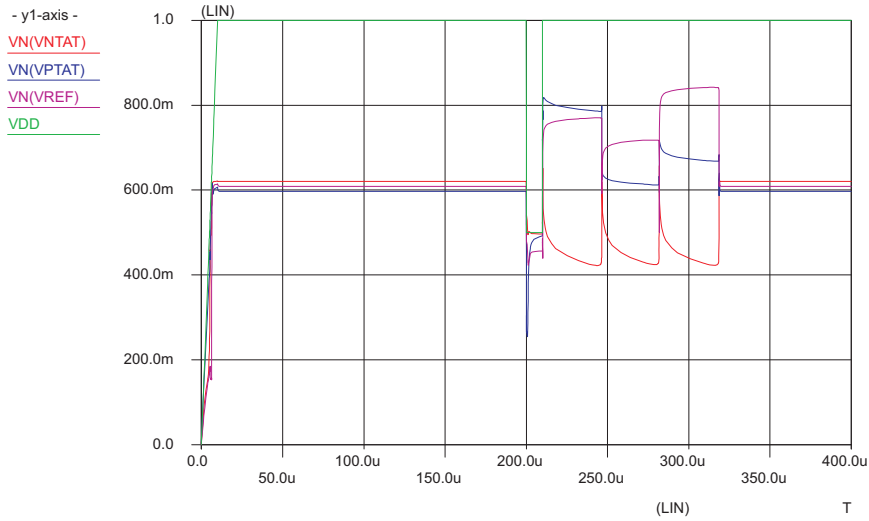


Figure 5.11: Stability simulation with a step on the supply voltage

From simulations it seems that the CTAT voltage block is unstable. A small step is applied at the input of the current source at the OPAMP and at the output (V_{ref1}) the transfer is examined. The simulation result is shown in figure 5.12.

It can be seen that a small step is at the input of the current source at the OPAMP (net043) the output (V_{ref1}) has an overshoot, that stabilizes with a first order behaviour. This can be explained by the fact that the current change because of the step on the current source arrives earlier via transistor M_{12} than via transistor M_{11} (see figure 5.13). Therefore charge is extracted M_1 and therefore the loop gets a positive feedback for a short time.

This becomes stable again after both current changes are present and therefore it is no explanation for the instability. It is assumed that the FinFET model is the problem (not accurate) and therefore this short positive feedback mechanism starts to oscillate.

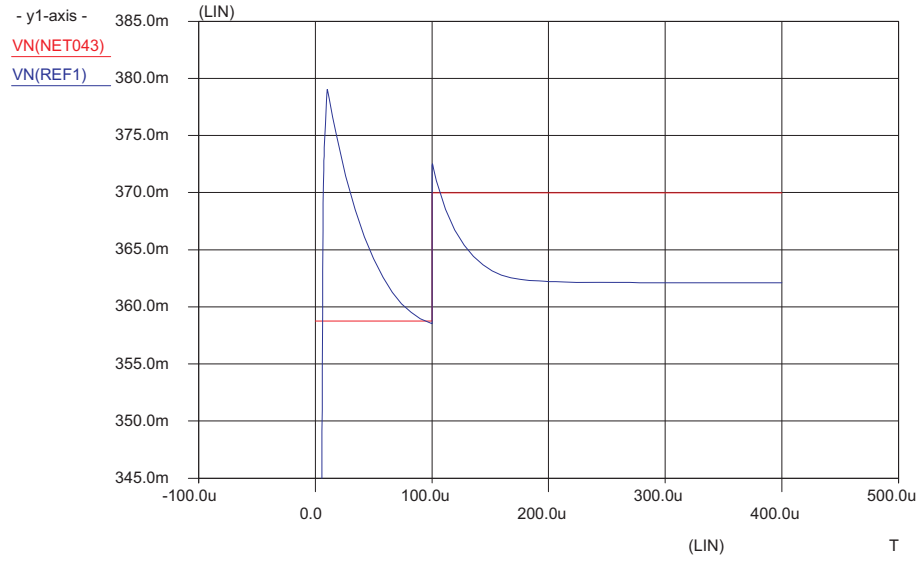


Figure 5.12: The OPAMP instability

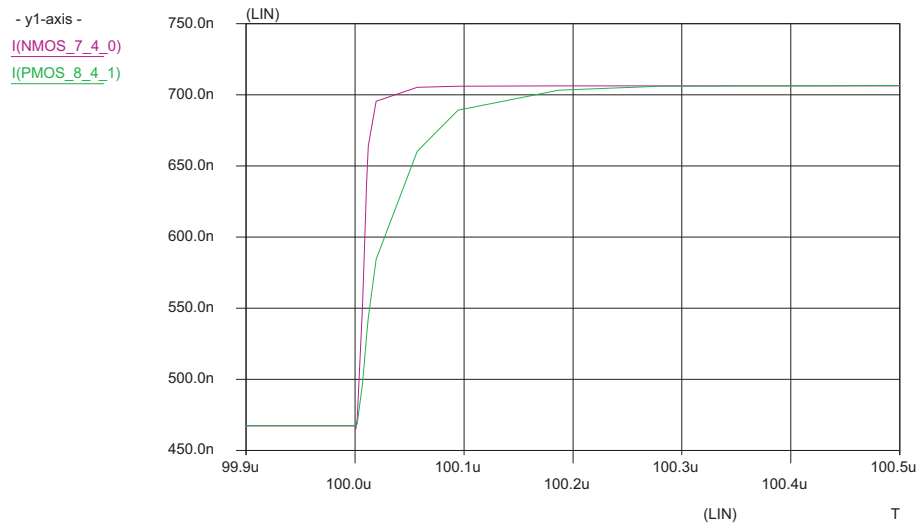


Figure 5.13: The currents in the OPAMP

5.3 Power Supply Rejection Ratio (PSRR)

For the bandgap reference it is important that the reference voltage is independent of the supply voltage. Therefore the Power supply rejection ratio is simulated. The result is shown in figure 5.14 for a temperature of 25 °C.

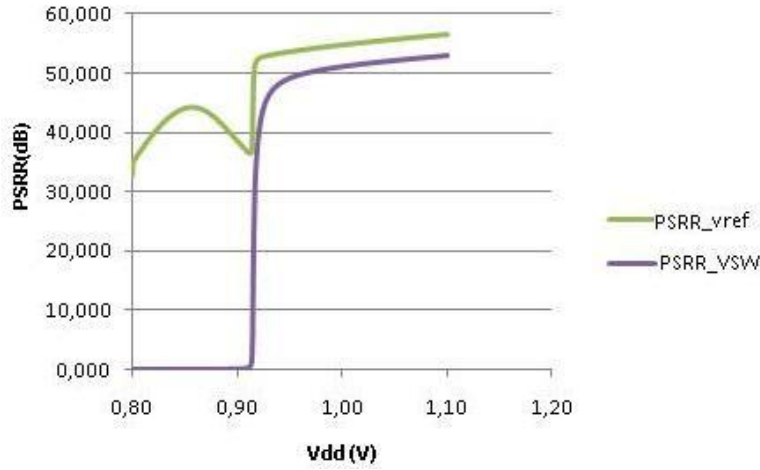


Figure 5.14: The PSRR of the reference voltage ($PSRR_{vref}$) and the PSRR of the 0.9V supply voltage for the triode resistor ($PSRR_{VSW}$) both at 25 °C

It can be seen that the reference voltage has a PSRR higher than 52dB for supply voltages higher than 920mV. For lower supply voltages the PSRR decreases rapidly. This is caused by the 0.9V reference voltage.

The Power Supply rejection Ratio at -40 °C is shown in figure 5.15 and the PSRR at 140 °C is shown in figure 5.16 in both figures psrr is the Power Supply rejection Ratio of the reference voltage.

It can be seen that the PSRR at -40 °C is approximately 52dB (1V) which is good. On the other hand the PSRR at 140 °C is lower, only 32dB (1V).

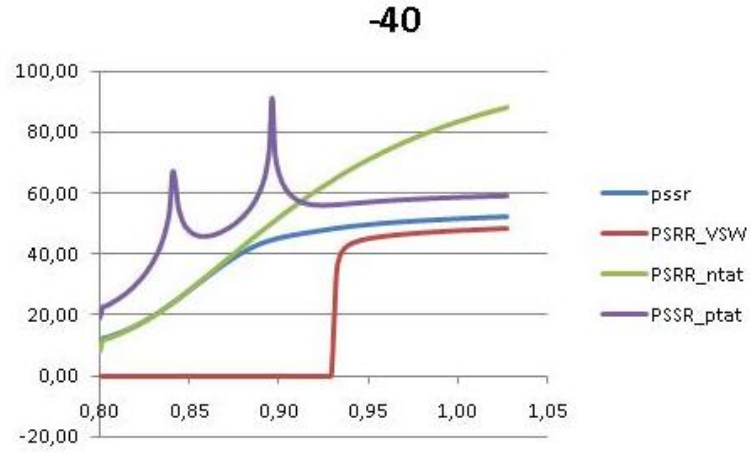


Figure 5.15: The PSRR of the reference voltage and the 0.9V supply voltage for the triode resistor at -40°C

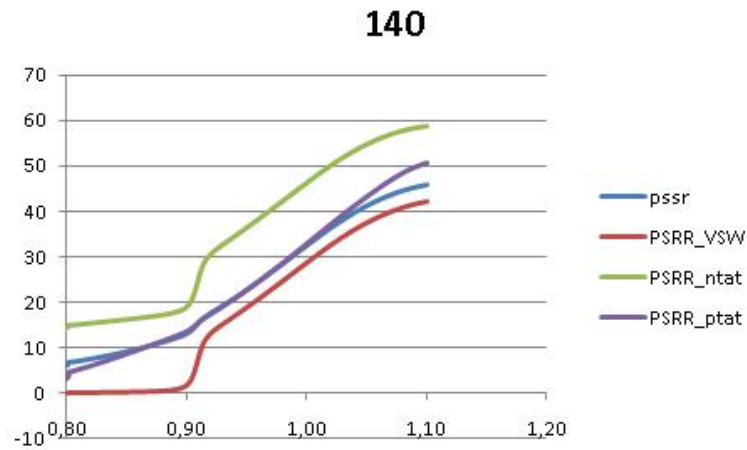


Figure 5.16: The PSRR of the reference voltage and the 0.9V supply voltage for the triode resistor at 140°C

This low rejection ratio is caused by the PTAT voltage stage (the PTAT voltage stage is shown in figure 5.17).

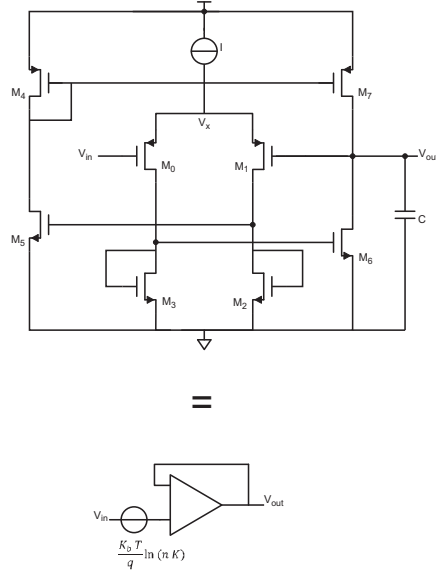


Figure 5.17: The final design solving the channel charge relocation problem

At 140°C the current mirroring to the output is the problem. The current through M7 decreases, because this transistor is close to triode (the drain source voltage is 178mV, while the overdrive voltage is 123mV). Therefore the current ratio of the current through M4 versus M7 decreases with higher temperatures. This is seen in figure 5.18.

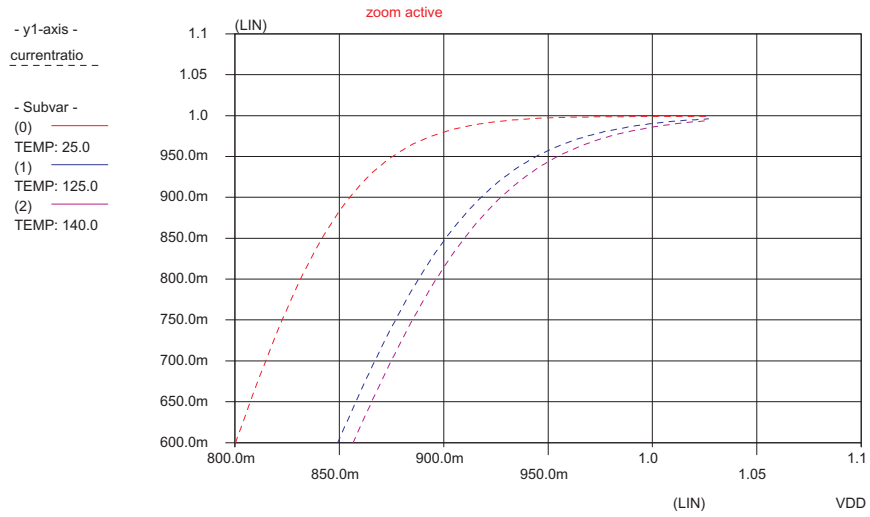


Figure 5.18: The current ratio in the current mirror of the last PTAT source

5.4 Mismatch

Another important characteristic in the design of the bandgap reference is the mismatch. The mismatch is simulated at 25^0C . More interesting would be the mismatch at low and high temperatures, because there the mismatch would be larger. But unfortunately the simulation at low temperature would not converge, the simulation result at high temperature is discussed later.

At 25^0C the reference voltage has a spread of 2.63mV at a mean reference voltage value of 605mV. Which means that the $\sigma_{vref} = 0.42\%$. This is within the specified value. The contribution of the different sections is interesting because then it is known what section has to be improved. It is difficult to derive the separate block mismatches, because there is a feedback-loop in the PTAT circuit. For now it is assumed that this feedback of the reference voltage has no large effect on the mismatch of the PTAT block, because the reference voltage is divided before it is used as an input for the PTAT stage.

The simulated results are shown in table 7.2.

From the simulated values of the σ and the mean value the percentage spread is calculated. Also the percentage spread of that block at the output is calculated.

	σ (mV)	mean (mV)	spread (%)	spread at the output (%)
V_{ref}	2.63	605.0	0.43	0.43
V_{ctat}	1.98	615.0	0.322	0.161
V_{ptat}	3.3	595.7	0.55	0.275

Table 5.2: The mismatch simulation results for 25^0C

The mismatch on the buffer can be calculated:

$$\sigma V_{buffer} = \sqrt{\left(\sigma V_{ref}^2 - \frac{(\sigma V_{ctat}^2 + \sigma V_{ptat}^2)}{4}\right)} \quad (5.2)$$

The spread referred to the output of the buffer is: 0.2887 %.

More interesting is the mismatch simulation result for high temperature (140^0C). At this temperature it is expected that the buffer mismatch increases, because the current ratio in the buffer increases and therefore the error at the output increases. The error on the output is (see equation 5.3):

$$\frac{V_{ref}}{dI} = \frac{1}{\sqrt{2k_n I_{ref}}} \frac{1 - \sqrt{\frac{1}{\alpha} - 1}}{4\sqrt{(1 - \alpha)}} \quad (5.3)$$

When α is equal to half (around 50^0C), both branches carry equal currents. The limits are α is zero (all current is in I_a) or α is one (all current is in I_b).

For the error on the reference voltage, it is seen that when α is equal to a half (the differential pair is in balance) there is no error at the output. When most current is in one branch ($\lim_{\alpha \rightarrow 0}$ and $\lim_{\alpha \rightarrow 1}$) the error becomes very

large.

This effect is also seen in the mismatch simulation results at high temperature. The spread referred to the output of the buffer is: 0.92 %.

	σ (mV)	mean (mV)	spread (%)	spread at the output (%)
V_{ref}	5.95	599.8	0.99	0.99
V_{ctat}	2.27	379.0	0.599	0.299
V_{ptat}	3.42	821	0.55	0.4165

Table 5.3: The mismatch simulation results for 140°C

At high temperature the most increase in the mismatch is seen at the buffer, while the mismatch for the other blocks only increase by a small amount.

Chapter 6

Layout

To make a good layout for the designed bandgap reference some important aspects need to be taken into account. Especially for the matching attention need to be paid that:

- The current sources of the buffer stages are equal and therefore need to be placed close together.
- The same holds for the current sources of the PTAT stage.
- Apart from the currents also the inner buffer stages as well as the outer stages need to be matched.
- And the PTAT stages themselves
- The diodes have to be placed in a square to achieve good matching

For each block dummies are used to make sure that the symmetry improves.

The layout of the total bandgap reference is shown in figure 6.1.

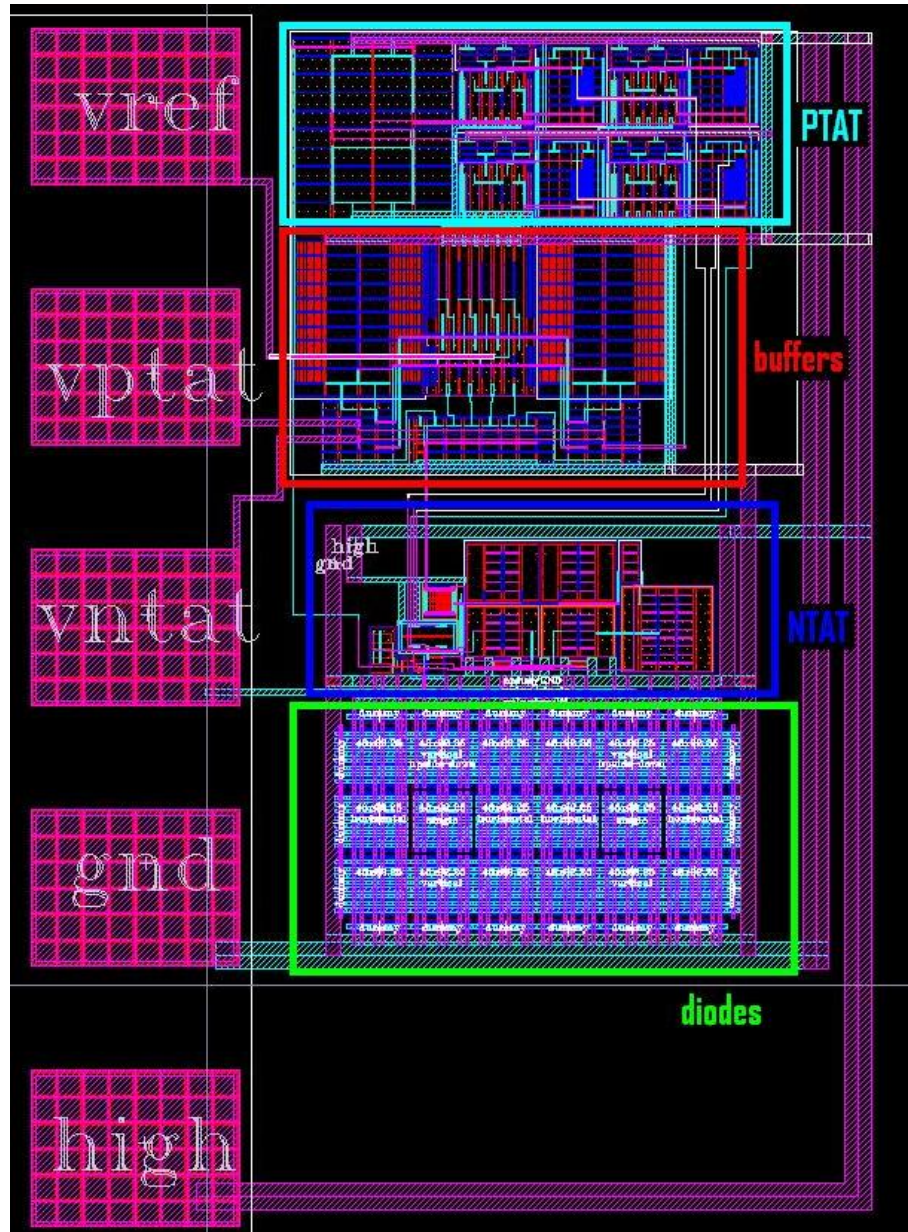


Figure 6.1: The layout of the designed bandgap reference with an indication of the different sub-blocks

Chapter 7

Conclusions and recommendations

The design and layout of a sub 1V bandgap reference in FinFET technology is completed and is currently in fabrication in a 32 nm FinFET process at IMEC.

An averaging bandgap reference structure is proposed to implement a low-supply voltage bandgap reference circuit in FinFET technology. The resistors that are typically required in known low-voltage bandgap references are replaced by a PTAT voltage source and a triode resistor. The PTAT voltage is made by cascaded voltage followers, with build-in PTAT offsets.

To make the triode resistor accurate over large voltage swings both a N-type and a P-type FinFET are used. These triode transistors need to be biased with a supply independent voltage.

The output voltage is the average of a CTAT and a PTAT voltage, using two stages of transimpedance amplifiers.

In the simulations a few problems can be found that should be considered in a later design.

- In a new design of the PTAT voltage generator. The overdrive voltage of the p-mos current mirrors has to be lower. So that the current mirroring will also work at high temperatures.
- At high temperature the most increase in the mismatch is seen at the buffer, while the mismatch for the other blocks only increase by a small amount. The best improvement in the mismatch can therefore be made by changing the design of the buffer.

Some target properties of the bandgap reference circuit that have are summarized in the table below including the simulated performance:

The mismatch at high temperatures is lower than expected. At high temperature the most increase in the mismatch is seen at the buffer, while the mismatch for the other blocks only increase by a small amount. The results of mismatch simulation are shown in table 7.1.

The error in the buffer comes from the current ratio in the differential pair. It is seen that when the current ratio is equal to a half (the differential pair

	Specified	Simulated
V_{ref}	$\approx 0.6V$	0.565V
σV_{ref}	0.5%	25 ⁰ C : 0.43% 140 ⁰ C : 0.99%
$PSRR$	40dB	-40 ⁰ C : 52dB 25 ⁰ C : 52dB 140 ⁰ C : 32dB
V_{dd}	1V	> 0.93V

Table 7.1: Comparison of the specified requirements and the simulated results

is in balance) there is no error at the output. When most current is in one branch ($\lim_{\alpha \rightarrow 0}$ and $\lim_{\alpha \rightarrow 1}$) the error becomes very large.

	σ (mV)	mean (mV)	spread (%)	spread at the output (%)
V_{ref}	5.95	599.8	0.99	0.99
V_{ctat}	2.27	379.0	0.599	0.299
V_{ptat}	3.42	821	0.55	0.4165

Table 7.2: The mismatch simulation results for 140⁰C

It can be seen that the PSRR at -40 ⁰C is approximately 52dB (1V) which is good. On the other hand the PSRR at 140 ⁰C is lower, only 32dB (1V).

This low rejection ratio is caused by the PTAT voltage stage. At 140 ⁰C the current mirroring to the output is the problem, because a FinFET is close to triode. The overdrive voltage of the p-mos current mirrors has to be lower. So that the current mirroring will also work at high temperatures.

The supply voltage from which the circuit start to work is around 0.93V.

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Appendix A

The PTAT voltage generator

A.1 Temperature variation resistor

The expression for the temperature variation is:

$$nTC_{error} = \frac{\partial V_{error}}{\partial R_1} \frac{\partial R_1}{\partial T} \Delta T \quad (\text{A.1})$$

This can be rewritten using the temperature expression for the resistor. Which is:

$$R = R_0 + R_0\alpha(T - T_0) \quad (\text{A.2})$$

Now the subparts of this equation can be solved. The resistance variation over temperature is:

$$\frac{\partial R_1}{\partial T} = \frac{\partial}{\partial T} R_1 + \alpha R_{1,T0}(T - T_0) = \alpha R_{1,T0} \quad (\text{A.3})$$

The error because of a changing resistor is:

$$\begin{aligned} V_{error} &= V_{diode} + V_R \\ \frac{\partial V_{error}}{\partial R_1} &= \frac{KT}{q} \ln\left(\frac{KT}{q} \frac{\ln N}{I_{d0} R_{T0}}\right) + \frac{KT}{q} \ln N \\ \frac{\partial V_{error}}{\partial R_1} &= -\frac{kT}{q} \frac{1}{R_{1,T0}} \end{aligned} \quad (\text{A.4})$$

So the total voltage error is:

$$\frac{\partial V_{error}}{\partial R_1} \frac{\partial R_1}{\partial T} \Delta T = -\frac{kT_0}{q} \alpha \Delta T \quad (\text{A.5})$$

A.2 Temperature coefficient measurement results

For the design of a bandgap reference the temperature dependence of the FinFET I-V curve is important. Therefore a measurement is done to check if the simulation model of a n-FinFET and a p-FinFET corresponds with the measurements.

The I-V curve measurements for temperatures: 25°C , 65°C and 105°C are shown in figure A.1 for a n-FinFET and in figure A.2 for a p-FinFET.

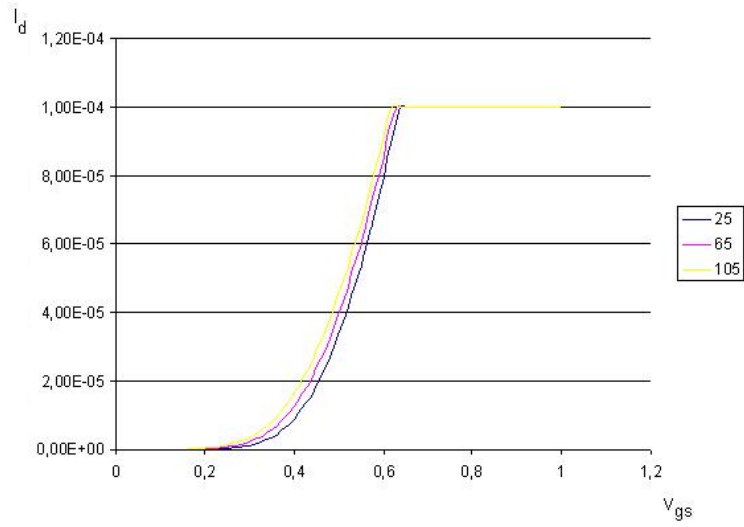


Figure A.1: The I-V curve measurement result of a n-FinFET

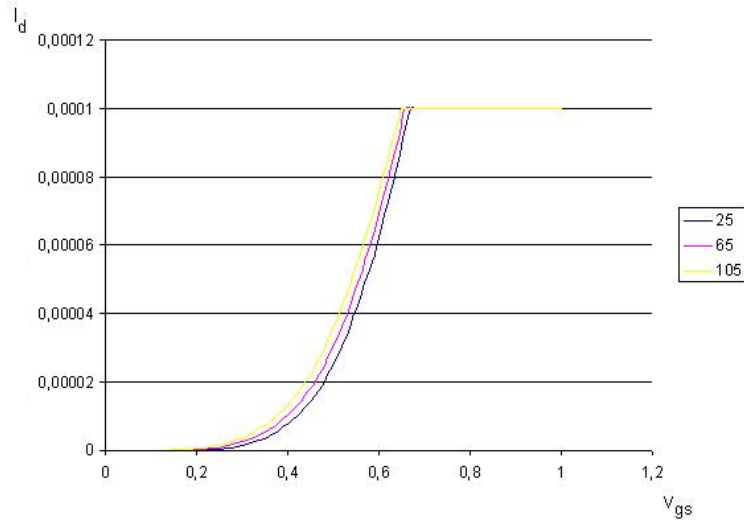


Figure A.2: The I-V curve measurement result of a p-FinFET

It can be seen that the n-FinFET and the p-FinFET curve behave approximately the same over temperature. For both FinFETs the current increases with temperature (for the same gate-source voltage). The comparison of a n and a p-FinFET I-V curve at 25°C is shown in figure A.3.

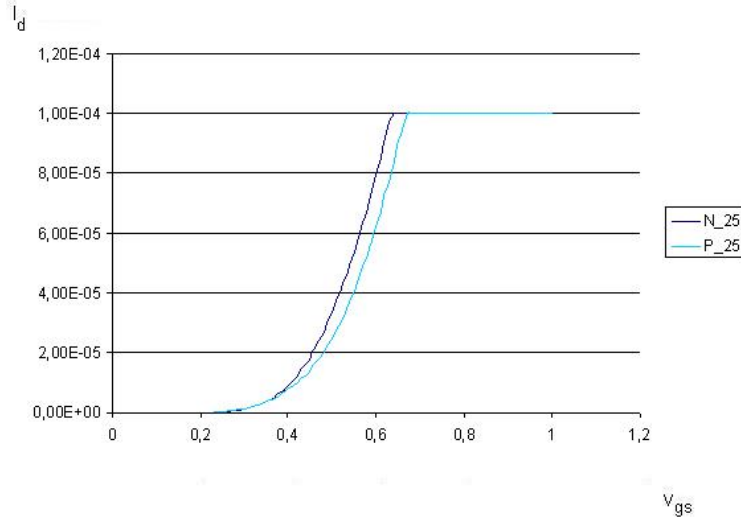


Figure A.3: The I-V curve comparison of a n-FinFET and a p-FinFET at 25°C

At 25°C the p-curve is a shifted version of the n-curve, this holds for all temperatures. Therefore the only difference in the FinFET model is the threshold voltage.

When the FinFET model is compared to the measurement results it is seen that at 25°C the curves match. On the other hand at other temperatures they do not match. Therefore the models for a n-FinFET and p-FinFET are curve fitted to the measured results.

As was already mentioned for the design also the temperature coefficient of a FinFET is important. From the measurement results a temperature coefficient of approximately 1mV/K for both a n-FinFET and a p-FinFET can be derived.

A.3 Charge relocation

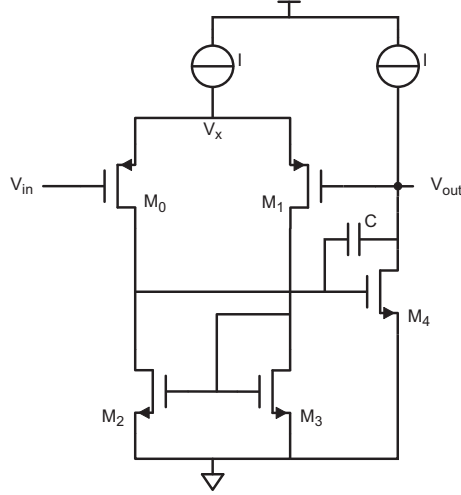


Figure A.4: The PTAT voltage stage with charge relocation problems

To check the stability of a PTAT voltage source the effect of a small signal voltage to the output is examined. To do this first the small signal equivalent is derived. This is shown in figure A.5.

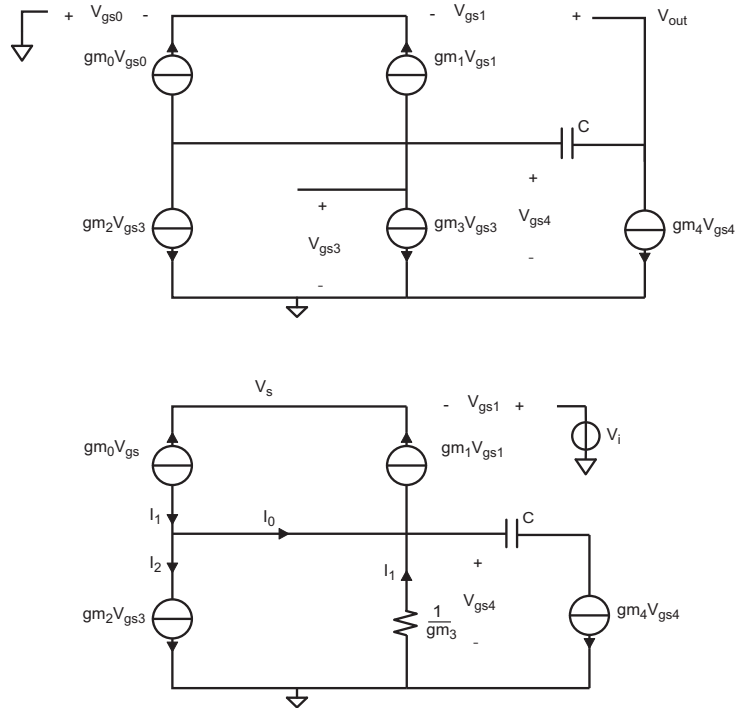


Figure A.5: Small signal equivalent of a PTAT voltage stage

The output voltage equation is:

$$v_{out} = v_{gs4} - v_f \quad (\text{A.6})$$

with v_f the voltage over the capacitor and:

$$\begin{aligned} v_{gs4} &= \frac{i_0}{gm_4} \\ v_f &= i_0 \frac{1}{j\omega C} \end{aligned} \quad (\text{A.7})$$

Rewriting the equation for the output voltage gives:

$$v_{out} = \frac{i_0}{gm_4} - i_0 \frac{1}{j\omega C} \quad (\text{A.8})$$

To derive the output voltage, the current i_0 has to be known. This is equal to:

$$i_0 = i_1 - i_2 \quad (\text{A.9})$$

These two current have to be derived. The current in the differential pair branches are equal:

$$\begin{aligned} gm_0 v_s &= gm_1 v_{gs1} \\ gm_0 v_s &= gm_1 (v_i - v_s) \end{aligned} \quad (\text{A.10})$$

From this the voltage at the sources of the differential pair can be derived:

$$v_s = v_i \frac{gm_1}{gm_1 + gm_0} \quad (\text{A.11})$$

Now the current i_1 is known:

$$i_1 = v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \quad (\text{A.12})$$

For the current in the current mirror (i_2), first the gate source voltage of the current mirror has to be known:

$$v_{gs3} = \frac{1}{gm_3} i_1 \quad (\text{A.13})$$

$$\begin{aligned} i_2 &= v_{gs3} gm_2 = -\frac{gm_2}{gm_3} i_1 \\ i_2 &= -\frac{gm_2}{gm_3} v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \end{aligned} \quad (\text{A.14})$$

Therefore also the current i_0 is known:

$$i_0 = v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \left(1 + \frac{gm_2}{gm_3} \right) \quad (\text{A.15})$$

Then, also the equation for the output voltage is known:

$$\begin{aligned} v_{out} &= i_0 \left(\frac{1}{gm_4} - \frac{1}{j\omega C} \right) \\ v_{out} &= -v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \left(1 + \frac{gm_2}{gm_3} \right) \left(\frac{1}{j\omega C} - \frac{1}{gm_4} \right) \end{aligned} \quad (\text{A.16})$$

Because this last stage must work as an integrator it can be assumed that:

$$\frac{1}{j\omega C} \gg \frac{1}{gm_4} \quad (\text{A.17})$$

It is also known that the current mirror has an amplification:

$$\frac{gm_2}{gm_3} = k \quad (\text{A.18})$$

Therefore the output voltage equation simplifies to:

$$v_{out} = -v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \frac{(k+1)}{j\omega C} \quad (\text{A.19})$$

It can be seen that for normal operation the PTAT voltage source is stable (a rising input voltage causes the output voltage to decrease). On the other hand, when charge relocation is taken into account the circuit becomes instable. When the voltage at the output becomes lower than the threshold voltage the channel of the FinFET discharges. This effect can be modeled as a current source with the sign opposite to the ordinary small signal equivalent. (when the voltage on the gate decreases the current due to the channel discharging effect increases). When this channel discharging effect becomes larger than the normal current the transconductance becomes negative and therefore the output voltage equation changes to:

$$v_{out} = v_i \frac{gm_0 gm_1}{gm_0 + gm_1} \frac{(k+1)}{j\omega C} \quad (\text{A.20})$$

This behavior results in a positive feedback mechanism. Therefore it behaves as a relaxation oscillator.

A.4 Design one stage

A.4.1 Mismatch

The equation for the mismatch in the threshold value is:

$$\sigma_{Vth} = \frac{A_{Vth}}{\sqrt{WL}} \quad (\text{A.21})$$

This mismatch has an effect on the differential pair and on the current mirror.

For the dimensions of the differential pair there has to be a factor N between M0 and M1. This is made by taking for W1 $W1 = \sqrt{N}W0$ and taking for L0 $L0 = \sqrt{N}L1$. This way the factor is there, but both devices have an equal contribution to the mismatch because there areas are equal. The effect on the differential pair is:

$$\begin{aligned} \sigma_{Vth,out,d} &= \sqrt{\left(\frac{A_{Vth}}{\sqrt{W_0L_0}}\right)^2 + \left(\frac{A_{Vth}}{\sqrt{W_1L_1}}\right)^2} \\ &= \sqrt{\left(\frac{A_{Vth}}{\sqrt{\sqrt{N}W_1L_0}}\right)^2 + \left(\frac{A_{Vth}}{\sqrt{\sqrt{N}W_0L_1}}\right)^2} \\ &= \sqrt{2} \frac{A_{Vth}}{\sqrt{W_0L_0}} \end{aligned} \quad (\text{A.22})$$

The effect on the current mirror can best be derived by taking the small signal equivalent of the current mirror and adding a source that represents the mismatch in one FinFET. This is shown for FinFET 3 in Figure A.6. From this the mismatch of the current mirror can be described by:

$$\sigma_{Vth,out,c} = \frac{1}{gm_0} \sigma I_2 - \frac{1}{gm_1} \sigma I_3 \quad (\text{A.23})$$

with:

$$\begin{aligned} I_d &= I_2 + I_3 \\ I_2 &= -I_3 \end{aligned} \quad (\text{A.24})$$

So this can be simplified to:

$$\sigma_{Vth,out,c} = \left(\frac{1}{gm_0} + \frac{1}{gm_1} \right) \sigma I_2 \quad (\text{A.25})$$

For the current holds:

$$\begin{aligned} I_2 &= gm_2 V_{gs2} \\ I_3 &= gm_3 V_{gs3} \end{aligned} \quad (\text{A.26})$$

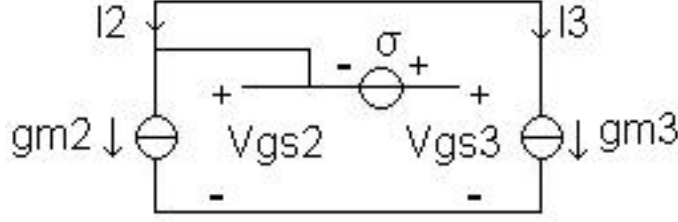


Figure A.6: Small signal circuit of the effect of mismatch on one side of the current mirror

When one FinFET has a mismatch in the threshold voltage (see figure A.6) this will influence the gate source voltage:

$$\begin{aligned}
 V_{gs3} &= V_{gs2} + \sigma_{Vth} & (A.27) \\
 I_2 &= -I_3 \\
 gm_2 V_{gs2} &= -gm_3 V_{gs3} \\
 gm_2 V_{gs2} &= -gm_3 (V_{gs2} + \sigma_{Vth}) \\
 V_{gs2} &= -\frac{gm_3 \sigma_{Vth}}{gm_2 + gm_3}
 \end{aligned}$$

The mismatch in the current is:

$$\begin{aligned}
 I_2 &= gm_2 V_{gs2} & (A.28) \\
 I_2 &= -\frac{gm_3 gm_2}{gm_2 + gm_3} \sigma_{Vth}
 \end{aligned}$$

So the final expression for the mismatch effect on one side of the current mirror is:

$$\sigma_{Vth,out,c} = -\frac{gm_0 + gm_1}{gm_0 gm_1} \frac{gm_3 gm_2}{gm_2 + gm_3} \sigma_{Vth} \quad (A.29)$$

When the other FinFET has a threshold mismatch this gives the same effect:

$$\sigma_{Vth,out,c} = \frac{gm_0 + gm_1}{gm_0 gm_1} \frac{gm_3 gm_2}{gm_2 + gm_3} \sigma_{Vth} \quad (A.30)$$

The total error for the current mirror is:

$$\sigma_{Vth,out,c} = \sqrt{\sigma_{Vth,out,cM2}^2 + \sigma_{Vth,out,cM3}^2} \quad (A.31)$$

It is known that $\frac{W_2}{L_2} = k \frac{W_3}{L_3}$. So the error in FinFET3 is k times smaller then the error in FinFET2.

So the total mismatch is:

$$\sigma_{Vth,out,c} = \sqrt{\left(\frac{1}{k} + 1\right)} \frac{gm_0 + gm_1}{gm_0 gm_1} \frac{gm_3 gm_2}{gm_2 + gm_3} \sigma_{Vth} \quad (A.32)$$

Now some attention need to be given to the different gm terms. Because of the large signal current difference ($I_2 = kI_3$) and the subthreshold and strong inversion FinFETs. The following relations for the gm terms hold:

subthreshold (M_0 and M_1): $gm = 40I_d$

Strong inversion (M_2 and M_3): $gm = \sqrt{2k_{n/p}I_d \frac{W}{L}}$

This gives for the gm terms:

$$\begin{aligned} gm_{M2} &= \sqrt{k} gm_{M3} \\ gm_{M0} &= k gm_{M1} \end{aligned} \quad (A.33)$$

Substituting these relations in equation A.30 gives:

$$\begin{aligned} \sigma_{Vth,out,c} &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{(1+k)gm_1}{kgm_1^2} \frac{\sqrt{k}gm_3^2}{(\sqrt{k}+1)gm_3} \sigma_{Vth} \\ &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{(1+k)\sqrt{k}}{k(\sqrt{k}+1)} \frac{gm_3}{gm_1} \sigma_{Vth} \\ &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{gm_3}{gm_1} \sigma_{Vth} \end{aligned} \quad (A.34)$$

The mismatch error for gm terms is known. But the device dimensions are needed. This are derived by substituting the equations for the gm terms and $\sigma_{Vth} = \frac{A_{Vth}}{\sqrt{WL}}$. This gives:

$$\begin{aligned} \sigma_{Vth,out,c} &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{\sqrt{2k_{n/p}I_d \frac{W_3}{L_3}}}{40I_d} \sigma_{Vth} \\ &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{\sqrt{2}}{40} \sqrt{\frac{k_{n/p} \frac{W_3}{L_3}}{I_d}} \frac{A_{Vth}}{\sqrt{W_3 L_3}} \\ &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{\sqrt{2}}{40} \sqrt{\frac{k_{n/p}}{I_d}} \frac{A_{Vth}}{L_3} \end{aligned} \quad (A.35)$$

This equation can be rewritten to area by substituting:

$$I_d = k_{n/p} \frac{W_3}{L_3} V_{gt}^2$$

This gives:

$$\begin{aligned} \sigma_{Vth,out,c} &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{\sqrt{2}}{40} \frac{\sqrt{k_{n/p}}}{\sqrt{k_{n/p} \frac{W_3}{L_3} V_{gt}}} \frac{A_{Vth}}{L_3} \\ &= \sqrt{\left(\frac{k+1}{k}\right)} \frac{1+k}{1+\sqrt{k}} \frac{1}{\sqrt{k}} \frac{\sqrt{2}}{40} \frac{A_{Vth}}{V_{gt} \sqrt{W_3 L_3}} \end{aligned} \quad (A.36)$$

Now both mismatch causes are expressed in an equation with area. So now the total mismatch can be expressed.

$$\begin{aligned} \sigma_{V_{th,out}}^2 &= \sigma_{V_{th,out,c}}^2 + \sigma_{V_{th,out,d}}^2 \\ &= \left(\frac{k+1}{k}\right) \frac{1+k^2}{1+\sqrt{k}^2} \frac{1}{k} \frac{2}{40^2} \frac{A_{V_{th}}^2}{V_{gt}^2 W_3 L_3} + \sqrt{2} \frac{A_{V_{th}}^2}{W_0 L_0} \end{aligned} \quad (A.37)$$

This is the total mismatch for one section. The total mismatch error for the PTAT voltage is M times the mismatch error shown in equation A.37. It can be seen that when the number of sections (M) is smaller the $\sigma_{V_{th,out}}$ per section can be higher and still have the same total mismatch. This means that the area's for FinFET zero and three can be smaller. So for the area it is better to take less sections.

There are still a lot of variables that can be chosen therefore an optimization is made to area. For this the previous equation is rewritten with: $A_0 = A_{tot} - A_3$ with a the area (WL) of FinFET zero and FinFET three.

$$\sigma_{V_{th,out}}^2 = \left(\frac{k+1}{k}\right) \frac{(1+k)^2}{(1+\sqrt{k})^2} \frac{1}{k} \frac{2}{40^2} \frac{A_{V_{th}}^2}{V_{gt}^2 A_3} + \sqrt{2} \frac{A_{V_{th}}^2}{A_{tot} - A_3} \quad (A.38)$$

This gives:

$$A_{tot} = \frac{\sqrt{2} A_{V_{th}}^2}{\left(\sigma_{V_{th,out}}^2 - \left(\frac{k+1}{k}\right) \frac{k^2+2k+1}{k+2\sqrt{k}+1} \frac{1}{k} \frac{2}{40^2 V_{gt}^2} \frac{A_{V_{th}}^2}{A_3}\right)} + A_3 \quad (A.39)$$

With the help of maple the optimum can be found. This is done by first taking the derivative of A_{tot} to k and then finding the minimum (derivative = 0).

The found expression for the minimum is then substituted in the equation for A_{tot} .

Then this substituted equation is differentiated to the area of FinFET three and this is solved to find equations for the area of FinFET three. This last step gives possible solutions for the area.

Then the value for k is calculated using the optimum for k and the different solutions for the area. From this also the value for N can be calculated ($N = \frac{C}{k}$).

Next the equations for the total area, the area for FinFET zero and the area for FinFET three can be calculated.

This gives the following solutions for k, N, $area_{tot}$, $area_0$ and $area_3$:

$$k = 7.427619736$$

$$N = 54.31470839$$

$$area_{tot} = \frac{0.1334220132e-4}{\sigma_{V_{th,out}}^2}$$

$$area_0 = \frac{0.1105850928e-4}{\sigma_{V_{th,out}}^2}$$

$$area_3 = \frac{0.2283692041e-510^{-5}}{\sigma_{V_{th,out}}^2}.$$

It can be seen that there is still a choice to be made. The sigma and the area are exchangeable. If a larger sigma is allowed then the area will decrease

drastically. This is also shown in figure 2.10. The total area is on the y-axis and the sigma on the x-axis.

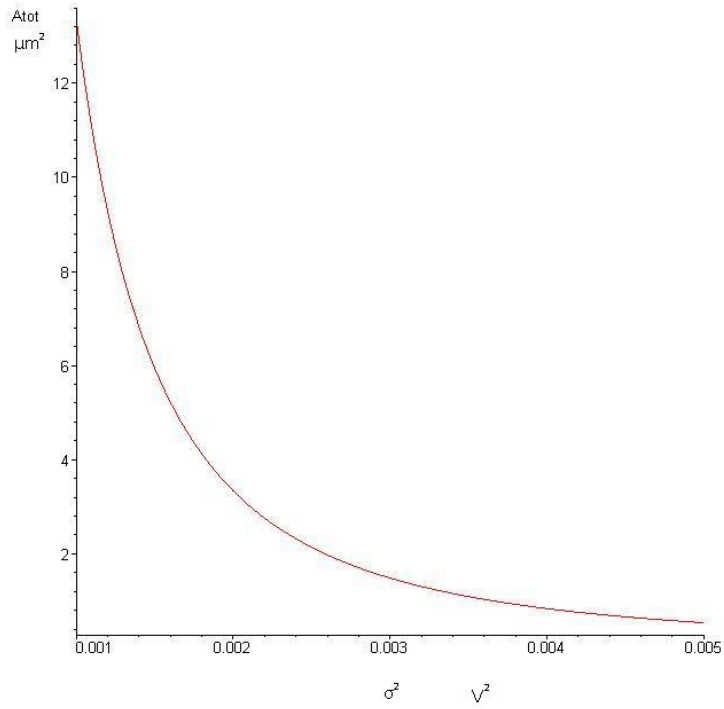


Figure A.7: The plotted total area of one section of the PTAT voltage

Now there are still some variables unknown: the W over L of each FinFET and the current. These can be derived using noise calculations.

A.5 Noise

The noise of the PTAT voltage circuit can be calculated. This can be done by adding the noise of each FinFET.

The contribution of the noise of FinFET zero can be derived by taking the small signal equivalent of the circuit with the noise source of FinFET zero, this is shown in figure A.8.

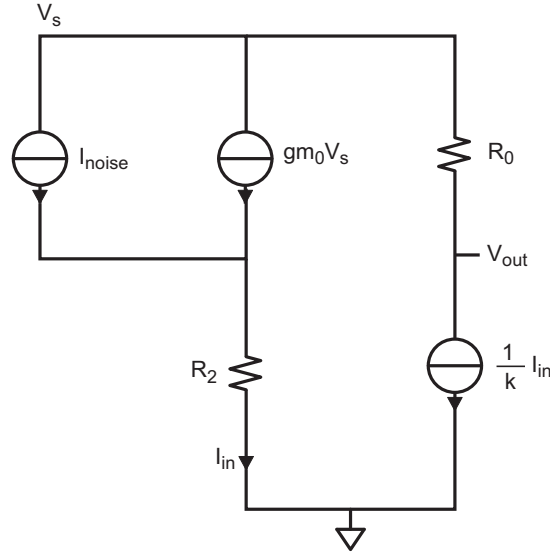


Figure A.8: The small signal equivalent with the noise source for M0

From this small signal equivalent it can be seen that for the current in the left and right branch $I_{in} = \frac{1}{k} I_{in}$ should hold. This means that I_{in} should be zero. In other words the current stays in the loop. And therefore:

$$\begin{aligned} I_{noise} &= gm_0 V_s \\ V_s &= \frac{I_{noise, M0}}{gm_0} \end{aligned} \quad (A.40)$$

The derivation of the contribution of the noise of FinFET one is done with the small signal circuit shown in figure A.9.

For this noise contribution also a contradiction in current can be seen. So also here the loop is closed. The noise contribution is:

$$V_s = \frac{I_{noise, M1}}{gm_1} \quad (A.41)$$

In the small signal equivalent of FinFET2 (see figure A.10) the currents in

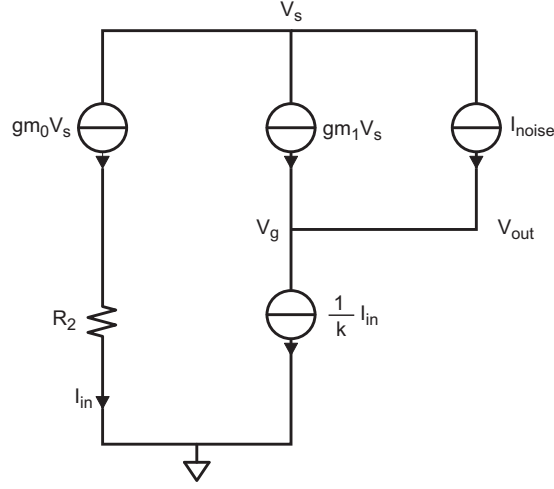


Figure A.9: The small signal equivalent with the noise source for M1

the node can be summed:

$$\begin{aligned} \frac{1}{K} I_{in} + I_R + I_{in} &= 0 \\ I_{in} &= -\frac{I_R K}{K+1} \end{aligned} \quad (\text{A.42})$$

and also:

$$V_1 = \frac{1}{gm_1} \frac{1}{K} I_{in} \quad (\text{A.43})$$

and

$$\begin{aligned} \frac{1}{K} I_{in} &= -gm_0 V_s \\ V_s &= -\frac{1}{K} \frac{I_{in}}{gm_0} \end{aligned} \quad (\text{A.44})$$

The output voltage is the source voltage minus voltage one.

$$\begin{aligned} V_{out} = V_s - V_1 &= -\frac{1}{K} \frac{I_{in}}{gm_0} - \frac{1}{gm_1} \frac{1}{K} I_{in} \\ &= -\frac{1}{K} \left(\frac{1}{gm_0} - \frac{1}{gm_1} \right) I_{in} \\ &= -\left(\frac{1}{gm_0} - \frac{1}{gm_1} \right) - \frac{I_R}{K+1} \\ &= \frac{I_R}{Kgm_1} \end{aligned} \quad (\text{A.45})$$

Finally the noise contribution for FinFET3 (see figure A.11).

$$\begin{aligned} \frac{1}{K} I_{in} + I_R + I_{in} &= 0 \\ I_{in} &= -\frac{I_R K}{K+1} \end{aligned} \quad (\text{A.46})$$

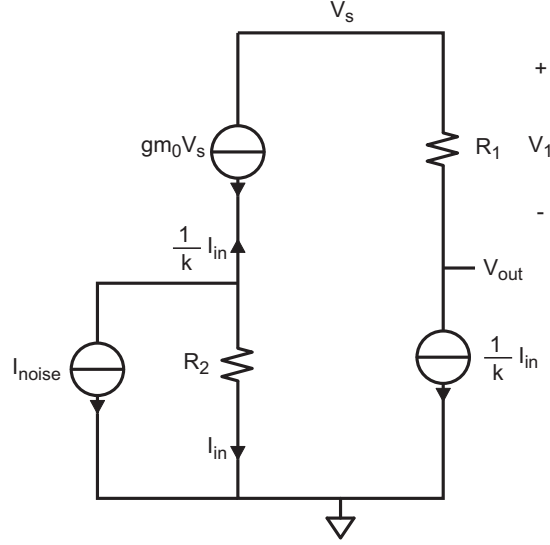


Figure A.10: The small signal equivalent with the noise source for M2

and also:

$$\begin{aligned} V_2 &= I_{in} \frac{1}{gm_1} \\ &= -\frac{I_R K}{K+1} \frac{1}{gm_1} \end{aligned} \quad (\text{A.47})$$

and

$$\begin{aligned} I_{in} &= V_s gm_0 \\ V_s &= \frac{I_{in}}{gm_0} \end{aligned} \quad (\text{A.48})$$

For the output voltage holds:

$$\begin{aligned} V_{out} &= V_s + V_2 = \frac{I_{in}}{gm_0} + \frac{I_{in}}{gm_1} \\ &= \left(\frac{1}{gm_0} + \frac{1}{gm_1} \right) - \frac{I_R K}{K+1} \\ &= \left(\frac{1}{K gm_1} + \frac{1}{gm_1} \right) - \frac{I_R K}{K+1} \\ &= \left(\frac{K+1}{K gm_1} \right) - \frac{I_R K}{K+1} \\ &= \frac{I_R}{gm_1} \end{aligned} \quad (\text{A.49})$$

So the equation for the total noise in one section of the PTAT voltage becomes:

$$\begin{aligned} V_{noise,tot}^2 &= V_{noise,m0}^2 + V_{noise,m1}^2 + V_{noise,m2}^2 + V_{noise,m3}^2 \quad (\text{A.50}) \\ V_{noise,tot}^2 &= \left(\frac{I_{noise,m0}}{gm_0} \right)^2 + \left(\frac{I_{noise,m1}}{gm_1} \right)^2 + \left(\frac{I_{noise,m2}}{kgm_1} \right)^2 + \left(\frac{I_{noise,m3}}{gm_1} \right)^2 \end{aligned}$$

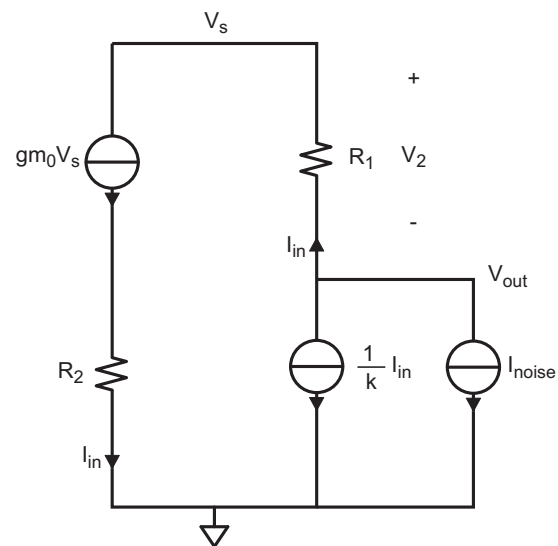


Figure A.11: The small signal equivalent with the noise source for M3

A.5.1 Thermal noise

For the thermal noise the equation is (for long devices):

$$I_{noise}^2 = \frac{8}{3}KTgm \quad (A.51)$$

So the total thermal noise is:

$$\begin{aligned} V_{noise,tot}^2 &= \frac{8}{3}KT \left(\frac{gm_0}{gm_0^2} + \frac{gm_1}{gm_1^2} + \frac{gm_2}{k^2gm_1^2} + \frac{gm_3}{gm_1^2} \right) \\ &= \frac{8}{3}KT \left(\frac{1}{gm_0} + \frac{1}{gm_1} + \frac{gm_2}{k^2gm_1^2} + \frac{gm_3}{gm_1^2} \right) \end{aligned} \quad (A.52)$$

In this equation can be substituting that:

$$gm_2 = Kgm_3 \text{ and } gm_0 = Kgm_1$$

This gives:

$$\begin{aligned} V_{noise,tot}^2 &= \frac{8}{3}KT \left(\left(\frac{1}{K} + 1 \right) \frac{1}{gm_1} + \left(\frac{1}{K} + 1 \right) \frac{gm_3}{gm_1^2} \right) \\ &= \frac{8}{3}KT \frac{1}{gm_1} \left(\left(\frac{1}{K} + 1 \right) \left(1 + \frac{gm_3}{gm_1} \right) \right) \end{aligned} \quad (A.53)$$

With:

$$gm_1 = 40I_3 \text{ and } gm_3 = \sqrt{2k_n \frac{W_3}{L_3}} I_3 \text{ This gives:}$$

$$V_{noise,tot}^2 = \frac{8}{3}KT \frac{1}{40I_3} \left(\left(\frac{1}{K} + 1 \right) \left(1 + \frac{\sqrt{2k_n \frac{W_3}{L_3}}}{40\sqrt{I_3}} \right) \right) \quad (A.54)$$

From this equation the standard deviation could be calculated. This is done by integrating the noise over a certain frequency range. It is not known till what frequency the thermal noise is constant. The assumption is made that this is the case till 1 GHz. So the standard deviation can be expressed with the following equation:

$$\begin{aligned} \sigma^2 &= \int_0^{1GHz} V_{noise,tot}^2 df \\ &= f \frac{8KT}{120I_3} \left(\left(\frac{1}{K} + 1 \right) \left(1 + \frac{\sqrt{2k_n \frac{W_3}{L_3}}}{40\sqrt{I_3}} \right) \right) \Big|_0^{1GHz} \end{aligned} \quad (A.55)$$

Sigma is chosen to be 1mV so from the previous equation the current can be calculated.

$$I_3 = f \frac{8KT}{120\sigma^2} \left(\left(\frac{1}{K} + 1 \right) \left(1 + \frac{2}{40V_{gt3}} \right) \right) \quad (A.56)$$

From this the I_3 can be calculated. So the I_2 is then $I_2 = KI_3$.

Now that the currents and the k and N are known the device dimensions can be calculated. Known is that the differential pair is in sub-threshold and the current mirror in saturation:

$$\begin{aligned} I_d &= \frac{W}{L} I_{d0} 10^{-10^{-at+b}} \exp \frac{qV_{gs}}{K_b T} \\ I_d &= k_n \frac{W}{L} (V_{gs} - V_{th})^2 \end{aligned} \quad (A.57)$$

t is the temperature in degrees Celsius. For this the sub-threshold parameters a and b need to be known. These are determined by measurements $a = 1.7510^{-3}$ and $b = 1.14$. The measurement results are shown in appendix [A.2](#).

Appendix B

The CTAT voltage generator

B.1 Sub-threshold FinFET diode

For a diode like behavior in FinFET technology, an exponential term is needed. The FinFET equation for sub-threshold contains an exponent:

$$I_D = 2 \frac{W}{L} C_g \mu_0 \left(\frac{k_B T}{q} \right)^2 e^{\frac{q(V_{gs} - V_{th})}{k_B T}} [1 - e^{\left(\frac{-q V_{DS}}{k_B T} \right)}] \quad (\text{B.1})$$

When V_{ds} is large this approximates to:

$$I_D \approx 2 \frac{W}{L} C_g \mu_0 \left(\frac{k_B T}{q} \right)^2 e^{\frac{q(V_{gs} - V_{th})}{k_B T}} \quad (\text{B.2})$$

This looks like an equation for a diode current. It is also important what the negative temperature coefficient is and whether a PTAT voltage can be generated.

To get the negative temperature coefficient the derivative of the FinFET voltage in sub-threshold need to be taken to temperature. This is shown in equation B.6.

$$\frac{dV_{gs}}{dT} = \frac{k_B}{q} \ln\left(\frac{I_d}{I_s}\right) + \frac{k_B}{q} \frac{1}{3} + \frac{dV_{th}}{dT} \quad (\text{B.3})$$

In this equation the only factor that is dependent on the device size is:

$$I_s = \frac{W}{L} C_g \mu_0 \left(\frac{k_B T}{q} \right)^2 \quad (\text{B.4})$$

From the derivative can be seen that the gate-source voltage of a sub-threshold FinFET has a negative temperature coefficient. An expression for $\frac{dV_{th}}{dT}$, however is needed.

The positive temperature coefficient is made with the difference in voltage between two diodes that have different current densities.

The current difference is made by different I_s and therefore different device sizes.

$$I_{d1} = I_{d2}$$

$$I_{s2} = nI_{s1}$$

It is assumed that that $\frac{dV_{th}}{dT}$ is device size independent, which means:

$$\frac{dV_{gs1}}{dT} - \frac{dV_{gs2}}{dT} = \frac{k}{q} \left[\left\{ \ln(I_{d1}) - \ln(I_{s1}) + \frac{k_B}{q} \frac{1}{3} + \frac{dV_{th1}}{dT} \right\} - \left\{ \ln(I_{d2}) + \ln(nI_{s2}) - \frac{k_B}{q} \frac{1}{3} - \frac{dV_{th2}}{dT} \right\} \right] \quad (\text{B.5})$$

It is assumed that the threshold voltage for both subthreshold FinFETs is equal. This gives:

$$\frac{d(V_{gs1} - V_{gs2})}{dT} = \frac{k}{q} \ln(n) \quad (\text{B.6})$$

It is thus seen that the positive temperature dependency can be made by using the voltage difference of two sub-threshold FinFETs that have different current densities.

A negative and a positive temperature coefficient can be made using sub-threshold FinFET. A disadvantage of using subthreshold FinFETs is that the gate source voltage needs to be lower then the threshold voltage (lower then 0.3V for a nFinFET at low temperature). The sub-threshold FinFET is diode connected so this means that the CTAT voltage will maximally be 0.3V (1 sub-threshold FinFET is used). This is a disadvantage because it is difficult to use in the averaging part of the circuit.

The diodes will therefore be made by gated pin diodes.

B.2 Diode measurements

A measurement of Salsa 2 gated diode is shown in figure B.1.

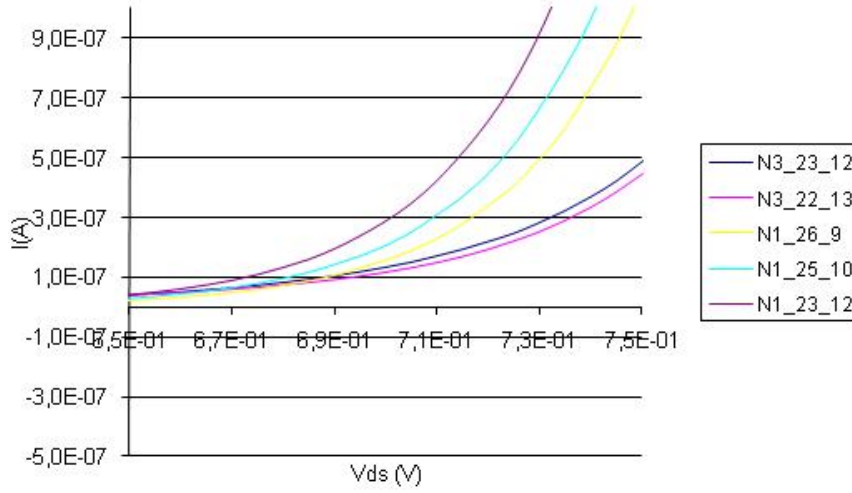


Figure B.1: Gated PIN diode measurements on different sized diodes

In the figure the measured I-V curves are shown for different diode sizes. For all measurement the gate is floating. From these curves the width and length for a certain temperature coefficient and bias current can be chosen.

Also the temperature coefficient a diode has been measured (see figure ??) to verify if the measured temperature coefficient equals the calculated.

The actual diode voltage is approximately 0.58V at 50 °C so the temperature coefficient is approximately -1.85mV/K.

The negative temperature coefficient can be calculated with:

$$\frac{\partial V_{be}}{\partial T} = \frac{V_{be} - (4 + m) \frac{K_b T}{q} - V_g}{T} \quad (\text{B.7})$$

with $E_g = 1.12\text{eV}$ and $m = 1.5$

This equation gives the correct temperature coefficient.

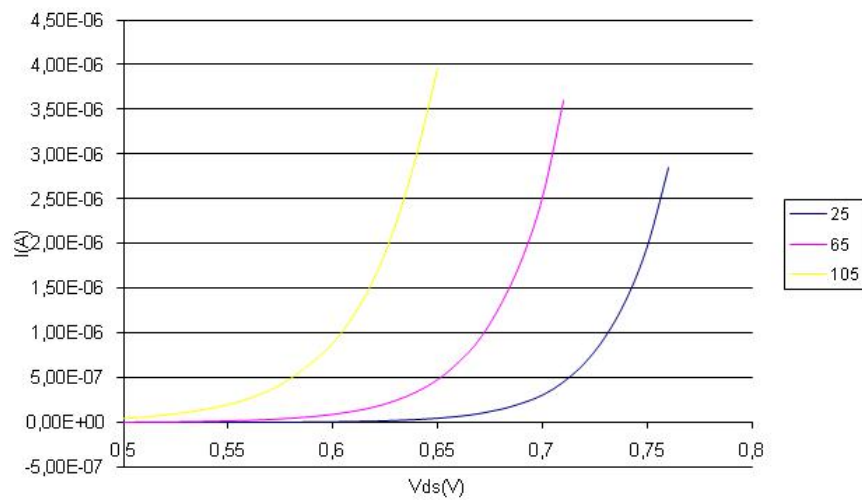


Figure B.2: The I-V curves of a diode for different temperatures

Appendix C

The buffer

C.1 Current ratios error

Because of the large voltage difference over the inputs of the differential pairs (at low and high temperatures) the current ratios in the differential pair will be high. This will give an error on the reference voltage.

This error can be described. Because two OTAs are connected together the current can flow from one OTA to the other. This is schematically shown in figure 4.2.

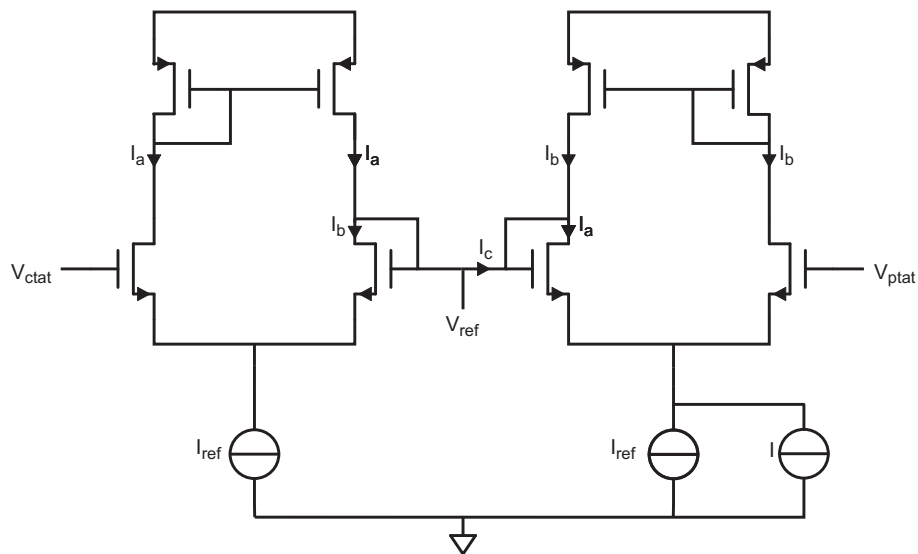


Figure C.1: The circuit of the buffer with the different currents

What is known is that the current source is equal to the added current in the differential pair.

$$I_{ref} = I_a + I_b$$

What is also known is that the current that flows from one OTA to the other is equal to:

$$I_c = I_a - I_b$$

First the error on the reference voltage because of a variation in the current of one stage can be derived by using the small signal equivalent.

From this circuit first a small signal equivalent for one buffer is made. In figure C.2 the small signal equivalent of one buffer is shown.

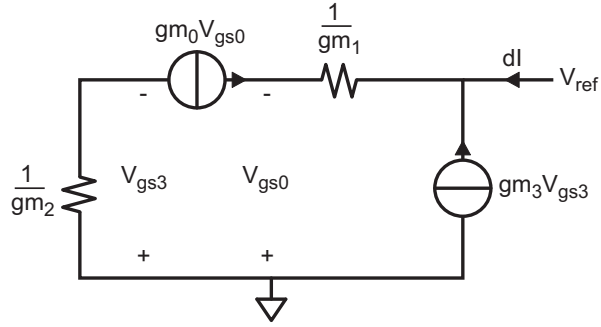


Figure C.2: The small signal equivalent of one buffer stage

The transistors for the current mirror are equal as well as the currents and therefore holds:

$$gm_2 = gm_3$$

This small signal equivalent can be redrawn.

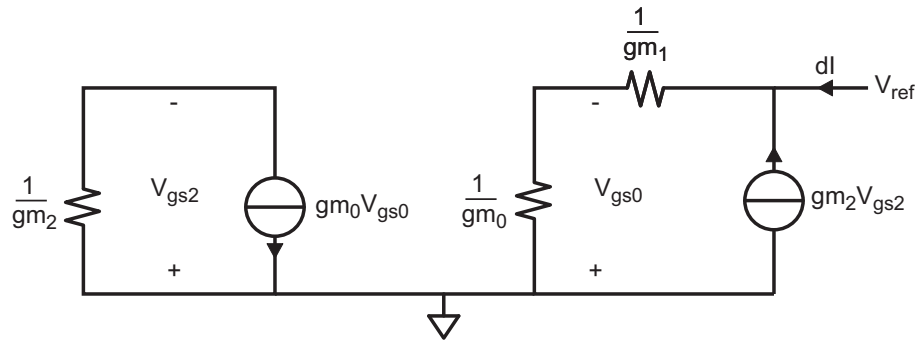


Figure C.3: The small signal equivalent of one buffer stage

From this small signal equivalent equations for the gate source voltage of

transistor 0 and 2 can be given:

$$\begin{aligned} V_{gs0} &= -V_{ref} \frac{\frac{1}{gm_0}}{\frac{1}{gm_0} + \frac{1}{gm_1}} \\ V_{gs2} &= \frac{gm_0 V_{gs0}}{gm_2} \\ &= -\frac{gm_0 gm_1}{gm_2 (gm_0 + gm_1)} V_{ref} \end{aligned} \quad (C.1)$$

The error current of one buffer stage can be expressed:

$$dI = \frac{V_{ref}}{\frac{1}{gm_0} + \frac{1}{gm_1}} - gm_2 V_{gs2} \quad (C.2)$$

Substituting the gate source voltage of transistor 2 gives:

$$dI = \frac{V_{ref}}{\frac{1}{gm_0} + \frac{1}{gm_1}} - \frac{gm_2 gm_0 gm_1}{gm_2 (gm_0 + gm_1)} V_{ref} \quad (C.3)$$

Rewriting this gives the following expression:

$$\frac{V_{ref}}{dI} = \frac{1}{2} \frac{gm_0 + gm_1}{gm_0 gm_1} \quad (C.4)$$

So one buffer section can be seen as a resistor with:

$$R = \frac{1}{2} \left(\frac{1}{gm_0} + \frac{1}{gm_1} \right) \quad (C.5)$$

Now the small signal equivalent of both buffer stages can be described by the previously given small signal equivalent of one stage with the resistor as a load that represents the other buffer stage.

The small signal equivalent of this can be seen in figure C.4. The lower small signal equivalent is a rewritten version of the upper. The transistors for the current mirror are equal as well as the currents and therefore holds: $gm_6 = gm_7$.

From this the gate source voltages of transistors 5 and 6 can be derived:

$$\begin{aligned} V_{gs6} &= \frac{gm_5 V_{gs5}}{gm_6} \\ V_{gs5} &= \frac{-I_3}{gm_5} \end{aligned} \quad (C.6)$$

with:

$$\begin{aligned} I_3 &= I_2 - dI \\ I_2 &= (V_{ref} + V_{gs5}) gm_4 \end{aligned} \quad (C.7)$$

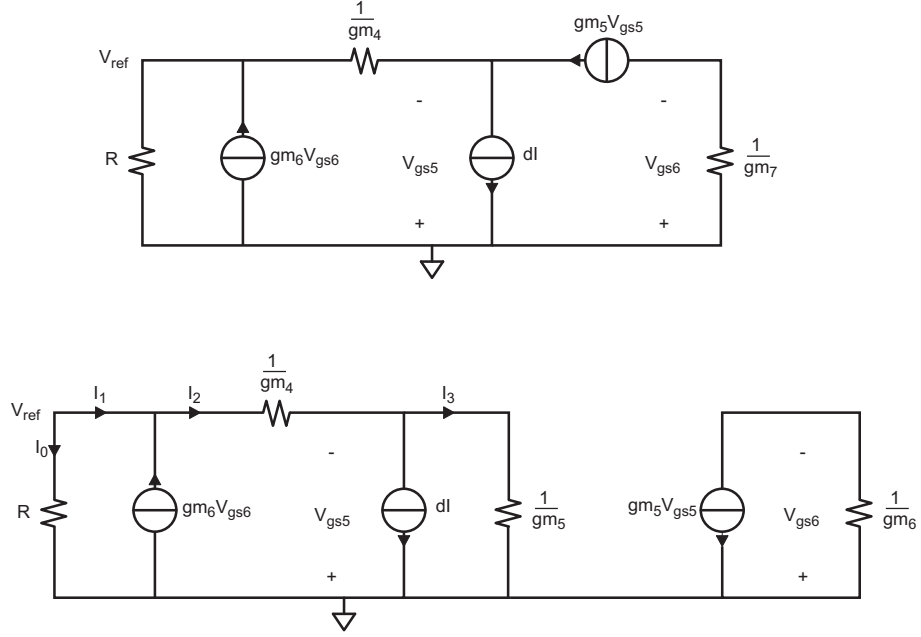


Figure C.4: The small signal equivalent of one buffer stage

Substituting these in equation C.6 gives:

$$V_{gs5} = \frac{-(V_{ref} + V_{gs5})gm_4 - dI}{gm_5} \quad (C.8)$$

$$V_{gs5} = \frac{\frac{-gm_4}{gm_5}V_{ref} + \frac{dI}{gm_5}}{1 + \frac{gm_4}{gm_5}}$$

$$V_{gs5} = \frac{-gm_4 V_{ref} + dI}{gm_5 + gm_4}$$

Now all the gate source voltages are know. The influence on the reference voltage for varying currents can be investigated: For the current I_1 is known:

$$I_1 = -\frac{V_{ref}}{R} \quad (C.9)$$

and

$$I_1 = I_2 - gm_6 V_{gs6} \quad (C.10)$$

$$I_1 = I_2 - gm_6 \frac{gm_5 V_{gs5}}{gm_6} \quad (C.11)$$

$$I_1 = I_2 - gm_5 V_{gs5}$$

In the last equation the previous found equation for I_2 can be substituted.

$$-\frac{V_{ref}}{R} = (V_{ref} + V_{gs5})gm_4 - gm_5 V_{gs5} \quad (C.12)$$

substituting the equation for V_{gs5} and rewriting gives:

$$-\frac{V_{ref}}{R} = V_{ref}gm_4 - (gm_5 - gm_4)V_{gs5} \quad (C.13)$$

Substituting V_{gs5} (equation C.8) gives:

$$-\frac{V_{ref}}{R} = V_{ref}gm_4 + (gm_5 - gm_4)\frac{gm_4V_{ref} + dI}{gm_5 + gm_4} \quad (C.14)$$

Rewriting this to V_{ref} :

$$V_{ref} = dI \frac{\frac{gm_5 - gm_4}{gm_5 + gm_4}}{\frac{1}{R} + gm_4 + \frac{gm_5 - gm_4}{gm_5 + gm_4}} \quad (C.15)$$

Rewriting gives:

$$\frac{V_{ref}}{dI} = \left(\frac{gm_5 - gm_4}{gm_5 + gm_4}\right)\left(\frac{1}{\frac{1}{R} + gm_4}\right) + \frac{1}{gm_4} \quad (C.16)$$

For the matching in the buffer FinFets M0 and M4 have to be equal and have the same current as well as M1 and M5:

$$\begin{aligned} gm_0 &= gm_4 \\ gm_1 &= gm_5 \\ R &= \frac{1}{2}\left(\frac{1}{gm_0} + \frac{1}{gm_1}\right) \end{aligned} \quad (C.17)$$

The previous equation can therefore be simplified:

$$\frac{V_{ref}}{dI} = \left(\frac{gm_1 - gm_0}{gm_1 + gm_0}\right)\left(\frac{1}{\frac{2gm_0gm_1}{gm_0 + gm_1} + gm_0}\right) + \frac{1}{gm_0} \quad (C.18)$$

To simplify the previous equation:

$$\begin{aligned} \frac{dI}{V_{ref}} &= \left(\frac{gm_1 + gm_0}{gm_1 - gm_0}\right)\left(\frac{2gm_0gm_1}{gm_0 + gm_1} + gm_0\right) + gm_0 \\ &= \frac{3gm_0gm_1}{gm_0 - gm_1} + \frac{gm_0^2}{gm_0 - gm_1} + gm_0 \end{aligned} \quad (C.19)$$

This gives:

$$\frac{V_{ref}}{dI} = \frac{1}{gm_0\left(\frac{4gm_1}{gm_1 - gm_0}\right)} \quad (C.20)$$

The intend for this calculation was to find an expression for the error on the reference voltage because of the current ratio. So the gm terms have to be substituted with:

$$\begin{aligned} gm_0 &= \sqrt{2k_n I_a} \\ gm_1 &= \sqrt{2k_n I_b} \end{aligned} \quad (C.21)$$

This gives:

$$\frac{V_{ref}}{dI} = \frac{1}{\sqrt{2k_n I_a} \left(\frac{4\sqrt{I_b}}{\sqrt{I_b} - \sqrt{I_a}} \right)} \quad (C.22)$$

The currents in the differential pair are a ratio from the current source:

$$\begin{aligned} I_a &= (1 - \alpha)I_{ref} \\ I_b &= \alpha I_{ref} \end{aligned} \quad (C.23)$$

This gives:

$$\begin{aligned} \frac{V_{ref}}{dI} &= \frac{1}{\sqrt{2k_n(1 - \alpha)I_{ref}} \left(\frac{4\sqrt{\alpha}}{\sqrt{\alpha} - \sqrt{(1 - \alpha)}} \right)} \\ &= \frac{1}{\sqrt{2k_n I_{ref}}} \frac{\sqrt{\alpha} - \sqrt{(1 - \alpha)}}{4\sqrt{\alpha}\sqrt{(1 - \alpha)}} \\ &= \frac{1}{\sqrt{2k_n I_{ref}}} \frac{1 - \sqrt{\frac{1}{\alpha} - 1}}{4\sqrt{1 - \alpha}} \end{aligned} \quad (C.24)$$

In this equation I_a and I_b are the currents flowing through the branches of the differential pair. When α is a half both branches have an equal current. The limits are α is zero (all current is in I_a) or α is one (all current is in I_b).

For the error on the reference these limits show that when the differential pair is in balance there is no error at the output while most current is in one branch the error becomes very large.

So for the design of the buffer two conditions are important:

- Small current ratio in the differential pair
- Matched current sources (small difference in drain source voltage)

Both conditions have a contradiction, because in the proposed schematic the drain source voltage of the current mirror has to be low (a larger gate source voltage) to have a small current ratio at high or low temperatures. On the other hand when the drain source voltage is low the current sources will not match very well.

This problem can be solved by decreasing the voltage step on the input of the buffer. This can be done by using more buffer stages.