UNIVERSITY OF TWENTE.

M.Sc. thesis

Fabrication and characterisation of cantilever arrays with integrated sharp tips

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Master of science thesis

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Summary

This thesis describes the design, fabrication and characterisation of silicon micro-cantilever arrays with integrated sharp tips. The arrays are developed for parallel readout experiments that are based on electric force microscopy (EFM). The final application of the arrays is in a probe based data storage system.
The high requirements for optical readout and EFM are realised by a SOI based process using sacrificial layer etch technology and a KOH etch combined with a LOCOS process. The powerful process features a single mask to fabricate cantilever arrays with tips that are self-aligned to the free end of the cantilever. A second mask is used for the backside etch, to release the cantilevers. The sacrificial layer etch method enables the fabrication of arrays that are uniform on wafer scale.
An essential aspect for obtaining sharp tips is the inclusion of a sacrificial layer to achieve a sharp mask corner by corner sharpening. Another critical factor is a straight etch profile after pattern transfer of the mask into the device layer.
The fabricated devices are characterised by means of scanning electron microscopy, atomic force microscopy and white light interferometry.

Acknowledgements

By finalising this thesis, my study comes to an end as well. It has been a unique journey, and the master thesis project has been an expedition itself. It included getting familiar with the cleanroom (both the people in it and the technology), dealing with the inconveniences that followed from moving to Carre and the tedious and complicated task of documenting all my findings. Many people have helped me along the way, and I would like to start by thanking the members of my (big) graduation committee: Miko Elwenspoek, Leon Abelmann, Wabe Koelmans, Hammad Nazeer, Meint de Boer and Edin Sarajlic. Thanks to Leon I was able to work on a project tailored to my needs: a great deal of cleanroom work, having a tangible product. I am grateful to Meint for the great amount of time he has put in the technological guidance during this thesis. I want to thank Wabe for being my supervisor. His visits to Zürich forced me to operate more independent. I thank Edin for joining the graduation committee as external member and supporting me in the cleanroom.
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Chapter 1

Introduction

This MSc thesis deals with the design, fabrication and characterisation of arrays of silicon micro cantilevers with integrated sharp tips for application in a probe based data storage system. In this introductory chapter the subject of the thesis is outlined. The chapter starts with a brief overview of the progress in the field of data storage followed by an introduction of probe based data storage systems. Furthermore, arrays of micro cantilevers with tips used in probe storage and various methods for the readout of cantilevers are discussed. The chapter concludes with the motivation and the goal of this project.

1.1 Data storage systems

The ongoing advances in, for example, multimedia applications lead to a constant growth in file size to accommodate the vast amount of data. This results in a demand for ever higher storage capacity of digital data and thereby increasing density demands of data storage devices.

Data storage systems can be categorised into volatile and non-volatile memory. Volatile memory requires power to preserve the stored information, while non-volatile memory does not. Advantages of non-volatile memory are the low cost per bit and high storage capacity. Non-volatile memory can be subdivided into two types: mechanically addressed memory and electrically addressed memory. Mechanically addressed systems use one or more heads for reading and writing data on a storage medium. Electrically addressed memory stores data in wired elements using electric charge or magnetism, hence avoiding moving elements.

The hard disk drive is an example of mechanically addressed memory. Its data density is very high: currently a commercially available 1TB hard drive has an average areal density of 330Gb/inch^2 [1]. Fundamental limits (like the superparamagnetic limit in magnetic recording) impose a limitation on areal density. For magnetic data storage as used in hard disk drives this theoretical limit is estimated to be around 100Tb/inch^2 [2]. This is why there is a need for a new type of storage system capable of ultra high density.

To compete with electrically addressed memory, the read access time of mechanically addressed memories needs to be reduced. Downscaling the elements results in higher resonance frequencies, enabling higher speeds and reduced access times. A promising type of mechanically addressed memory is probe based data storage. Parallel read and write heads enable high data speeds while ultra high capacity is realised by reducing the size of these heads.

1.2 Probe based data storage

Inspired by the invention of scanning probe microscopy (SPM) and the development of atomic force microscopy (AFM) [3], probe based storage systems use sharp tips for writing and reading data. Since the spatial interaction determines the data density, nanometer-sharp tips are key to ultra high density. Probes of this size fall within the category of microelectromechanical systems (MEMS).

1.2.1 Readout of probes

To read back the data from the probes, various methods are available. These can be divided into two types: integrated and external readout. Integrated readout operates with a sensor placed onto the probe, which is usually included in the fabrication process. External readout on the other hand is physically separated from the probe. Both methods use the deflection of the cantilever for readout. Piezoresistive (an example of integrated readout) and optical (an example of external readout) readout are shortly described in the following paragraphs.

Integrated readout

Deflection of a probe can be detected using a sensor integrated in the probe. A common type of integrated readout is the piezoresistive element [4]. This kind of sensor is for example applied by LG in a cantilever array [5]. A piezoresistive element experiences a change in electrical resistance when mechanic stress is applied. This stress is induced by the deflection of the probe, since the piezoresistive element follows the shape of the bent cantilever. Devices capable of measuring strain are also called strain gauges. A schematic illustration of this principle is presented in Figure 1.1. In case of multiple cantilevers every cantilever needs to be equipped with such a piezo element. There are several downsides to the use of piezoresistive elements. Production of the elements, especially at micro-scale, is difficult. Electrical connections have to be incorporated towards every element, which contributes to a complex design.

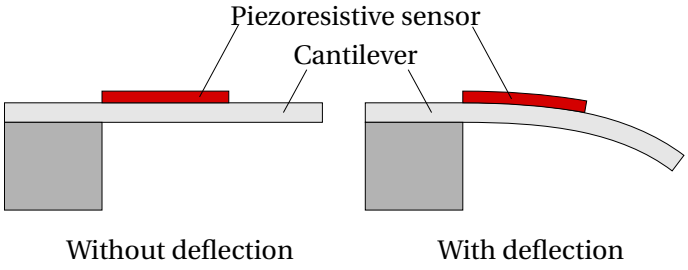


Figure 1.1: Schematic representation of piezoresistive readout of a single cantilever

The Millipede [6] from IBM is an example of a probe based storage system with integrated readout. This system consists of MEMS-based arrays of cantilevers in combination with a polymer storage medium. The tips of the cantilevers are used to thermomechanically read and write data in the polymer film by means of indentations [7]. The strong point of this system is the cantilevers working in parallel, all covering an individual region. This way an increase in read/write speed is feasible. A drawback of the thermomechanical readout is the limit it imposes on the speed. When a cantilever is used as a thermal readback sensor, pulses are used to heat the resistor and a difference in cooling distinguishes indentations from non-indentations. This cooling-cycle is the restriction responsible for the speed limit.

External readout

In AFMs the deflection of the single cantilever is generally measured optically, which is an external readout method. Laser light is directed to the free end of the cantilever, reflected off the cantilever and captured by a position sensitive detector (PSD). This PSD usually consists of two or four photodiodes, each generating a current that is dependent on the amount of incoming light. Figure 1.2 schematically shows optical readout of a single cantilever. This optical readout method is known as the optical lever and is described in [8]. Advantages of optical readout are simplicity of the cantilevers, the high speed and the non-invasive nature. A disadvantage is the need for alignment of the laser spot with the cantilever after which the reflected spot needs to be aligned to the centre of the detector.

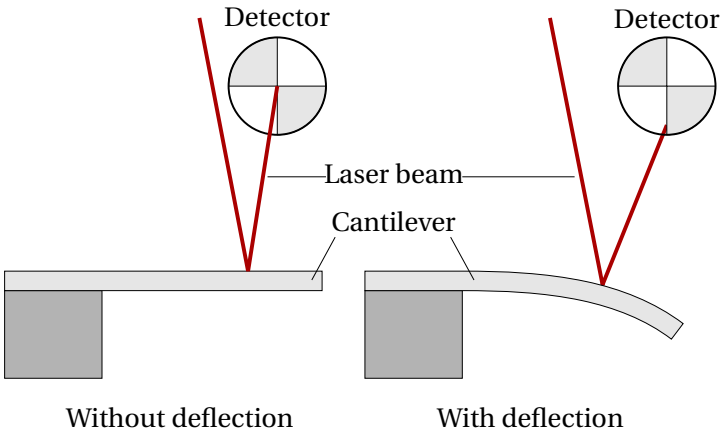


Figure 1.2: Schematic representation of optical readout of a single cantilever

Within the micro scanning probe array memory (μSpam) project[1] the transducers science and technology (TST) group is working on probe based storage. By studying several elements of probe storage, such as optical readout, the group also participates in the probe-based terabit memory (ProTeM) project[2].

The ProTeM project aims for the development of techniques and systems for ultra-high capacity memories. The project has a particular focus on archival applications. An important feature of archival systems is their reliability, even when a part of the system fails or breaks down. Imagine a probe array with the readout integrated in the cantilevers. When such an element breaks down, readout of the cantilever is no longer possible. Because the sensor is incorporated in the cantilever (situated only tens of nanometers above the medium), replacement is certainly not straightforward. Separating the readout element from the information part facilitates replacement of the readout system. This concept is known as “cold redundancy”. Its principle is similar to a DVD system: when the DVD-player breaks down, the information is nevertheless safely stored on the disc and can be retrieved by replacing the malfunctioning player. The importance of reliability is the motivation for studying external readout, and optical readout in particular, within the ProTeM project.

[1] http://www.uspam.nl
[2] http://www.protem-fp6.org

1.3 Parallel optical readout

To perform optical readout of an array of cantilevers instead of a single cantilever, a slightly different approach is needed. Equipping each cantilever with a light source and detector may be realisable with small amounts of cantilevers, but is not an option when larger arrays are involved. Another problem is the potential interference of light when cantilevers are placed close together.
Optical readout of an array of eight cantilevers is reported in [9]. This is achieved with eight light sources and optical sensors, each cantilever fitted with an individual combination. The light sources, which are lasers, are controlled in a time-multiplexed fashion.
In [10] parallel optical readout of multiple cantilevers is reported. One light source and a single detector are used for readout of an array of three cantilevers operating in dynamic mode (vibrating the cantilever near its resonance frequency) [11]. Frequency separated cantilevers without tips are used to successfully detect the resonance frequency shift of one cantilever within the array. These cantilevers are created out of a single cantilever by focused ion beam (FIB).

1.3.1 Scope of this thesis

The goal of this MSc project is to develop a process scheme for the fabrication of arrays of multiple cantilevers with integrated sharp tips. In contrast to the cantilevers without tips, such arrays can be used in experiments based on electric force microscopy (EFM) to investigate parallel readout of multiple cantilevers more thoroughly. A sketch of a cantilever array combined with optical readout for use in probe based data storage is presented in Figure 1.3. Five cantilevers with tips at their free ends are placed in parallel above a recording medium. An elongated laser spot is used to detect the deflection of all five cantilevers. The number of cantilevers is not predetermined and is five for illustrative purposes only.

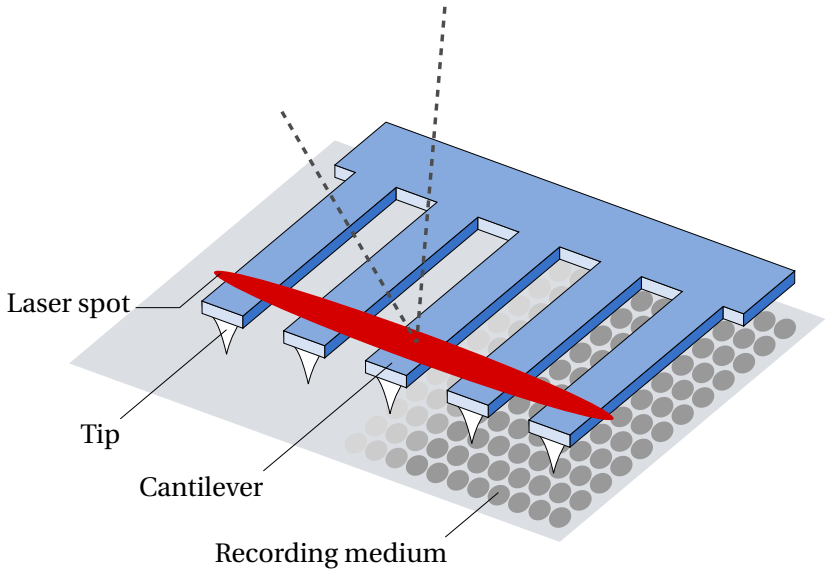


Figure 1.3: Schematic representation of cantilever array with optical readout

In order to satisfy the requirements following from, for instance, the readout method, sophisticated use of silicon micromachining is required. Silicon micromachining offers great flexibility in array design. Variations in for example length, width, shape, spacing and number of cantilevers can be

incorporated in the design.
This thesis can be roughly divided into four parts. First, in Chapter 2, the requirements of the devices are defined and the complete process scheme is fully designed. After this, Chapter 3 deals with the fabrication of the cantilever array. Following the fabrication, the devices are characterised in Chapter 4, in order to check whether the requirements are met. Finally, in Chapter 5, the conclusions of the project are discussed and recommendations are given.

Chapter 2

Design

In this chapter, specifications of the device are defined. Three components can be considered within the device: the tip, the cantilever and the cantilever array. Once the requirements are defined, an introduction into tip manufacturing is given and potential ways to fabricate tips are described. When the most suitable method of fabrication is determined, the relevant aspects of the fabrication method of tip, cantilever and array are discussed.

2.1 Specifications

In this chapter, the specifications are defined which are needed to develop the device. The part of the array depicted in Figure 2.1 indicates length L, width w and thickness t of a cantilever. The bending direction of the cantilevers is demonstrated by the arrow. Another important parameter, the spacing S between cantilevers, is also indicated.

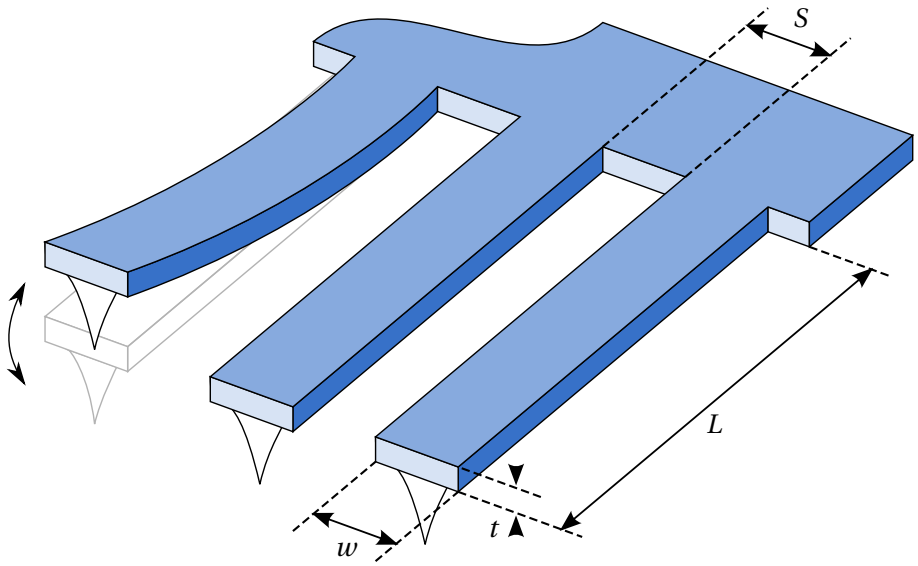


Figure 2.1: Part of cantilever array showing parameters: S = spacing, w = width, t = thickness, L = length. The cantilevers can bend in vertical direction as indicated.

2.1.1 Electric Force Microscopy (EFM) requirements

As mentioned in Chapter 1, the micro-cantilever arrays will be used for experiments based on EFM, to investigate parallel readout of multiple cantilevers. In EFM, a conductive AFM tip interacts with a sample through long-range Coulomb forces. When a difference in potential is applied between tip and sample, the vertical gradient of the electric field can be mapped by monitoring the oscillation amplitude and phase of the cantilever. Within the parallel readout experiments, a single voltage is applied to all the cantilevers within the array. With regard to EFM, the following demands need to be fulfilled.

Tip requirements In EFM it is common to model the tip as a mesoscopic cone with opening angle ϕ and tip apex radius r_{tip} [12]. The model for an EFM tip is presented in Figure 2.2. The resolution in EFM depends on the probe tip radius. High resolution EFM measurements require tips with a radius of curvature below ~100nm. Moreover, a small cone opening angle results in improved EFM results. This is because with a small opening angle, the base of the tip is more narrow, resulting in a smaller amount from the base to the EFM signal. No explicit tip height follows from the requirements of non-contact EFM, but common values are in the order of micrometers.

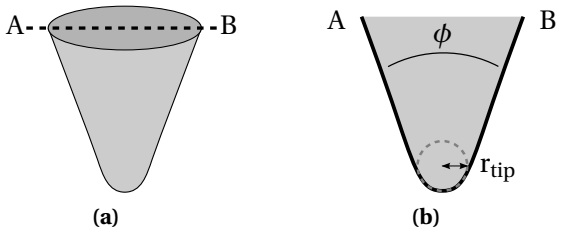


Figure 2.2: Model as used in EFM: the tip is a cone with opening angle ϕ and apex radius r_{tip}. (b) is a cross section along the line $A-B$ in (a)

Cantilever requirements Non-contact EFM operates in dynamic mode, in which the cantilever is vibrating near its resonance frequency. The amplitude of this oscillation is in the order of tens of nanometers. The resonance frequency needs to be compatible with the AFM and the experimental setup and therefore is required to be between 50 and 300kHz. The spring constant of EFM probes is usually around 3N/m, but EFM probes with a spring constant of 40N/m exist as well.

Array requirements To be able to apply a potential to the tips, the cantilevers and tips need to be electrically conductive. A probe resistance of 350Ω is mentioned in [13], aimed for higher-resolution measurements of electric characteristics of specimens. Matching this value is not required, since for the parallel readout experiments no extremely high resolution or measurement speed is required. This means the parallel readout experiments can be performed with arrays having a higher resistance.
When an EFM tip is separated more than 10nm from the sample, the electrostatic force is larger than the van der Waals force (VdW), as can be seen in Figure 2.3. Usually for non-contact EFM, the vibrating tip is situated between 10 and ~100nm above the sample. At said distances, the tip-sample separation of all tips is required to be smaller than tens of nanometers. The variation in tip-sample separation within an array is illustrated in Figure 2.4. A micro-cantilever array should have a variation in tip-sample distance of less than 100nm to be suitable for EFM experiments. If

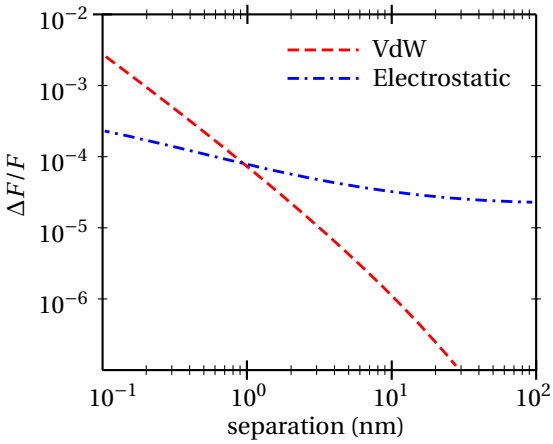


Figure 2.3: Computed distance dependence of normalised frequency shift. Parameters used: tip radius = 10 nm, tip oscillation amplitude = 20 nm, cantilever spring constant = 30 N/m, potential difference between tip and sample = 1V. Graph is taken from [14]

this high requirement is met, all tips can be placed within 10 to 110nm from the sample. From Figure 2.3, it can be seen that the frequency shift due to the electric field gradient at a distance of 10nm is almost the same as 100nm from the sample.

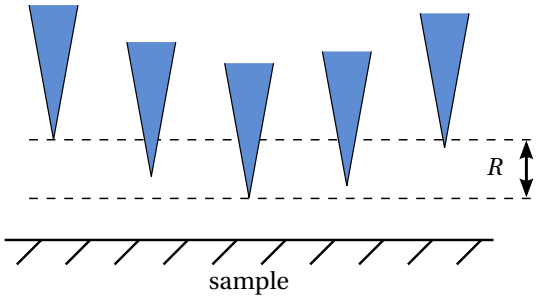


Figure 2.4: Array of tips above a sample. The variation in tip-sample distance R must be smaller than 100nm for EFM.

2.1.2 Parallel optical readout requirements

Considering the parallel optical readout of cantilever arrays, more requirements need to be satisfied.

Tip requirements For operation, chips are placed with a certain mount angle α between the plane of the sample and the cantilever axis. In the AFM, α is 10°and in the experimental parallel optical readout setup, α is 4°, but can be adjusted if needed.
Given a tip height h_{tip} of, for example 5µm, this means the distance d from the end of the cantilever must be below 28µm to prevent the cantilever from touching the sample. In Table 2.1, the allowed distance d is listed for a tip height from 1 to 10µm. These values are calculated using $\alpha = 10°$ (the mount angle of the AFM).

Cantilever requirements With regard to calculations (for example equation 2.2–2.7), it is convenient if the cantilevers have a simple shape. Rectangular cantilevers for example simplify the

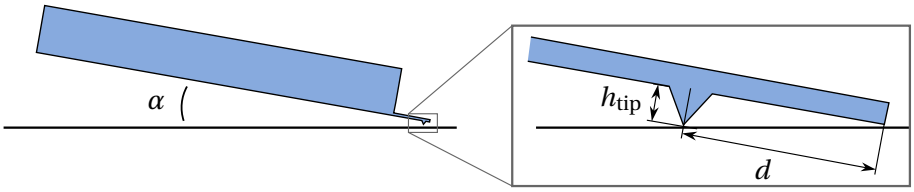


Figure 2.5: Schematic side view of chip above a sample. In the AFM, α is 10°.

Table 2.1: The allowed distance d from the end of the cantilever depends on tip height h_{tip}:

h_{tip} (µm)	1	2	3	4	5	6	7	8	9	10
d (µm)	5.7	11.3	17.0	22.7	28.4	34.0	39.7	45.4	51.0	56.7

calculations. Also, the shape must be equal for all the cantilevers within one array.

Array requirements The elongated laser spot has a length of a few centimetres. Using this laser spot, arrays having a width of several centimeters can be completely covered. The detector limits the width of the array, because it is roughly 1cm. Since small arrays of no more than 1mm will be fabricated, the width requirement originating from the detector is easily satisfied.

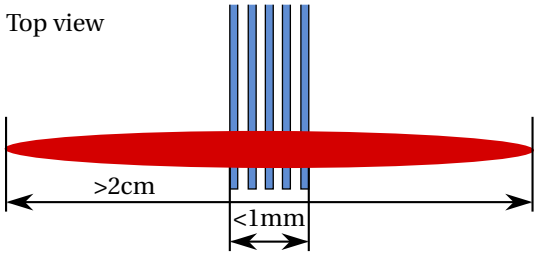


Figure 2.6: The length of the elongated laser spot exceeds the width of the arrays needed for the experiments

The detector needs a certain amount of light, which must be reflected from the cantilevers. For this demand, the cantilever area and reflectivity are of importance. Also, every cantilever needs to reflect an equal amount of light. So the cantilevers are required to have identical areas and only differences in bending between cantilevers within 10% are allowed. No specific area requirements can be given, but we believe that the experiment will be successful if standard sized cantilevers (length ± 225µm, width ± 30µm) are used.

2.1.3 Overview of requirements

The requirements specified by EFM and parallel optical readout lead to a set of demands for the micro-cantilever array, listed in Table 2.2.

2.2 Fabrication concepts

The specifications listed above result in very high requirements for a micro-cantilever array. The most critical requirements are the variation in tip-sample separation, which must be smaller than

Table 2.2: Specifications of cantilever array

Parameter	Specification
chip size (see section 2.2.8)	1.6 × 3.2mm
mount angle (in AFM)	10°
mount angle (in experimental setup, adjustable)	4°
tip radius	< 100nm
tip height (at 5µm from cantilever end)	> 1µm
variation in tip-sample separation	< 100nm
cantilever width (indication)	~ 30µm
cantilever length (indication)	~ 225µm
cantilever thickness (indication)	~ 3µm
resonance frequency	50 – 300kHz
spring constant	2 – 40N/m
number of cantilevers per array	1 – 30
array width	< 1mm

100nm, and the tip radius that is required to be under 100nm. Arrays meeting the specifications are not commercially available, and no standard fabrication procedure is available to manufacture them. We will present a new process flow to fabricate arrays that meet the high demands.
Within the design of the cantilever array, three components can be regarded: the tip, the cantilever and the array. First an introduction to the manufacturing of tips is presented.

2.2.1 Introduction to tip manufacturing

Two main technologies to produce sharp tips can be distinguished: direct and indirect. The indirect or moulding method uses a Si substrate with inverted tips: pits shaped like the desired tips. These holes are filled with a material, after which the Si is completely etched away, leaving only the cantilevers and tips. An example of the indirect method can be found in [15]. The authors bond Si wafers to glass wafers to build cantilever arrays. The cantilevers are shaped by use of photolithography and dry etching. Tips are created by using inverted pyramidal pits and filling these. The process of wafer bonding is not trouble-free so for the sake of feasibility this should be avoided within this project.
In the direct method, material surrounding a mask is etched in such a way that tips remain. An example of cantilevers with tips using the direct method is found in Lutwyche et al. [16], in which they start with the creation of tips by isotropic etching. These are then protected by a thick photoresist layer, so that the cantilevers can be shaped by dry etching. A problem with this method can be the uniformity. Deviations caused by lithography can cause tip height differences. Saya et al. [17] apply anisotropic etching to create triangular cantilevers. The shape of the cantilevers can unfortunately not be changed due to the anisotropic fabrication method. The disadvantage of triangular shaped cantilevers is that the number of cantilevers that fit in an array (with a restricted width), is limited by the triangular shape. The arrays do show a good uniformity regarding tip height.
The following paragraphs are used to describe the benefits and drawbacks of two different types of direct tip fabrication. From the available alternatives, one type is chosen to be implemented in the probe design. The most suitable method will follow from the requirements and will be a compromise between a perfectly sharp tip and the simplicity of the fabrication procedure.

2.2.2 Method I: spire shaped Si tips by isotropic etching

A very straightforward way to make tips is by using masks that are shaped like circles. After isotropic etching spire shaped tips are formed underneath the masks. The amount of underetch needed depends on the radius of the mask. This concept is illustrated in Figure 2.7. A similar method is for example used for the fabrication of tips in [16, 18, 19]. The symmetrical nature of these tips is an advantage for practical use. Apart from isotropic etching, anisotropic etching is used as well to form tips of this type [20, 21].

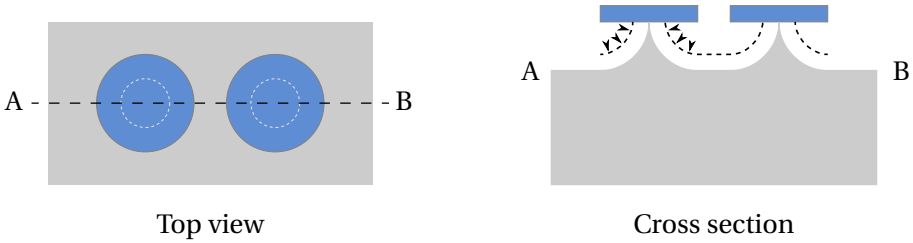


Figure 2.7: Method I, spire shaped tips by isotropic etching

Although the simplicity of this technique is very appealing, obtaining uniform results is difficult. Despite the fact that identical circles are required to obtain similar tips, the actual mask shapes never are perfectly circular at the nanometer scale (due to mask fabrication by laser lithography) and thereby not uniform. A mask with a certain radius will produce higher tips than a mask with a smaller radius. This is due to the isotropic etch, which causes a fixed amount of Si to be etched starting from the edge of every mask. Figure 2.8 elucidates this situation. Only if indistinguishable copies of mask shapes can somehow be created and if every step in the fabrication process is perfectly uniform, this method will generate uniform tips. Patterning by laser lithography will inevitably result in differences in mask shape. As mentioned earlier, non-uniformities in fabrication, like difference in etch rate, are inevitable on wafer scale. If this method is used, a way to integrate the tips with an array of cantilevers has to be developed. Related to the integration, alignment of the tips at a fixed distance from the free ends of the cantilevers is complicated.

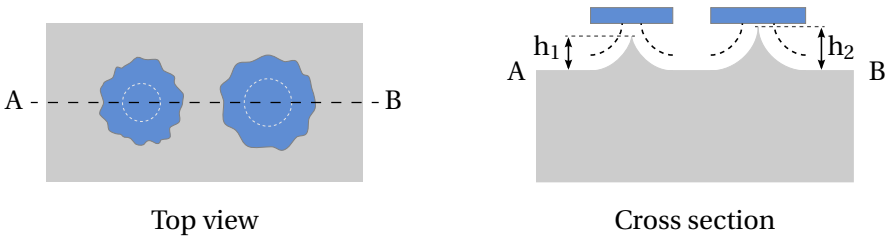
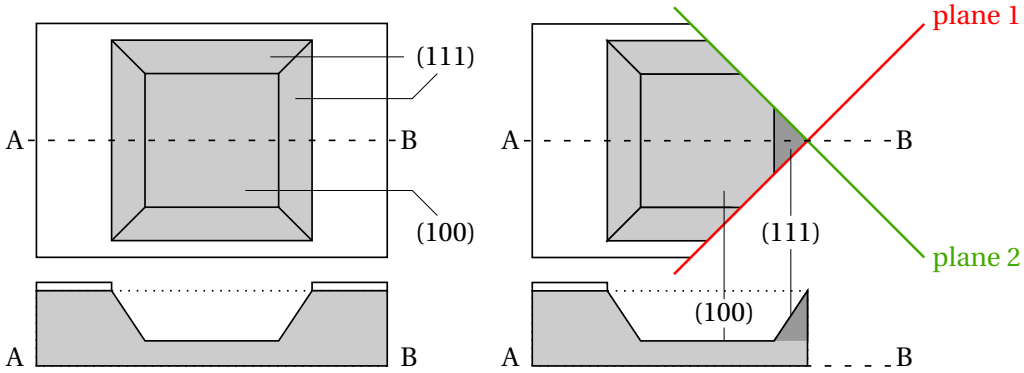


Figure 2.8: Difference in tip height due to dissimilar mask size. The tip created by the larger mask is bigger than the one created by the smaller mask ($h_2 > h_1$)

2.2.3 Method II: tetrahedral Si tips by KOH etching

Another way to define the shape of a tip is by anisotropic etching. The (111) plane resulting from a KOH etch of a Si (100)-oriented wafer, is used as one of the sides of a tetrahedral tip (the tip is actually semi-tetrahedral but is nevertheless referred to as tetrahedral in this report). Albrecht et

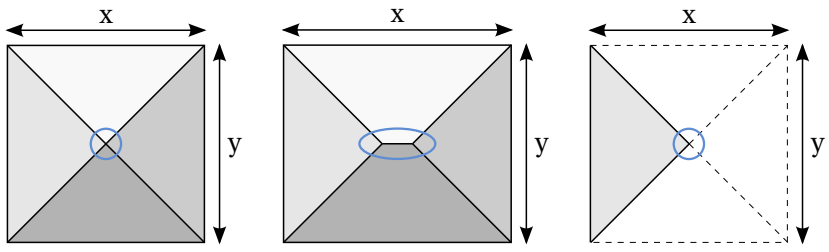
al. apply this in a process to manufacture "SiO_2 cantilevers with integrated tetrahedral tips" [22]. A similar method is described more detailed in a publication by Kitazawa et al. [13]
Figure 2.9a shows the result of an anisotropic wet etch in KOH, using a mask with a square opening. The (100) plane and two of the four (111) planes are indicated. Suppose two vertical planes are introduced, like in Figure 2.9b. Because of the intersection with the Si, a tip becomes evident (it is indicated by a darker colour). This tetrahedron shaped tip has one side confined by plane 1, one side confined by plane 2, and the other side formed by the (111) plane. The (111) plane creates an angle of 54.74° with the (100) plane.



(a) Anisotropic etch **(b)** Tip confined by three planes

Figure 2.9: Method II, tip by anisotropic etching of Si. The two lower schematics are cross sections along the lines A-B indicated in the top views above. (a) The result of a KOH etch. (b) Tip (darker coloured) confined by plane 1, plane 2 and the (111) plane

The beauty of a tip having an apex confined by three planes, is the single point at which the planes intersect. When used as a probe, it is very convenient that the apex results in a single point. This is not always the case: think of a tip confined by four planes (a pyramidal tip) for example. A square mask will ideally produce a point apex (Figure 2.10a shows a top view). But due to laser writing, it is rendered into a rectangle rather than a square, resulting in the apex to be like a knife edge (Figure 2.10b) [23]. Figure 2.10c illustrates the single point formed at the apex of a tetrahedral tip. This illustration shows this type of tip is in fact a quarter of a pyramid.



(a) Square **(b)** Rectangle **(c)** Quarter of square

Figure 2.10: The shape of any apex is defined by the intersecting planes. (a) A perfect square (x = y) results in a pyramidal tip with one cross point. (b) A rectangle (x > y) produces a knife edge apex. (c) One quarter of a perfect square (x = y) gives rise to an apex confined by three planes, ensuring a single cross point

This method of fabrication has the advantage of producing nearly identical tips on wafer scale

because of the uniform nature of the KOH etch (the uniformity is ±4% on wafer scale). The etch rate in the ⟨100⟩ direction is about 80 times larger than in the ⟨111⟩ direction when 25% KOH @75°C is used [24]. The slow rate, at which the (111) plane is etched, is the mechanism responsible for reducing the tip height. Since this etch rate is uniform (±4%) over the complete wafer, no significant variation in tip height is expected: tips of 5µm high will have a maximum variation of ~8.7nm on wafer-scale. Because the variation scales with the etch time and thus with the tip height, lower tips will have less variation in tip height.
Two methods to fabricate tips have been described. Method I is interesting because of its simplicity, but getting uniform tips will be difficult. Method II produces uniform tips with a single point apex. Considering the importance of tip height uniformity within the arrays, method II is needed. In the following section the fabrication method is described in more detail.

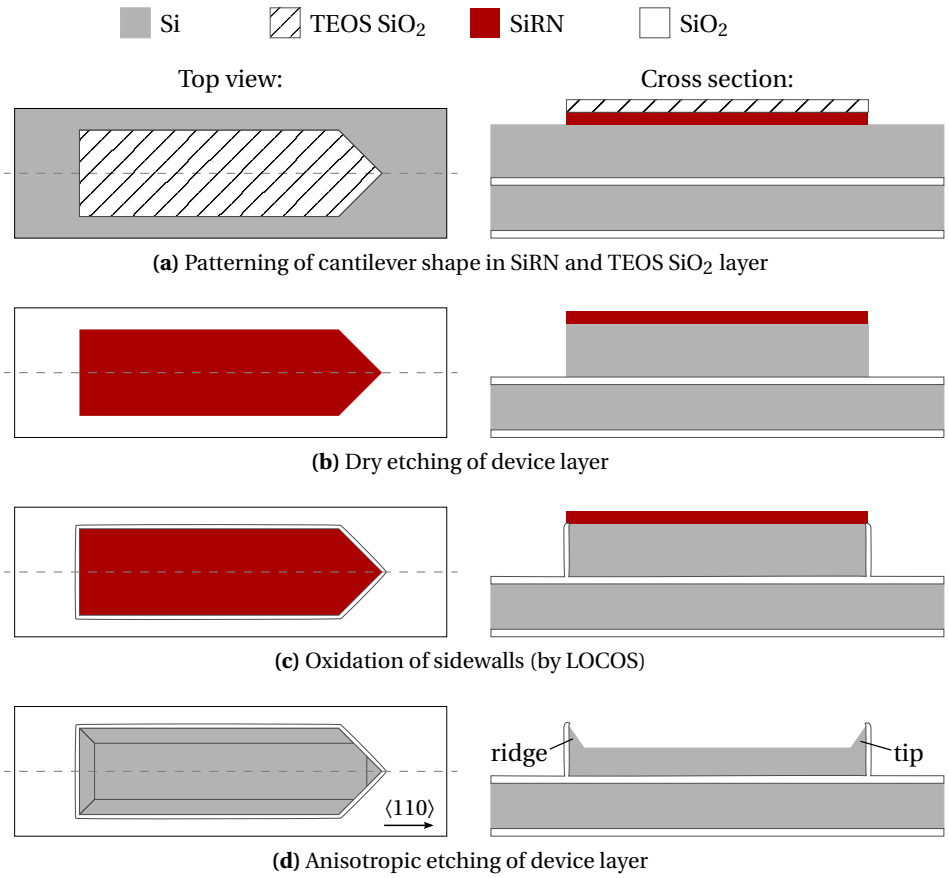
2.2.4 Integration of tip on cantilever using KOH

To construct cantilevers with identical dimensions, we have chosen for a silicon on insulator (SOI) based process. The use of a SOI wafer has advantages considering uniformity in tip height, uniformity in cantilever thickness, uncoupling of cantilevers and chip isolation. These advantages are discussed in more detail in the corresponding sections in this chapter.
SOI wafers have a layered silicon-insulator-silicon configuration. The insulator material is SiO_2 and has a thickness of 0.5µm. Because both sides of this layer are facing Si it is called buried oxide (BOX). As shown in Figure 2.11, the device layer is 10µm and the handle layer is 380µm in thickness. Table A.1 in the Appendix shows all the properties of the type of SOI wafer that is used.
For a spring constant of 3N/m, a cantilever thickness of roughly 3µm is needed (calculated using the Matlab code in C.1.1 for a length of 225µm and a width of 30µm). This means a device layer thickness of 6µm would be ideal. This way, cantilevers with tips having a tip height of 3µm can be fabricated. But because SOI wafers with a device layer thickness of 6µm were not available within the TST group, it was decided to use the available SOI wafers with a device layer thickness of 10µm. The device layer is highly doped single crystal Si and has a resistivity of $0.01 - 0.02\Omega$cm. For a cantilever of 225µm long, 30µm wide and 5µm thick, this means the resistance is between 15kΩ and 30kΩ.

Figure 2.11: Schematic representation of SOI wafer with dimensions

On the backside of the wafer, a layer of SiO_2 similar to the BOX is present. This is due to the fabrication process and also reduces bending of the wafer (bow) caused by stress. In case of an (extreme) wafer bow of ~130µm, the bow over a 200µm wide array is only ~0.5nm (as will be shown in section 4.3.1). The crystal orientation of the wafer is (100), meaning the top surface of the wafer is aligned with the (100) face.
On top of this wafer, a layer of silicon rich nitride (SiRN) and a layer of Tetraethyl Orthosilicate (TEOS) SiO_2 are created in the shape of the cantilever (Figure 2.12a). The device layer is etched using the TEOS SiO_2 as mask, resulting in a mesa (Figure 2.12b). Next, the sidewalls are oxidised,

while at the top of the mesa oxidation is prevented by the nitride cap (Figure 2.12c), a process called local oxidation of silicon (LOCOS). After removal of the SiRN, an anisotropic KOH etch thins the device layer and forms the upward pointing tip (Figure 2.12d).



(a) Patterning of cantilever shape in SiRN and TEOS SiO_2 layer

(b) Dry etching of device layer

(c) Oxidation of sidewalls (by LOCOS)

(d) Anisotropic etching of device layer

Figure 2.12: Concept of fabrication method of cantilever with integrated tip

An advantage of using the direct KOH method in combination with LOCOS is that the tips will always be self-aligned at the exact free end of the cantilever. This is convenient, as alignment errors between tip and cantilever are now prevented, ensuring the tip is always located on the cantilever. Additionally, the distance between self-aligned tip and the free end of the cantilever is equal (i.e. zero) for every cantilever.

Using a cantilever thickness of 3µm in combination with a device layer thickness of 10µm, results in a tip height of 7µm. Together with the tip, a ridge with a similar height will be present (as will be explained in section 2.2.7). To reduce the influence of the ridge on the mechanical behaviour, a low ridge is required, which can be achieved by a shorter KOH etch. But for good EFM performance, the tip-apex is required to be separated from the cantilever several (>1) micrometers. With a tip height of 5µm, the separation between the tip apex and the cantilever is sufficient. The height of the ridge will also be 5µm (equal to the cantilever thickness), which will result in minor influence on the mechanical behaviour.

2.2.5 Material selection

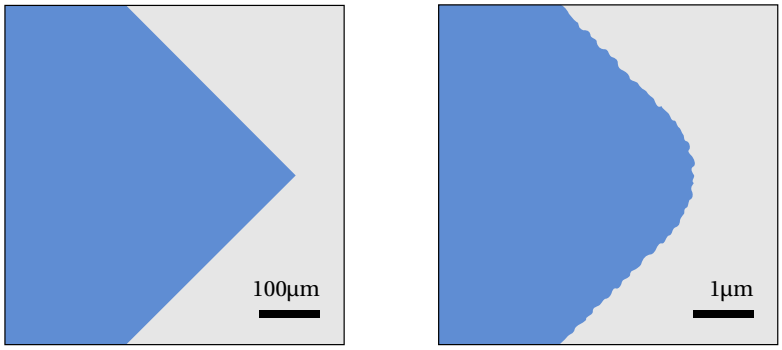
The direct KOH method demands mono-crystalline Si to be used as material for the tip. An advantage of the fabrication method is that the cantilever is formed at the same time the tip is formed. This means the cantilever material is also mono-crystalline Si. Si is used commonly for the fabrication of cantilevers, because of its good mechanical properties.
The motivation for the choice in material supporting the fabrication comes mainly from the specific processes used for the fabrication steps as described in section 2.2.4. TEOS SiO_2 is a suitable material to be used as mask for cryogenic RIE. LOCOS involves the use of silicon nitride as mask. SiRN is chosen as deposited material because of its low stress compared to Si_3N_4. For etch masks for KOH both silicon nitride and SiO_2 are suitable. Silicon nitride is hardly etched (<1nm/hour) while SiO_2 is etched with approximately 180nm/hour. Because it can be easily selectively grown by means of LOCOS, SiO_2 is used as mask.

2.2.6 Sharp tip by KOH etching

Assuming the tip is formed by three planes, it will be very sharp at the end. But unfortunately, the tip will not be as perfect in real life as the tip is in theory. To create a sharp tip, two conditions are important: (I) a sharp corner in the (TEOS SiO_2) mask and (II) a straight etch profile in the top part of the device layer (close to the future tip apex).

Pattern transfer for a sharp tip

To obtain a sharp tip, the corner at the free end of the cantilever as seen from above needs to be sharp. But technical limitations of the lithography manufacturing cause deviation from a sharp corner. When this corner is not sharp, the apex of the tip results in an edge rather than a single point. And because there will be irregularities along the corner, there will be multiple non-uniform tips located on the edge. Our optical contact (1:1) lithography has a resolution of 1µm, making the corner at the free end of the cantilever appear round at micrometer level. In Figure 2.13 this effect is schematically illustrated. Furthermore, the reflow of the photoresist during the post-exposure bake increases the corner rounding effect. In order to keep the corner rounding as small as possible, this bake step can be omitted. But performing the post-exposure bake will have the advantage of reducing standing waves and irregularities in the pattern outline. If there is a way to get around the corner rounding effect, the downside of the post-exposure bake is avoided and the advantages remain.
Because this corner rounding effect will significantly decrease the uniformity of the tips, a way needs to be found to avoid rounded corners. A way to overcome the rounding effect is found in the inclusion of an extra layer which is used to retract the underlying layer by deliberate under-etching (see Figure 2.14).
The transformation from a rounded to a sharp corner is schematically illustrated in Figure 2.14. A stack of SiRN, TEOS SiO_2 and SiRN is covered by a layer of photoresist. After patterning this layer, the corner rounding effect leads to a rounded corner. Dry etching transfers the rounded corner into the top SiRN layer. This top SiRN layer is used as a hard mask and will be removed later. During a wet etch, the conversion from a rounded to a sharp corner is established by under-etch of the TEOS SiO_2 layer. Finally, the top SiRN can be removed and the bottom SiRN layer can be etched so it conforms to the shape of the TEOS SiO_2 mask.
The principle behind this method is closely related to convex corner preservation, which is illustrated in Figure 2.15. Due to convex corner preservation, a sharp convex corner is maintained when



(a) (b)

Figure 2.13: Corner transferred into photoresist by lithography presented schematically at different scales (top view) (a) The corner looks sharp (b) Shown in a magnified view rounding is visible

etched isotropically [18]. Isotropic etching has a uniform speed independent of direction. So the envelope of the original corner (*A* in Figure 2.15) is copied into the etched shape (*B* in Figure 2.15).

The principle of convex corner preservation does not apply in case of a rounded convex corner. Instead, the radius of the rounded corner is reduced. Again the envelope of the original corner (*A* in Figure 2.16) is copied into the etched shape (*B* in Figure 2.16). The isotropic etching causes the radius of the rounded corner to be reduced. Figure 2.16 shows the decrease in radius from *A* to *E*. When the distance between original edge and etched shape is larger than the radius of the original rounded corner, its radius is so small that it can not be reduced further which means the corner is perfectly sharp (*F* in Figure 2.16).

Using the method described above, the corner rounding effect can be circumvented and a sharp corner can be realised. This method only requires the inclusion of an extra layer of SiRN and one extra dry etching step. The fabrication process is not made significantly more complicated while the increase in corner sharpness will have a positive effect on the final tip sharpness.

Furthermore, as a result of the retracting sandwiched TEOS SiO_2 layer, the length of cantilevers is equalised. The photoresist pattern of the cantilevers contains irregularities which, without layer retraction, cause differences in cantilever length. This also means that without layer retraction, the tips will be positioned at dissimilar distances from the cantilever base, while ideally they are located in a straight line. With the implementation of layer retraction, the irregularities are evened out and the cantilever length is regulated by the global outline of the cantilever and the etch time.

Straight etch profile for sharp tip with uniform height

When choosing an etch technique, the demand for a straight etch-profile (which will be discussed in 3.2.3) has to be taken into account. Considering the scalloped etch-profile of the Bosch process, it is unsuitable. The scalloping effect will at the apex of the tip influence its sharpness. This scalloped profile is caused by the discontinues nature (the repeated alternation of etching and passivation) of the process and is in the range of 100 to 200µm if a standard process is used. Using a continuous process will result in a smoother etch profile. The etch-profile is allowed to be tapered (positive or negative, to a certain extent), as long as the transition of the mask and the Si is smooth. More information about the etch shapes that are (not) allowed can be found in section 3.2.3.

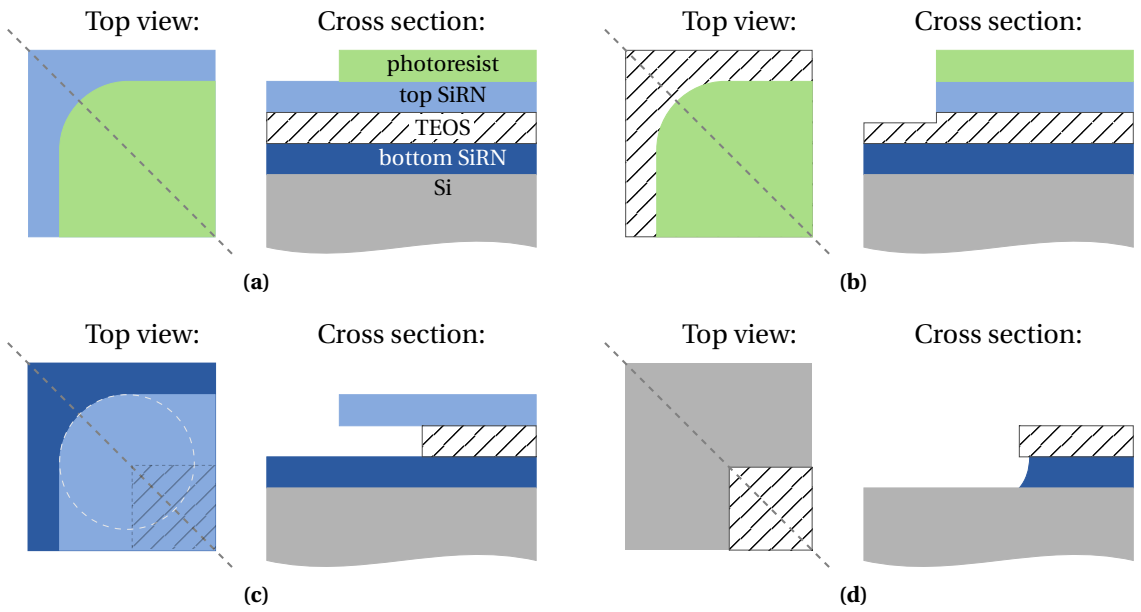


Figure 2.14: Conversion of round into sharp corner (not to scale) (a) Pattern photoresist (b) Dry etch top SiN layer (c) Wet etch of TEOS SiO_2 (d) Wet etch of top and bottom SiN layers

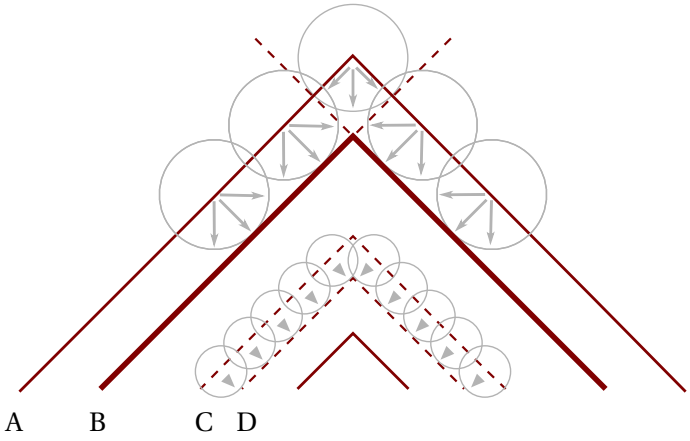


Figure 2.15: Convex corner preservation

2.2.7 Cantilever

The use of a SOI wafer in combination with the KOH process also has advantages for the cantilevers. Because the thickness of the cantilevers is determined by the device layer thickness and the KOH etch duration, no major variation in cantilever thickness is expected. The uniformity of the device layer is ±5% (from Table A.1 in the Appendix). This means the thickness of the device layer varies from 9.5 to 10.5µm, a maximum variation of 1µm. KOH has a wafer-scale non-uniformity of approximately ±4%. This means that the KOH etch produces a maximum variation in cantilever thickness over the complete wafer of 0.4µm (for a tip height of 5µm). The cantilever thickness will vary from 4.8 to 5.2µm. Over a single array, the variation in cantilever thickness is even smaller. No alternative etch

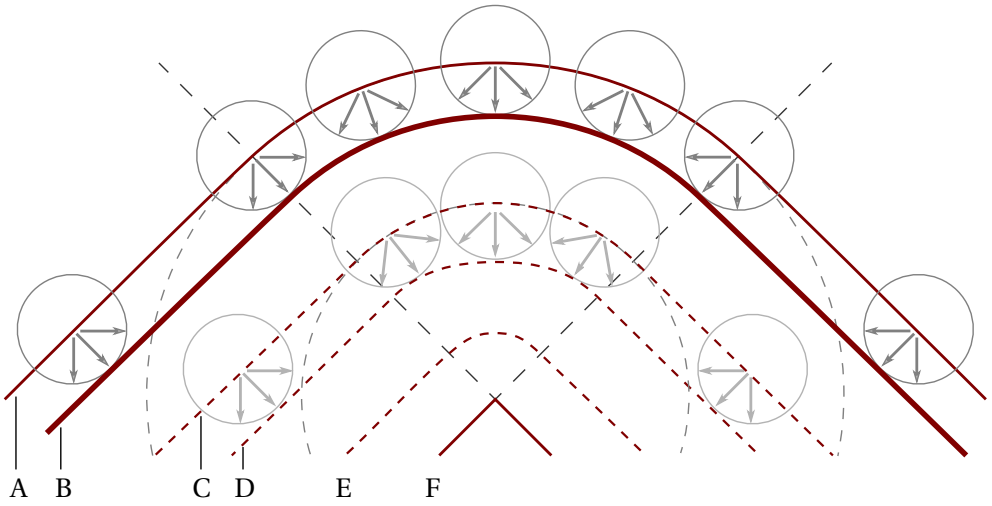


Figure 2.16: Radius reduction at convex corner

method which is as simple can measure up to the high uniformity in cantilever thickness that can be achieved by KOH.
As can be seen in Figure 2.17, the KOH etch step as presented in Figure 2.12 not only forms a tip, but also creates a ridge at the cantilever sides parallel to the ⟨110⟩ direction of Si.

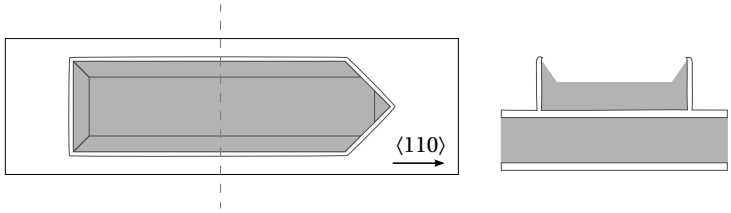


Figure 2.17: Ridge formation at the edges of the cantilever (left: top view, right: cross section)

When operating the cantilever, it will be mounted with a certain tilt angle α between the plane of the sample and the cantilever axis (Figure 2.18). In the AFM this angle is 10°. The protruding ridges can interfere with the EFM readout when the distance between ridge and sample is small. In the extreme case, the ridges can even touch the sample surface at point a or b. Furthermore, because the line $a-b$ never is perfectly parallel to the sample, one of the ridges will be even closer to the sample. Since the tip must be the object closest to the sample, a way to inhibit the ridges is desired.

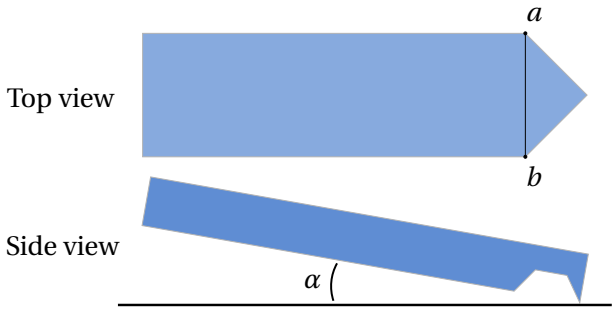


Figure 2.18: Schematic view of cantilever above a sample. α is 10° in our AFM

Ridge prevention

Figure 2.19 shows no ridge exists on the side of the cantilever between point R and point T. This is a result of the fabrication method. On cantilever sides parallel to the ⟨110⟩ direction, (111) planes persist after the KOH etch. Because segment $R-T$ has an angle of 45 degrees with respect to the ⟨110⟩ direction, the (111) plane is not the only crystal plane accessible for etching. Any plane having an etch rate which is higher than that of the (111) plane will cause the ridge to be etched away [25].

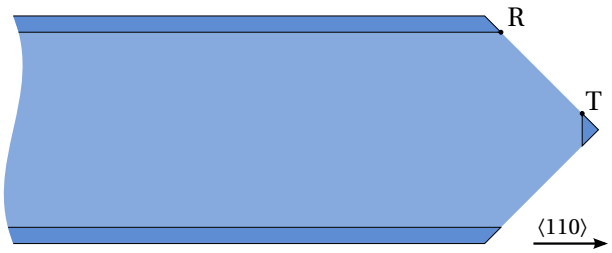


Figure 2.19: End of cantilever with tip and ridges pointing up

When a cantilever has its sides at an angle of 45 degrees with respect to the ⟨110⟩ direction (similar to segment $R-T$ in Figure 2.19), the ridges are prevented. This will result in a v-shaped or triangular cantilever. The modified shape however has consequences for the mechanical behaviour of the cantilever. The spring constant of a v-shaped cantilever as specified by the parallel beam approximation is

$$k = \frac{Ewt^3}{2L^3} \tag{2.1}$$

The parallel beam approximation models the V-shape as two rectangular beams joined at one end. The spring constant of a single rectangular cantilever (will be given in Equation(2.4)) is simply doubled.
The width at the base of the cantilever is increased due to tapering. A wider base decreases the number of cantilevers that fit into an array (when the width is restricted). Furthermore, because of the wider base, an elongated laser spot with an increased length is required and, what is more problematic, a bigger detector is needed. We can conclude that triangular or v-shaped cantilevers are not suited for implementation in arrays.
A possible alternative to inhibit the ridge is by using 'steps' illustrated in the top part of Figure 2.20. The convex corners numbered $1-6$ cause the (111) planes at the sections parallel to the ⟨110⟩ direction to be etched. This is indicated by the small black arrows. At convex corners, many fast etching crystal planes are accessible. These planes cause the ridges to be etched away in the direction of the arrows.
Derived from cantilevers having an outline with steps, it is also possible to prevent the ridge from being formed by using a straight edge (see Figure 2.20, bottom part). When angle θ between a straight edge and the ⟨110⟩ direction corresponds to the angle of the average path of the stepped outline any ridge is suppressed. By absence of walls oriented parallel to the ⟨110⟩ direction, (111) planes are unprotected. Due to the pixels created by laser writing any straight line will actually consist of tiny steps. Similar to the stepped configuration any (111) plane will be etched from the wide side of the tapered cantilever.
Now that a way to suppress the ridge is available the total cantilever shape can be defined more accurately. Although a disadvantage of the ridge is its influence on the mechanical behaviour, there is no absolute need to prevent the ridge over the complete length of the cantilever. This will only

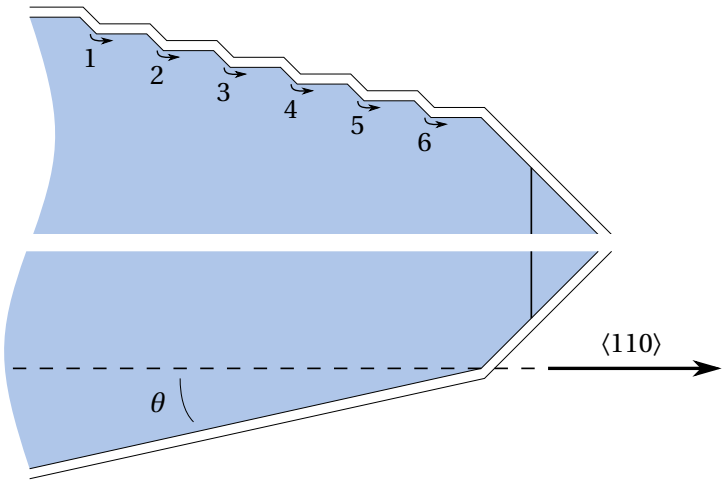


Figure 2.20: Ridge prevention on sides of cantilever (top view). Top part: small 'steps' are used to inhibit the ridge. Bottom part: the correct angle θ between the crystal ⟨110⟩ direction and the straight edge also suppresses the ridge

make the cantilever wider than necessary (because a taper is needed). It is sufficient if the free end of the cantilever is ridge-free to a certain distance from the end. An important condition is that the ridge must be separated from the sample, so that it can not interfere with the readout. The area over which no ridge should exist depends on the angle between cantilever and sample. In Figure 2.21 this angle α is illustrated.

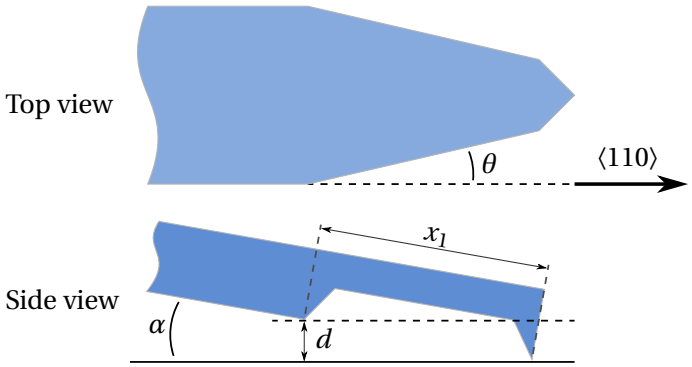


Figure 2.21: Schematic view of a tapered cantilever above a sample with tilt angle α

For the ridge to have no influence, its distance to the sample must be greater than that between the rest of the cantilever and the sample. The cantilever is closest to the sample at the free end. The distance here is specified by roughly the tip height (actually it is $\cos(\alpha) \times$ tip height, but this is almost equal to the tip height at small angles). So distance d should be greater than the tip height. At an angle α of four degrees and a tip height of five µm the area of the cantilever that should be ridge-less, x_1, is at least $\left(\frac{5\mu m}{\sin 4^\circ}\right) \approx 71.7\mu m$.

The cantilever shape with taper has an advantage with regard to EFM. One of the design rules for a good electrostatic probe is that the tip height must be in the order of the cantilever width [12]. For rectangular cantilevers having a width of 30µm, this means that a tip in the same order is required. But since the cantilevers in our design have a reduced width at the free end of the cantilever, a

smaller tip height is required in order to obtain good electrostatic performance. This is convenient for the uniformity of the KOH etch. For reduced tip height, a shorter KOH etch is needed. And variation in tip height, resulting from differences in etch rate, decreases when the etch time is decreased.

Reflectivity of detector side of cantilever

Another advantage of using a SOI wafer as substrate comes to light when the reflectivity of cantilevers is considered. Optical readout uses the detector side of a cantilever as a mirror for the reflection of a beam of light. The light is reflected by the cantilever and aimed at the PSD. The detector needs a certain amount of light to function. Since the reflector side of the cantilever is the BOX-layer side of the SOI device layer, it will be very flat and thus have a better reflectivity compared to a rough surface. Si is used regularly as material for cantilevers and we believe that the reflectivity of Si at the wavelength of the laser is good enough to achieve the required intensity at the detector. In case the reflectivity turns out to be insufficient, the detector side of the cantilever can be coated with a reflective material like gold or aluminum. This is a common enhancement for cantilevers.

Separated resonance frequencies

As mentioned earlier, parallel optical readout requires cantilevers with distinct resonance frequencies. First we need an equation for the resonance frequency of a cantilever. The most straightforward shape for a cantilever beam is a rectangular one, since this simplifies the modelling of a cantilever. In the following approximation, the change in dynamics due to the ridges is not taken into account. The vertical deflection z at the end of a cantilever can be calculated by

$$z = \frac{L^3 F_z}{3EI} \tag{2.2}$$

where L is the length of the cantilever, E is Young's modulus, F_z is applied force and I is the ratio of the moment of inertia to the mass. For a cantilever with a rectangular cross section having width w and thickness t, I is

$$I = \frac{1}{12} w t^3 \tag{2.3}$$

By combining Hooke's law, Equation (2.2) and Equation (2.3) the spring constant k is found to be

$$k = \frac{E w t^3}{4L^3} \tag{2.4}$$

Besides the spring constant, another important parameter is a cantilever's resonance frequency. The fundamental resonant frequency f_0 of a cantilever is related to the spring constant k and the mass m_{eff} by

$$f_0 = \frac{1}{2\pi}\omega_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m_{\text{eff}}}} \tag{2.5}$$

Since the mass used in Equation (2.5) is a point mass, the total mass of the cantilever needs to be converted into an effective mass m_{eff}, which for a rectangular cantilever is

$$m_{\text{eff}} = \frac{33}{140} m \tag{2.6}$$

where m is the mass of the cantilever. Inserting Equations (2.4) and (2.6) in Equation (2.5) yieds

$$f_0 \approx \frac{t}{2\pi L^2}\sqrt{\frac{E}{\rho}} \tag{2.7}$$

Equation (2.7) teaches us that tweaking of the resonance frequency can be done by changing either the thickness or the length of the cantilever. Since the fabrication process is based on SOI wafers (with fixed device layer thickness) and anisotropic etching, the thickness will be the same over the whole wafer. This means no variations in thickness can be implemented within one wafer. This leaves altering the length of the cantilevers to change the resonance frequency.
But when the shape of the cantilevers deviates from the rectangular shape Equation (2.7) is valid for, the resonance frequencies of cantilevers can be separated without varying their length. When tapered, the width of the cantilever is not constant over its length. In this case the approximation in Equation (2.7) (which assumes the cantilever is rectangular) is not valid. If the ends of two cantilevers are tapered with dissimilar angles, their resonance frequencies will differ.
For the parallel readout experiments, two adjacent cantilevers are required to have a difference in resonance frequency of approximately 2kHz. The small width of the cantilevers, in combination with the minimum required taper length, sets a maximum for angle θ. Given a width of 40µm and an end-width of 7µm, θ is limited to 13°. The amount of frequency separation is limited by the minimum (10°) and maximum (13°) angle θ. For cantilevers having a width of 40µm, a length of 400µm, and angle θ of 10°, 11°, 12° and 13°, the resonance frequencies are estimated to be 55.9kHz, 54.6kHz, 53.5kHz and 52.6kHz, respectively (calculated using the Matlab code in C.1.1). Since the differences in arrays with different taper angles are smaller than 2kHz, arrays with varying cantilever length are incorporated in the design as well to realise the required frequency separation.

Uncoupling of adjacent cantilevers

The misalignment and the tapered etch profile of the backside etch (section 2.2.8) can cause underetch underneath the device layer at the edges of the chip. At the cantilever side, this results in an extending plate over the complete width of the chip, to which all the cantilevers are connected. The cantilever behaviour can be influenced by this flexible plate. The design aims for uncoupling of adjacent cantilevers by preventing the extending plate. Again, the use of a SOI wafer proves to be beneficial. In Figure 2.22, the device layer and the buried SiO_2 layer are partially removed nearby the border where cantilevers extend. This way, the formation of an extending sheet is prevented, both in the device layer and in the BOX-layer. In case no BOX layer is available (for example when no SOI wafers are used), this simple type of uncoupling of adjacent cantilevers is not achievable.

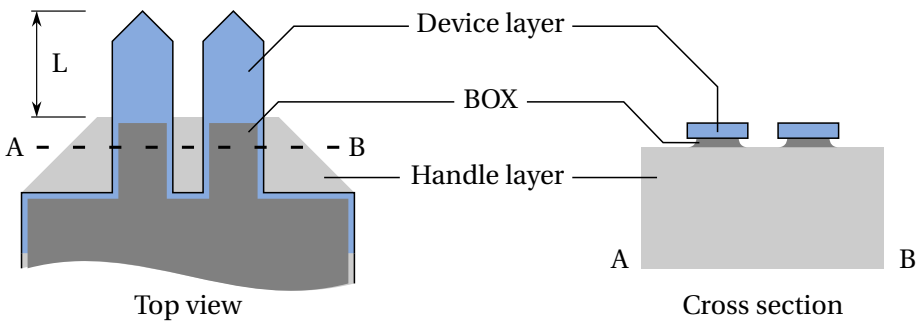


Figure 2.22: Uncoupled cantilevers

2.2.8 Chip

Every cantilever array is supported by a chip. The dimensions of this chip are chosen to be compatible with the AFM in our lab: a Nanoscope Dimension 3100 (Veeco - Digital Instruments, Santa Barbara, CA). The width is 1600µm, the length is 3200µm and the height is 385.5µm. Since this size is industry standard, the chips fit into most commercial AFMs. Chip sizes are visually presented in Figure 2.23. As mentioned earlier, when operating the cantilever array, the chip will be mounted with a certain tilt angle α (4°/10°) between the plane of the sample and the chip. To avoid contact between chip and sample (when a rotation around axis R causes the chip to be out of line with the sample), the two corners near the cantilevers are cut off in the design.

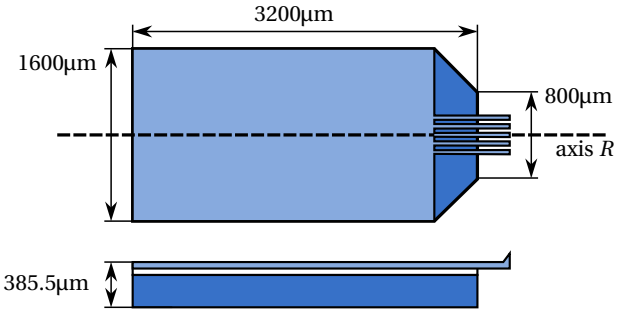


Figure 2.23: Top and side view of a chip − sizes are indicated

Backside (handle layer) etch

A great advantage of the fabrication principle is that both cantilever and tip are defined in a single mask. Another mask is required for the backside etch, bringing the total number of masks to two. Because the frontside mask is used to transfer the first pattern to the wafer, misalignment is not critical. Misalignment of the backside mask with the pattern of the frontside mask on the wafer can result in deviations of cantilever length. Furthermore, the etch profile of the backside etch will not be perfectly vertical, but will have a taper. This effects the cantilever shape as well. The backside etch takes advantage of the BOX-layer in the SOI wafer as etch-stop. Without a buried SiO_2 layer, this backside etch process can not be applied. The complete handle layer of 380µm is to be etched in this step. Parameters of the backside etch process are listed in Table A.4 in the Appendix.

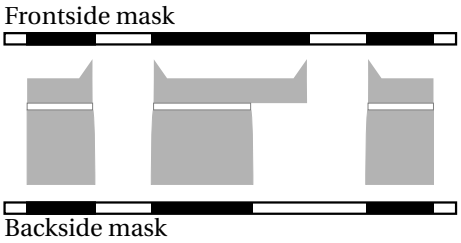
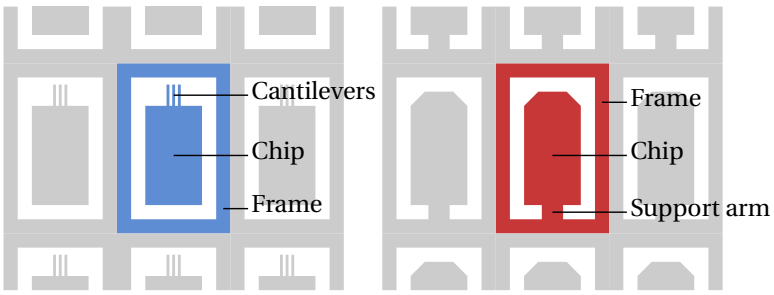


Figure 2.24: Frontside mask (for device layer) and backside mask (for handle layer)

2.2.9 Frame

The chips are arranged in a frame. The complete frame consists of multiple frame elements. Figure 2.25 shows a single frame element. The chips are connected to the frame by a support-arm.

The cantilevers are defined in the device layer (by the frontside mask) and the support-arm is defined in the handle layer (by the backside mask). The support-arm is located at the rear end of the chip, opposite to the cantilever array. This is the best location to prevent tiny parts of Si to end up at the cantilevers when breaking out the chip. The support-arm is realised in the handle layer to give the chip sufficient hold. A support-arm in the device-layer only would be too fragile to sustain a chip.
Another purpose of the support-arm is to transfer heat from the chip during backside etching. Due to the bombardment of the surface by ions from the plasma during etching, the wafer heats up. When the silicon around the chip (the white space surrounding the chip in Figure 2.25b) is etched and the SiO_2 of the BOX-layer is reached, the chip can only loose its heat through the support-arm. If the support-arm is too thin, the amount of heat released from the chip can cause it to break down. Because the etch process is not uniform over the wafer, and because we want every chip to be free, local over-etching after the BOX-layer is reached is inevitable.
The space between a chip and a frame element is 400µm. The thickness of a frame element is 400µm. The backside etch was completed successfully using this frame-size. However, it must be noted that the specialist (Meint de Boer) believes it was a close call. In his opinion, a design with more body is preferred. Also, Meint de Boer believes that the width of the support arm should not be decreased.



(a) Frontside mask **(b)** Backside mask

Figure 2.25: Mask design. The coloured section is a frame element

2.2.10 Wafer layout

A total number of 360 chips is fitted on a 4-inch (100mm) wafer. Each chip has a unique number. When results need to be verified it is convenient to be able to find the very same chip used during the measurement. The chip numbers are shown in Figure 2.26. Variations in design are distributed over (segments of) rows of multiple chips (shown in identical colours). Chips 1 through 8 for instance have an array of 2 cantilevers where only the spacing is varied per chip. Chips 157 through 166 are equipped with two cantilevers of which the width and spacing differ every chip.

Design variations

Several implementations of the cantilever arrays are included in the design. For example, arrays are designed with a different number of cantilevers. Variations in dimensions of the cantilevers are also employed. All the parameters of the arrays are indicated in Figure 2.27. The variations of these parameters are listed in the table in Figure 2.27. Please note that when angle $\psi \neq 0$, θ is no longer the angle between the segment of the cantilever edge and the $\langle 110 \rangle$ crystal direction.

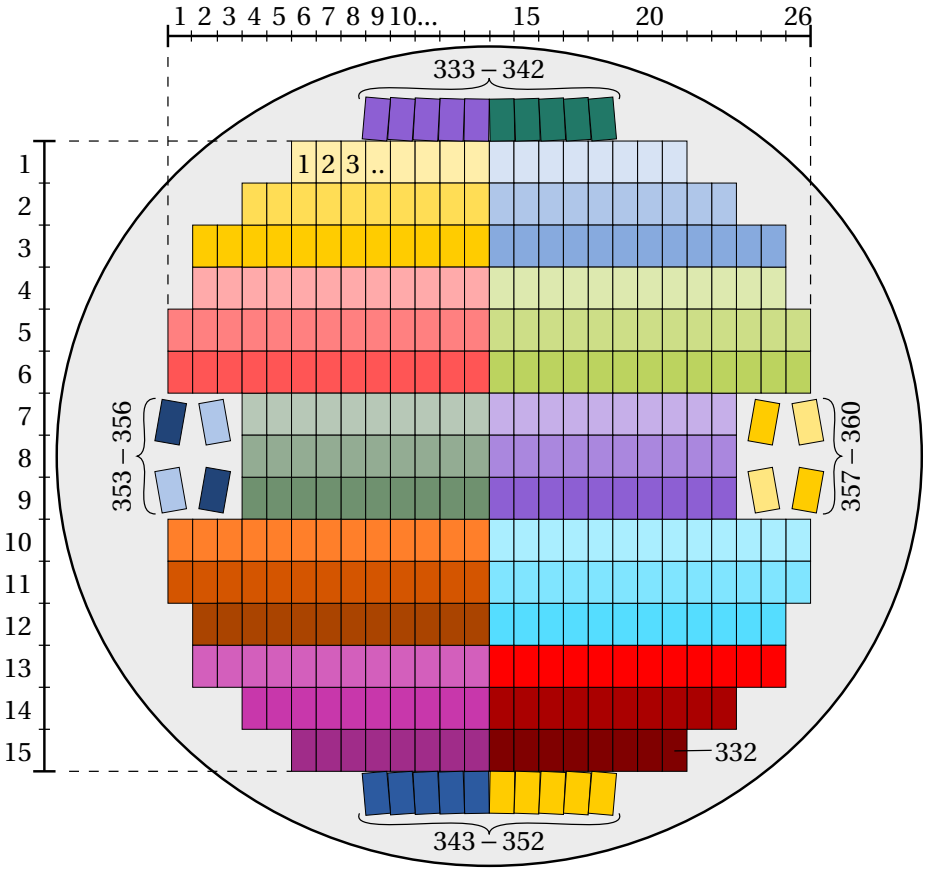
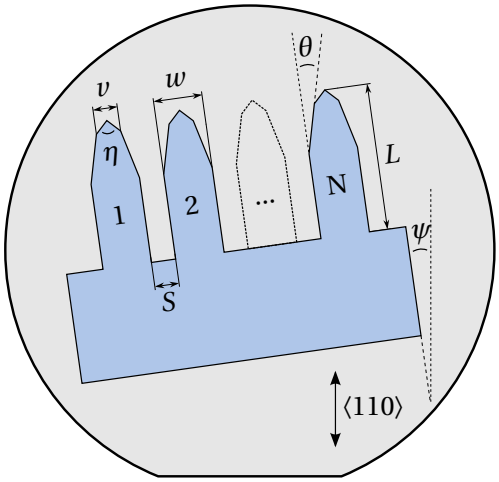


Figure 2.26: Wafer layout showing chip numbering



Parameter	Symbol	Specification
number of cantilevers per array	N	1 – 30
spacing between cantilevers	S	10 – 50 µm
cantilever width	w	15 – 75 µm
cantilever length	L	150 – 400 µm
resonance frequencies	f_0	50 – 200 kHz
cantilever end width	v	7 – 30 µm
cantilever end angle	η	90°
cantilever taper angle	θ	0 – 20°
rotation	ψ	0 – 10°

Figure 2.27: Specifications of cantilevers and cantilever array

This parameterisation is successful as long as either parameter ψ or parameter θ is zero. This condition is satisfied because rotation of the complete chip (i.e. $\psi \neq 0$) is only applied to chips with cantilevers that are not tapered ($\theta = 0$). An overview with array parameters of every chip is included in Appendix B.3.

2.3 Conclusions

In order to realise the high requirements that are listed in section 2.1.3, a new process scheme is developed. The new process uses two masks: one mask for the cantilevers and the tips and one mask for isolating the chips. The process scheme is based on a SOI wafer, and the advantage of a KOH etch process in combination with LOCOS is that the cantilevers and tips are formed in a single step.
Fabrication of tips having a small radius of curvature (< 10nm) can be achieved if two conditions are met. The first condition is a sharp mask corner for the pattern transfer into the device layer. A sharp corner is achieved by the inclusion of a sacrificial layer to perform corner sharpening. The second condition is a straight etch profile at the top part (±1 μm) of the device layer, and is to be achieved by cryogenic etching.
A rectangular cantilever produced by the KOH etch process has ridges. The ridges can be (partly) prevented by applying a taper to the cantilever.
Advantages of the process being SOI-based and the implemented KOH etch are a uniform tip height on wafer-scale and a uniform cantilever thickness on wafer-scale. In addition, a clean and flat detector-side-surface for good reflectivity, the option to uncouple adjacent cantilevers and the possibility to use DRIE for backside etching are beneficial consequences of using SOI substrates.

Chapter 3

Fabrication

This chapter describes the fabrication of the cantilever arrays. In section 3.1 the fabrication process outline is presented. The results and discussion of the fabrication are discussed is section 3.2.

3.1 Process outline

Table 3.1 shows the complete process flow. The complete process documents are included in Appendix D.

Table 3.1: Process flow

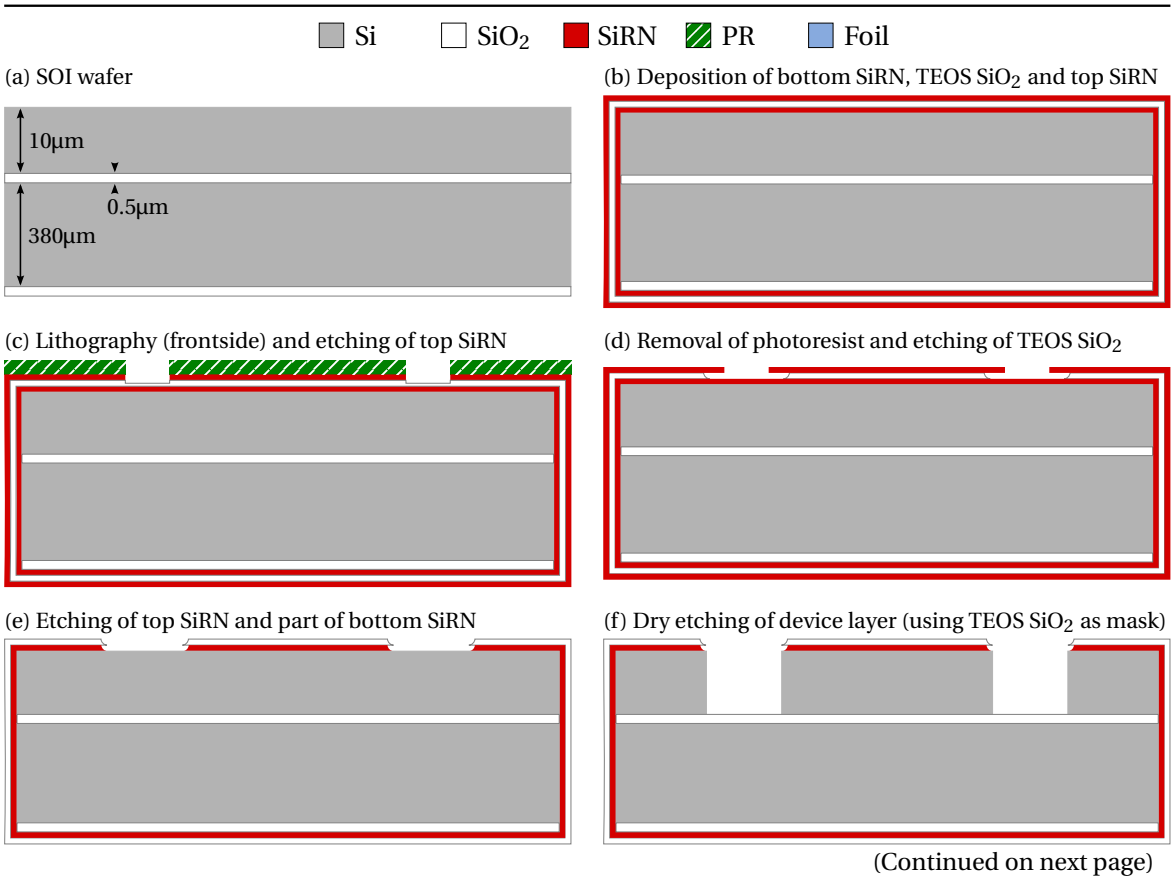


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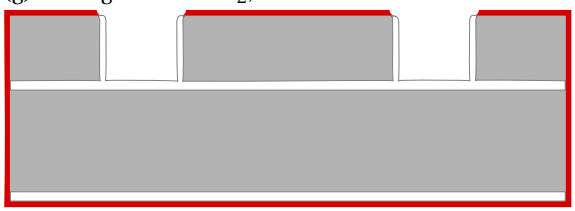
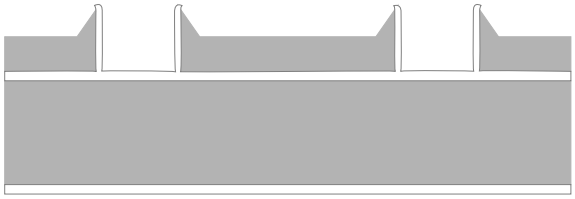
Table 3.1 Process flow *(continued)*

(g) Etching of TEOS SiO_2, then LOCOS

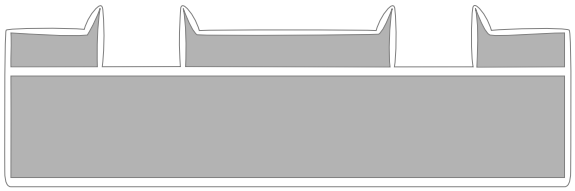


(h) Wet etching of bottom SiRN

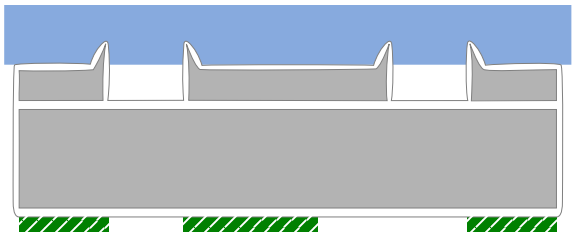
(i) Wet (anisotropic) etching of device layer



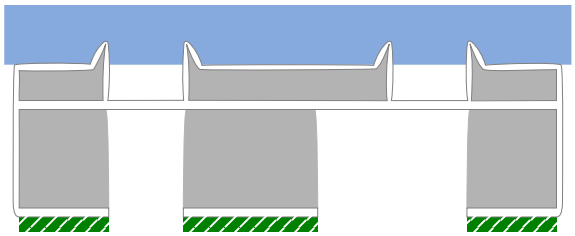
(j) Etching of SiO_2 followed by thermal oxidation



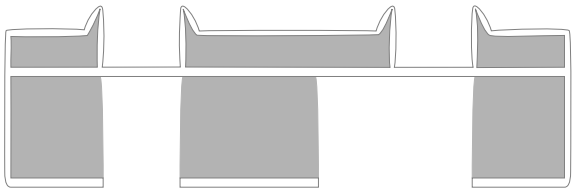
(k) Lithography (backside) and fitting of foil (frontside)



(l) Backside DRIE: through SiO_2 and Si (PR as mask)



(m) Removal of foil and photoresist



(n) Etching of SiO_2

Process flow description

(a) The starting point for the fabrication is a SOI wafer. As mentioned before, the device layer of this wafer is 10µm in thickness, the BOX layer thickness is 0.5µm and the handle layer thickness is 380µm.

(b) On top of the device layer, 25nm of SiRN, 100nm of TEOS SiO_2 and 20nm of SiRN are deposited successively. All layers are deposited using LPCVD. The minimum thickness of the bottom SiRN layer follows from the amount that is needed to prevent the oxidation of the underlying Si. This minimum required thickness is 15 - 20nm[24]. Because the TEOS SiO_2 is used as a mask during dry etching of the device layer, a certain amount of TEOS SiO_2 is etched. The etch rate of Si is 2.5µm/min so it takes four minutes to etch 10µm of Si (the thickness of the device layer). The required thickness for the TEOS SiO_2 layer now follows from its etch rate (±10nm/min) and should be more than 40nm. The top SiRN layer is thinner than the bottom SiRN layer, so that, when the bottom layer is etched, the top layer will be completely removed.

(c) Using standard photolithography, a mask for dry etching of the top SiRN layer is formed. A post-bake is explicitly omitted because this step increases the corner rounding in the photoresist. Reactive Ion Etching (RIE) with CHF_3 and O_2 as gas is used to perform this etch step. The dry etch should completely remove the uncovered SiRN. To be sure no top SiRN remains some over-etch is applied by which several tens of nanometers of underlying TEOS SiO_2 are etched. This is harmless since the exposed TEOS SiO_2 will be etched away in the next step.

(d) After stripping of the photoresist, an isotropic wet etch is applied to etch the TEOS SiO_2. Using the patterned top SiRN layer as sacrificial layer and mask, the TEOS SiO_2 is wet etched for 12 minutes and 30 seconds by means of Buffered Hydrogen Fluoride (BHF). For the removal of 100nm of TEOS SiO_2, etching in BHF for 34 seconds is sufficient (etch rate is 180nm/min). Extending the duration of this wet etch causes the sides of the sandwiched TEOS SiO_2 layer to be retracted, creating two effects. (1) The radius of convex corners is reduced, while (2) the radius of concave corners is increased. This means rounded profiles of the TEOS SiO_2 layer are weakened and the rounded corner at the free end of a cantilever (as seen from above) is converted into a sharp corner. More details about this mechanism are already treated in section 2.2.6. In section 3.2.1 is described how the BHF etch time needed to attain a sharp corner is determined.

(e) Now that the TEOS SiO_2 is patterned as desired, this pattern is transferred into the bottom SiRN layer and in addition the top SiRN layer is removed. Both actions are performed simultaneously in a single hot phosphoric acid (H_3PO_4) etch. The duration of this etch is critical since the complete 25nm thin SiRN layer must be removed while over-etch must be kept at a minimum. Remainders of SiRN will act as masks and over-etching will cause the bottom SiRN layer to retract and can possibly influence the future etch profile of the device layer, as is described in section 3.2.2. SiRN is hydrophilic while Si is hydrophobic. This means complete removal of SiRN can be optically detected by means of the surface showing hydrophobic behaviour. The time needed to etch away the uncovered bottom SiRN is 8 minutes and 50 seconds.

(f) The outline of the cantilevers is now defined in the Si device layer by means of a dry etch. The patterned TEOS SiO_2 serves as a mask for pattern transfer into the device layer. In order to obtain a straight etch profile (with minimal undercut), a continuous cryogenic RIE process is applied. SF_6 and O_2 are used simultaneously in this process.

(g) The TEOS SiO_2 is now removed in 1% HF during 5 minutes. The Si is not attacked by 1% HF owing to the high selectivity. After this the Si is thermally oxidised for 5 hours at 950°C. The remaining bottom SiRN prevents the Si it covers from oxidising. This process of selectively oxidising Si is known as Local Oxidation of Silicon (LOCOS). The thickness of this SiO_2 layer is determined by the KOH etch. Because it is used as a mask, the SiO_2 must persist the complete KOH etch. During a 5 minute etch at least 15nm of SiO_2 is consumed. After 5 hours of dry oxidation (at 950°C) 95nm of SiO_2 at {100} planes and 117nm of SiO_2 at {110} planes is grown.

(h) The bottom SiRN is now stripped in hot H_3PO_4. Owing to the high etch selectivity of SiRN over Si and SiO_2 by hot H_3PO_4, over-etching is applied without side effects. The duration of this etch is 12 minutes and 30 seconds.

(i) Si is etched anisotropically when immersed in KOH. Where Si is covered by SiO_2 it will not be attacked by KOH, because the SiO_2 serves as a mask. During a five minute KOH etch the Si device layer is anisotropically etched from the top. With the etch rate of Si being 1µm/min this means 5µm of Si is etched, reducing the thickness of the device layer from 10µm to 5µm. A solution containing 25% KOH and 75% water is used at 70°C. The anisotropic behaviour leaves ridges next to the SiO_2 masks parallel to the ⟨110⟩ direction. The slow etching {111} planes are causing these ridges. At the free end of each cantilever a semi-tetrahedral tip is formed by such a ridge.

(j) Frontside processing is now completed. Before backside processing can start a dry thermal oxidation is performed for two reasons. First, it protects the tips during backside processing and secondly, a sharpening effect is established after stripping of the SiO_2. The SiO_2 used as mask in the KOH etch is still present and will prevent sharpening of the covered Si, so it has to be removed first. Removal of the SiO_2 is done in 1% HF for 30 minutes and the thermal SiO_2 is grown at 950°C for five hours.

(k) A layer of photoresist is spin coated on the backside, exposed using the backside mask and developed. The backside mask is aligned with the pattern on the frontside using alignment marks. A protective foil (DuPont MX5000) is fitted onto the frontside. This foil mechanically protects the tips and if any holes are formed in the wafer, the foil ensures a good thermal contact of the wafer with the electrode during DRIE of the backside of the wafer.

(l) With the tips protected by both SiO_2 and foil the backside etch can take place. This backside etch forms the chips holding the cantilevers and is done by Deep Reactive Ion Etching (DRIE). First the SiO_2 layer is etched by a pulsed DRIE CH_4 plasma step at -40°C (2 minutes and 30 seconds is sufficient). A pulsed DRIE step at -100°C is then used to perform a wafer-through etch.

(m, n) Both the protective foil and the photoresist are removed in an O_2 plasma. Removing both the BOX and the protecting SiO_2 in one single step finalises the fabrication. They are removed by vapour HF. After three minutes of etching most of the cantilevers are free of SiO_2. Wide cantilevers have some remaining SiO_2.

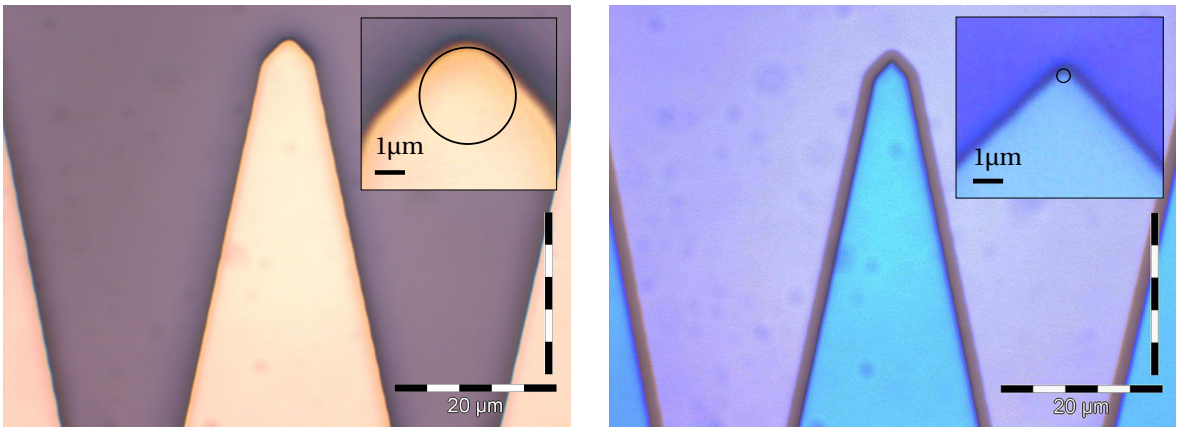
Essential aspects within the flow are the corner sharpening procedure, the straight etch profile of the device layer and the anisotropic etch in combination with LOCOS creating semi-tetrahedral tips. In section 3.2 they are described in more detail.

3.2 Results and discussion

3.2.1 TEOS SiO_2 corner sharpening

As discussed in section 2.2.6, the radius of any rounded convex corner in the TEOS SiO_2 layer is reduced by a sacrificial-layer-based BHF etching step. The etch duration needed to get a sharp corner depends on the rounded corner radius.
During the fabrication, dummy wafers are used to determine the required TEOS SiO_2 etch duration. The radius of rounded corners is first estimated. This radius is estimated between 1.5 and 2µm using an optical microscope (Olympus BH-2). After ten minutes of etching, the under-etch is optically inspected and estimated to be between 1 and 1.5µm. Based on the experiments with dummy wafers,

the appropriate etch time for the SOI wafers is decided to be 12 minutes and 30 seconds. Figure 3.1 shows the pattern of a cantilever before and after corner sharpening. In the inset in Figure 3.1b, the corner which is achieved after sharpening is presented. The radius of the corner is estimated to be below 250nm.



(a) **(b)**

Figure 3.1: Corner sharpening effect illustrated. (a) Before corner sharpening, photoresist pattern is the yellow region. Inset: corner radius is estimated to be greater than 1.5µm (b) After corner sharpening, TEOS SiO_2 pattern is blue. The top SiRN is visible as purple outline. The under-etch is estimated to be 1.6µm. Inset: corner after sharpening and removal of SiRN. Corner radius is estimated to be below 250nm.

3.2.2 SiRN mask for LOCOS

In step (e) of the process flow, the importance of a correct SiRN etch time is emphasised. Figure 3.2 indicates the consequence in case of over-etching. When too much of the bottom SiRN is etched, the revealed part of the underlying Si will be oxidised in the LOCOS step. Only a vertical wall of SiO_2 is desired, but due to over-etching of the bottom SiRN, the SiO_2 wall will have a canopy (as illustrated in C in Figure 3.2). Because in the KOH step 62.5nm of Si will be etched in the ⟨111⟩ direction (see section 3.2.3), the size of the canopy is confined to ±75nm. This means the revealed part of Si must be less than ±75nm (taking into account the so called bird's beak effect [26], also visible in C in Figure 3.2). This is the reason that a thin layer of bottom SiRN is used: by using a thin layer (a bottom SiRN thickness of 25nm is used in our fabrication), the size of the canopy is suppressed while some over-etching can be applied to be sure the complete layer of bottom SiRN is removed.

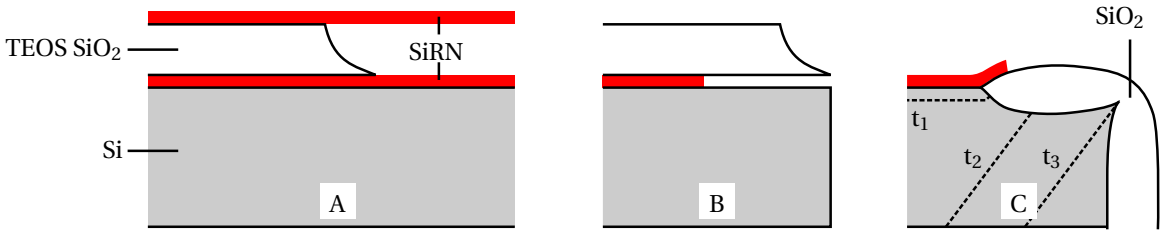
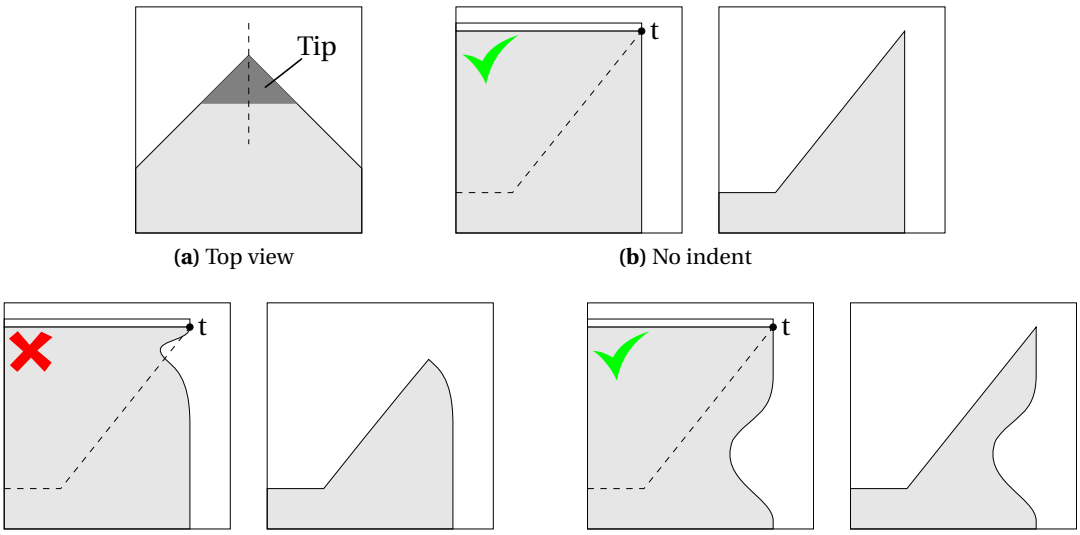


Figure 3.2: Detail of LOCOS process. **A**: situation after step (d) **B**: the bottom SiRN layer is retracted due to over-etching **C**: thermal oxidation of Si now results in a SiO_2 canopy (etching by KOH is indicated)

3.2.3 Etch profile of device layer

The shape of the etch profile is of great importance when aiming for a sharp tip. Figure 3.3 clearly illustrates this phenomenon. Irregularities in the etch profile close to the end of the future tip (point t), like undercut, can dramatically reduce the sharpness. A straight etch-profile produces a sharp tip (Figure 3.3b). Indents close to point t result in a blunt tip (Figure 3.3c). When irregularities only exist at a certain distance from point t and the top part of the etch-profile is straight, the sharpness of the tip is not affected (Figure 3.3d). Whether or not the tip sharpness is disturbed depends on the depth and the location of the indent: further away from t larger indents are allowed than close to point t.

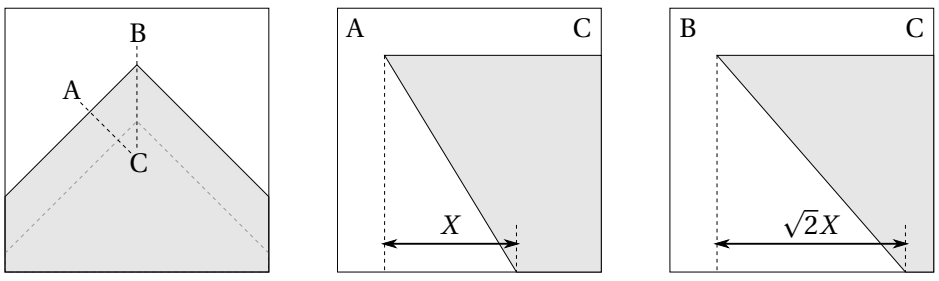


(a) Top view **(b)** No indent

(c) Indent close to point t **(d)** Indent at bottom, separated from t

Figure 3.3: Schematic representation of etch profile influencing tip sharpness. (a) Top view: dashed line indicates cross sections. (b) Straight vertical profile results in a sharp tip. (c) Indent at top part of profile results in a blunt tip. (d) Indent at bottom part of profile does not affect tip sharpness

Because of the properties of two sidewalls converging into a corner, any indent in the etch profile of these planes (for example $A-C$) will be amplified in $B-C$, as can be seen in Figure 3.4. This amplification limits the allowed deviation from a straight etch-profile even more.



(a) Top view **(b)** Cross section along A-C **(c)** Cross section along B-C

Figure 3.4: Profile amplification of two sidewalls at a 90° corner illustrated schematically. The amount of indent at $B-C$ is $\sqrt{2}$ times that at $A-C$

Figure 3.5 shows profile shapes that are allowed in order to achieve a sharp tip. Figure 3.5a shows underetch, which enables the formation of a sharp tip. A positive (Figure 3.5b) and negative (Figure 3.5b) taper are also allowed in the etch profile, as long as they are under a certain limit. The angle between the (111) and the (100) plane is 54.74°. When the negative taper has an angle of 26.6°, the angle of the etch profile at the corner is (90°-54.74°=) 35.26°(due to the amplification effect described above). In this case, the etch sidewall is parallel to the (111) plane, so it is impossible to form a tip. So for the negative taper, a maximum angle of approximately 15°is allowed. With regard to the positive taper, if the angle is bigger than 15°, a tip is still formed. The opening angle of the tip increases with the angle of the positive taper. In order to restrict the opening angle of the tip, the we apply the same angle of 15°as limit for the positive taper angle.

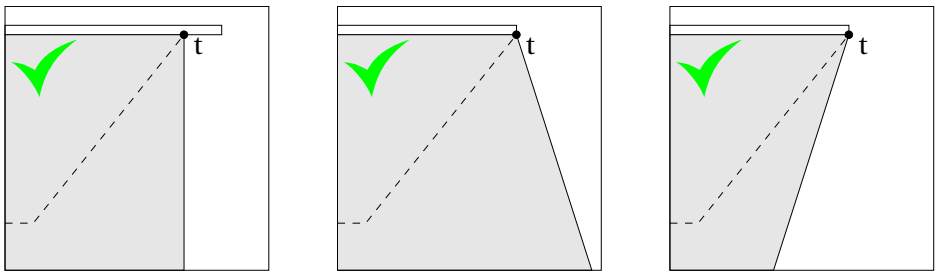
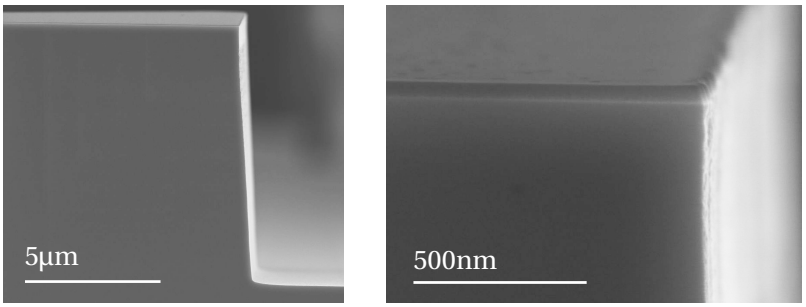


Figure 3.5: Allowed profile shapes for pattern transfer into Si device layer

The two planes forming the two perpendicular faces of the tetrahedral tip are dry etched using cryogenic etching. During a calibration run, a cryogenic etching process using SF_6 and O_2 is optimised to attain a straight etch profile when etching 10µm of Si (the thickness of the device layer). Table 3.2 contains the process parameters from the calibration. First the time is adjusted so the correct depth is etched (run 1 – 3). In run 4 and 5 the oxygen flow is optimised in order to attain a smooth connection at the TEOS SiO_2 mask. Increasing the oxygen flow causes more passivation at the sidewalls. The positive tapered etch profile (best visible in run 4) is another effect resulting from extra passivation.



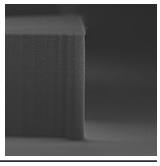
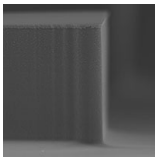
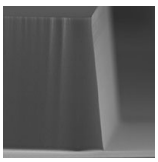
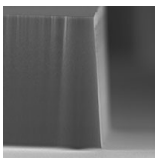
(a) Complete profile

(b) Magnification of top part: no undercut is visible

Figure 3.6: Cryogenic etch profile (TEOS SiO_2 mask only)

The etch profile obtained after the calibration shows a smooth transition from the TEOS SiO_2 mask to the Si (Figure 3.6). When a layer of SiRN is present between the TEOS SiO_2 mask and the Si, the

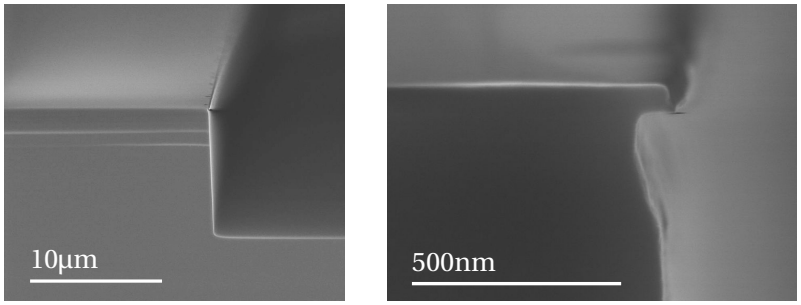
Table 3.2: Cryogenic etch calibration

Run	SF_6 flow (sccm)	0_2 flow (sccm)	ICP (Watts)	CCP (Watts RF)	APC (%)	Temp (°C)	Time (min)	Etch depth (µm)	Etch rate (µm/s)	Under-etch (nm)	TEOS SiO_2 thickness (nm)	Profile
1	100	10	500	20	100	-100	6	11.58	1.930	140	30	
2	100	10	500	20	100	-100	4	7.64	1.910	40	56	
3	100	10	500	20	100	-100	5	9.72	1.944	130	45	
4	100	15	500	20	100	-100	5	9.28	1.856	0	52	
5	100	13	500	20	100	-100	5	9.58	1.916	0	55	

etch profile is affected and undercut is observed (Figure 3.7). The gap between the TEOS SiO_2 and the Si (caused by over-etching of SiRN: see B in Figure 3.2) can also play a role in the undercut. This layer of SiRN can not be omitted since it is needed as mask during the LOCOS. The amount of horizontal undercut is 60nm. After five minutes in KOH, 62.5nm of Si is etched in the ⟨111⟩ direction (indicated in Figure 3.8). This gives rise to a decrease in tip height of almost 110nm. The right image in Figure 3.8 shows an estimate of the SiO_2 wall (in white) and the resulting tip (in black). This illustration indicates that the sharpness of the tip is not reduced by the undercut.

3.2.4 Tip damage due to KOH

Some wafers that are processed during the pre-study revealed damage to the tips. Figure 3.9 shows SEM photographs of several damaged tips ((a)–(f)) and one tip without damage ((g)). The surfaces



(a) Complete profile **(b)** Magnification of top part: undercut

Figure 3.7: Cryogenic etch profile (TEOS SiO_2 mask on top of bottom SiRN layer)

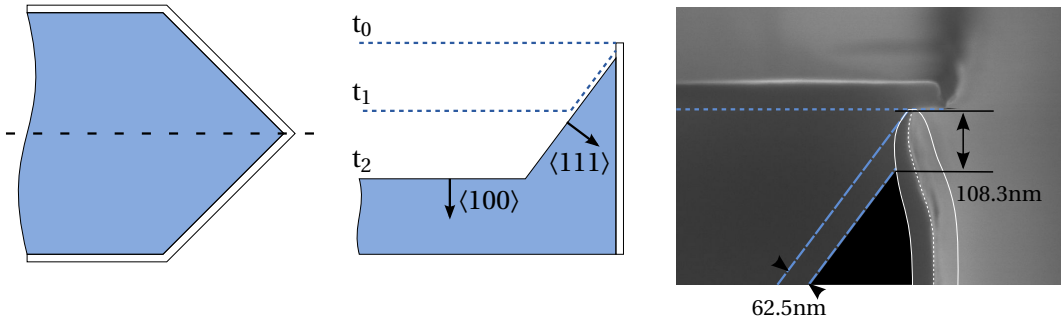


Figure 3.8: Effect of undercut on tip sharpness

exposed by the gaps correspond to the crystal planes of Si, indicating the damage is caused by KOH etching. This suggests the SiO_2 wall from step (g) did not successfully protect the underlying Si from the KOH. The SEM photographs also show the planar surfaces are intact and etching only occurred at the intersection of the sidewalls. This confirms the idea of insufficient protection by the SiO_2 wall. Dry oxidation at 950°C leads to a nonuniform thickness of SiO_2: at corners (intersections of the sidewalls) the wall is thinner than at planar surfaces, as is visible in Figure 3.10b. As a consequence, the corner is a weak spot. After the thickness is decreased by etching, holes can start to emerge at the weak corner. Extending the oxidation time in step (g) to 5 hours increases the wall thickness and solves the issue of tip damage.

3.2.5 Sharpening by oxidation

Oxidation is used for two reasons. One purpose is to protect the tips during the backside processing. Another goal is to sharpen the tips even more. The SiO_2 wall which was created during the LOCOS can either be removed or maintained before this oxidation step. For the protection it is irrelevant whether the LOCOS-walls are present. On the other hand this SiO_2 wall will have consequences for the sharpening effect. If the walls are maintained, only the (111) plane is uncovered and will be oxidised. Some oxidation will take place through the existing SiO_2 wall, but this effect is relatively small. In case the walls are removed before oxidation, all three planes of the tip will be oxidised.
The sharpening is performed by dry thermal oxidation at 950°C. The temperature during thermal oxidation has great influence on the SiO_2 profile. Figure 3.10a presents the profile after oxidation at 1100°C, the profile in Figure 3.10b is the result of oxidation at 950°C. Marcus et al. studied the oxidation of Si shapes and concluded the difference in SiO_2 profile is due to stress at the $Si-SiO_2$

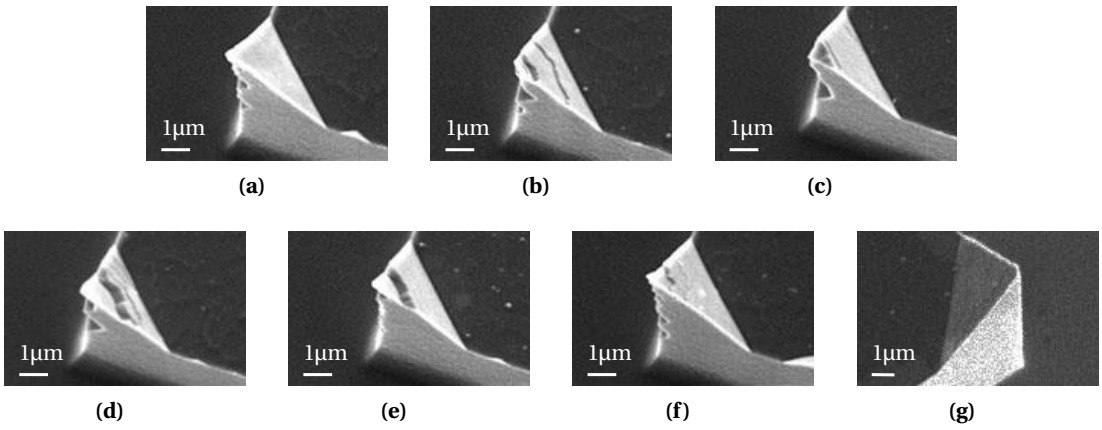
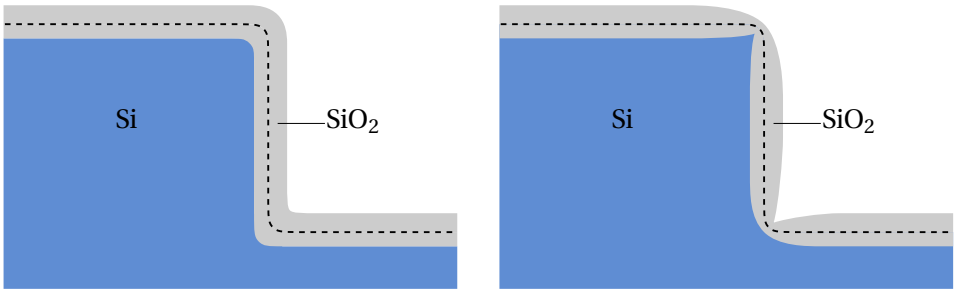


Figure 3.9: SEM photographs showing damage to tips. The tip in (g) is not damaged



(a) Dry oxidation at 1100°C **(b)** Dry oxidation at 950°C

Figure 3.10: Influence of temperature on SiO_2 profile by thermal oxidation. The dashed line indicates the Si surface before oxidation

interface. When the temperature during oxidation is higher than 1050°C, stress is relieved because decreased viscosity permits flow of SiO_2. At 950°C the viscosity is higher, and a buildup of stress at a Si step locally reduces the oxidation rate [27].

3.2.6 Frontside leakage barrier

The aim of the backside etch is to etch through the complete thickness of the 380µm handle layer. Because of its directional profile, high etch rate for Si and selectivity to the BOX-layer in the SOI wafer, DRIE is a very suitable technique. The back-etch is accomplished using the Bosch process on an Adixen AMS 100 SE system. In this process, the bombardment by ions for directional etching causes the temperature of the wafer to increase. By applying helium backside cooling during the etching process, the wafer is kept at a constant temperature and the DRIE process will be stable. If openings appear in the wafer during etching, helium leaks away and the optimum helium pressure can not be maintained. Since the BOX-layer is only 500nm in thickness, it is vulnerable to rupturing. A supporting layer is required at the frontside of the wafer to avoid leakage. In the ideal case, this barrier is easily removed after completion of the backside etch. Possible materials for this supporting layer are:

- Pyralin

- AZ 4999 (spray-coated)
- SU-8
- DuPont MX5000 (foil)

Within the TST-group, Pyralin has been successfully used as leakage barrier. However, in those experiments the structures to be covered were smaller in height (around 3µm). The height of cantilever plus tip is 10µm. To completely cover the tips, a layer thickness > 10µm is required. Pyralin PI 2611 can be spin-coated with a maximum thickness of 8µm. This makes Pyralin unsuitable to cover the 10 µm high cantilever-tip devices.
Experiments with spray-coated AZ 4999 as leakage barrier are performed using a Süss MicroTec Delta Altaspray. An advantage of spray-coating is the high degree of coverage, since the material is sprayed from four different directions. Based on a 4-layer recipe, thickness can be increased by 6.2µm. For example, two consecutive 4-layer recipes produce a thickness of 12.4µm. Different baking/curing and exposure procedures are applied, but the AZ 4999 showed cracks after etching at -40°C.
Another photoresist used in the TST-group is SU-8, which can be coated in thicknesses up to 2 millimeters. A set of experiments with spin-coated SU-8 5 and SU-8 2005 is performed. The edge-bead, originating from spin-coating of the viscous material, leads to leakage at the connection with the support-ring of the DRIE-system. This prevents the system from reaching the low pressure required for etching.
The best option is to use DuPont MX5000 foil, which is applied by means of lamination. This foil is selected for the fabrication process because it withstands low temperatures, causes no edge-bead problems and has sufficient thickness to cover the 10µm high devices. Experiments with a 20µm polymer film at -40°C show no degradation. Due to the insulating properties of the foil, the wafer temperature can be higher than -40°C, possibly affecting the etch profile. Removal of the MX5000 foil is done by an O_2 plasma.

Chapter 4

Device characterisation

This chapter describes the characterisation of the cantilevers and tips. Section 4.1 is devoted to the cantilever ridge height. The sharpness of the tips is verified by (HR-)SEM images in section 4.2. Uniformity is evaluated by means of approach-curve measurements (section 4.3) and by measuring the resonance frequency of different cantilevers in one array (section 4.4).

4.1 Ridge height

Special measurement structures enabled measuring the ridge height as a function of the angle with respect to the ⟨110⟩ direction. Ridge height (RH) is measured by performing surface profile measurements on a Veeco Dektak 8. In Figure 4.1 a graph of the normalised ridge height (reduced RH divided by original RH) as a function of angle θ is presented. When angle $\theta = 0°$ (segment $A-B$ is parallel to the ⟨110⟩ direction) the ridge is not reduced. This means the normalised ridge height is one. In case angle $\theta = 10°$ the ridge at segment $A-B$ is reduced to zero, which means the normalised ridge height is zero. For values of angle θ between 0° and 10°, a linear relation between ridge height and angle θ is revealed.

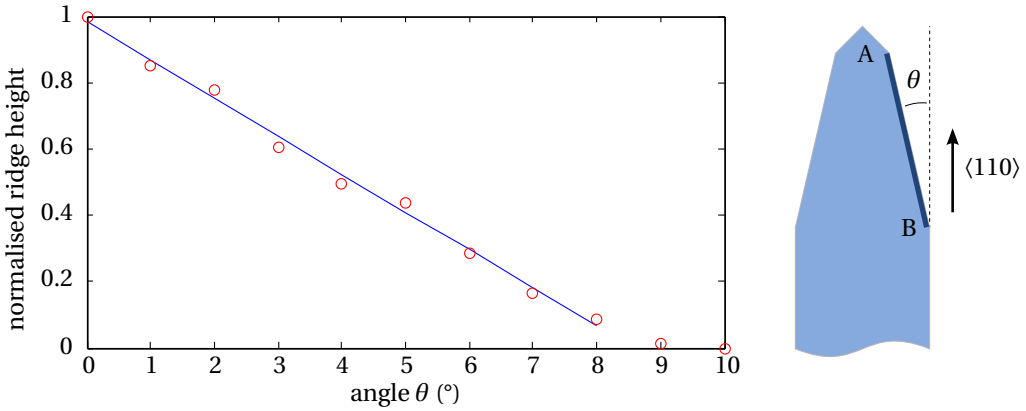
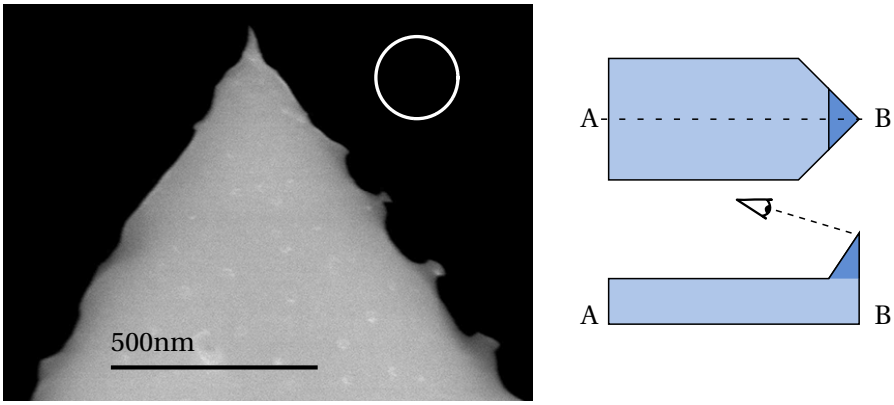


Figure 4.1: Normalised ridge height versus θ. The red points are measurements, the blue line is a linear fit.

Because of the symmetry of the crystal planes in a (100)-wafer, the ridge occurs on sides of the cantilever that make an angle smaller than 10° with any one of the equivalent ⟨110⟩ directions.

4.2 Tip sharpness

SEM images are used to determine the tip radius. In the introduction an indication for the required sharpness was given. Ideally, the tip radius is below ~100nm. Figure 4.2a shows a SEM image of the very end of one of the fabricated tips . The white circle is included as a reference, and has a radius of 100nm. It can be seen that the radius of the tip is below the required 100nm. The radius of the very sharp apex is estimated to be below 10nm.



(a) **(b)**

Figure 4.2: (a) SEM photo of fabricated tip. The white circle has a radius of 100nm. (b) Illustration showing the point of view used in the SEM photo

From the SEM image it also becomes apparent that the edges that are visible in Figure 4.2a reveal a certain roughness in the order of 50nm. This roughness originates from the dry etch through the device layer (step (f) in section 3.1). As a result of the roughness, the outline of the tip fluctuates, leading to some tips being sharper than others. This is an unwanted effect, since uniform tips are preferred.
Figure 4.3 is a SEM image of another tip from the opposite side. The white circle is included as a reference, and has a radius of 100nm. The radius of this tip is also below the required 100nm. The radius of the apex is estimated to be below 10nm.

4.3 Uniformity of cantilever array

4.3.1 Wafer bow

SOI wafers are known to have a curvature due to the wafer manufacturing process[28]. In Figure 4.4, the wafer bow is illustrated schematically. It is defined as the height difference δ between the centre of the wafer and the edge of the wafer. In this case the wafer is assumed to be in the shape of a shallow spherical cap. In general, the bow is small compared to the wafer thickness t_w, so $\delta \leq \frac{1}{3} t_w$ [28].
While the layer of SiO_2 at the backside reduces the bow caused by stress at the BOX−Si interfaces, the final chips do not have this SiO_2 layer to compensate stress. This can result in a bow of the chips, which are 1.6 × 3.2 mm. In the extreme case that the wafer bow $\delta = \frac{1}{3} t_w \approx 130.2\mu$m, we calculated a corresponding chip bow of 33nm. In this calculation, only the bow over the width of the chip (1.6mm) is relevant, since this will affect the measurable array uniformity. The bow over the length of the chip is neglected. A bow of 33nm over the width of the chip corresponds to a bow of 0.5nm

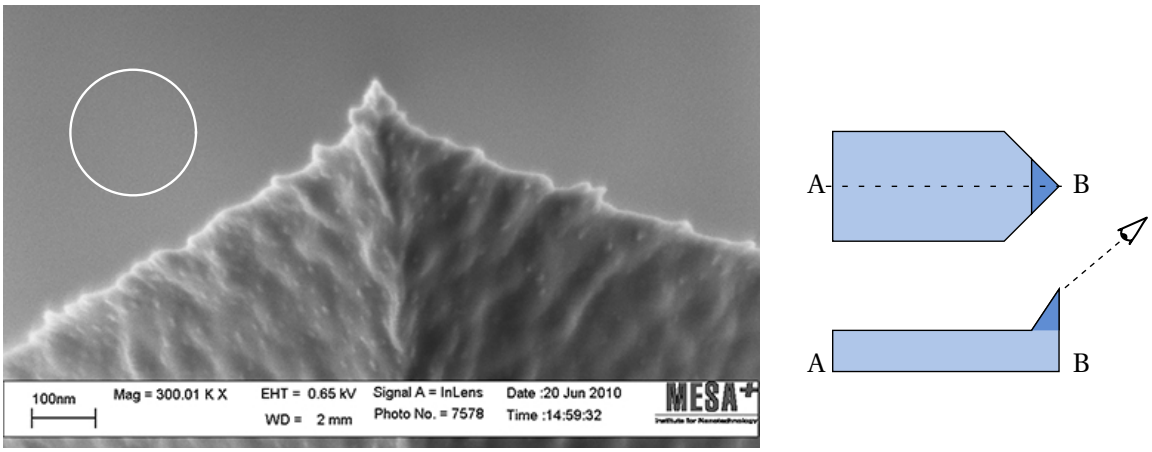


Figure 4.3: (a) SEM photo of fabricated tip. The white circle has a radius of 100nm. (b) Illustration showing the point of view used in the SEM photo.

over a 200µm wide array. In this case the cantilever in the middle is located at a height difference of 0.5nm with the outermost cantilevers. Details of the calculations regarding the bow over the chip are located in Appendix C.2.

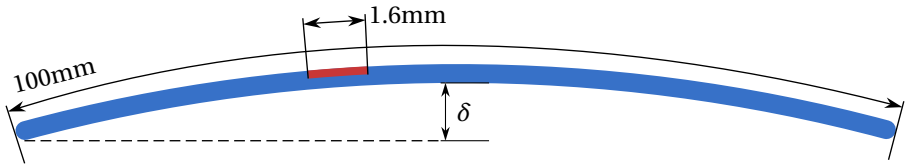


Figure 4.4: Schematic representation of wafer bow δ with chip indicated (not to scale)

The bow of several of the fabricated chips is inspected by means of white light interferometer measurements. Topography over almost 1mm of the width of the chip is measured. In order to remove any offset and linear slope from the measured data, linear regression is applied to the outermost parts ($0-30$µm and $970-1000$µm) of the data. This operation is allowed because we are interested in the bow of the chip. The linear regression perfectly aligns the chip with the interferometer, resulting in the topography of the chip. No significant bow over the width of the chips was detected, which is in agreement with the calculations above. The deflection has a maximum variation of 20nm over approximately 0.9mm, as can be seen in Figure 4.5. This suggests that the absence of the SiO_2 layer at the backside of the chips does not cause any measurable bow over the chips.

4.3.2 AFM approach-curves

The method we employ to determine the uniformity of the array takes advantage of the force spectroscopy capabilities of an AFM. Unlike in imaging mode, raster-scanning is disabled in this procedure. A chip with a cantilever array is inserted into the AFM. The laser spot is then aligned with one of the cantilevers. Now when the complete array is moved towards the surface of a flat sample, the deflection does not change as long as the sample is out of reach (A in Figure 4.6). When the tip comes into contact with the sample a deflection is detected (B in Figure 4.6). This point is

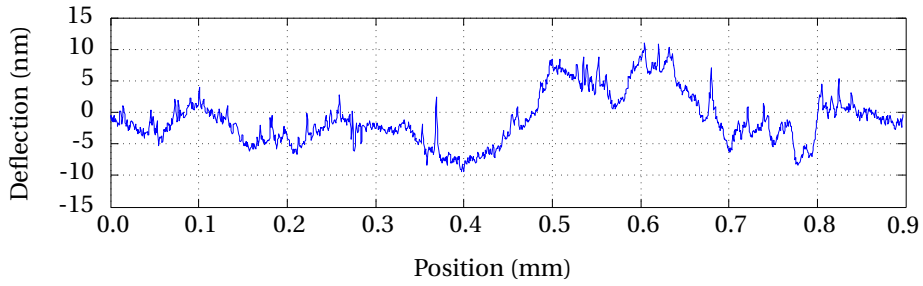


Figure 4.5: Deflection over the width of chip 134: no bow is observed.

called the point of contact (POC). From this point on, the bending of the cantilever causes a change in deflection, which is measured by the PSD. By aiming the laser spot on all of the cantilevers one by one and making the array approach the sample, the POC of every cantilever can be measured. The distribution of the POCs of the cantilevers is a measurement of the variation in tip-sample separation. The total displacement of the array during an approach is called the ramp. As flat sample, a Si wafer is used. This way both tip and sample are of the same material, and the stiffness of the sample is larger than the stiffness of the cantilever.

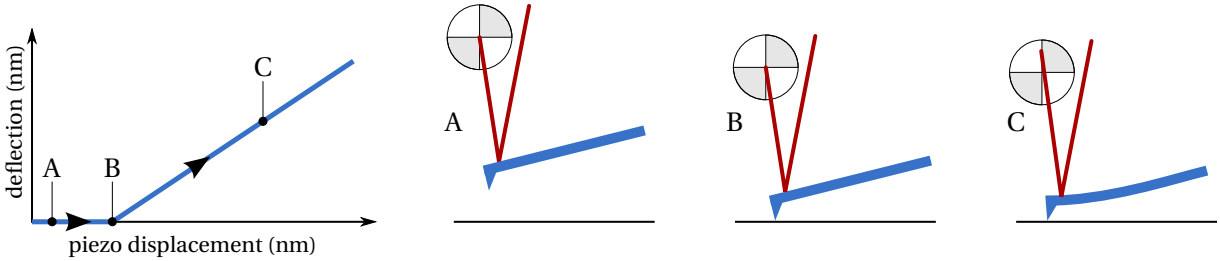


Figure 4.6: A typical approach-curve. Point B is known as the point of contact (POC)

A large number of sources of non-uniformity amount to this type of measurement. For example, differences in the bending of cantilevers, differences in cantilever length and differences in tip height all contribute to the measured POCs. The results are thereby a nonspecific indication of uniformity.

Drift

The displacement is controlled by a piezoelectric tube, and such elements are known to experience drift. In order to get an estimate of the drift during the measurements, the drift was examined over a period of 10 minutes. Approaches were continuously performed (ones every second) with a ramp size of 500nm. The approach-curve was captured every minute, resulting in the graph in Figure 4.7. Although the linear fit suggests there is almost no drift, the difference between successive measurements is several nanometers. The estimated drift is approximately 6nm/min. Measuring the POCs of an array of five cantilevers takes about one minute.

Reproducibility

The approach-curve measurements were checked on reproducibility. The results of different measurements on chip134 are shown in Figure 4.8. Measurement B is acquired five days after measure-

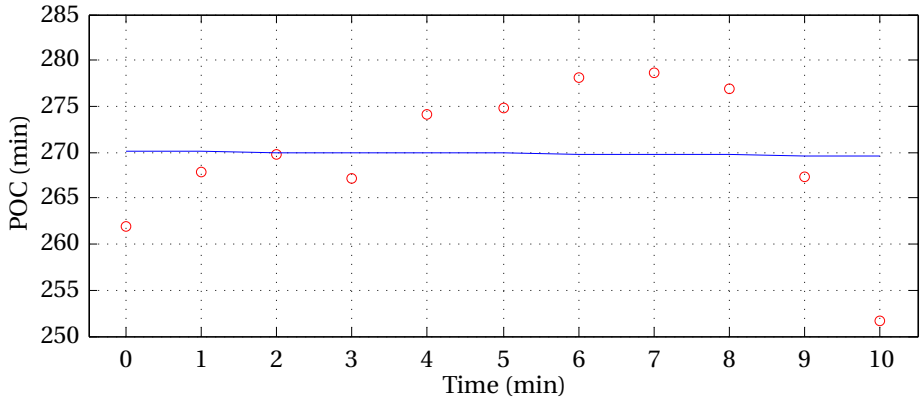


Figure 4.7: Drift in approach-curve measurements. The red points are measuments, the blue line is a linear fit.

ment A. This means the chip and the sample are removed from the AFM in between the experiments. Nevertheless, the obtained POCs of measurement B match the POCs of measurements A within 10nm. The greatest deviation occurs at cantilever 3, where it is 7 ± 2nm. In case two sets of approach-curves are measured successively, the results are consistent. Moreover, when a second experiment is performed several days after the first one, no inconsistencies are found.

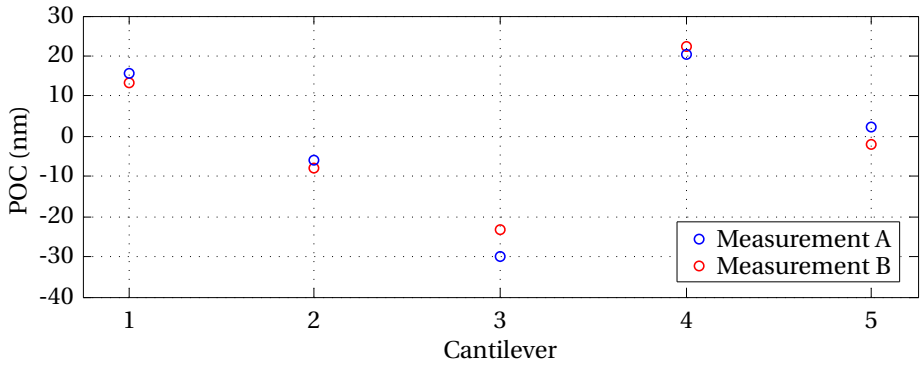


Figure 4.8: Two measurements of chip 134 on different days

Measurement results

Figure 4.9a shows the approach-curve measurements of all five cantilevers within one array – the array of chip 134. At the points of contact, snap-in of the probes is measured (see Figure 4.9b for an example). This snap-in effect occurs as a result of the attractive van der Waals force. Since the experiments are performed in ambient conditions, a thin film of water is present on the Si sample and the Si tip. The capillary force of this water layer also attracts the tip towards the sample.
The points of contact of the cantilevers can be extracted from the approach-curves. For the same chip that was measured in Figure 4.9, they are plotted in Figure 4.10.
A linear increase is observable. This is caused by the effect mentioned in section 2.2.7: the chip is never placed in such a way that the array is aligned perfectly parallel to the sample. This situation is illustrated in Figure 4.10b. The way to compensate for this effect is by correcting the data using a linear fit (like the blue line in Figure 4.10a). This mathematical operation is in fact the same as

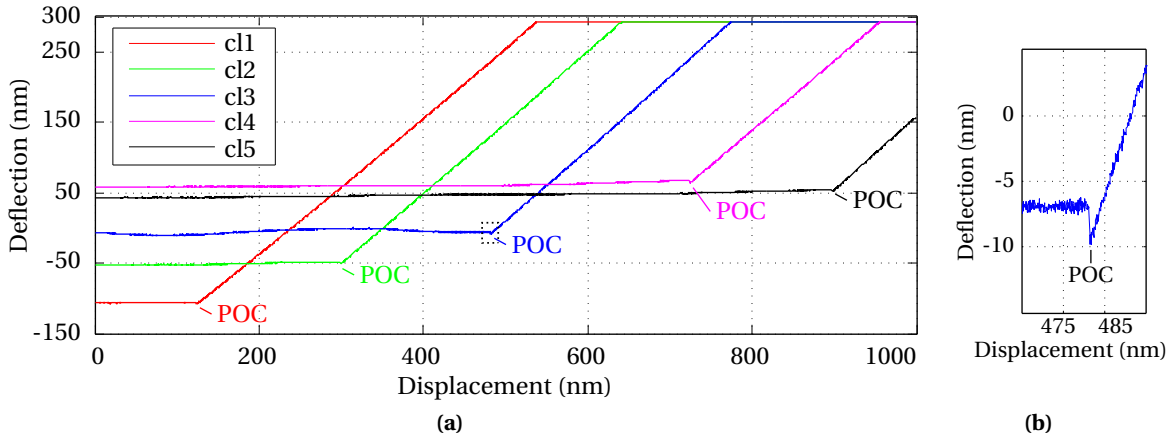


Figure 4.9: (a) Approach-curve measurements of cantilever 1 through 5 of chip #134 - the POCs are indicated (b) Enlarged view of cantilever 3 around POC showing snap-in

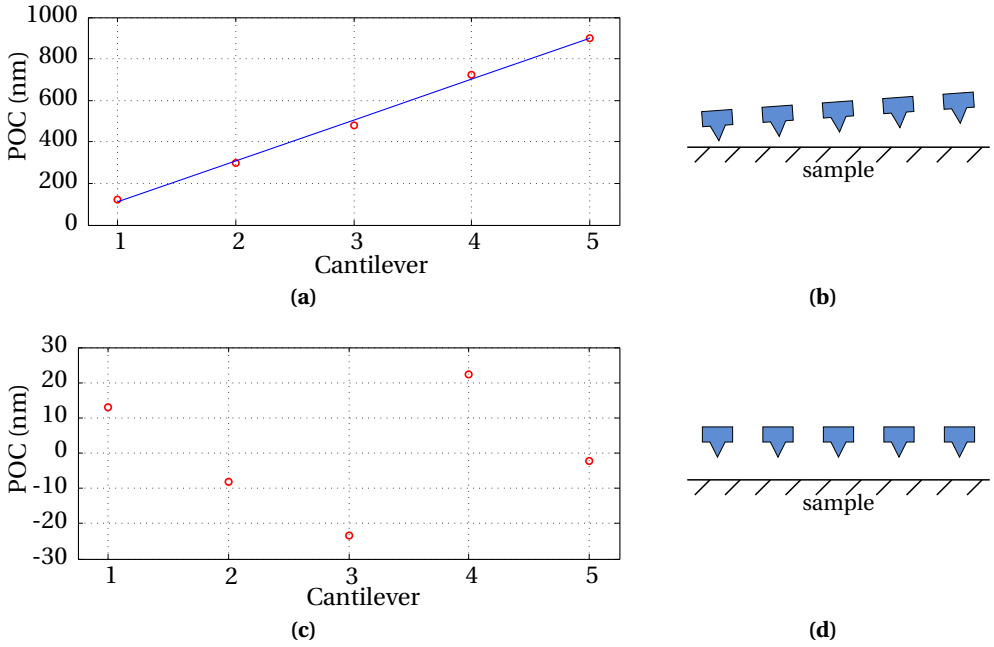


Figure 4.10: (a) The POCs of the cantilever array of chip #134. The red data points are the POCs as seen in Figure 4.9, the blue line is a linear fit. (b) The equivalent situation before correction (c) Corrected POCs of the cantilever array of chip #134. (d) The equivalent situation after correction.

perfectly aligning the array with the sample. The result is presented in Figure 4.10c. The highest (relative) POC is 20 ± 2nm while the lowest (relative) POC is -30 ± 2nm. This results in a range of 50 ± 4nm over an array having a total width of 190µm. Using the linear fit to compensate for misalignment has another advantage. If the drift of the piezoelectric tube is linear, it will be cancelled out together with the slope contained in the measurement data.

Figure 4.11 shows the corrected POCs of two other arrays. The results of five different arrays are organised in Table 4.1. As expected, more variation is measured in arrays with greater width. This is expected, because many sources of non-uniformity scale with the array width. The length of cantilevers does not seem to have a significant influence on uniformity. This suggests no significant

differences in cantilever bow exist. Remarkable is the rotated chip showing a disproportionate higher non-uniformity. It is not clear what causes this. No increased variation in cantilever thickness, cantilever bending or tip height is expected. Variation in cantilever length can be caused by the rotation, because the free ends of the cantilevers are not parallel to the scanlines of the laser writer. SEM inspection revealed that length differences are under 1µm. Using $\alpha = 10°$, it can be calculated that 1µm difference in length results in a change in POC of $1 \times \tan(10°) \approx 0.2$µm. This can explain the increased variation in tip-sample separation for rotated chips.

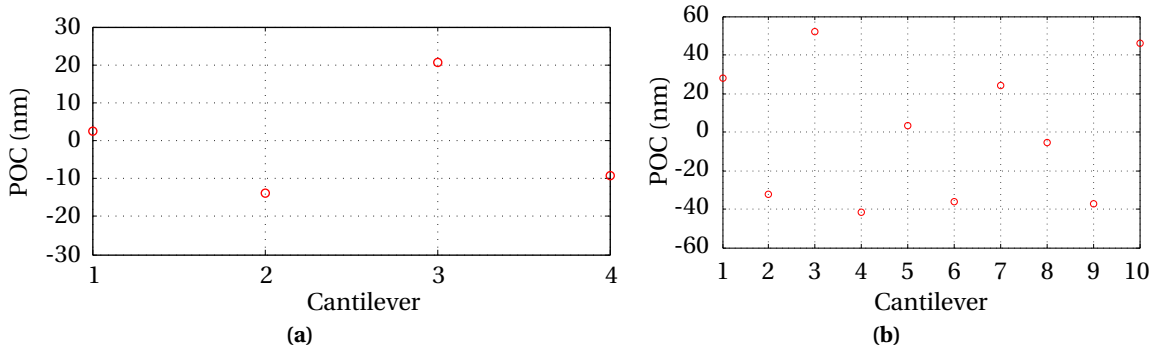


Figure 4.11: Variation in POCs of cantilevers on (a) chip 264 (b) chip 282

Table 4.1: Parameters of five characterised chips

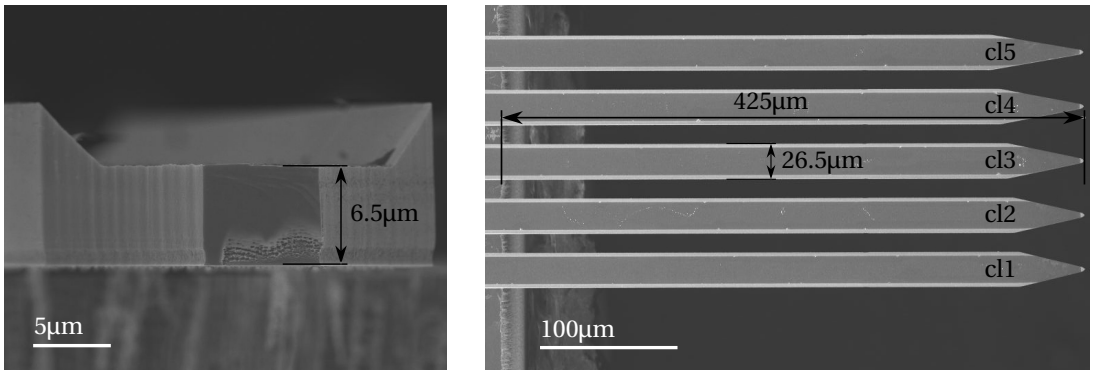
Parameter	chip #108	chip #134	chip #264	chip #282	chip #355
number of cantilevers	5	5	4	10	10
spacing between cantilevers (µm)	10	10	10	20	10
cantilever width (µm)	30	30	30	25	15
cantilever length (µm)	225	400	300	400	400
array width (µm)	190	190	150	430	240
resonance frequencies (kHz)	175 – 186	54 – 56	113	55	55
cantilever end width (µm)	7	7	7	25	15
cantilever end angle (°)	10 – 14	10 – 14	10	0	0
rotation (°)	0	0	0	0	10
max POC (after levelling)	20 ± 2	22 ± 2	21 ± 2	52 ± 2	58 ± 2
min POC (after levelling)	-41 ± 2	-24 ± 2	-14 ± 2	-42 ± 2	-58 ± 2
range of POCs (after levelling)	61 ± 4	46 ± 4	35 ± 4	94 ± 4	116 ± 4

4.4 Resonance frequency of cantilevers

4.4.1 Measured resonance frequency

Measurements to determine the resonance frequency of cantilevers are performed on a Polytec Micro System Analyser (MSA-400) and the Nanoscope AFM. These measurements show a deviation from the expected resonance frequencies. For example, the resonance response of the middle

cantilever (cl3) of chip 134 showed it has its resonance frequency around 55kHz, while it is designed to be 44kHz.
One of the causes for this deviation is found in the cantilever thickness. SEM inspection shows that the thickness of the cantilever on chip 17 is 6.5µm instead of the 5µm it was designed to be (see Figure 4.12a). Apparently, the duration of the KOH etch was less than five minutes or the etch rate was lower than 1µm/min. The first explanation is the most plausible one and can be caused by a thin layer of SiO_2 or SiRN covering the Si, reducing the time the Si is etched. Since SiRN is etched with a rate under 1nm/hour, a thin layer of SiRN does not seem to be the cause (etching of one monolayer takes much more than 1.5 minute). Considering the etch-rate of SiO_2 in KOH is 180nm/hour, a SiO_2 layer with a thickness of 3nm is etched away after one minute.
Furthermore, the length of the fabricated cantilevers deviate from the design. For the cantilevers on chip 134, the designed length is 400µm while the measured length is 425µm (see Figure 4.12b). This is a deviation of 6.25%. The negative tapered etch profile of the backside etch probably causes this deviation. In the design, the profile of the backside etch is assumed to be perfectly vertical. Because the real profile has a negative taper, the length of cantilevers is increased.



(a) cross section of cantilever - end of cantilever including tip is snapped off (chip 17)

(b) top view of cantilever array (chip 134)

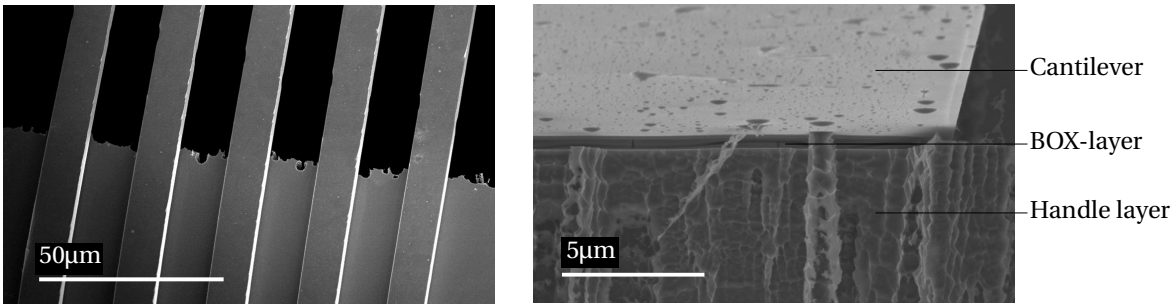
Figure 4.12: SEM images showing (a) thickness of cantilever (b) length and width of cantilever

If the measured cantilever dimensions are used to calculate the resonance frequency, a value of 50kHz is obtained. The difference between this calculated value and the actual resonance frequency is 5kHz. This can be explained by the shape of the fabricated cantilever, which is not rectangular but has a taper at the end. The length of a rectangular cantilever, corresponding to a cantilever with taper similar to cl3, is estimated to be roughly 400µm. In order to have a resonance frequency of 55kHz, a rectangular cantilever having a width of 26.5µm and a thickness of 6.5µm, must have a length of 406µm. The difference between the expected resonance frequency and the resonance frequency of the fabricated cantilever is now resolved.

4.4.2 Variation of resonance frequency within array

The resonance frequencies of all ten cantilevers within the array on chip 282 are measured. The cantilevers are designed to be identical. The measured average resonance frequency is 54.96kHz with a standard deviation of 0.1kHz.
A possible cause for the variation in resonance frequency is the imprecision of the backside etch. As can be seen in Figure 4.13a, the chip-edge created by the backside etch shows roughness. For

the cantilevers to have the same length, the chip-edge should be perfectly straight. The BOX-layer connecting the cantilevers to the handle layer also affects the cantilever length. But due to the vapour HF step, the BOX-layer follows the roughness introduced by the backside etch. This is indicated in Figure 4.13b.



(a) **(b)**

Figure 4.13: (a) SEM image showing chip-edge roughness (chip 17) (b) SEM image of the connection between cantilever and handle layer (chip 358). The edge of the BOX-layer is not straight.

4.5 Conclusions

No ridge is present on the cantilever sides when angle θ is bigger than 10°, where θ is the angle between the ridge and the ⟨110⟩ direction). The angle of ten degrees is used as taper at the cantilever ends to partly remove the ridge.
SEM images are used to examine the tip sharpness. They show that the fabricated tips have a radius of curvature of 10nm, well below the required 100nm.
Approach curves are used to measure the variation of the tip-sample distance. This range falls within the required 100nm for most chips. Chips that are rotated ten degrees with respect to the ⟨110⟩ direction have a bigger range. The range varies from 35 ± 4nm to 116 ± 4nm in the chips that were measured.
The measured resonance frequencies deviate from what they are expected to be. This is because the thickness and length of the cantilevers differ from the thickness and length in the design. The difference in thickness is probably caused by a thin film covering the Si. The KOH first had to etch this layer, hereby reducing the time the Si was etched. The cantilevers are longer because of the negative taper in the backside etch profile.

Chapter 5

Conclusions and recommendations

5.1 Conclusions

In this report, the successful fabrication of silicon micro-cantilever arrays with tips for parallel optical readout experiments is presented. We have developed a powerful SOI-based fabrication process, which has the advantage that both the cantilever and the tip are formed in a single KOH step. The high uniformity of the KOH etch enables fabrication of cantilever arrays with a high uniformity in tip height (±4.3nm on wafer scale) and cantilever thickness (±0.2μm on wafer scale). The variation in tip-sample distance is 35 ± 4nm over a 150μm wide array of four (300μm long) cantilevers and 94 ± 4nm over a 430μm wide array of ten (400μm long) cantilevers. On wafer scale, all arrays show a variation in tip-sample distance smaller than 100nm.

Furthermore, we have achieved a tip sharpness below 10nm radius of curvature. The small radius of the tips is enabled by (I) the inclusion of a sacrificial layer etch to achieve a sharp mask corner (radius < 250nm) by corner sharpening, and (II) obtaining a straight etch profile by pattern transfer of the mask into the device layer. By optimisation of the RIE process, the undercut resulting from etching 10μm of silicon, is limited to 60nm so it does not affect the sharpness of the tips. The undercut does however reduce the uniformity of tip height on wafer scale.

Advantages of using a SOI wafer as substrate are a clean and flat detector side surface of cantilevers for reflectivity, the option to uncouple adjacent cantilevers and the possibility to use DRIE for backside etching.

We have satisfied requirements posed by optical readout experiments and EFM: the variation in tip-sample distance is required to be smaller than 100nm over the complete array (when the array is aligned with the sample). Additionally, the tip sharpness is required to be under 100nm radius of curvature.

During the fabrication, several problems were encountered. During the formation of the tips and cantilevers by etching in KOH, an insufficient thickness of the SiO_2 mask resulted in local tip damage. Increasing the thickness of the SiO_2 mask successfully prevented tip damage. Good thermal contact of the wafer with the electrode during backside DRIE could not be established by the usual procedure, because of the large height of the structures (~10μm). Different approaches have been tested, and the most suitable solution proved to be the use of a foil.

The developed process features a single mask to fabricate cantilever arrays with tips that are self-aligned to the free end of the cantilever. A second mask is used for the backside etch, to release the cantilevers.

5.2 Recommendations

In order to increase the performance of the devices, here are some suggestions to optimise fabrication steps.

Increase tip height uniformity

The variation in tip-sample distance can be further reduced, by increasing the uniformity of the tip height. Figure 5.1 shows a schematic representation of the etch profile at the end of a tip. The tip height over the wafer has a variation due to (I) the KOH-etch non-uniformity in the (111) direction of Si (±4%) and (II) the undercut as a result of pattern transfer into the device layer.
The variation caused by the KOH etch can be reduced by a shorter etch, because the variation scales with the etch time. Because a shorter KOH results in a lower tip height, this option is allowed only if lower tips are permitted (for example if an alternative to EFM is used). Using the device layer thickness as a variable, the spring constant of the cantilevers can be controlled.
By optimising the RIE process, the undercut in the device layer etch can be further reduced. If the undercut can be reduced to zero, the pattern transfer will not be responsible for variation in tip height. Optimising the RIE process will require SEM inspection after every adjustment in the process to examine the result.

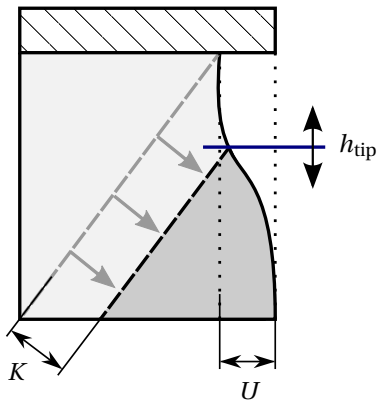


Figure 5.1: Illustration of factors influencing tip height. The tip height h_{tip}, the KOH etch K, and the undercut U are indicated

Better control over tip shape

The fabricated tips show a variation in tip apex shape, which was not expected. This variation is caused by roughness on the planar surfaces of the tip and is in the order of tens of nanometers. The roughness is an inevitable result of the cryogenic RIE process that is used to etch the device layer. The roughness can be reduced by increasing the duration of the dry thermal oxidation in step (j). Four SOI wafers that have undergone all process steps prior to step (k) are available for this.

Tips with higher aspect ratio

By reducing the angle η (see Figure 5.2a) at the free end of the cantilever, tips with a higher aspect ratio can be fabricated. A higher aspect ratio tip will increase the resolution in EFM measurements. Also, a high aspect ratio is beneficial when the tip is used in AFM for probing samples with steep

trenches and inclined sidewalls. Figure 5.2a shows the end angle η as applied in the fabricated cantilevers. When a smaller end angle η is used (as in Figure 5.2b), the width of the tip is reduced while the height is maintained. The opening angle has a lower limit of 20 degrees, since below this value the ridge emerges.

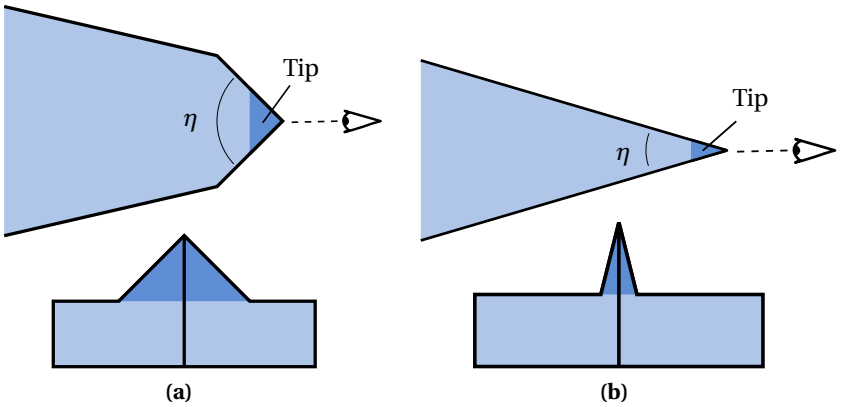


Figure 5.2: (a) Top and front view of cantilever (end angle η is 90°) (b) Top and front view of cantilever (end angle η is 32°)

Cantilevers with lower spring constants

The cantilever thickness of 6.5µm results in the spring constant being higher than it is designed be. The cantilever thickness can be reduced very easily by increasing the KOH etch duration. This way, cantilevers with lower spring constants can be fabricated. We experienced that after 5 minutes of KOH etching, 3.5µm instead of the expected 5µm of Si was removed. We therefore strongly advise to use dummy wafers to determine the etch time required for the desired cantilever thickness.

Glossary

µSpam	Micro Scanning Probe Array Memory
AFM	Atomic Force Microcopy
BHF	Buffered Hydrogen Fluoride
BOX	Buried Oxide
DRIE	Deep Reactive Ion Etching
EFM	Electric Force Microscopy
FIB	Focused Ion Beam
H_3PO_4	Phosphoric Acid
LOCOS	Local Oxidation of Silicon
MEMS	MicroElectroMechanical Systems
POC	Point Of Contact
ProTeM	Probe-based Terabit Memory
PSD	Position Sensitive Detector
RH	Ridge Height
RIE	Reactive Ion Etching
SiRN	Silicon Rich Nitride
SOI	Silicon On Insulator
SPM	Scanning Probe Microscopy
TEOS	Tetraethyl Orthosilicate
TST	Transducers Science and Technology
VdV	Van der Waals force

Bibliography

[1] Seagate, *Webpage on Barracuda® Desktop Hard Drive Specifications*, June 2010. [Online]. Available: http://www.seagate.com/www/en-us/products/desktops/barracuda_hard_drives/#tTabContentSpecifications

[2] M. H. Kryder and C. S. Kim, "After hard drives-what comes next?" *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 3406 – 3413, 2009. [Online]. Available: http://dx.doi.org/10.1109/TMAG.2009.2024163

[3] G. Binnig, C. Quate, and C. Gerber, "Atomic force microscope," *Phys. Rev. Lett. (USA)*, vol. 56, no. 9, pp. 930 – 3, 1986. [Online]. Available: http://dx.doi.org/10.1103/PhysRevLett.56.930

[4] M. Tortonese, H. Yamada, R. Barrett, and C. Quate, "Atomic force microscopy using a piezoresistive cantilever," *TRANSDUCERS '91. 1991 International Conference on Solid-State Sensors and Actuators. Digest of Technical Papers (Cat. No.91CH2817-5)*, pp. 448 – 51, 1991//. [Online]. Available: http://dx.doi.org/10.1109/SENSOR.1991.148908

[5] Y.-S. Kim, H.-J. Nam, S.-M. Cho, J.-W. Hong, D.-C. Kim, and J. Bu, "Pzt cantilever array integrated with piezoresistor sensor for high speed parallel operation of afm," *Sens. Actuators A, Phys. (Switzerland)*, vol. A103, no. 1-2, pp. 122 – 9, 2003. [Online]. Available: http://dx.doi.org/10.1016/S0924-4247(02)00311-4

[6] E. Eleftheriou, T. Antonakopoulos, G. Binnig, G. Cherubini, M. Despont, A. Dholakia, U. Durig, M. Lantz, H. Pozidis, H. Rothuizen, and P. Vettiger, "Millipede - a mems-based scanning-probe data-storage system," *IEEE Trans. Magn. (USA)*, vol. 39, no. 2, pp. 938 – 45, 2003. [Online]. Available: http://dx.doi.org/10.1109/TMAG.2003.808953

[7] H. Mamin and D. Rugar, "Thermomechanical writing with an atomic force microscope tip," *Appl. Phys. Lett. (USA)*, vol. 61, no. 8, pp. 1003 – 5, 1992. [Online]. Available: http://dx.doi.org/10.1063/1.108460

[8] G. Meyer and N. Amer, "Novel optical approach to atomic force microscopy," *Appl. Phys. Lett. (USA)*, vol. 53, no. 12, pp. 1045 – 7, 19 Sept. 1988. [Online]. Available: http://dx.doi.org/10.1063/1.100061

[9] H. P. Lang, M. Hegner, and C. Gerber, "Cantilever array sensors," *Materials Today*, vol. 8, no. 4, pp. 30 – 36, 2005. [Online]. Available: http://dx.doi.org/10.1016/S1369-7021(05)00792-3

[10] W. W. Koelmans, J. W. van Honschoten, P. Vettiger, L. Abelmann, and M. C. Elwenspoek, "Parallel optical readout of a cantilever array in dynamic mode," *Proceedings of the International Workshop on Nanomechanical cantilever sensors, Jeju, South Korea*, May 2009. [Online]. Available: http://purl.org/utwente/67989

[11] F. Battiston, J.-P. Ramseyer, H. Lang, M. Baller, C. Gerber, J. Gimzewski, E. Meyer, and H.-J. Guntherodt, "A chemical sensor based on a microfabricated cantilever array with simultaneous resonance-frequency and bending readout," *Sens. Actuators B, Chem. (Switzerland)*, vol. B77, no. 1-2, pp. 122 – 31, 2001. [Online]. Available: http://dx.doi.org/10.1016/S0925-4005(01)00683-9

[12] J. Colchero, A. Gil, and A. Baro, "Resolution enhancement and improved data interpretation in electrostatic force microscopy," *Phys. Rev. B, Condens. Matter (USA)*, vol. 64, no. 24, pp. 245 403 – 1, 2001. [Online]. Available: http://dx.doi.org/10.1103/PhysRevB.64.245403

[13] M. Kitazawa and A. Toda, "Fabrication of sharp tetrahedral probes with platinum coating," *Japanese journal of applied physics. Pt. 1, Regular papers & short notes*, vol. 41, no. 7, pp. 4928–4931, July 2002. [Online]. Available: http://ci.nii.ac.jp/naid/110006341640/en/

[14] M. Guggisberg, M. Bammerlin, C. Loppacher, O. Pfeiffer, A. Abdurixit, V. Barwich, R. Bennewitz, A. Baratoff, F. Meyer, and H.-J. Guntherodt, "Separation of interactions by noncontact force microscopy," *Phys. Rev. B, Condens. Matter (USA)*, vol. 61, no. 16, pp. 11 151 – 5, 2000. [Online]. Available: http://dx.doi.org/10.1103/PhysRevB.61.11151

[15] G.-W. Hsieh, C.-H. Tsai, W.-C. Lin, C.-C. Liang, and Y.-W. Lee, "Bond-and-transfer scanning probe array for high-density data storage," *IEEE Trans. Magn. (USA)*, vol. 41, no. 2, pp. 989 – 91, 2005. [Online]. Available: http://dx.doi.org/10.1109/TMAG.2004.842070

[16] M. Lutwyche, C. Andreoli, G. Binnig, J. Brugger, U. Drechsler, W. Haberle, H. Rohrer, H. Rothuizen, P. Vettiger, G. Yaralioglu, and C. Quate, "55 2d afm cantilever arrays a first step towards a terabit storage device," *Sensors and Actuators, A: Physical*, vol. 73, no. 1-2, pp. 89 – 94, 1999. [Online]. Available: http://dx.doi.org/10.1016/S0924-4247(98)00259-3

[17] D. Saya, K. Fukushima, H. Toshiyoshi, G. Hashiguchi, H. Fujita, and H. Kawakatsu, "Fabrication of single-crystal si cantilever array," *Sensors and Actuators, A: Physical*, vol. 95, no. 2-3, pp. 281 – 287, 2002. [Online]. Available: http://dx.doi.org/10.1016/S0924-4247(01)00742-7

[18] D. Kobayashi, Y. Mita, T. Shibata, T. Bourouina, and H. Fujita, "Batch bulk-micromachined high-precision metal-on-insulator microspires and their application to scanning tunneling microscopy," *Journal of Micromechanics and Microengineering*, vol. 14, no. 9, pp. S76 – S81, 2004. [Online]. Available: http://dx.doi.org/10.1088/0960-1317/14/9/013

[19] H. Bhaskaran, A. Sebastian, U. Drechsler, and M. Despont, "Encapsulated tips for reliable nanoscale conduction in scanning probe technologies," *Nanotechnology*, vol. 20, no. 10, p. 105701, 2009. [Online]. Available: http://stacks.iop.org/0957-4484/20/i=10/a=105701

[20] Z. Yang, X. Li, Y. Wang, H. Bao, and M. Liu, "Micro cantilever probe array integrated with piezoresistive sensor," *Microelectron. J. (UK)*, vol. 35, no. 5, pp. 479 – 83, 2004. [Online]. Available: http://dx.doi.org/10.1016/j.mejo.2003.12.001

[21] O. Wolter, T. Bayer, and J. Greschner, "Micromachined silicon sensors for scanning force microscopy," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom. (USA)*, vol. 9, no. 2, pp. 1353 – 7, 1991. [Online]. Available: http://dx.doi.org/10.1116/1.585195

[22] T. R. Albrecht, S. Akamine, T. E. Carver, and C. F. Quate, "Microfabrication of cantilever styli for the atomic force microscope," *Journal of Vacuum Science & Technology A:*

Vacuum, Surfaces, and Films, vol. 8, no. 4, pp. 3386–3396, 1990. [Online]. Available: http://dx.doi.org/10.1116/1.576520

[23] E. Sarajlic, C. Yamahata, and H. Fujita, "Towards wet anisotropic silicon etching of perfect pyramidal pits," *Microelectronic Engineering*, vol. 84, no. 5-8, pp. 1419 – 1422, 2007. [Online]. Available: http://dx.doi.org/10.1016/j.mee.2007.01.250

[24] Y. Zhao, "High-resolution stamp fabrication by edge lithography," Ph.D. dissertation, University of Twente, Zutphen, May 2010. [Online]. Available: http://dx.doi.org/10.3990/1.9789036530361

[25] R. van Kampen and R. Wolffenbuttel, "Effects of 110-oriented corner compensation structures on membrane quality and convex corner integrity in (100)-silicon using aqueous koh," *J. Micromech. Microeng. (UK)*, vol. 5, no. 2, pp. 91 – 4, 1995. [Online]. Available: http://dx.doi.org/10.1088/0960-1317/5/2/008

[26] R. Marcus and T. Sheng, "The oxidation of shaped silicon surfaces," *J. Electrochem. Soc. (USA)*, vol. 129, no. 6, pp. 1278 – 82, 1982.

[27] R. Marcus, T. Ravi, T. Gmitter, K. Chin, D. Liu, W. Orvis, D. Ciarlo, C. Hunt, and J. Trujillo, "Formation of silicon tips with 1 nm radius," *Appl. Phys. Lett. (USA)*, vol. 56, no. 3, pp. 236 – 8, 1990. [Online]. Available: http://dx.doi.org/10.1063/1.102841

[28] K. Turner and S. Spearing, "Modeling of direct wafer bonding: effect of wafer bow and etch patterns," *J. Appl. Phys. (USA)*, vol. 92, no. 12, pp. 7658 – 66, 2002/12/15. [Online]. Available: http://dx.doi.org/10.1063/1.1521792

Appendix A

Experimental data

A.1 Properties of SOI wafers

An overview of properties of the SOI wafers used in this research is presented in Table A.1

Table A.1: SOI properties

Property	Value
Type / dopant:	P / B
Orientation:	(100)
Diameter:	100 ± 0.1mm
Device thickness:	10 ± 0.5µm
Device resistivity	0.01 - 0.02Ω
Handle thickness:	380 ± 5µm
Handle resistivity:	1 - 20Ω
Box: ON D	0.5µm ± 5%

A.2 Deposition

Spin coating Uniform layers of positive photoresist (Olin 907-17 and Olin 908-35) and negative photoresist (SU-8) are obtained by spin-coating. All layers are coated on Delta 20 spin-coaters. Olin 907-17 is spin-coated at 4000rpm, resulting in a thickness of 1.7µm. Olin 908-35 is also spin-coated at 4000rpm, resulting in a thickness of 3.5µm. SU-8 5 and SU-8 2005 are spin-coated at 1000rpm resulting in a thickness of approximately 13µm.

Spray coating AZ4999 is spray-coated using a Süss MicroTec Delta Altaspray. The recipe used was *4Layer_Nozzle1*. This program sprays four layers onto the wafer, rotating the wafer 90 degree between every layer. This way a uniform coating is achieved. Parameters: N_2 pressure = 1bar, flowrate = 3.5/min, speed = 180mm/sec, width = 100mm, pitch = 3mm. This recipe produces a layer thickness of ±6.2µm. Thicker layers are obtained by performing the program multiple times.

Dry oxidation of silicon Silicon is dry oxidised using an Amtech Tempress Omega Junior system (named *A2* in the Mesa+ cleanroom). The gases available in the system are O_2 and N_2. The standby temperature is 700°C and the maximum temperature is 1150°C. The temperature used for dry oxidation is 950°C. Ramping up and down is done in steps of 2°C/min while N_2 continuously flushes the system. At the desired temperature, 0_2 is released into the system.

LPCVD of silicon rich nitride SiRN is deposited by means of an Amtech Tempress Diffusion system (named G4 in the Mesa+ cleanroom). The standby temperature is 700°C. Deposition is performed at a temperature of 850°C and a pressure of 200mTorr. Gas flow of SiH_2Cl_2 (150sccm) and NH_3 (50sccm) result in a deposition rate of 10nm/min.

LPCVD of TEOS TEOS SiO_2 is deposited by way of an Amtech Tempress Omega Junior system (named B4 in the Mesa+ cleanroom). The standby temperature is 600°C. Deposition is achieved at a temperature of 700°C and pressure of 200mTorr by pyrolysis of $Si(OC_2H_2$ (with a flow rate of 50sccm). The deposition rate is 10nm/min.

A.3 Dry plasma etching

The Tepla 300 O_2 plasma etching system is used to strip organic materials. Its maximum operating power is 1000W and the pressure inside the chamber is 1mBar. The temperature can not be controlled, but is measured to be around 140°C during operation.
For reactive ion etching, an Elektrotech Twin system PF 340 is used. This machine consists of a parallel-plate system and an RF generator at 13.56MHz. The substrate holder is water cooled at 10°C. The available gases are CHF_3, SF_6 and N_2. The parameters for the etching of SiRN are presented in Table A.2.
The device layer is etched using the Alcatel/Adixen AMS 100 SE DRIE system. This is a dual source system with maximum ICP of 2500W. It also is equipped with two CCP sources: a 300W radio frequency (@13.56MHz) source and a 500W low frequency (@ 25 – 460kHz) source. Both cryogenic (down to -180°C) mixed-mode and room temperature pulsed-mode can be processed. The wafer is mechanically clamped, which allows helium cooling for effective heat transfer. The parameters are listed in Table A.3.
Backside wafer-through etching is achieved using the same Alcatel/Adixen AMS 100 SE DRIE system. The parameters used for this etch are given in Table A.4.

Table A.2: SiRN RIE recipe

Parameter	Value
System	Elektrotech Twin system PF 340
Gas [flow (sccm)]	CHF_3 [25]
	O_2 [5]
Substrate temperature (°C)	10
Power (W)	75
Chamber pressure (mTorr)	10

Table A.3: Cryogenic Si etching recipe

Parameter	Value
System	Alcatel/Adixen AMS 100 SE DRIE system
Gas [flow (sccm)]	SF_6 [15]
	O_2 [13]
Substrate temperature (°C)	-100
He pressure (bar)	10
ICP power (W)	200
CCP (LF) power (W)	20 (20msec ON, 80msec OFF)
Substrate distance from source (mm)	200
Throttle valve position (%)	100

Table A.4: Backside wafer-through etching recipe

Parameter	Value	
System	Alcatel/Adixen AMS 100 SE DRIE system	
	Etch	Deposition
Gas	SF_6	C_4F_8
Flow (sccm)	400	25
Time (sec)	4	0.5
Priority	2	1
APC (%)	15	15
ICP (Watt)	2500	2500
CCP (LF) power (W)	n/a	20 (20msec ON, 80msec OFF)
SH (mm)	110	110
Substrate temperature (°C)	-40	-40
He pressure (bar)	10	10

Appendix B

Lithography masks

B.1 Frontside mask

The frontside mask for the cantilevers and tips is presented in Figure B.1.

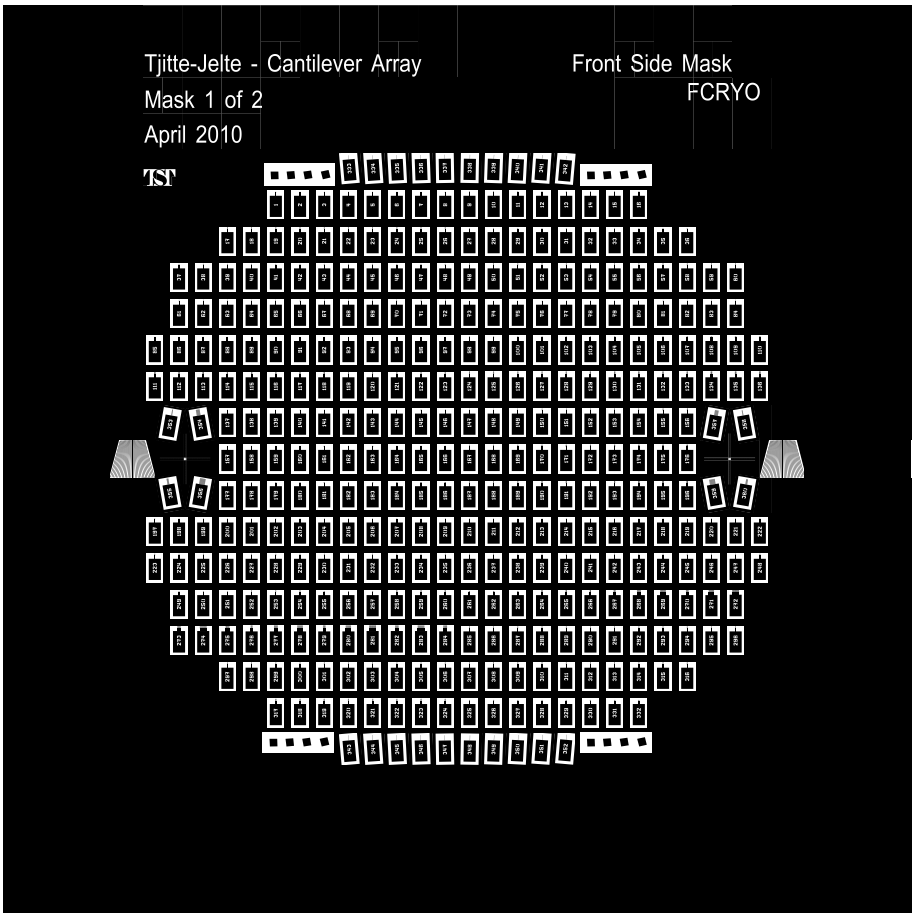


Figure B.1: Frontside mask for pattern transfer into device layer

B.2 Backside mask

The backside mask for the frame and the chips is presented in Figure B.2.

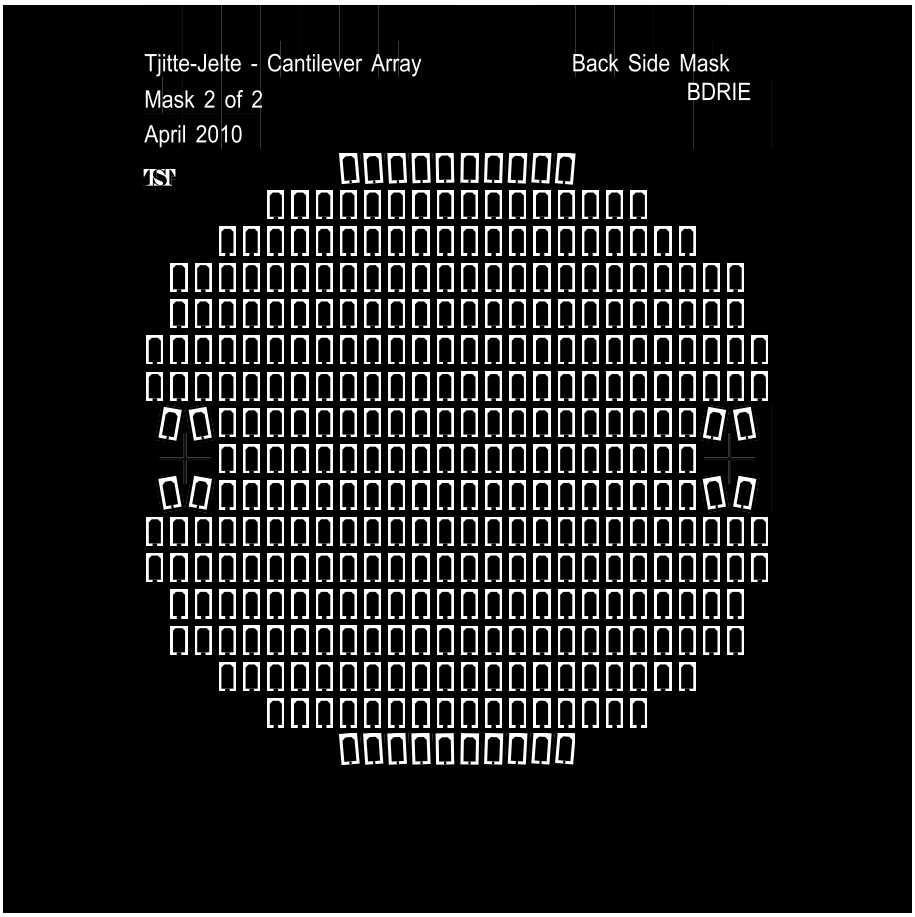


Figure B.2: Backside mask for wafer through etching of handle layer

B.3 Array parameters listed by chip number

Cantilever width = w
Cantilever length = L
Cantilever spacing = S
Cantilever end width = v
Cantilever taper angle = θ
Chip rotation = ψ
Notation x:y:z means from x to z in steps of size y

Table B.1: Array parameters

chip	# CLs	w (µm)	L (µm)	S (µm)	v (µm)	θ (°)	ψ (°)
1 – 8	2	30	150, 150.5	9 : 3 : 30	7	10	0
9 – 16	2	30	225, 227	9 : 3 : 30	7	10	0
17 – 26	2	30	300, 304	12 : 2 : 30	7	10	0

Continued on next page

Table B.1 – continued from previous page

chip	# CLs	w (µm)	L (µm)	S (µm)	v (µm)	θ (°)	ψ (°)
27 – 36	2	30	150, 150.5	12 : 2 : 30	7	10	0
37 – 48	2	30	225, 227	8 : 2 : 30	7	10	0
49 – 60	2	30	300, 304	8 : 2 : 30	7	10	0
61 – 72	1	30:2:52	300	-	7:2:29	10	0
73 – 84	1	30	150:15:300	-	7	10	0
85 – 87	5	30	150	10	7	10, 11, 12, 13, 14	0
88 – 92	4	30	150	10	7	10, 11, 12, 13	0
93 – 97	3	30	150	10	7	11, 12, 13	0
98 – 102	3	30	225	10	7	11, 12, 13	0
103 – 107	4	30	225	10	7	10, 11, 12, 13	0
108 – 110	5	30	225	10	7	10, 11, 12, 13 , 14	0
111 – 113	5	30	300	10	7	10, 11, 12, 13 , 14	0
114 – 118	4	30	300	10	7	10, 11, 12, 13	0
119 – 123	3	30	300	10	7	11, 12, 13	0
124 – 128	3	30	400	10	7	11, 12, 13	0
129 – 133	4	30	400	10	7	10, 11, 12, 13	0
134 – 136	5	30	400	10	7	10, 11, 12, 13 , 14	0
137 – 146	1	30:5:75	150	10	7:5:52	10	0
147 – 156	1	30:5:75	300	10	7:5:52	10	0
157 – 166	2	30:5:75	150, 150.5	10	7:5:52	10	0
167 – 176	2	30:5:75	300, 304	10	7:5:52	10	0
177 – 186	2	30:5:75	150, 150.5	10	7:5:52	10	0
187 – 196	2	30:5:75	300, 304	10	7:5:52	10	0
197 – 199	2	30	150	5	7	10 , 20	0
200 – 204	2	30	150	10	7	10 , 20	0
205 – 209	2	30	150	15	7	10 , 20	0
210 – 214	2	30	150	20	7	10 , 20	0
215 – 219	2	30	150	25	7	10 , 20	0
220 – 222	2	30	150	30	7	10 , 20	0
223 – 225	2	30	300	5	7	10 , 20	0
226 – 230	2	30	300	10	7	10 , 20	0
231 – 235	2	30	300	15	7	10 , 20	0
236 – 240	2	30	300	20	7	10 , 20	0
241 – 245	2	30	300	25	7	10 , 20	0
246 – 248	2	30	300	30	7	10 , 20	0
249 – 251	2	30	150	10	7	10	0
252 – 254	2	30	300	10	7	10	0
255 – 257	3	30	150	10	7	10	0
258 – 260	3	30	300	10	7	10	0
261 – 263	4	30	150	10	7	10	0
264 – 266	4	30	300	10	7	10	0
267	10	15	300	10	15	0	0
268	20	15	300	10	15	0	0
269	30	15	300	10	15	0	0
270	10	20	300	15	20	0	0
271	20	20	300	15	20	0	0
272	30	20	300	10	20	0	0
273	10	25	300	20	25	0	0
274	20	25	300	20	25	0	0
275	10	30	300	20	30	0	0
276	10	15	400	10	15	0	0
277	20	15	400	10	15	0	0
278	30	15	400	10	15	0	0

Continued on next page

Table B.1 – continued from previous page

chip	# CLs	w (µm)	L (µm)	S (µm)	v (µm)	θ (°)	ψ (°)
279	10	20	400	15	20	0	0
280	20	20	400	15	20	0	0
281	30	20	400	10	20	0	0
282	10	25	400	20	25	0	0
283	20	25	400	20	25	0	0
284	10	30	400	20	30	0	0
285 – 296	2	30	300, 302	38:2:60	7	10	0
297 – 306	2	30	300, 310	42:2:60	7	10	0
307 – 316	2	30	300, 320	42:2:60	7	10	0
317 – 324	3	30	300, 304, 308	39:3:60	7	10	0
325 – 332	3	30	150, 150.5, 151	39:3:60	7	10	0
333 – 337	1	25	150	-	25	0	1:1:5
338 – 342	1	25	150	-	25	20	-5:1:-1
343 – 347	1	25	300	-	25	0	1:1:5
348 – 352	1	25	300	-	25	20	-5:1:-1
353	5	15	400	10	15	0	-10
354	20	15	400	10	15	0	10
355	10	15	400	10	15	0	10
356	30	15	400	10	15	0	-10
357	20	15	300	10	15	0	-10
358	5	15	300	10	15	0	10
359	30	15	300	10	15	0	10
360	10	15	300	10	15	0	-10

Appendix C

Calculations

C.1 Matlab M-Files

C.1.1 Cantilever calculations

For a rectangular cantilever, the following code can be used to calculate resonance frequency and spring constant.

```
t = 3e-6;          % cantilever thickness
l = 225e-6;        % length
w = 30e-6;         % width
E = 169e9;         % youngs modulus of material
rho = 2330;        % density of material

f_Hz = (1/(2*pi))*(1.029*t)/(l^2)*sqrt(E/rho);

k = (E*t^3*w)/(4*l^3); % spring constant

m = l*w*t*rho;   % mass
meff=(33/140)*m; % effective mass

w_res = sqrt(k/meff);
f_res_Hz = w_res/(2*pi); % don't forget the 2pi to go to Hz!
```

C.1.2 Plotting of POCs

After importing the data from the approach-curve measurements and saving the POCs in a variable, the following code plots the POCs, a linear fit and the leveled POCs.

```
num = 10;                  % number of cantilevers
varname = chip355;         % name of variable

x = filename(1:num,1);
y = filename(1:num,2);
tilt = polyfit(x,y,1);
f = polyval(tilt,x);       % linear fit
```

```
8
9  correction = zeros(1,num);
10 for bla = 1:num;
11 correction(bla) = tilt(2) + tilt(1)*bla;
12 end
13 leveled = y - correction';  % leveled data/POCs (using the linear fit)
14
15 o = plot(x,y,'o');          % plot the POCs
16 set(o,'Color','red')
17 hold on;
18 fit = plot(x,f);            % plot the linear fit
19 set(fit,'Color','blue')
20
21 %p=plot(x,leveled,'o');
22 %set(p,'Color','red')
23 %xx = filename(1:num,1);
24 %yy = filename(1:num,2);
25 %ding = plot(xx,yy,'o');
26 %set(ding,'Color','black');
27
28 hold off;
29 figure;
30 q=plot(x,leveled,'o');      % plot the leveled POCs
31 set(q,'Color','red')
```

C.2 Wafer-bow calculations

Angle at centre theorem

Angle α_1 at the centre of the circle in Figure C.1a is twice angle α_2 at the circumference, as long as both angles stand on arc $A-B$. This means that wherever point C is located on the circle, except on arc $A-B$, $\alpha_1 = 2\alpha_2$.
This can be proved using Figure C.1b:
Because the blue (left) triangle is an isosceles triangle, the two angles 'a' are equal. The sum of the three angles is equal to 180°:

$$2a + c = 180 \Rightarrow c = 180 - 2a \tag{C.1}$$

Because the green (right) triangle is an isosceles triangle, the two angles 'b' are equal. The sum of the three angles is equal to 180°:

$$2b + d = 180 \Rightarrow d = 180 - 2b \tag{C.2}$$

At the centre of the circle, the sum of α_1, c and d is equal to 360°:

$$\alpha_1 + c + d = 360 \Rightarrow \alpha_1 = 360 - c - d \tag{C.3}$$

Now if we insert equation (C.1) and (C.2) into equation (C.3), we obtain

$$\alpha_1 = 360 - (180 - 2a) - (180 - 2b) = 2a + 2b = 2(a + b) \tag{C.4}$$

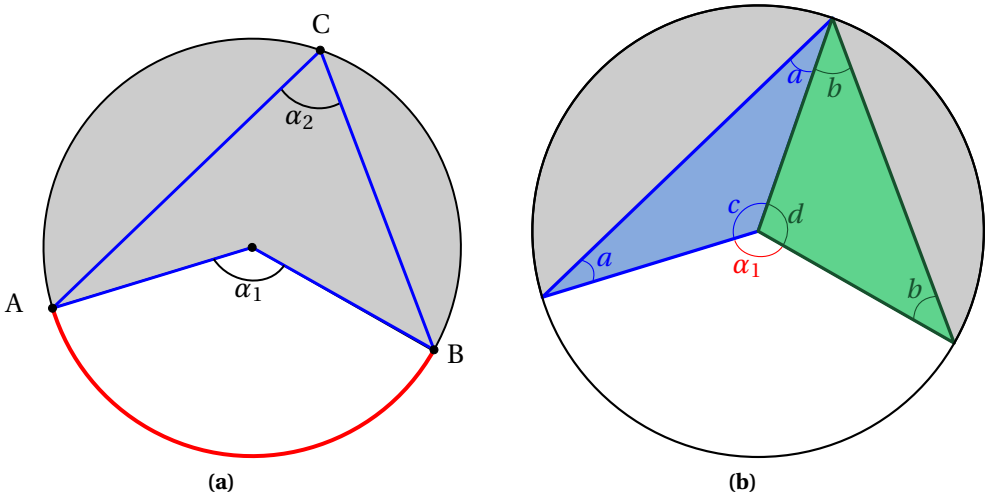


Figure C.1: Angle α_1 is twice angle α_2, as long as both angles stand on arc $A-B$

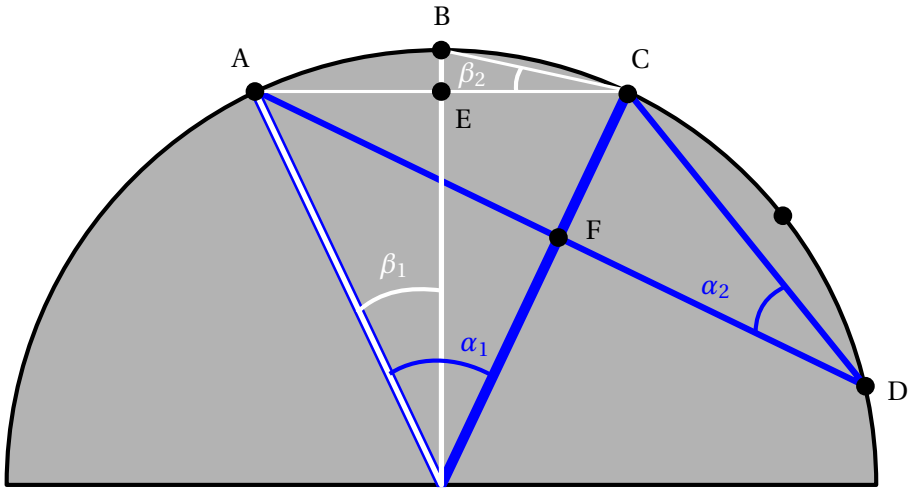


Figure C.2: Because $\alpha_1 = 2\alpha_2$, $\beta_1 = 2\beta_2$ and $\beta_1 = \frac{1}{2}\alpha_1$ it follows that $\beta_2 = \frac{1}{2}\alpha_2$

Because $\alpha_2 = (a+b)$, this is proof that $\alpha_1 = 2\alpha_2$.
Now think of arc $A-D$ as a wafer with bow $C-F$. The bow of half of this wafer (for example arc $A-C$) can be represented by $B-E$. If β_2 is known, the distance between B and E can be calculated using simple trigonometry functions, since distance $A-C$ is also known.
Thanks to the *angle at centre theorem*, we now know that $\alpha_1 = 2\alpha_2$. We also know that $\beta_1 = 2\beta_2$. If $\beta_1 = \frac{1}{2}\alpha_1$ (as is the case in Figure C.2) it follows that $\beta_2 = \frac{1}{2}\alpha_2$.
The bow $B-E$ can now be calculated if distance $A-D$ and distance $C-F$ are known. They are known, since distance $A-D$ is the wafer diameter and distance $C-F$ is the bow.
Analog to this, the bow of a 1.6×10^3µm wide chip can be calculated using wafer diameter = 100×10^3µm and wafer-bow = 130.2µm:

$$\alpha_2 = \tan^{-1}\frac{130.2\mu m}{50\times10^3\mu m} \tag{C.5}$$

$$\gamma_2 = \frac{1.6 \times 10^3 \mu m}{100 \times 10^3 \mu m} \cdot \alpha_2 = 0.016\alpha_2 \tag{C.6}$$

$$\text{bow}_{\text{chip}} = \frac{1}{2} w_{\text{chip}} \cdot \tan(\gamma_2) = 800\mu m \cdot \tan(0.016\alpha_2) \approx 0.0333\mu m = 33.3nm \tag{C.7}$$

And the bow of a cantilever array having a width of 200µm:

$$\text{bow}_{\text{array}} = \frac{1}{2} w_{\text{array}} \cdot \tan(\gamma_{\text{array}}) = 100\mu m \cdot \tan(0.002\alpha_2) \approx 0.00052\mu m = 0.52nm \tag{C.8}$$

Appendix D

Process Documents

D.1 Calibration of Cryogenic RIE

Table D.1: Process steps

#	Process	Comment
1	(#subs001) **Substrate selection - Silicon <100> OSP** CR112B / Wafer Storage Cupboard Supplier: Orientation: <100> Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side Resistivity: 5-10Ωcm Type: p	10 wafers
2	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
3	(#depo004) **LPCVD TEOS** CR112B / Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0°C Temperature: 700°C pressure: 400mTorr • program: TEOS05 • deposition rate: 10.7 nm/min (25 wafers) • Uniformity/ wafer: 3% • Nf: : 1.44 • stress after deposition: -5 Mpa • stress after two weeks : -20.0 Mpa • stres after anneal of 700°C: + 5 Mpa	Thickness = 100nm ± 10nm Time = 10min
4	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	

Continued on next page

Table D.1 – continued from previous page

#	Process	Comment
5	(#lith057) **Lithography - Olin 907-17** CR112B / Suss Micro Tech Spinner (Delta 20) Hotplate 120°C: • Dehydration bake (120°C): 5min HexaMethylDiSilazane (HMDS): • Spin program: 4 (4000rpm, 20sec) Olin 907-17: • Spin program: 4 (4000rpm, 20sec) Hotplate 95°C: • Prebake (95°C): 90s CR117B / EVG 620 Electronic Vision Group 620 Mask Aligner: • Hg-lamp: 12 mW/cm^2 • Exposure Time: 4sec CR112B / Wet-Bench 11 Hotplate 120°C (CR112B or CR117B): • After Exposure Bake (120°C): 60sec Developer OPD4262: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	
6	(#char001) **Optical microscopic inspection - Lithography** CR112B / Nikon Microscope	Inspection of lithography
7	(#lith009) **Lithography - Postbake standard** CR112B / Hotplate 120°C • Time: 30min	
8	(#etch024) **Etching BHF (1:7) SiO_2** CR112B / Wet-Bench 3-3 HF/NH_4F(1:7) VLSI: BASF • Quick Dump Rinse <0.1µS • Spin drying Etchrate thermal SiO_2 = 60-80nm/min Etchrate PECVD SiO_2 = 125/nm/min Etchrate TEOS SiO_2 = 180/nm/min	Time: 35sec
10	(#lith016) **Stripping of Olin PR - HNO_3 standard** CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20min • Quick Dump Rinse <0.1µS • Spin drying	

Continued on next page

Table D.1 – continued from previous page

<table>
<tr><th>#</th><th>Process</th><th>Comment</th></tr>
<tr><td>11</td><td>(#etch077) Plasma etching of Si - C-Cryo-SF$_6$
CR125c/Adixen SE
Application: Etching of deep trenches
Parameters after optimisation (see section 3.2.3):
<table><tr><th>Parameters</th><th>Etch</th></tr><tr><td>Gas SF$_6$ (sccm)</td><td>100</td></tr><tr><td>Gas O$_2$ (sccm)</td><td>13</td></tr><tr><td>ICP (Watt)</td><td>500</td></tr><tr><td>CCP (Watt [pulsed LF])</td><td>20</td></tr><tr><td>on/off (msec)</td><td>20/80</td></tr><tr><td>SH (mm)</td><td>200</td></tr><tr><td>APC (%)</td><td>100</td></tr><tr><td>He (mBar)</td><td>10</td></tr><tr><td>Electrode temp. (°C)</td><td>-100</td></tr></table></td><td>Etch depth: 10µm
(device layer)
Time: 5:00min</td></tr>
<tr><td>12</td><td>(#char007) Ellipsometer Measurement
CR118B / Plasmos Ellipsometer</td><td></td></tr>
<tr><td>13</td><td>(#char005) Surface profile measurement
CR118B / Veeco Dektak 8</td><td>Thickness TEOS</td></tr>
<tr><td>14</td><td>(#char003) SEM Inspection
CR130C / JEOL 5610</td><td>inspect
underetch</td></tr>
</table>

D.2 Pre-study

Table D.2: Process steps

Step	Process	Comment
1	(#subs001) **Substrate selection - Silicon** ⟨100⟩ **OSP** CR112B / Wafer Storage Cupboard Supplier: Orientation: ⟨100⟩ Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side Resistivity: 5-10Ωcm Type: p	13 wafers
2	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
3	(#etch027) **Etching HF (1%) Native Oxide** CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	Just before SiRN deposition
4	(#depo002) **LPCVD SiRN - uniform thickness** CR125C / Tempress LPCVD G4 Program: LSNit-G4 • SiH_2Cl_2 flow: 155 sccm • NH_3 flow: 45 sccm • temperature: 830/850/873°C • pressure: 200 mTorr • N_2 flow: 150 sccm • deposition rate: ± 6−7 nm/min • N_f: ± 2.18	Thickness = 30nm ± 5nm Time = 2:40min
5	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
6	(#depo004) **LPCVD TEOS** CR112B / Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0°C Temperature: 700°C pressure: 400mTorr • program: TEOS05 • deposition rate: 10.7 nm/min (25 wafers) • Uniformity/ wafer: 3% • Nf: : 1.44 • stress after deposition: -5 Mpa • stress after two weeks : -20.0 Mpa • stres after anneal of 700°C: + 5 Mpa	Thickness = 100nm ± 10nm Time = 10min

Continued on next page

Table D.2 – continued from previous page

Step	Process	Comment
7	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
8	(#depo002) **LPCVD SiRN - uniform thickness** CR125C / Tempress LPCVD G4 Program: LSNit-G4 • SiH_2Cl_2 flow: 155 sccm • NH_3 flow: 45 sccm • temperature: 830/850/873°C • pressure: 200 mTorr • N_2 flow: 150 sccm • deposition rate: ± 6−7 nm/min • N_f: ± 2.18	Thickness = 25nm ± 5nm Time = 2:10min
9	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
10	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
11	(#lith057) **Lithography - Olin 907-17** CR112B / Suss Micro Tech Spinner (Delta 20) Hotplate 120°C: • Dehydration bake (120°C): 5min HexaMethylDiSilazane (HMDS): • Spin program: 4 (4000rpm, 20sec) Olin 907-17: • Spin program: 4 (4000rpm, 20sec) Hotplate 95°C: • Prebake (95°C): 90s CR117B / EVG 620 Electronic Vision Group 620 Mask Aligner: • Hg-lamp: 12 mW/cm^2 • Exposure Time: 4sec CR112B / Wet-Bench 11 Hotplate 120°C (CR112B or CR117B): • After Exposure Bake (120°C): 60sec Developer OPD4262: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	Frontside mask, hard contact *No postbake!*
12	(#char001) **Optical microscopic inspection - Lithography** CR112B / Nikon Microscope	Inspection of lithography
13	(#etch004) **Plasma etching SiN (Etske)** CR102A / Elektrotech PF310/340 Dirty chamber Styros + Quartz electrode • Electrode temp.: 10°C	Etch through top nitride layer (40sec), stop in TEOS SiO_2 layer

Continued on next page

Table D.2 – continued from previous page

Step	Process	Comment
	• CHF_3 flow: 25sccm • O_2 flow: 5sccm • pressure: 10mTorr • power: 75W Etchrate SiN = 50nm/min (for V_{DC}=-460V) Etchrate SiN = 75 nm/min (for V_{DC} = -580V) Etchrate Olin resist = 95nm/min If DC-Bias < 375V apply chamber clean (#etch003)	Total time: 90sec
14	(#char002) **Optical microscopic inspection** CR112B / Nikon Microscope CR117B / Olympus Microscope CR102B / Olympus Microscope	
15	(#lith016) **Stripping of Olin PR - HNO_3 standard** CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 40min • Quick Dump Rinse <0.1µS • Spin drying	
16	(#etch024) **Etching BHF (1:7) SiO_2** CR112B / Wet-Bench 3-3 HF/NH_4F(1:7) VLSI: BASF • Quick Dump Rinse <0.1µS • Spin drying Etchrate thermal SiO_2 = 60-80nm/min Etchrate PECVD SiO_2 = 125/nm/min Etchrate TEOS SiO_2 = 180/nm/min	Time: 1min and 5:33min
17	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
18	(#etch027) **Etching HF (1%) Native Oxide** CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	
19	(#etch053) **Etching of SiN (Hot H_3PO_4)** CR112B / Wet-Bench 3-1 H_3PO_4 85% Merck VLSI 1.00568.2500 Apply always first a Standard Wafer Clean (#clean003) and a 1% HF dip (#etch027) to remove native oxide. • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1 µS • Spin drying Etchrate SiRN: 3.5 nm/min High selective for SiO_2 layers Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed.	Time: 10min

Continued on next page

Table D.2 – continued from previous page

Step	Process	Comment
	Temperature (°C) / etch rate Si_xN_y (nm/min) / etch rate SiO_2 (nm/min) 180 / 4.1 / 0.48 160 / 1.4 / 0.16 140 / 0.5 / 0.05	
20	(#etch077) **Plasma etching of Si - C-Cryo-SF_6** CR125c/Adixen SE Application: Etching of deep trenches Parameters / Etch Gas SF_6 (sccm) / 100 Gas O_2 (sccm) / 13 ICP (Watt) / 500 CCP (Watt [pulsed LF]) / 20 on/off (msec) / 20/80 SH (mm) / 200 APC (%) / 100 He (mBar) / 10 Electrode temp. (°C) / -100	Etch depth: 10µm (device layer) Time: 6:00min
21	(#char005) **Surface profile measurement** CR118B / Veeco Dektak 8	
22	(#etch028) **Etching HF (1%)** CR116B / Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1µS • Spin drying	Time: 2:30min
23	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
24	(#depo031) **Dry Oxidation of Silicon at 950°C** CR112B / Furnace A2 Standby temp.: 700°C • Program: Dry950C • Temp.: 950°C • Gas: O_2	LOCOS Time: 70min

Continued on next page

Table D.2 – continued from previous page

Step	Process	Comment
	Growthrate: Oxidation (min) / Si ⟨100⟩ oxide (nm) / Si ⟨110⟩ oxide (nm) 0 / 2.27 / 2.38 6 / 8.29 / 12.33 12 / 12.2 / 17.51 24 / 17.78 / 25.67 48 / 28.06 / 38.58 96 / 45.68 / 59.1 192 / 75.88 / 91.43	
25	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
26	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
27	(#etch027) **Etching HF (1%) Native Oxide** CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	
28	(#etch053) **Etching of SiN (Hot H_3PO_4)** CR112B / Wet-Bench 3-1 H_3PO_4 85% Merck VLSI 1.00568.2500 Apply always first a Standard Wafer Clean (#clean003) and a 1% HF dip (#etch027) to remove native oxide. • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1 µS • Spin drying Etchrate SiRN: 3.5 nm/min High selective for SiO_2 layers Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed. Temperature (°C) / etch rate Si_xN_y (nm/min) / etch rate SiO_2 (nm/min) 180 / 4.1 / 0.48 160 / 1.4 / 0.16 140 / 0.5 / 0.05	Time: 12:00min
29	(#char002) **Optical microscopic inspection** CR112B / Nikon Microscope CR117B / Olympus Microscope CR102B / Olympus Microscope	

Continued on next page

Table D.2 – continued from previous page

Step	Process	Comment
30	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
31	(#etch027) **Etching HF (1%) Native Oxide** CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	
32	(#etch038) **Etching of Silicon by KOH - standard** CR102B / KOH KOH: MERCK 105019.500 KOH:DI = (1:3) 25wt% KOH: 500g KOH pellets in 1500ml DI water • Temp.: 75°C • Stirrer • Quick Dump Rinse <0.1µS • Spin drying Etchrates: Si ⟨100⟩ = 1µm/min Si ⟨111⟩ = 12.5nm/min SiO_2 (thermal) = 180nm/hr SiRN < 0.6nm/hr	5 min
33	(#clean007) **Cleaning RCA-2 (HCL/H_2O_2/H_2O)** CR112B / Wet-Bench 130 HCL (36%) Selectipur, BASF H_2O_2 (31%) VLSI, BASF Only use the dedicated wafer carriers and rod! HCL:H_2O_2:H_2O (1:1:5) vol% • add HCL to H_2O • add H_2O_2 when mixure at 70°C • temperature 70-80°C • cleaning time 10-15min • Quick Dump Rinse <0.1µS • Spin drying	
34	(#char005) **Surface profile measurement** CR118B / Veeco Dektak 8	
35	(#char003) **SEM Inspection** CR130C / JEOL 5610	nitride profile
36	(#etch024) **Etching BHF (1:7) SiO_2** CR112B / Wet-Bench 3-3 HF/NH_4F(1:7) VLSI: BASF • Quick Dump Rinse <0.1µS • Spin drying Etchrate thermal SiO_2 = 60-80nm/min Etchrate PECVD SiO_2 = 125/nm/min Etchrate TEOS SiO_2 = 180/nm/min	Strip SiO_2 Time: 1min

D.3 Cantilever arrays

Table D.3: Process steps

Step	Process	Comment
1a	(#subs001) **Substrate selection - Silicon** ⟨100⟩ **OSP** CR112B / Wafer Storage Cupboard Supplier: Orientation: ⟨100⟩ Diameter: 100mm Thickness: 525µm +/- 25µm Polished: Single side Resistivity: 5-10Ωcm Type: p	10 wafers (dummies)
1b	(#subs010) **Substrate selection - Silicon** ⟨110⟩ **DSP** CR112B / Wafer Storage Cupboard Supplier: Orientation: ⟨110⟩ Diameter: 100mm Thickness: 380µm +/- 10µm Polished: Double side Resistivity: 5-10Ωcm Type: p	2 wafers (dummies)
1c	**Substrate selection - SOI** ⟨100⟩ **DSP** Supplier: Orientation: ⟨100⟩ Diameter: 100mm Device thickness: 10µm +/- 0.5µm Device resistivity: 0.01-0.02Ωcm Handle thickness: 380µm +/- 5µm Handle resistivity: 1-20Ωcm BOX thickness: 0.5µm +/- 5% Type: p	5 wafers (process wafers)
2	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
3	(#etch027) **Etching HF (1%) Native Oxide** CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	Just before SiRN deposition
4	(#depo002) **LPCVD SiRN - uniform thickness** CR125C / Tempress LPCVD G4 Program: LSNit-G4 • SiH_2Cl_2 flow: 155 sccm • NH_3 flow: 45 sccm • temperature: 830/850/873°C • pressure: 200 mTorr	Thickness = 25nm ± 5nm Time = 2:10min

Continued on next page

Table D.3 – continued from previous page

Step	Process	Comment
	• N_2 flow: 150 sccm • deposition rate: ± 6−7 nm/min • N_f: ± 2.18	
5	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
6	(#depo004) **LPCVD TEOS** CR112B / Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0°C Temperature: 700°C pressure: 400mTorr • program: TEOS05 • deposition rate: 10.7 nm/min (25 wafers) • Uniformity/ wafer: 3% • Nf: : 1.44 • stress after deposition: -5 Mpa • stress after two weeks : -20.0 Mpa • stres after anneal of 700°C: + 5 Mpa	Thickness = 100nm ± 10nm Time = 10min
7	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
8	(#depo002) **LPCVD SiRN - uniform thickness** CR125C / Tempress LPCVD G4 Program: LSNit-G4 • SiH_2Cl_2 flow: 155 sccm • NH_3 flow: 45 sccm • temperature: 830/850/873°C • pressure: 200 mTorr • N_2 flow: 150 sccm • deposition rate: ± 6−7 nm/min • N_f: ± 2.18	Thickness = 20nm ± 5nm Time = 1:40min
9	(#char007) **Ellipsometer Measurement** CR118B / Plasmos Ellipsometer	Use dummies
10	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
11	(#lith057) **Lithography - Olin 907-17** CR112B / Suss Micro Tech Spinner (Delta 20) Hotplate 120°C: • Dehydration bake (120°C): 5min HexaMethylDiSilazane (HMDS): • Spin program: 4 (4000rpm, 20sec) Olin 907-17: • Spin program: 4 (4000rpm, 20sec) Hotplate 95°C: • Prebake (95°C): 90s CR117B / EVG 620 Electronic Vision Group 620 Mask Aligner:	Frontside mask, FCRYO hard contact *No postbake!*

Continued on next page

Table D.3 – continued from previous page

Step	Process	Comment
	• Hg-lamp: 12 mW/cm^2 • Exposure Time: 4sec CR112B / Wet-Bench 11 Hotplate 120°C (CR112B or CR117B): • After Exposure Bake (120°C): 60sec Developer OPD4262: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	
12	(#char001) **Optical microscopic inspection - Lithography** CR112B / Nikon Microscope	Inspection of lithography
13	(#etch003) **Plasma etching - chamber cleaning (Etske)** CR102A / Elektrotech PF310/340 Select chamber for desired etch process Select electrode for desired etch process • Electrode temp.: 10°C or 25°C • O_2 flow: 20sccm • pressure: 50mTorr • power: 150W • DC-Bias: 780V Chamber is clean when plasma color is white	
14	(#etch004) **Plasma etching SiN (Etske)** CR102A / Elektrotech PF310/340 Dirty chamber Styros + Quartz electrode • Electrode temp.: 10°C • CHF_3 flow: 25sccm • O_2 flow: 5sccm • pressure: 10mTorr • power: 75W Etchrate SiN = 50nm/min (for V_{DC}=-460V) Etchrate SiN = 75 nm/min (for V_{DC} = -580V) Etchrate Olin resist = 95nm/min If DC-Bias < 375V apply chamber clean (#etch003)	Etch through top nitride layer (30sec), stop in TEOS SiO_2 layer Total time: 60sec
15	(#char002) **Optical microscopic inspection** CR112B / Nikon Microscope CR117B / Olympus Microscope CR102B / Olympus Microscope	
16	(#lith016) **Stripping of Olin PR - HNO_3 standard** CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 40min • Quick Dump Rinse <0.1µS • Spin drying	
17	(#lith042) **Stripping of Olin PR wires by oxygen plasma Tepla 300** CR125A / Tepla 300 Barrel Etcher (2.45 GHz) Ultra clean system only (no metals except Al) • See list with recipes in CR • O_2 flow: 200sccm (50%) • Power: up to 1000W • Pressure: 1 mbar	10min

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Table D.3 – continued from previous page

<table>
<tr><th>Step</th><th>Process</th><th>Comment</th></tr>
<tr><td>18</td><td>(#char002) Optical microscopic inspection
CR112B / Nikon Microscope
CR117B / Olympus Microscope
CR102B / Olympus Microscope</td><td>Inspection of
PR-residue
(wires)
after RIE</td></tr>
<tr><td>19</td><td>(#etch024) Etching BHF (1:7) SiO_2
CR112B / Wet-Bench 3-3
HF/NH_4F(1:7) VLSI: BASF
• Quick Dump Rinse <0.1µS
• Spin drying
Etchrate thermal SiO_2 = 60-80nm/min
Etchrate PECVD SiO_2 = 125/nm/min
Etchrate TEOS SiO_2 = 180/nm/min</td><td>Time: 12:30min</td></tr>
<tr><td>20</td><td>(#char003) SEM Inspection
CR130C / JEOL 5610</td><td>inspect
underetch</td></tr>
<tr><td>21</td><td>(#clean003) Cleaning Standard
CR112B / Wet-Bench 131
HNO_3 (100%) Selectipur: MERCK
HNO_3 (69%) VLSI: MERCK
• Beaker 1: fumic HNO_3 (100%), 5min
• Beaker 2: fumic HNO_3 (100%), 5min
• Quick Dump Rinse <0.1µS
• Beaker 3: boiling (95°C) HNO_3 (69%), 10min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>22</td><td>(#etch027) Etching HF (1%) Native Oxide
CR112B / Wet-Bench 3-3
HF (1%) VLSI: MERCK 112629.500
• Etch time: >1min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>23</td><td>(#etch053) Etching of SiN (Hot H_3PO_4)
CR112B / Wet-Bench 3-1
H_3PO_4 85% Merck VLSI 1.00568.2500
Apply always first a Standard Wafer Clean (#clean003)
and a 1% HF dip (#etch027) to remove native oxide.
• Temp.: 180°C (caution!)
• Quick Dump Rinse <0.1 µS
• Spin drying
Etchrate SiRN: 3.5 nm/min
High selective for SiO_2 layers
Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed.
<table><tr><th>Temperature (°C)</th><th>etch rate Si_xN_y (nm/min)</th><th>etch rate SiO_2 (nm/min)</th></tr><tr><td>180</td><td>4.1</td><td>0.48</td></tr><tr><td>160</td><td>1.4</td><td>0.16</td></tr><tr><td>140</td><td>0.5</td><td>0.05</td></tr></table></td><td>Etch rate determined
with dummy wafer
Time: 8:50min</td></tr>
<tr><td>24</td><td>(#char003) SEM Inspection
CR130C / JEOL 5610</td><td>Inspect bottom
nitride profile</td></tr>
<tr><td>25</td><td>(#char005) Surface profile measurement
CR118B / Veeco Dektak 8</td><td>Thickness bottom
nitride + TEOS</td></tr>
<tr><td>26</td><td>(#etch079) Plasma etching of Si - Cleaning chamber
CR125c/Adixen SE</td><td></td></tr>
</table>

Continued on next page

Table D.3 – continued from previous page

Step	Process	Comment
	Application: Cleaning (FC-residues) of chamber before silicon etching, use a dummy during cleaning. Check rise in V_{DC} value. Parameters / Etch: Gas O2; Flow (sccm) 200; Time (min) 10; Priority nvt; APC (%) 100; ICP (Watt) 2000; CCP (Watt [LF]) 0; Pulsed - LF (msec) off; He (mBar) 10; SH (mm) 110; Electrode temp. (°C) -100°C	
27	(#etch077) **Plasma etching of Si - C-Cryo-SF_6** CR125c/Adixen SE Application: Etching of deep trenches **Note:** The gas flow is optimised for the mask (differs from pre-study mask) Parameters / Etch: Gas SF_6 (sccm) 100; Gas O_2 (sccm) 12; ICP (Watt) 500; CCP (Watt [pulsed LF]) 20; on/off (msec) 20/80; SH (mm) 200; APC (%) 100; He (mBar) 10; Electrode temp. (°C) -100	Etch depth: 10µm (device layer) Time: 4:35min
28	(#char005) **Surface profile measurement** CR118B / Veeco Dektak 8	
29	(#etch028) **Etching HF (1%)** CR116B / Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1µS • Spin drying	Time: 5min
30	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
31	(#depo031) **Dry Oxidation of Silicon at 950°C** CR112B / Furnace A2 Standby temp.: 700°C	LOCOS Time: 5h

Continued on next page

Table D.3 – continued from previous page

<table>
<tr><th>Step</th><th>Process</th><th>Comment</th></tr>
<tr><td></td><td>• Program: Dry950C
• Temp.: 950°C
• Gas: O_2
Growthrate:
<table><tr><th>Oxidation (min)</th><th>Si ⟨100⟩ oxide (nm)</th><th>Si ⟨110⟩ oxide (nm)</th></tr><tr><td>0</td><td>2.27</td><td>2.38</td></tr><tr><td>6</td><td>8.29</td><td>12.33</td></tr><tr><td>12</td><td>12.2</td><td>17.51</td></tr><tr><td>24</td><td>17.78</td><td>25.67</td></tr><tr><td>48</td><td>28.06</td><td>38.58</td></tr><tr><td>96</td><td>45.68</td><td>59.1</td></tr><tr><td>192</td><td>75.88</td><td>91.43</td></tr></table></td><td></td></tr>
<tr><td>32</td><td>(#char007) Ellipsometer Measurement
CR118B / Plasmos Ellipsometer</td><td>Use dummies</td></tr>
<tr><td>33</td><td>(#clean003) Cleaning Standard
CR112B / Wet-Bench 131
HNO_3 (100%) Selectipur: MERCK
HNO_3 (69%) VLSI: MERCK
• Beaker 1: fumic HNO_3 (100%), 5min
• Beaker 2: fumic HNO_3 (100%), 5min
• Quick Dump Rinse <0.1µS
• Beaker 3: boiling (95°C) HNO_3 (69%), 10min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>34</td><td>(#etch027) Etching HF (1%) Native Oxide
CR112B / Wet-Bench 3-3
HF (1%) VLSI: MERCK 112629.500
• Etch time: >1min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>35</td><td>(#etch053) Etching of SiN (Hot H_3PO_4)
CR112B / Wet-Bench 3-1
H_3PO_4 85% Merck VLSI 1.00568.2500
Apply always first a Standard Wafer Clean (#clean003)
and a 1% HF dip (#etch027) to remove native oxide.
• Temp.: 180°C (caution!)
• Quick Dump Rinse <0.1 µS
• Spin drying
Etchrate SiRN: 3.5 nm/min
High selective for SiO_2 layers
Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed.
<table><tr><th>Temperature (°C)</th><th>etch rate Si_xN_y (nm/min)</th><th>etch rate SiO_2 (nm/min)</th></tr><tr><td>180</td><td>4.1</td><td>0.48</td></tr><tr><td>160</td><td>1.4</td><td>0.16</td></tr><tr><td>140</td><td>0.5</td><td>0.05</td></tr></table></td><td>Time: 12:30min</td></tr>
<tr><td>36</td><td>(#char002) Optical microscopic inspection
CR112B / Nikon Microscope</td><td></td></tr>
</table>

Continued on next page

Table D.3 – continued from previous page

Step	Process	Comment
	CR117B / Olympus Microscope CR102B / Olympus Microscope	
37	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
38	(#etch027) **Etching HF (1%) Native Oxide** CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	
39	(#etch038) **Etching of Silicon by KOH - standard** CR102B / KOH KOH: MERCK 105019.500 KOH:DI = (1:3) 25wt% KOH: 500g KOH pellets in 1500ml DI water • Temp.: 75°C • Stirrer • Quick Dump Rinse <0.1µS • Spin drying Etchrates: Si ⟨100⟩ = 1µm/min Si ⟨111⟩ = 12.5nm/min SiO_2 (thermal) = 180nm/hr SiRN < 0.6nm/hr	5 min
40	(#clean007) **Cleaning RCA-2 ($HCL/H_2O_2/H_2O$)** CR112B / Wet-Bench 130 HCL (36%) Selectipur, BASF H_2O_2 (31%) VLSI, BASF Only use the dedicated wafer carriers and rod! $HCL:H_2O_2:H_2O$ (1:1:5) vol% • add HCL to H_2O • add H_2O_2 when mixure at 70°C • temperature 70-80°C • cleaning time 10-15min • Quick Dump Rinse <0.1µS • Spin drying	
41	(#char005) **Surface profile measurement** CR118B / Veeco Dektak 8	
42	(#char003) **SEM Inspection** CR130C / JEOL 5610	inspect bottom nitride profile
43	(#etch028) **Etching HF (1%)** CR116B / Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1µS • Spin drying	Remove SiO_2 Time: 30min
44	(#clean003) **Cleaning Standard** CR112B / Wet-Bench 131	

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Table D.3 – continued from previous page

<table>
<tr><th>Step</th><th>Process</th><th>Comment</th></tr>
<tr><td></td><td>HNO_3 (100%) Selectipur: MERCK
HNO_3 (69%) VLSI: MERCK
• Beaker 1: fumic HNO_3 (100%), 5min
• Beaker 2: fumic HNO_3 (100%), 5min
• Quick Dump Rinse <0.1µS
• Beaker 3: boiling (95°C) HNO_3 (69%), 10min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>45</td><td>(#depo031) Dry Oxidation of Silicon at 950°C
CR112B / Furnace A2
Standby temp.: 700°C
• Program: Dry950C
• Temp.: 950°C
• Gas: O_2
Growthrate:
<table><tr><th>Oxidation (min)</th><th>Si ⟨100⟩ oxide (nm)</th><th>Si ⟨110⟩ oxide (nm)</th></tr><tr><td>0</td><td>2.27</td><td>2.38</td></tr><tr><td>6</td><td>8.29</td><td>12.33</td></tr><tr><td>12</td><td>12.2</td><td>17.51</td></tr><tr><td>24</td><td>17.78</td><td>25.67</td></tr><tr><td>48</td><td>28.06</td><td>38.58</td></tr><tr><td>96</td><td>45.68</td><td>59.1</td></tr><tr><td>192</td><td>75.88</td><td>91.43</td></tr></table></td><td>Sharpening + protection
Time: 5h</td></tr>
<tr><td>46</td><td>(#lith059) Lithography - Olin 908-35
CR112B / Suss Micro Tech Spinner (Delta 20)
Hotplate 120°C:
• Dehydration bake (120°C): 5min
HexaMethylDiSilazane (HMDS):
• Spin program: 4 (4000rpm, 20sec)
Olin 908-35:
• Spin program: 4 (4000rpm, 20sec)
Hotplate 95°C:
• Prebake (95°C): 120s

CR117B / EVG 620
Electronic Vision Group 620 Mask Aligner:
• Hg-lamp: 12 mW/cm^2
• Exposure Time: 9sec

CR112B / Wet-Bench 11
Hotplate 120°C (CR112B or CR117B):
• After Exposure Bake (120°C): 60sec
Developer OPD4262:
• Time: 30sec in Beaker 1
• Time: 15-30sec in Beaker 2
• Quick Dump Rinse <0.1µS
• Spin drying</td><td>Backside mask, BDRIE
hard contact</td></tr>
<tr><td>47</td><td>(#lith009) Lithography - Postbake
CR112B / Hotplate 120°C
• Time: 60min</td><td></td></tr>
</table>

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Table D.3 – continued from previous page

<table>
<tr><th>Step</th><th>Process</th><th>Comment</th></tr>
<tr><td>48</td><td>Apply DuPont MX5000 Foil
Thickness: 20µm
Laminator settings:
Temperature: 90°C
Speed: 2</td><td>See document by
Marcus L:
Process details
DuPont MX5000</td></tr>
<tr><td>49</td><td>(#etch079) Plasma etching of Si - Cleaning chamber
CR125c/Adixen SE
Application: Cleaning (FC-residues) of chamber before
silicon etching, use a dummy during cleaning.
Check rise in V_{DC} value.
<table><tr><th>Parameters</th><th>Etch</th></tr><tr><td>Gas</td><td>O2</td></tr><tr><td>Flow (sccm)</td><td>200</td></tr><tr><td>Time (min)</td><td>10</td></tr><tr><td>Priority</td><td>nvt</td></tr><tr><td>APC (%)</td><td>100</td></tr><tr><td>ICP (Watt)</td><td>2000</td></tr><tr><td>CCP (Watt [LF])</td><td>0</td></tr><tr><td>Pulsed - LF (msec)</td><td>off</td></tr><tr><td>He (mBar)</td><td>10</td></tr><tr><td>SH (mm)</td><td>110</td></tr><tr><td>Electrode temp. (°C)</td><td>-40°C</td></tr></table></td><td></td></tr>
<tr><td>50</td><td>(#etch075) Plasma etching of Si - Twin-3 BOX / Beuken met Robert
CR 125c/Adixen SE
<table><tr><th>Parameters</th><th>Value</th></tr><tr><td>Flow CHF_3 (sccm)</td><td>100</td></tr><tr><td>Flow Ar (sccm)</td><td>100</td></tr><tr><td>V_{DC} (V)</td><td>560</td></tr><tr><td>APC (%)</td><td>100</td></tr><tr><td>ICP (Watt)</td><td>1200</td></tr><tr><td>CCP (Watt)</td><td>150</td></tr><tr><td>Electrode temp.</td><td>-40°C</td></tr><tr><td>He (mbar)</td><td>10</td></tr><tr><td>SH (mm)</td><td>200</td></tr></table>Etch rate SiO_2: 250 µm/min</td><td>etch oxide (500nm)
Time: 2:30min</td></tr>
<tr><td>51</td><td>(#etch075) Plasma etching of Si - A-pulsed-C_4F_8
CR 125c/Adixen SE
Application: trenches, wafer through using thick photoresist (908-35)
See document DRIE H.V. Jansen on downloads on this TST technology page</td><td>etch silicon (380µm)
Time: 32min</td></tr>
</table>

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Table D.3 – continued from previous page

Step	Process	Comment
	Parameters / Etch / Deposition (pulsed) Gas: SF_6 / C_4F_8 Flow (sccm): 400 / 25 Time (sec): 4 / 0.5 Priority: 2 / 1 APC (%): 15 / 15 ICP (Watt): 2500 / 2500 CCP (Watt): nvt / 20 Pulsed (msec): nvt / 20 on/180 off SH (mm): 110 / 110 Electrode temp.: -40°C / -40°C He (mbar): 10 / 10	
52	(#lith042) **Stripping of Olin PR by oxygen plasma Tepla 300** CR125A / Tepla 300 Barrel Etcher (2.45 GHz) Ultra clean system only (no metals except Al) • See list with recipes in CR • O_2 flow: 200sccm (50%) • Power: up to 1000W • Pressure: 1 mbar • Time: see recipes on the wall	Time: 60min
53	(#etch071) **Vapor HF etching of SiO_2** Idonius Vapor HF Tool • Temperature: 25°C After 1 min VHF etching, the results are monitored every 30 seconds. After $1 + 4 \times 0.5 = 3$min almost all cantilevers were free of oxide.	Total time: 3min