UNIVERSITY OF TWENTE.

**Faculty of Electrical Engineering,
Mathematics & Computer Science**

Characterization of a Gallium Nitride Half-Bridge module for use in a Multi-Freqeuncy Multilevel Modular Converter

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B.Sc. Thesis
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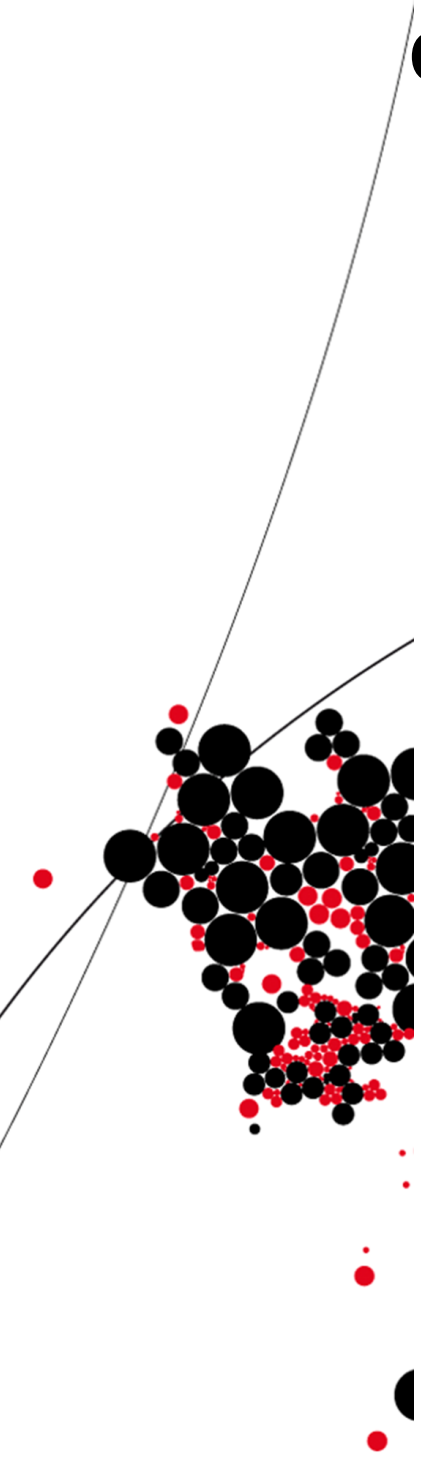

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Summary

This reports shows measurements done on a gallium nitride half-bridge module, these measurements will be the basis of EMI research of modules like this in a Multi-frequency Multilevel Modular Converter (M3C) system, which will be a corner stone of a Smart Grid. Devices have to obey many rules and regulations to be Electromagnetic Compatible (EMC), this makes versatility and controllability of signals within a device a must in the design of such devices. This report gives some insight in the ringing effects on the output with frequencies from 10 kHz up to 1 MHz, done with both the internal PWM generator and an FPGA as PWM input. Ringing can be a cause of Electromagnetic Interference (EMI). The FPGA is used to verify its capability for being used as an input for the GaN module, since the FPGA is easily programmable which results in easy manipulation of signals. The ringing shows to be independent on frequency but dependent on $\frac{dV}{dt}$ of the output. Furthermore the FPGA is capable of generating a PWM signal with a frequency of up to 1 MHz without introducing different ringing, showing a viable option as input generator. At last some measurements with variable dead time are show which are done with the FPGA. The variation in dead time has shown to be a viable way of decreasing overshoot at the output thus being able to influence EMI.

Keywords

Multi-frequency Multilevel Modular Converter (M3C)
Gallium Nitride Half-Bridge
Ringing
Dead time
Rise and Fall time
Smart Grid

Contents

1 Introduction

The so called 'Smart Grid' is the upcoming term of the last few years. Research on Smart Grid is aimed at renewable energy, this includes a more efficient power transfer from and towards the electrical grid. The current electrical grid is still governed by a 50/60 Hz sinusoidal voltage, from a time where that was the only feasible way to transfer power. With the introduction of high power semiconductors, for instance Gallium Nitride and Silicon Carbide, high voltage DC lines became realisable. GaN and SiC have the advantage of being smaller and faster than Silicon based semiconductors. GaN devices are grown on a standard silicon wafer whereas SiC needs a relatively expensive substrate [1].
Both AC and DC systems have their advantages and disadvantages [2]. First a few pros and cons for AC and DC systems will be reviewed and after that Multi-frequency Multilevel Modular Converters (M3C) will be explained.

AC systems

Since the invention of electricity AC systems are the standard. This is because voltage level conversion was only realisable via inductors, semiconductors had not been invented yet, thus only AC would work. This results in an immense amount of experience and engineering practice combined with long standing protocols. The current 50Hz 230V and 60Hz 110V grids, as standard and widely implemented, give easy implementable compatibility with regards to system design. The robustness on a large scale is achieved by interconnections and reserve generation, where as on small scale the grid still relies on energy storage, predictive generation or load shedding especially in renewable energy systems.

DC systems

DC (micro)grids are becoming more realisable due to progress in power electronics both in high voltage (HVDC) and low voltage (LVDC). Increase in renewable energy sources, such as solar, wind and thermal will benefit from HVDC systems due to simplicity and economic reasons [3]. There is an increasing number of consumer devices using DC, with an electrical grid that provides AC, results in most devices needing an AC-DC converter which is a possible cost reduction if the grid would be DC. On the consumer level there is a huge increase in local renewables which usually output DC, like solar panels and small windmills this increases complexity to transfer power to the grid. [4] [5]

Multi-frequency Multilevel Modular Converters

'Multi-frequency Multilevel Modular Converters' (M3C)[2][6][7] is the next step towards highly modular and adaptable power grids. M3C is based on multiple sub-modules (SM) which are part of a HVDC grid. Figure 1.1 shows the envisioned system using power shifter modules. A power shifter consists of multiple SM's, which are individually controlled to shift power between two frequencies. To increase the voltage of the power shifter several SM's need to be stacked, since every SM is voltage and current limited. Figure 1.2 shows a circuit model of a power shifter with stacked SM's. Each SM's consists of a half bridge with the ability to shift power from and towards the grid depending on its operational mode, figure 1.1 and figure 1.2 shows a few examples. The half bridge is a fundamental part in the M3C, quite literally the bridge between system and control.

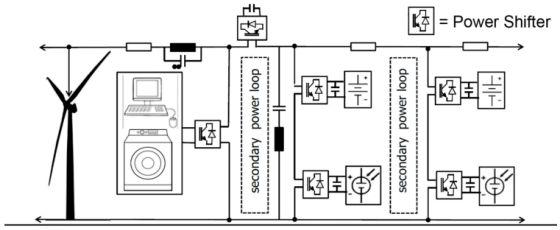


Figure 1.1: Envisioned HVDC Power Electronics System

Now that M3C is introduced the topic of this report can be looked into. As the title suggests this report is about characterizing a gallium nitride half bridge module. A GaN Half bridge module has been bought and will be characterized with regards to switching frequency and limitations thereof. The underlying focus is electromagnetic interference (EMI) and possible ways to reduce it in a working M3C system. Though this is not the focus of this report characterization on a conductive level needs to be done for better understanding of eventual EMI characteristics. This report will be investigating the function of a single module on a conductive level. It will be the basis for further research of multiple modules stacked in a M3C system.

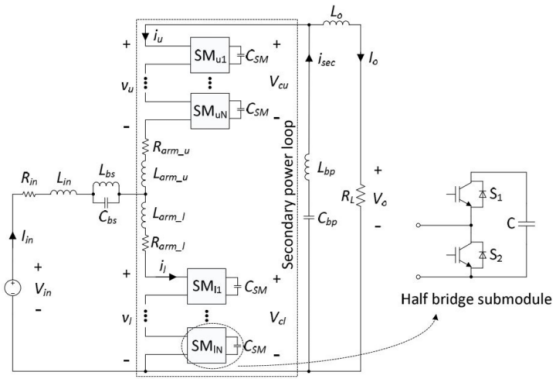


Figure 1.2: Circuit model of a tuned filter M3C, from [8]

2 Theory

This section will introduce a couple of definitions and theories on EMI. In the introduction electromagnetic interference (EMI) has been mentioned. EMI describes the signals that cause interference from one device to another or from the environment to a device. An example of EMI generated by devices is a cellphone causing interference on an audio amplifier resulting in distorted sounds.
The principle of electromagnetic compatibility (EMC) is both not producing or be susceptible to interference. Since more and more devices are electrically controlled and steered, rules and regulations have been put into place to ensure proper function of all devices. Dependent on country or continent legislation EMC can vary.

Without going into detail about the legislation, insight in noise sources of devices is vital to be able to counter EMI. With regard to the GaN module there are four points of interest [9]. Since the output is a PWM signal, points of interest are ringing, rise/fall times, duty cycle and dead time. The focus of will be on emission of the module.

2.1 Ringing

Ringing happens when a signal switches from one logic level to another it gets the tendency to oscillate around both the logical levels. Ringing is caused by the parasitic capacitances and inductances of the circuitry. For the rising flank this will result in overshoot and for the falling flank this will result in undershoot. This oscillation will add to the spectrum of the original signal thus adding towards EMI. Ringing oscillation has the mathematical form shown in equation (2.1) which shows a dampened sinusoidal waveform where α is the dampening factor and ω_r is the angular frequency resulting in the ringing frequency being $f_r = \frac{\omega_r}{2\pi}$. (C. R. Paul, (1992), Introduction to Electromagnetic Compatibility vol. 32 (pp. 137-139)).

$$Ke^{-\alpha t}sin(\omega_r t) \tag{2.1}$$

Figure 2.1 shows an example of ringing.

2.2 Rise and Fall time

Rise and fall time can have an effect on the spectrum as well (C. R. Paul, (1992), Introduction to Electromagnetic Compatibility vol. 32 (pp. 123-132)). The given pages

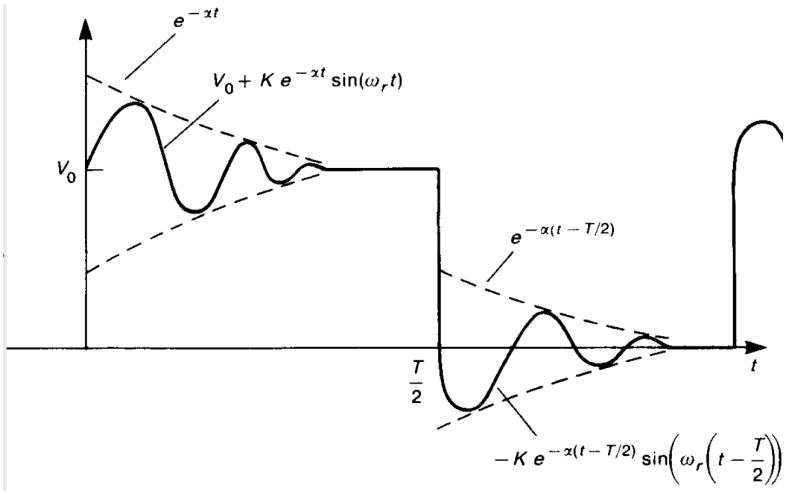


Figure 2.1: Example of ringing on a pulse signal, from [9]

show that for a pulse train a smaller (faster) rise and fall time give different spectral content than a larger (slower) rise and fall time.

2.3 Duty Cycle

Duty cycle is the percentage of time the PWM signal is on versus the signal being off, so 50% duty cycle means the PWM signal is turned on half of the period and turned off the other half. In sinusoidal PWM varying the duty cycle is used to generated a PWM signal that represents a sine wave when if filtered with a low pass filter, by rule of thumb the carrier frequency should be about ten times higher than the original signal. It is notable that in the situation of the half bridge configuration in this report a 50% duty cycle is practically impossible due to added dead time.

2.4 Dead time

Dead time is the time between switching on or off one transistor in a half bridge and turning off or on the other in said half bridge. This dead time is for safety so both transistors can never be on at the same time which would result in a short circuit. Dead time will affect the output signal. With a PWM signal it adds a delay before each switch lowering the duty cycle, this may add different harmonics than a signal without dead time. Variation of the dead time may be used to alter EMI emission of the device which will be shortly looked into later in the report.

3 Analysis of the Modules

The introduction already mentioned that an existing GaN half bridge module, the GS66504B with the GS665EVBMB motherboard from GaN systems, will be used. This chapter will briefly discuss the schematics, components and some specifications of the motherboard and the module provided. Furthermore reasoning of using an external PWM signal using an FPGA will be discussed. At last the kind of measurements that will be done are explained together with some reasoning

3.1 Motherboard (GS665EVBMB)

The design of the motherboard consists of an MC7805 and a 74VHC132. The MC7805 is a DC-DC converter that generates 5 V from the 12 V input. The 5 V is used to power the components on the motherboard and on the module. The 74VHC132 is a schmitt trigger which uses a sine wave input to generate a PWM signal of the same frequency. The PWM signal consists of a high signal and a low signal with a deadtime of 100 ns between the switches of the two. Deadtime is introduced to make sure the output transistors are not on at the same time, which would result in a short. The schmitt trigger is able to generate PWM signal with a frequency up to several megahertz. The schematic of the motherboard and the useful pages of the data sheet of the schmitt trigger can be found in Appendix A and Appendix B respectively.

3.2 GaN module (GS66504B)

The Half Bridge module has, apart from the two GaN transistors, two gate drivers (SI8271GB-IS) and two 9 V DC-DC converters (PES1-S5-S9-M). Data sheets show that the gate drivers have a typical rise and fall time of 10.5 ns and 13.3 ns respectively and uses the 9 V generated by the 9 V DC-DC converters to drive the gate. The input PWM signals can be either 3.3 V or 5 V. The GaN transistors are specified to work up to drain source voltage of 650 V. Figures 3.1 and 3.2 show the design of one of the gate drivers, including the output GaN transistor, and the 9 V DC-DC converter respectively. The entirety of the schematic can be found in appendix C, the relevant pages from the data sheet of gate driver are shown in appendix D.

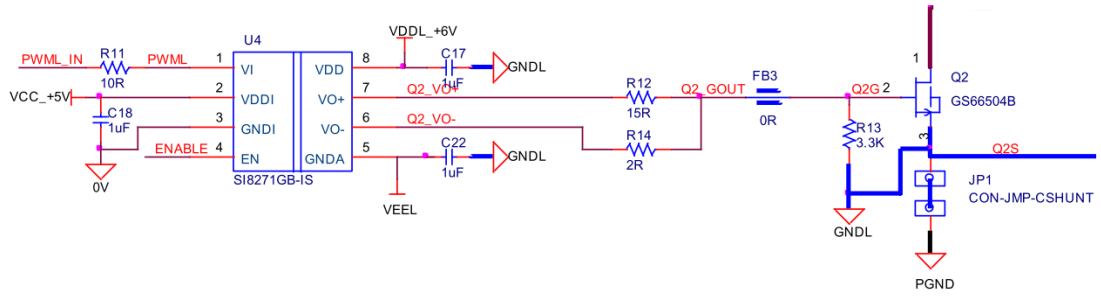


Figure 3.1: Circuit schematic of the gate driver

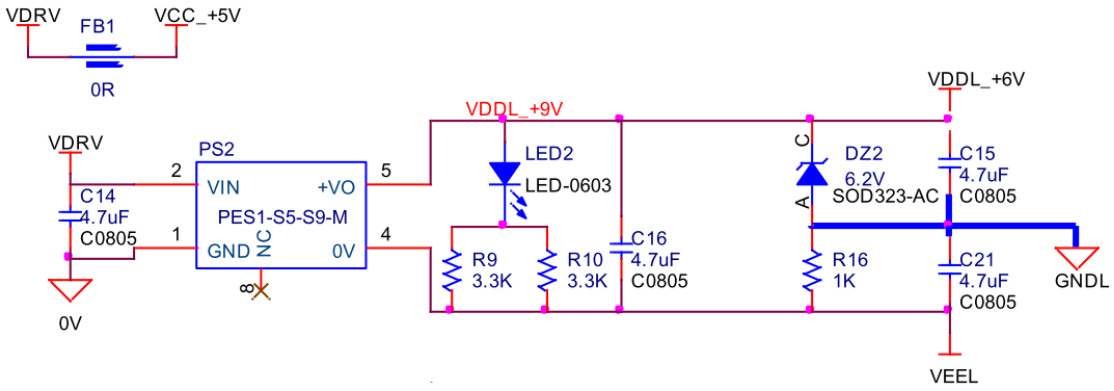


Figure 3.2: Circuit schematic of the 9V DC-DC converter

3.3 FPGA

Next to using the internal schmitt trigger for PWM generation an external PWM signal can be applied directly to the gate drivers. This would be done using an FPGA. The advantage of using this FPGA is the possibility to easily and quickly modify input signals for example with regards to frequency, deadtime, rise and fall times. The FPGA is capable of generating a PWM signal up to 1 MHz [10](to be published).

3.4 Method of Measuring

The FPGA can be used up to 1 MHz, measurements with the internal schmitt trigger will be done up to 2 MHz because this will show that the module does not limit the signal up to 1 MHz and if the module works consistent even beyond 1 MHz. The system will be tested with a input signal with a frequency of 10 kHz up to 2 MHz with both the internal PWM generated signal and a frequency of up to 1 MHz with the FPGA generated PWM

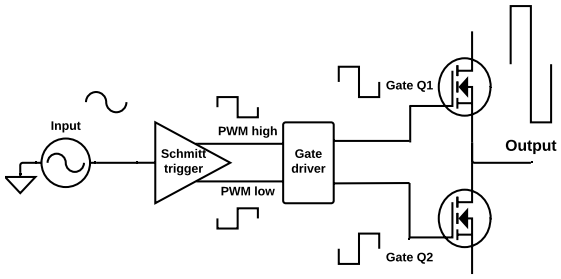


Figure 3.3: Diagram of the module

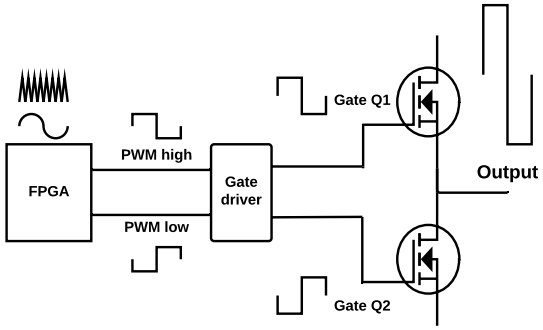


Figure 3.4: Diagram of the module with the FPGA

signal. The Figures 3.3 and 3.4 show a diagram of the system without and with the FPGA respectively. The duty cycle will be 50%. Noting that the 100ns internal dead time is not included in the duty cycle, so practically it is lower than 50% depending on input frequency, on and off time have the same length. The duty cycle is not shown in the diagrams but the effect will be shown in the results section. For the FPGA a few measurements with several different dead times with a range of frequencies is also done to see what the influence of variable dead time is.
The first measurement point of interest is the output of the schmitt trigger. Second point is the output of both the gate drivers and the last point the output of the half bridge, the output will be measured loaded and unloaded with a linear impedance. For the FPGA measurements the same three points will be looked into, where the first point is not the output of the schmitt trigger but the output of the FPGA.

4 Measurements

This section will give a brief overview of measurements done and results. Several Figures will be shown in the appendix to not overcrowd this section with Figures.

4.1 Measurements with internal PWM

Measuring the system as explained in the previous sections resulted in the following. The PWM signal from the schmitt trigger, the gate signals and the output are measured. Figure 4.1 shows the PWM signal and the gate signal of the upper part of the half bridge and the output, as shown in Figure 3.3. It shows measurements with an output voltage of 15 volt without a load and with several frequencies from 10 kHz up to 2 MHz. The schmitt trigger has a rise a time of 2.7 ns. The falling flank of the gate transistor Q1 has a step, this step is due to the dead time, the gate driver of Q1 has the output as a reference voltage, so if the the gate driver turns off and transistor Q2 is not yet turned on, the gate will drop with 9 V and will become the same as the output. Figure 4.2 shows the same measurements as the previous Figure, but this time it shows the lower part of the module. From the Figures one can clearly see that rise time is not influenced by change in frequency. The rise time of the output signals is 3.4 ns, the fall times are 3.6 ns.
The following Figures, Figure 4.3 and 4.4, show an output voltage of 15, 30 and 45 volt and a frequency of 100 kHz. The overshoot, in case of Figure 4.3 is 30%, 27% and 25% respectively and a rise time of around 3.9 ns for the 15 V output and around 9 ns for the 30 V and 45 V output. The undershoot in case of Figure 4.4 25%, 21% and 17% respectively with a fall time of around 10 ns. The ringing is visibly different in the three cases. The ringing frequencies are crudely estimated by measuring the time between periods of the visible signals, an FFT in matlab could not give an accurate insight in the spectrum due to lack of data points. The estimated frequencies are around 24 MHz, 108 MHz, 250 MHz and 500 MHz, where for the higher output voltage the lower ringing frequencies get more predominant than the high frequencies.

4.2 Measurements with FPGA generated PWM input signals

Now that several different points on the module have been measured the FPGA can added as input signal. Figures 4.54.6 show the same signals as the section before, this time the PWM signal is generated by the FPGA which is the top plot in the Figures. The frequencies shown are 100 kHz up to 600 kHz with an output amplitude of 15 V. The

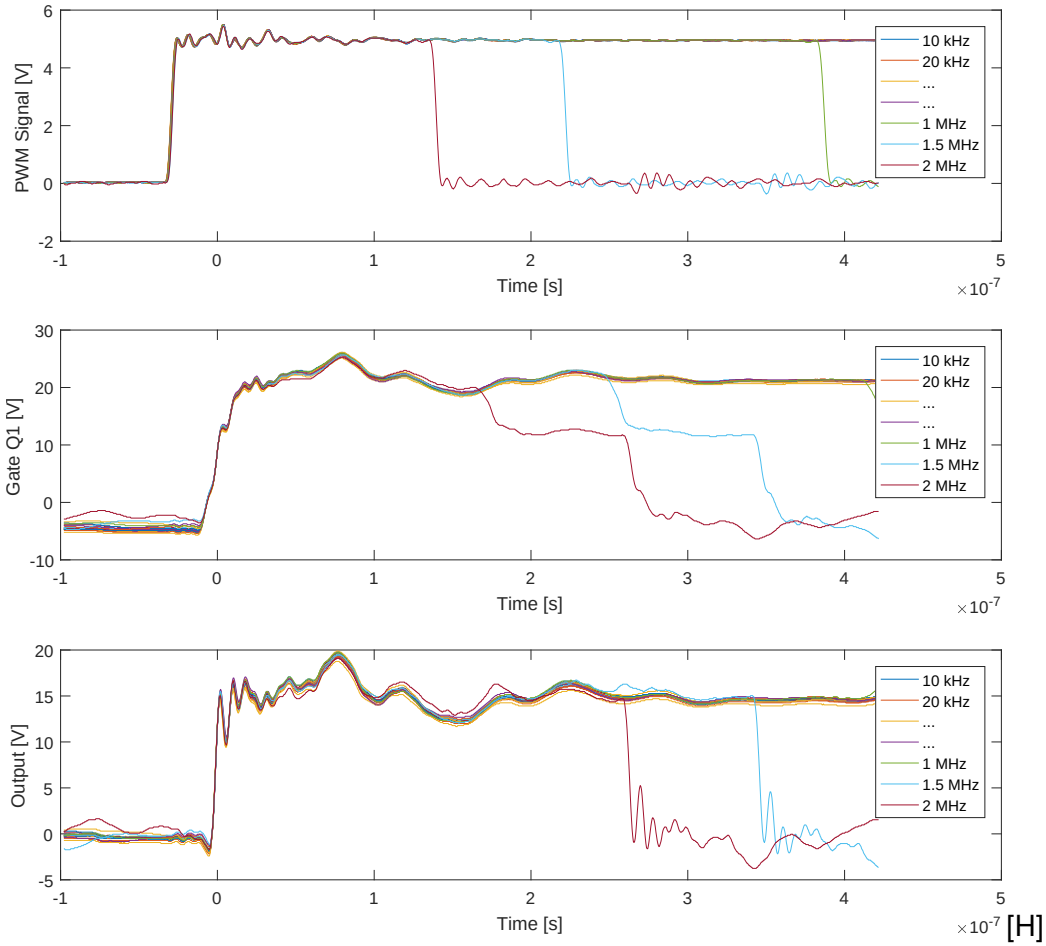


Figure 4.1: From top to bottom: PWM signal schmitt trigger, gate signal Q1 and the output

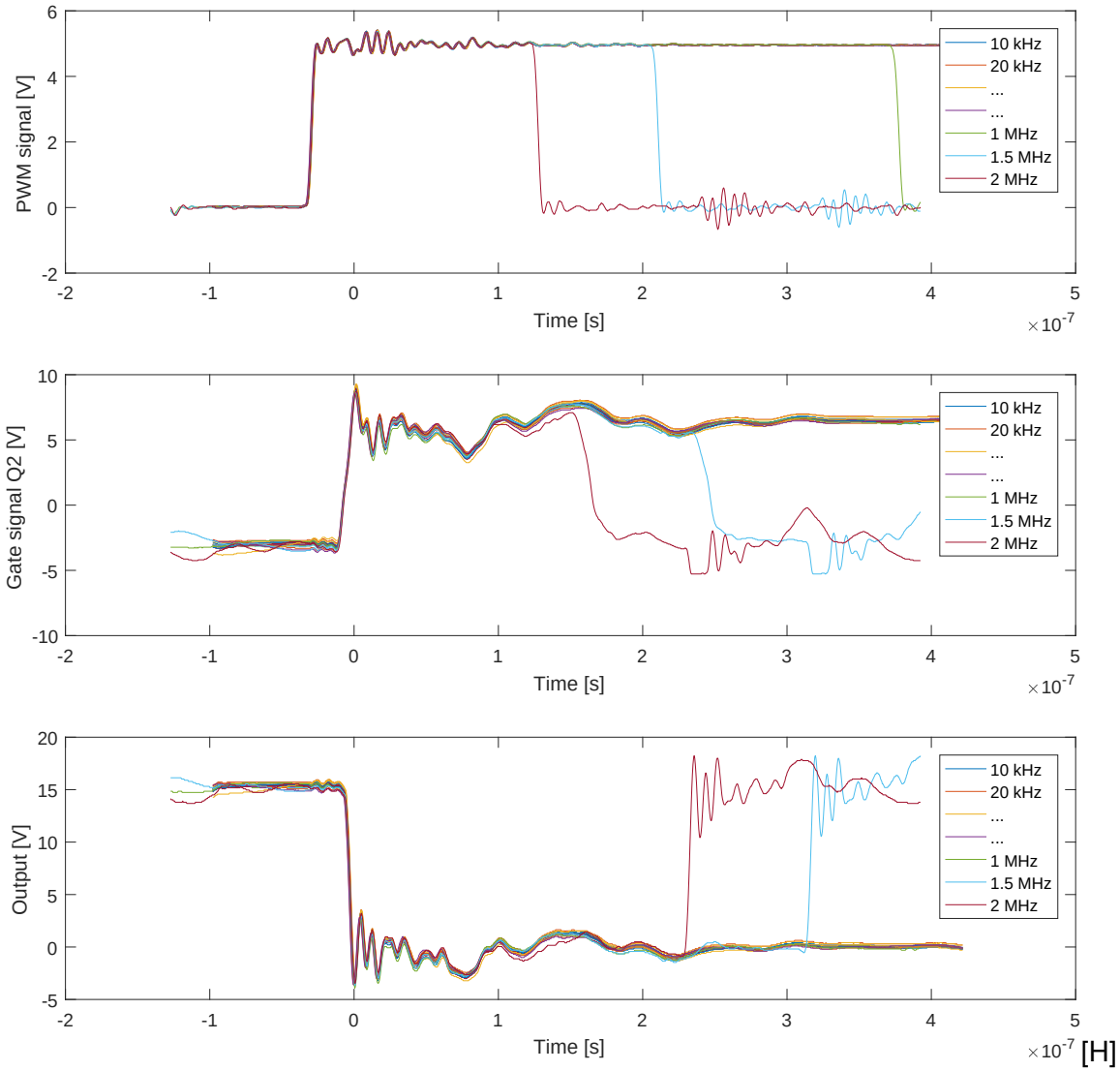


Figure 4.2: From top to bottom: PWM signal schmitt trigger, gate signal Q2 and the output

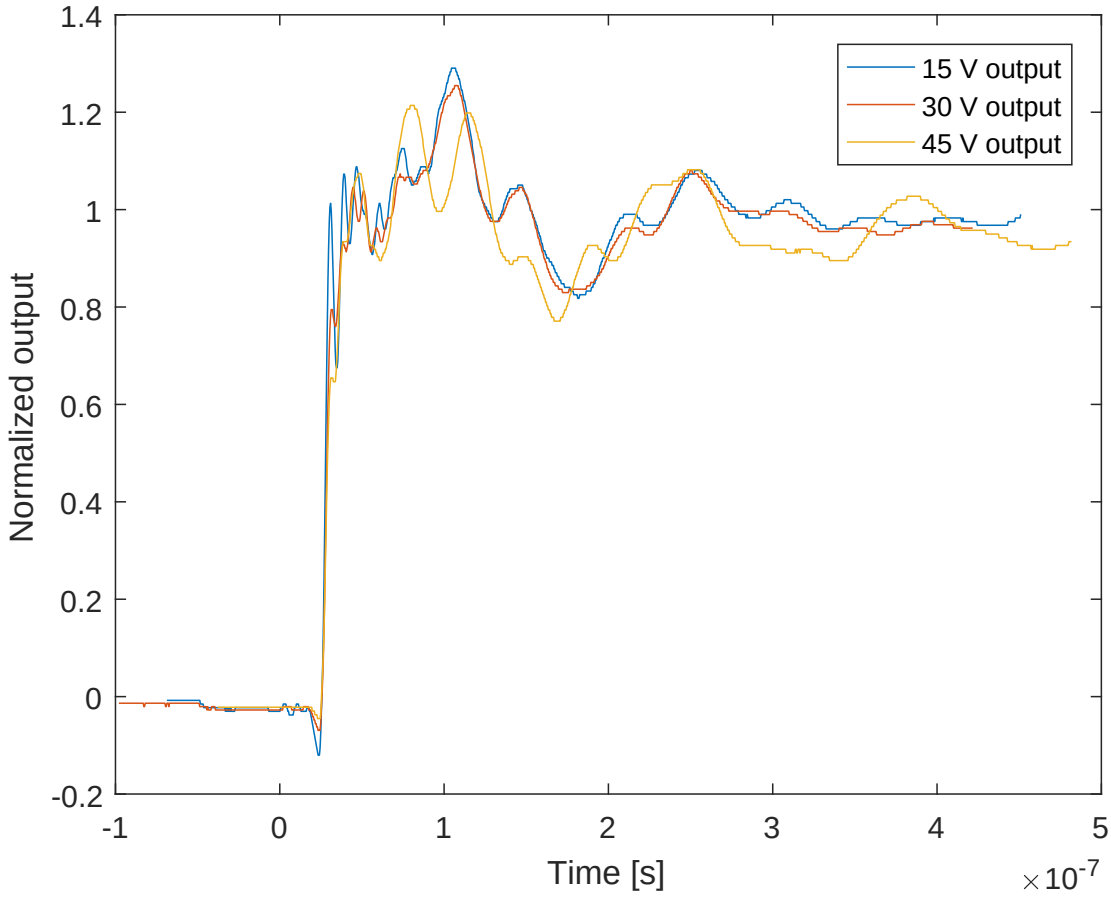


Figure 4.3: Normalized outputs of the rising flank with 15 V, 30 V and 45 V

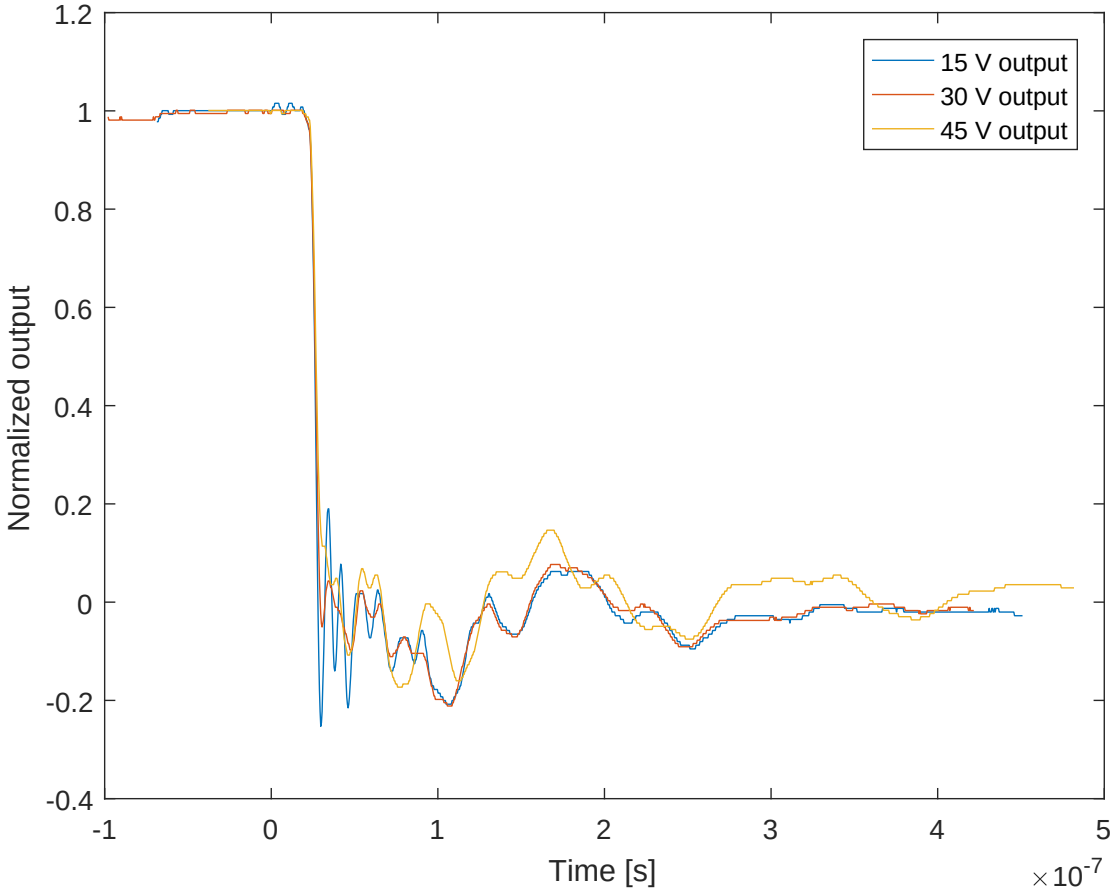


Figure 4.4: Normalized outputs of the falling flank with 15 V, 30 V and 45 V

rise time and fall time of the output is comparable to the previous measured rise and fall times with a rise time of around 3.4 ns and a fall time of around 3.6 ns. The rise time of the PWM signal generated by the FPGA is 12 ns.

4.3 Comparison between the outputs with and without FPGA

For better comparison of the output signal, a signal of the output with and without the FPGA at 500 kHz is shown in Figure 4.7. The output amplitude is 15V, the overshoot is around 32$\%$ for both signals

4.4 Measurements with load

All the previous Figures show signals with an unloaded output. The next few Figures will show the output with a resistive load of 60Ω. Figures 4.8 and 4.9 show the two input signals generated by the FPGA and the output. Figure 8 shows the rising flank of the output where Figure 4.9 shows the falling flank of the output. The output amplitude is 35 V, the frequencies used are 100 kHz up to 1 MHz and the dead time is 100 ns. The rise time is around 17 ns for every frequency, the fall time is around 4 ns for every frequency. The overshoot is 32$\%$ and the undershoot is 45$\%$ for all frequencies.

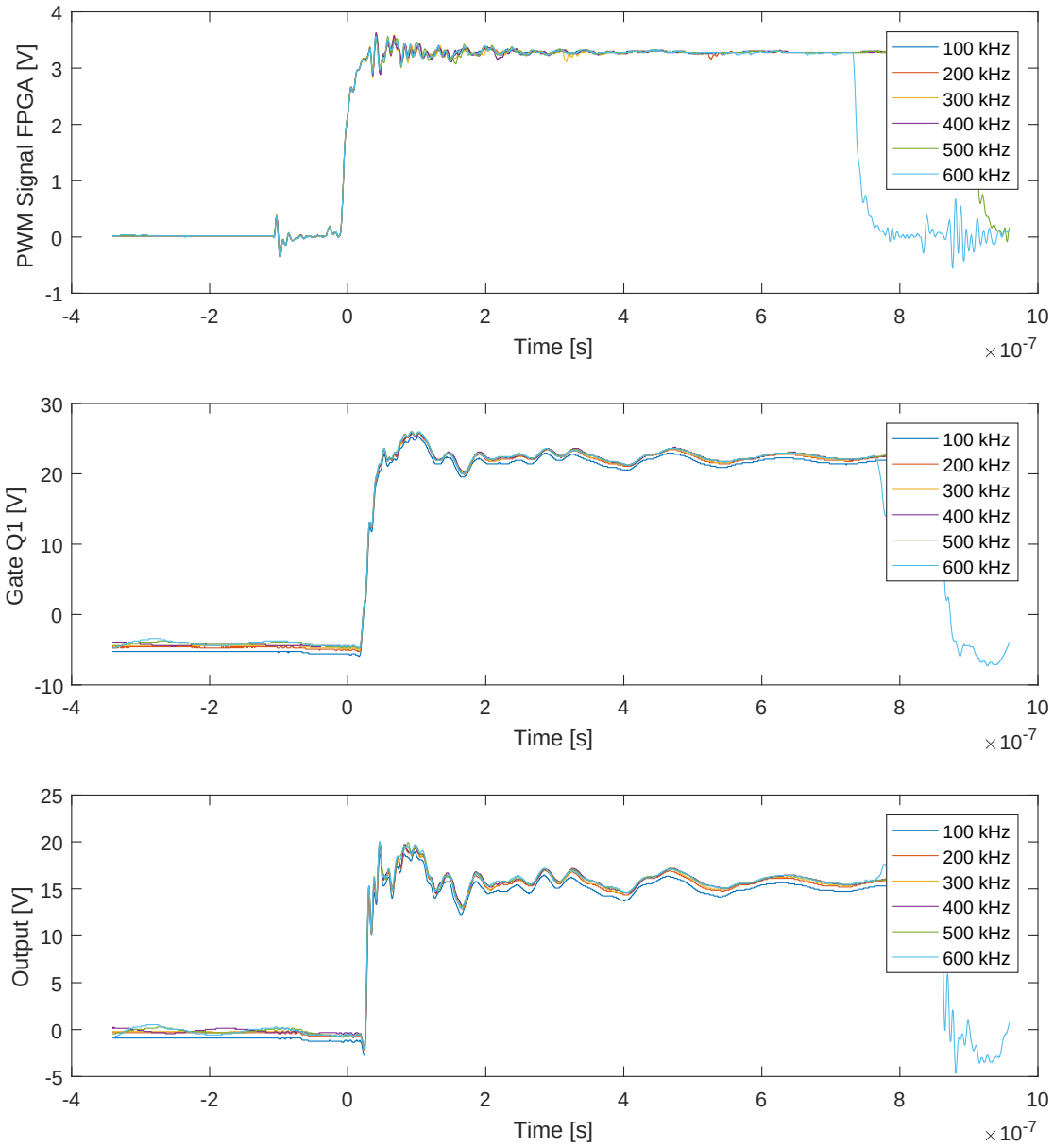


Figure 4.5: Top to bottom: FPGA signal, gate signal Q1 and the output

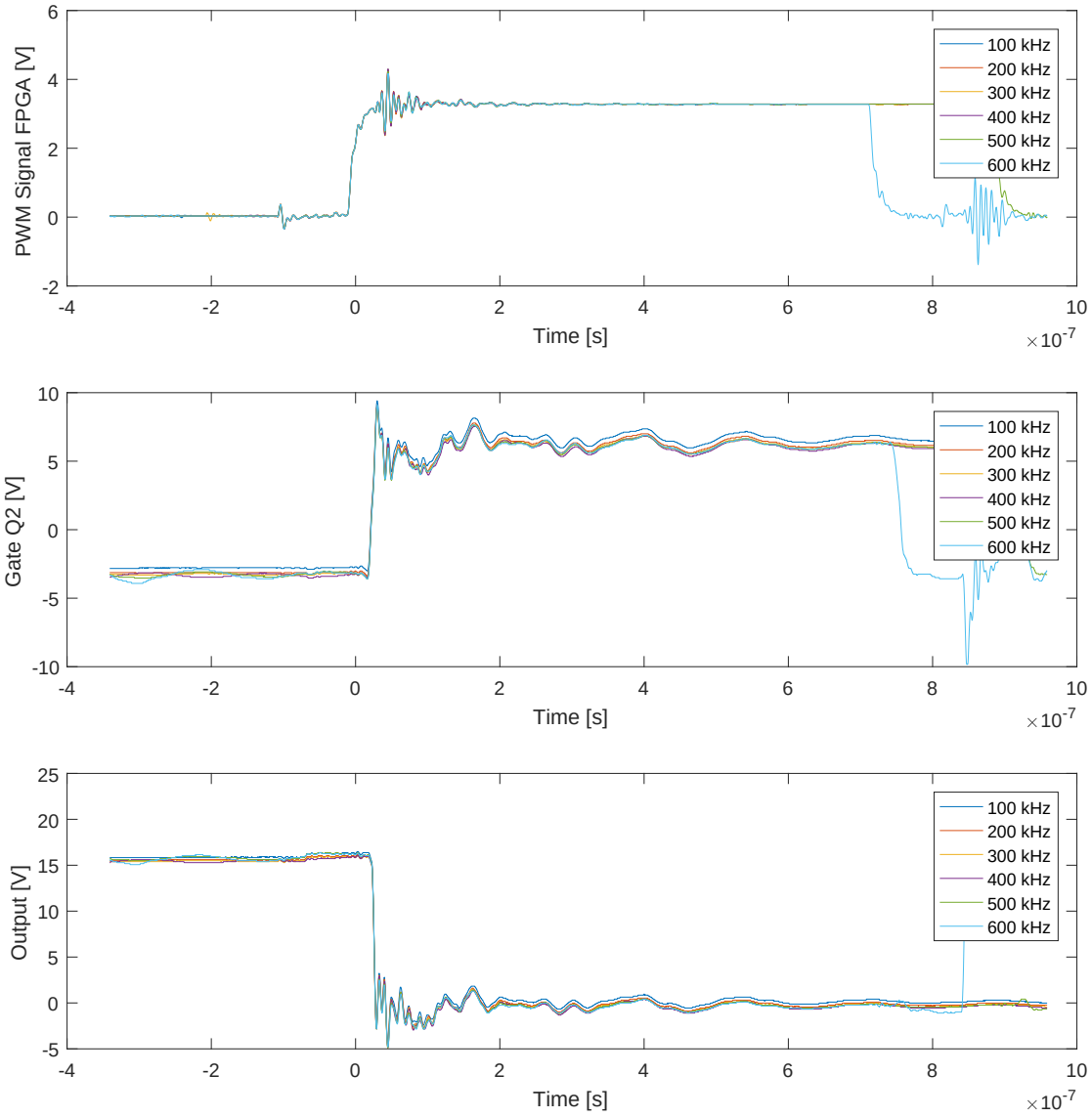


Figure 4.6: Top to bottom: FPGA signal, gate signal Q2 and the output

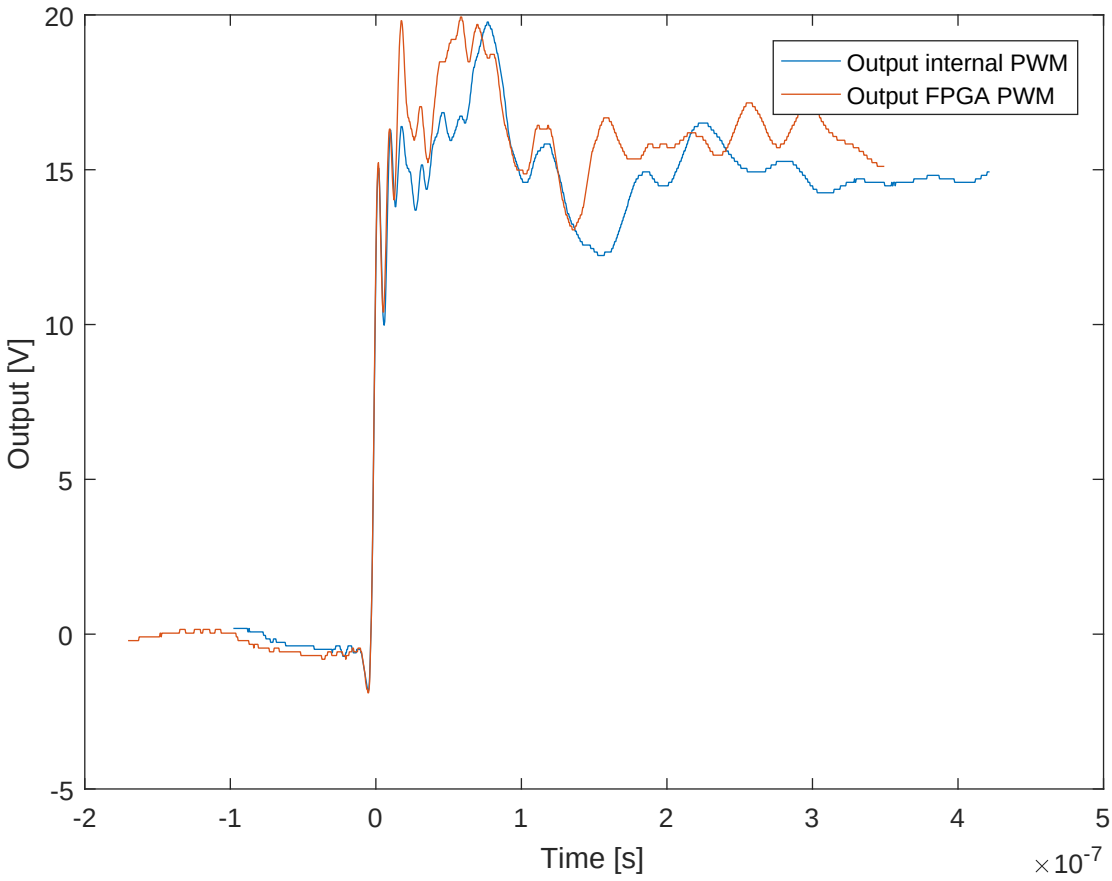


Figure 4.7: Comparison of a 500 kHz output signal with and without the FPGA

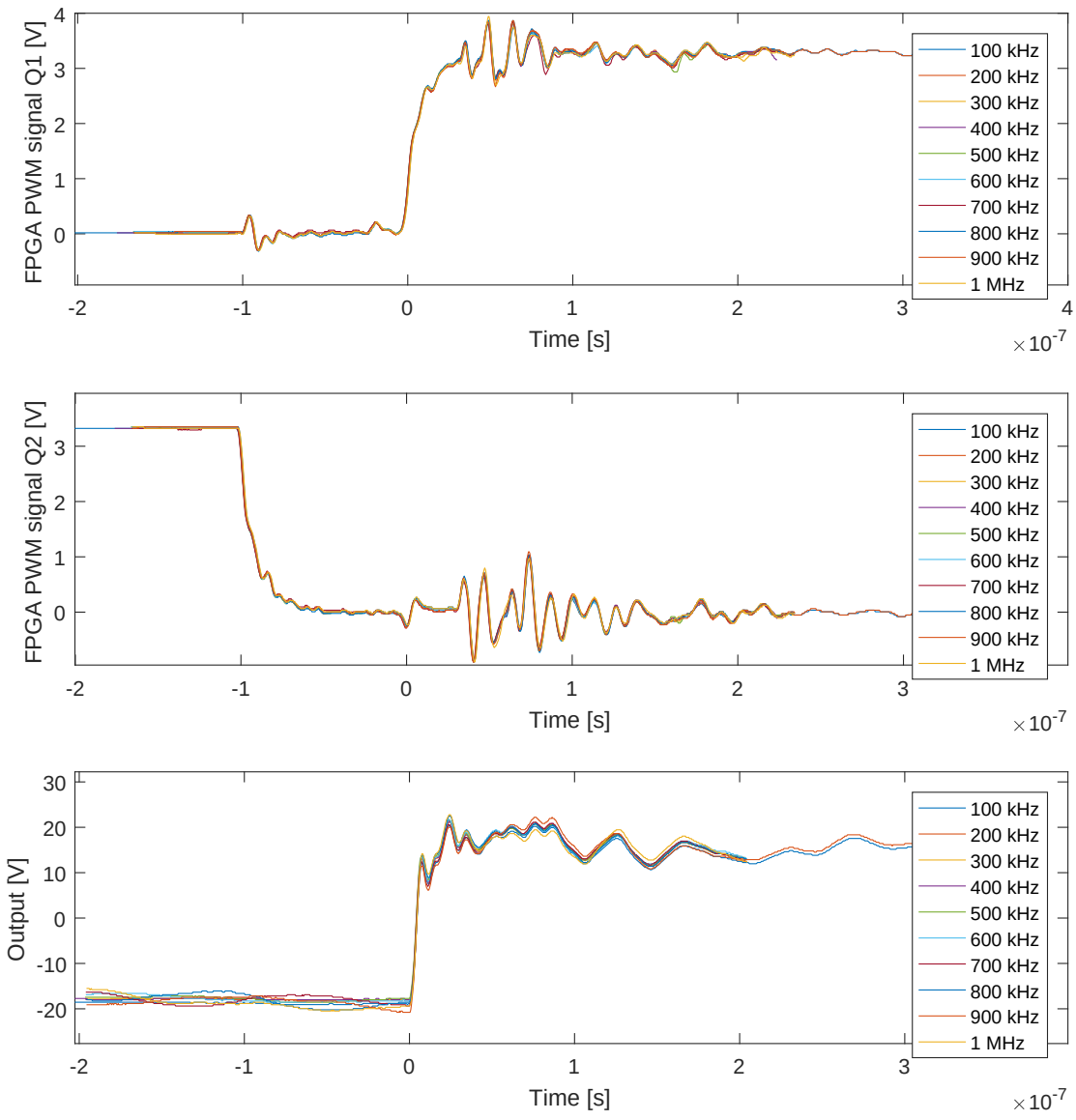


Figure 4.8: Loaded output with a PWM signal of 100 kHz up to 1 MHz

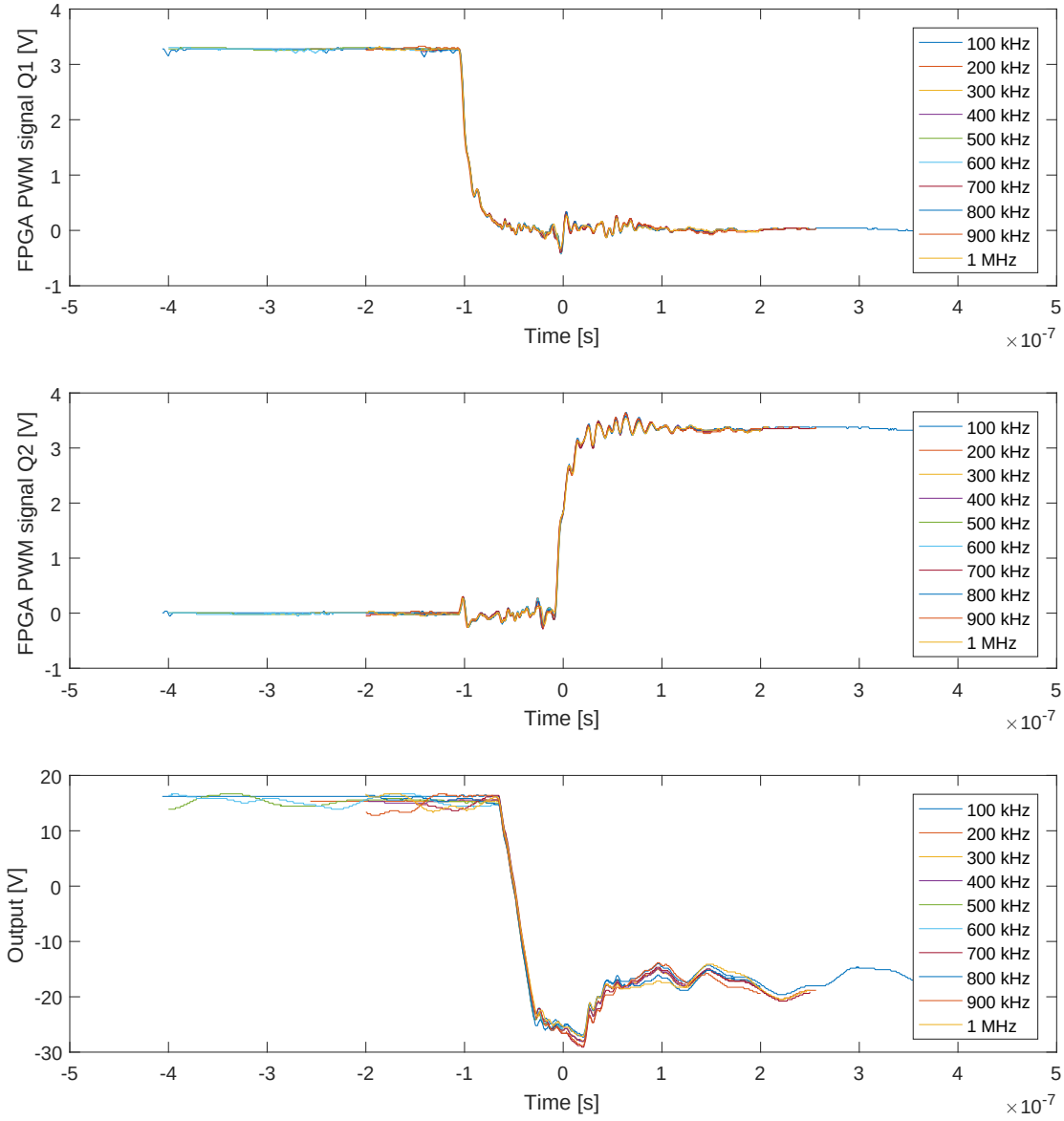


Figure 4.9: Loaded output with a PWM signal of 100 kHz up to 1 MHz

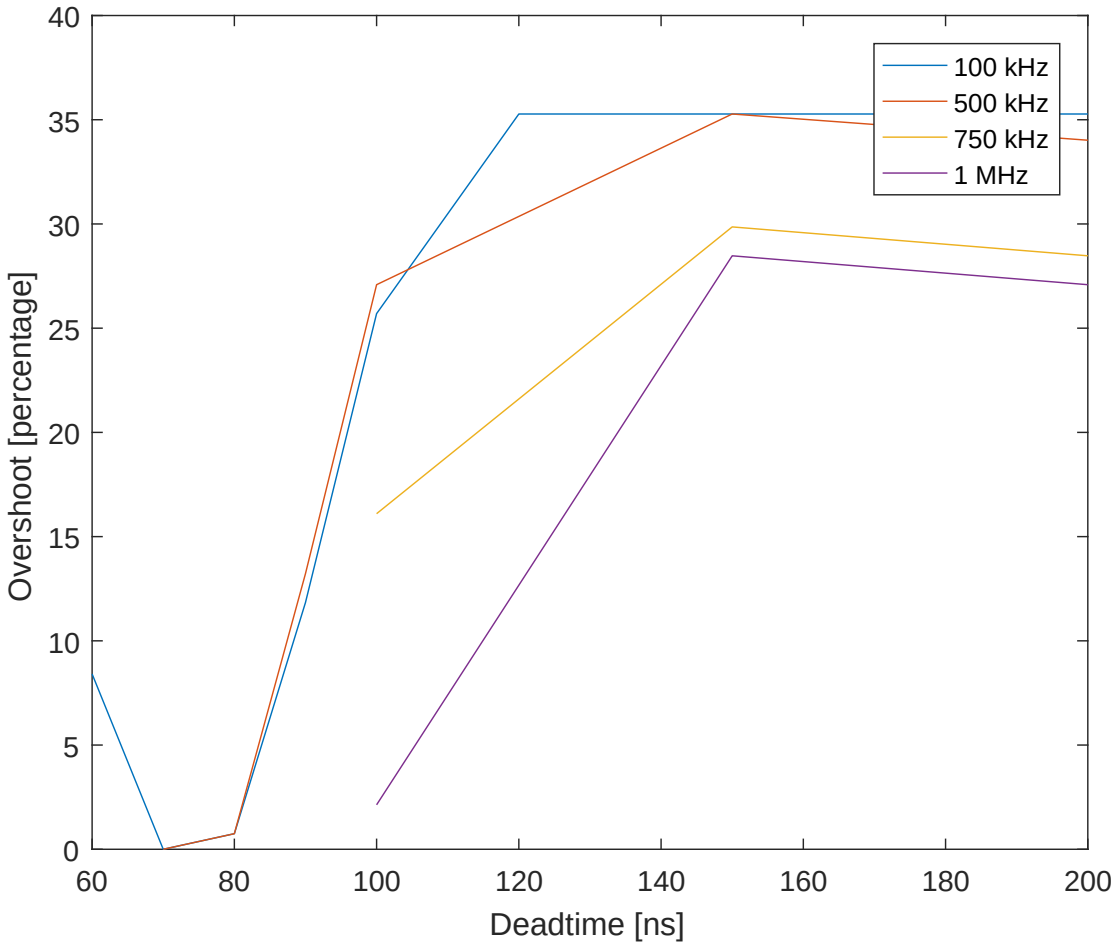


Figure 4.10: The Y axes shows the percentage of overshoot at the output, the X axes shows the set dead time

4.5 Variation in deadtime

By changing a bit of code the FPGA can change the output signal, in this case we measured the output signal with several frequencies and different dead times per frequency. Figure 4.10 shows the the overshoot at the output for different dead times per frequency.

5 Evaluation Discussion

5.1 Conclusion

The previous section of this report showed several measurements. Figures 4.1 and 4.2 show the ringing generated at the output is independent of the frequency where the input frequency is increased up to a frequency of 2 MHz. Also can be concluded that the rise and fall time stay the same for an unloaded Half-Bridge. Where the rise and fall time is the amount of time needed for the signal to get to its end state.
Figures 4.3 and 4.4 compares the same frequency with different output voltages. The rise times seem to get higher for higher voltage outputs, this is probably due to the ringing frequency interfering and keeping the signal under the 90$\%$ signal mark, since rise and fall time is the time it takes for the signal to get from 10$\%$ to 90$\%$. Overshoot is comparable percent wise, from that can be concluded that the amount of overshoot scales linearly with output voltage. The data shows ringing frequencies from 12 MHz up to 250 MHz, where it seems for higher output voltages the lower ringing frequencies get more predominant. The signals have similar rise time which means the 45 V signal has a higher $\frac{dV}{dt}$ than the 15 V and 30 V signals, this will have an influence on the parasitics and thus the ringing.
Figure 4.7 shows the effect of the FPGA on the output signal with the same output amplitude and same input frequency. The rise time is not affected by the FPGA, also the ringing frequencies range from 24 MHz to 500 MHz.
In the case of a loaded output the ringing frequencies are slightly different to the unloaded case, they are in the range of 20 MHz to around 200 MHz shown in Figures 4.8 and 4.9. These Figures also show that the FPGA is capable of driving the Half-Bridge module up to a frequency of 1 MHz, furthermore it shows that a load does not influence characteristics of the signal if the output voltage is constant and the frequency is changed. The last Figure shows that there is a relation between overshoot and dead time, dead time can be used to decrease overshoot and influence EMI.

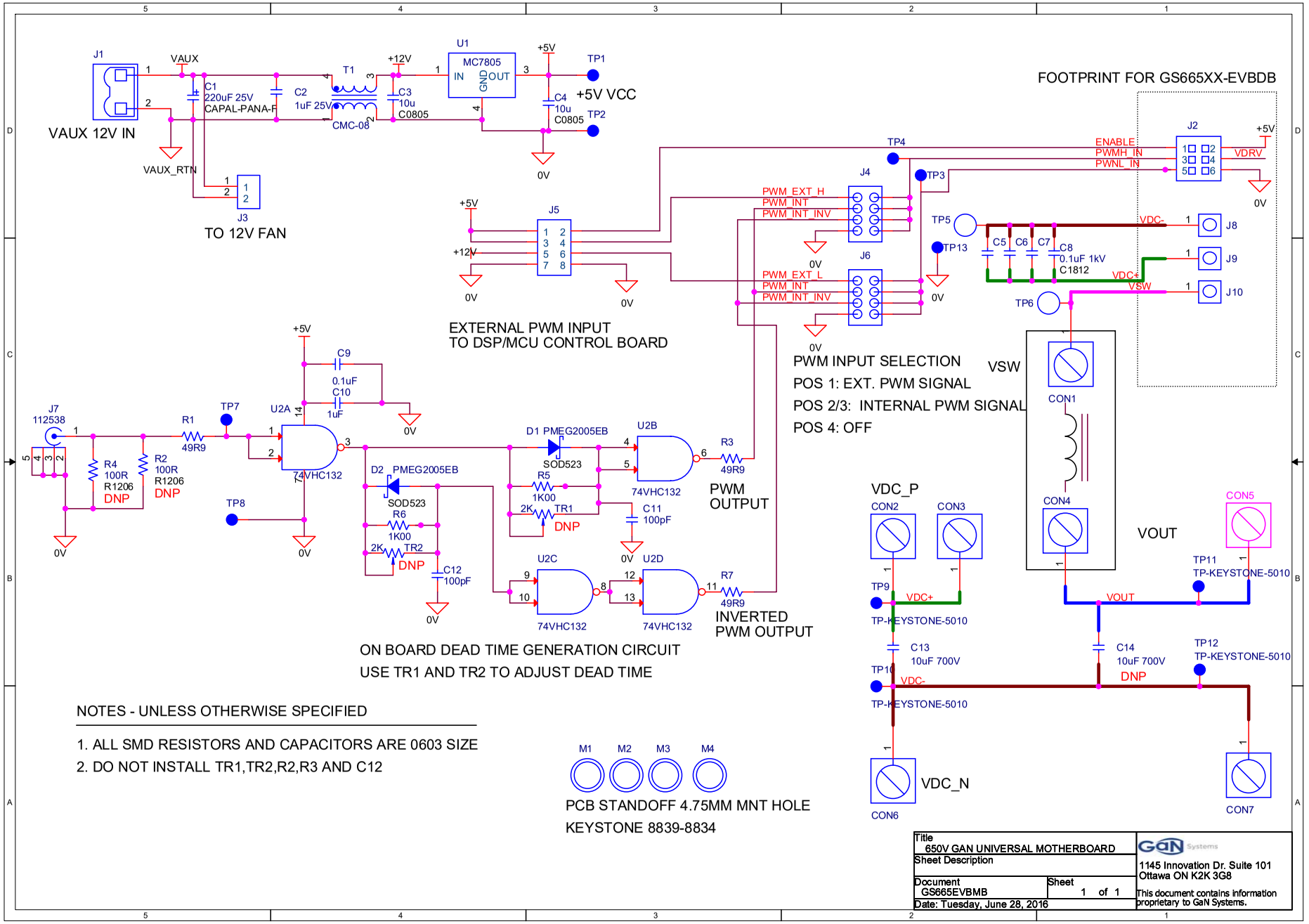
5.2 Future research

The report has shown that the module is capable of switching high frequencies up to 2 MHz and that the FPGA can drive the module as intended up to 1 MHz. Shown is that dead time has an influence on overshoot, a programmable FPGA might show useful in case the module will be stacked in a M3C system, where a slight variation in signal variables might make the difference between being electromagnetic compatibility or not.

Future research should look into the relation between dead time and the overshoot and ringing of the signal, also include several different output voltages and loads to see if results from this paper also apply to higher voltages up to 600 Volt.

Appendix

The following pages show relevant documents. It consists of parts of data sheets and circuit diagrams.


VAUX 12V IN
VAUX_RTN
TO 12V FAN
+5V VCC
MC7805
EXTERNAL PWM INPUT
TO DSP/MCU CONTROL BOARD
PWM INPUT SELECTION
POS 1: EXT. PWM SIGNAL
POS 2/3: INTERNAL PWM SIGNAL
POS 4: OFF
PWM OUTPUT
INVERTED
PWM OUTPUT
ON BOARD DEAD TIME GENERATION CIRCUIT
USE TR1 AND TR2 TO ADJUST DEAD TIME
FOOTPRINT FOR GS665XX-EVBDB
VDC_P
VDC_N
VSW
VOUT
NOTES - UNLESS OTHERWISE SPECIFIED
1. ALL SMD RESISTORS AND CAPACITORS ARE 0603 SIZE
2. DO NOT INSTALL TR1,TR2,R2,R3 AND C12
PCB STANDOFF 4.75MM MNT HOLE
KEYSTONE 8839-8834
Title
650V GAN UNIVERSAL MOTHERBOARD
Sheet Description
Document
GS665EVBMB
Sheet
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Date: Tuesday, June 28, 2016
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This document contains information proprietary to GaN Systems.

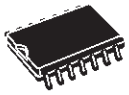
B

74VHC132

QUAD 2-INPUT SCHMITT NAND GATE

PRELIMINARY DATA

- HIGH SPEED: t_{PD} = 4.9 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 2 µA (MAX.) at T_A = 25 °C
- TYPICAL HYSTERESIS: V_h = 1V at V_{CC} = 4.5V
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 132
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.8V (Max.)



M
(Micro Package)

T
(TSSOP Package)

ORDER CODES :

74VHC132M 74VHC132T

DESCRIPTION

The 74VHC132 is an advanced high-speed CMOS QUAD 2-INPUT SCHMITT NAND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

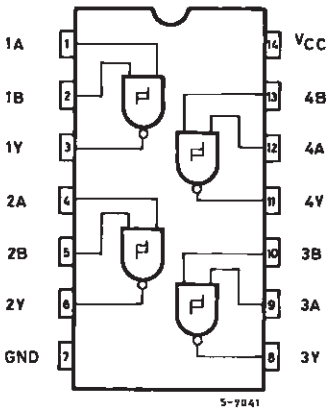
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

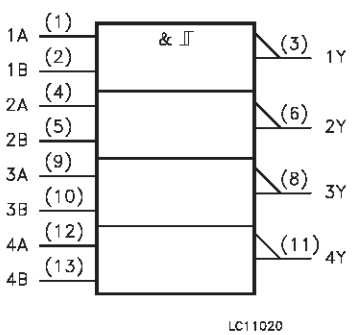
Pin configuration and function are the same as those of the VHC00 but the VHC132 has hysteresis.

This together with its schmitt trigger function allows it to be used on line receivers with slow rise/fall input signals.

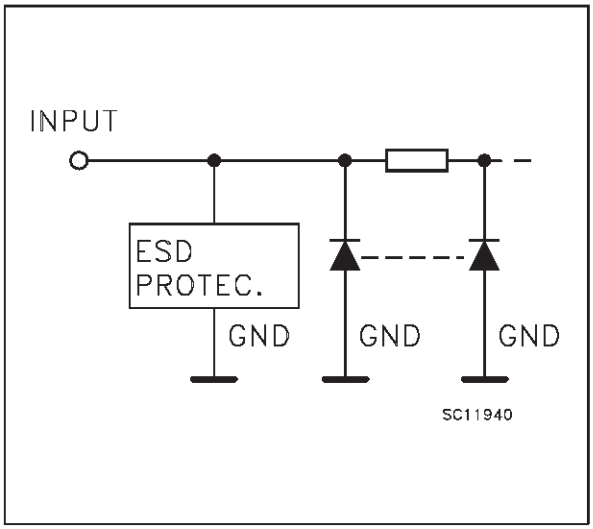
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.0 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{t+}	High Level Threshold Voltage	3.0		2.2			2.2		V
		4.5		3.15			3.15		
		5.5		3.85			3.85		
V_{t-}	Low Level Threshold Voltage	3.0				0.9		0.9	V
		4.5				1.35		1.35	
		5.5				1.65		1.65	
V_h	Hysteresis Voltage	3.0		0.3		1.2	0.3	1.2	V
		4.5		0.4		1.4	0.4	1.4	
		5.5		0.5		1.6	0.5	1.6	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		
		4.5	I_O=-50 µA	4.4	4.5		4.4		
		3.0	I_O=-4 mA	2.58			2.48		
		4.5	I_O=-8 mA	3.94			3.8		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1	
		4.5	I_O=50 µA		0.0	0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44	
		4.5	I_O=8 mA			0.36		0.44	
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			2		20	µA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f =3 ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	3.3(*)	15			7.6	11.9	1.0	14.0	ns
		3.3(*)	50			10.1	15.4	1.0	17.5	
		5.0(**)	15			4.9	7.7	1.0	9.0	
		5.0(**)	50			6.4	9.7	1.0	11.0	

(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T_A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			4	10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)			16				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per Gate)

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{t+}	High Level Threshold Voltage	3.0		2.2			2.2		V
		4.5		3.15			3.15		
		5.5		3.85			3.85		
V_{t-}	Low Level Threshold Voltage	3.0				0.9		0.9	V
		4.5				1.35		1.35	
		5.5				1.65		1.65	
V_h	Hysteresis Voltage	3.0		0.3		1.2	0.3	1.2	V
		4.5		0.4		1.4	0.4	1.4	
		5.5		0.5		1.6	0.5	1.6	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		
		4.5	I_O=-50 µA	4.4	4.5		4.4		
		3.0	I_O=-4 mA	2.58			2.48		
		4.5	I_O=-8 mA	3.94			3.8		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1	
		4.5	I_O=50 µA		0.0	0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44	
		4.5	I_O=8 mA			0.36		0.44	
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			2		20	µA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f =3 ns)

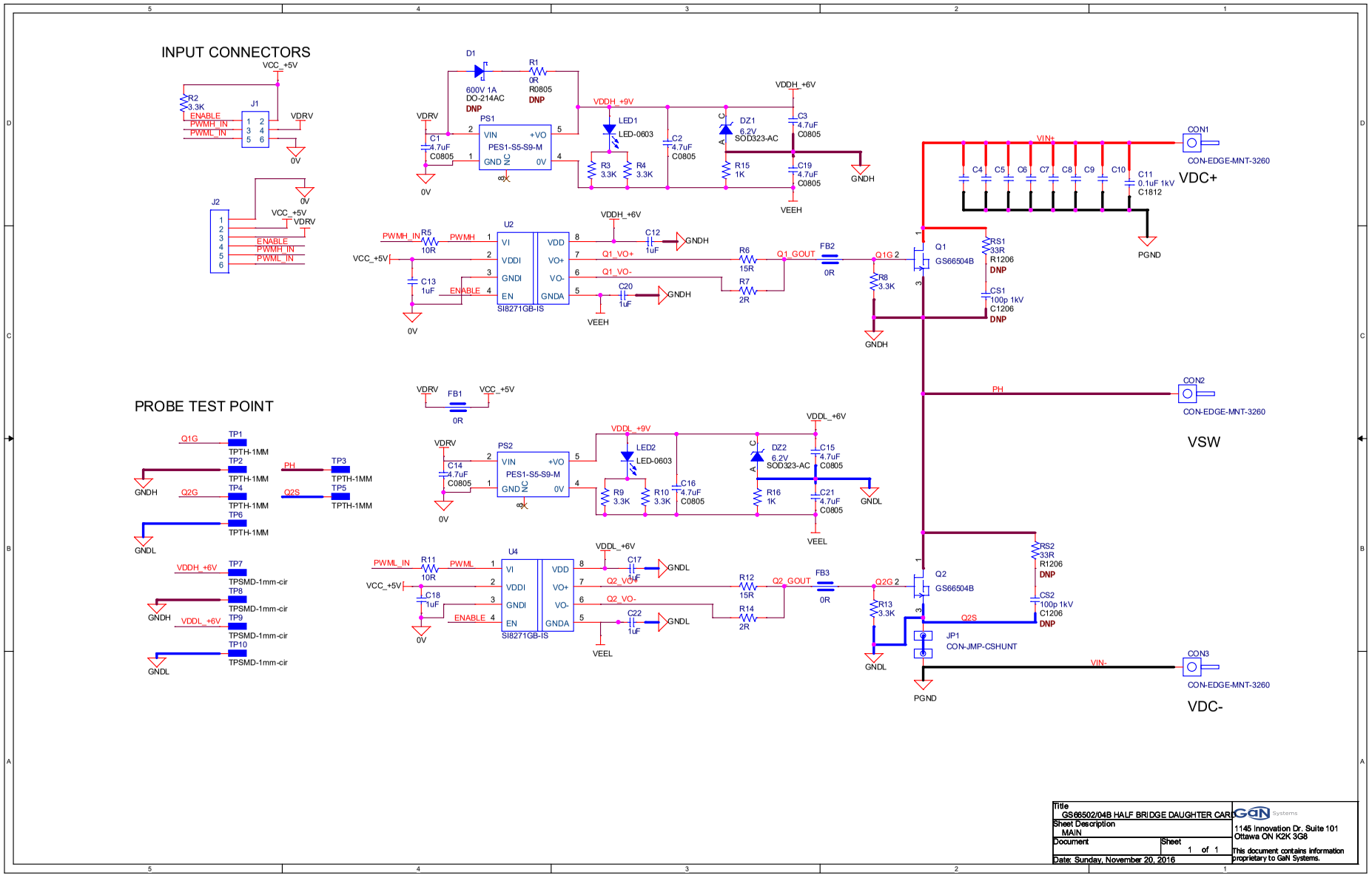
Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	3.3(*)	15			7.6	11.9	1.0	14.0	ns
		3.3(*)	50			10.1	15.4	1.0	17.5	
		5.0(**)	15			4.9	7.7	1.0	9.0	
		5.0(**)	50			6.4	9.7	1.0	11.0	

(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T_A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			4	10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)			16				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per Gate)


INPUT CONNECTORS
PROBE TEST POINT
VCC_+5V
VDRV
0V
ENABLE
PWMH_IN
PWML_IN
VDDH_+6V
VDDH_+9V
VDDL_+6V
VDDL_+9V
VEEH
VEEL
GNDH
GNDL
PGND
PH
Q1_GOUT
Q2_GOUT
Q1_VO+
Q1_VO-
Q2_VO+
Q2_VO-
Q1G
Q2G
Q2S
VIN+
VIN-
VSW
VDC+
VDC-
SI8271GB-IS
PES1-S5-S9-M
GS66504B
CON-EDGE-MNT-3260
CON-JMP-CSHUNT
TPTH-1MM
TPSMD-1mm-cir
600V 1A
DO-214AC
LED-0603
SOD323-AC
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C0805
C1812
R1206
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4. Electrical Specifications

Table 4.1. Electrical Characteristics

V_{DDI} = 5 V, GNDI = 0 V, VDDA/B-GNDA/B = 30 V, T_A = –40 to +125 °C; typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input Supply Voltage	VDDI		2.5	—	5.5	V
Driver Supply Voltage	(VDDA/B – GNDA/B)		4.2	—	30	V
Input Supply Quiescent Current	IDDI(Q)		—	7.9	10.0	mA
Input Supply Active Current	IDDI	f = 500 kHz	—	8.0	10.0	mA
Output Supply Quiescent Current	IDDx(Q)		—	2.5	4.0	mA
Output Supply Active Current	IDDx	f = 500 kHz	—	10.0	11.0	mA
Gate Driver						
High Output Transistor RDS (ON)	R_{OH}		—	2.7	—	Ω
Low Output Transistor RDS (ON)	R_{OL}		—	1.0	—	Ω
High Level Peak Output Current	I_{OH}	$V_{DDA/B}$ = 15 V, See Figure 4.2 IOH Source Current Test Circuit on page 19 for Si827xG, V_{DD} = 4.2 V, T < 250 ns	—	1.8	—	A
Low Level Peak Output Current	I_{OL}	$V_{DDA/B}$ = 15 V, See Figure 4.1 IOL Sink Current Test Circuit on page 19 for Si827xG, V_{DD} = 4.2 V, T_{PW_IOL} < 250 ns	—	4.0	—	A
UVLO						
VDDI UVLO Threshold +	$VDDI_{UV+}$		1.85	2.2	2.45	V
VDDI UVLO Threshold –	$VDDI_{UV-}$		1.75	2.1	2.35	V
VDDI Hysteresis	$VDDI_{HYS}$		—	100	—	mV
UVLO Threshold + (Driver Side)						
3 V Threshold	$VDDX_{UV+}$		2.7	3.5	4.0	V
5 V Threshold			4.9	5.5	6.3	V
8 V Threshold			7.2	8.3	9.5	V
12 V Threshold			11	12.2	13.5	V
UVLO Threshold - (Driver Side)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
3 V Threshold	$VDDX_{UV-}$		2.5	3.2	3.8	V
5 V Threshold			4.6	5.2	5.9	V
8 V Threshold			6.7	7.8	8.9	V
12 V Threshold			9.6	10.8	12.1	V
UVLO Lockout Hysteresis						
3 V Threshold	VDD_{HYS}		—	300	—	mV
5 V Threshold			—	300	—	mV
8 V Threshold			—	500	—	mV
12 V Threshold			—	1400	—	mV
Digital						
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VIHYST		350	400	—	mV
Logic High Output Voltage	VOH	IO = –1 mA	VDDA/B – 0.04	—	—	V
Logic Low Output Voltage	VOL	IO = 1 mA	—	—	0.04	V
AC Switching Parameters						
Propagation Delay Si8271/3/5 with low jitter	t_{PLH}, t_{PHL}	C_L = 200 pF	20	30	60	ns
Propagation Delay Si8271/3/5 with de-glitch option	t_{PLH}, t_{PHL}	C_L = 200 pF	30	45	75	ns
Propagation Delay Si8274 with low jitter	t_{PHL}	C_L = 200 pF	20	30	60	ns
Propagation Delay Si8274 with de-glitch option	t_{PHL}	C_L = 200 pF	30	45	75	ns
Propagation Delay Si8274 with low jitter	t_{PLH}	C_L = 200 pF	30	45	75	ns
Propagation Delay Si8274 with de-glitch option	t_{PLH}	C_L = 200 pF	65	85	105	ns
Pulse Width Distortion Si8271/3/5 all options	PWD	|tPLH – tPHL|	—	3.6	8	ns
Pulse Width Distortion Si8274 with low jitter	PWD	|tPLH – tPHL|	—	14	19	ns
Pulse Width Distortion Si8274 with de-glitch option	PWD	|tPLH – tPHL|	—	38	47	ns
Peak to Peak Jitter Si827x with low jitter			—	200	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmed dead-time (DT) for products with 10–200 ns DT range	DT	RDT = 6 kΩ	10	20	30	ns
		RDT = 15 kΩ	26	38	50	
		RDT = 100 kΩ	150	210	260	
Programmed dead-time (DT) for products with 20–700 ns DT range	DT	RDT = 6 kΩ	23	40	57	ns
		RDT = 15 kΩ	60	95	130	
		RDT = 100 kΩ	450	610	770	
Rise time	t_R	CL = 200 pF	4	10.5	16	ns
Fall time	t_F	CL = 200 pF	5.5	13.3	18	ns
Device Startup Time	t_{START}		—	16	30	µs
Common Mode Transient Immunity Si827x with de-glitch option		See Figure 4.3 Common Mode Transient Immunity Test Circuit on page 20. VCM = 1500 V	200	350	400	kV/µs
Common Mode Transient Immunity Si827x with low jitter option		See Figure 4.3 Common Mode Transient Immunity Test Circuit on page 20. VCM = 1500 V	150	300	400	kV/µs

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