June 28, 2018

BACHELOR ASSIGNMENT

ELECTROMAGNETIC INTERFERENCE ANALYSIS OF CLASS D AMPLIFIERS

Harm Reurslag

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Integrated circuit design

UNIVERSITY OF TWENTE.

Abstract:
Class D amplifiers provide audio amplification with a very high efficiency as they use uses pulse width modulation instead of linear gain, this modulation is easier to amplify using two MOSFETs. The downside of this system is the rapid switching and therefore rapid current change, which induces voltages in parasitic inductors which combined with parasitic capacitors produce oscillations and create electromagnetic interference (EMI). This paper aims to shed light on where the parasitic inductors and capacitors are located so that these oscillations can be reduced in future designs. In order to find these parasitics the class D amplifier circuit was simulated in LTspice and the induced voltage of every inductor was analysed by multiplying the rate of current change with the inductance value. These inductors were tested for their ability to change the frequency. With this information a circuit was built and the effect of the inductors was tested by varying the length of the wires between every component. The parasitic capacitances of the transistors were tested by adding capacitances in parallel to the transistors. The most significant inductors are located in a loop through the powerMOSFETs and the decoupling capacitors. The significant parasitic capacitor was located in the power-NMOS capacitances. With this information the root cause of parasitic oscillations is known and can be used to optimize the power stage for minimum EMI.

Contents

Chapter 1

Introduction

1.1 Context

The use of class D amplifiers is increasing every day as they compare favorably energy consumption wise to other audio amplifiers while their audio quality is similar. The disadvantage however is the EMI (electromagnetic interference) that is produced by the frequent voltages drops and rises and the very fast switching currents. In this report an analysis of this EMI will be done to identify what components cause this behavior. This research is based on the research done earlier by Ragheed Haddad whose inductor values [1] are used in this report.

1.2 Class D amplifier basics

The reason why a class D amplifier creates a lot of EMI is because it amplifies pulse width modulation (PWM) signals instead of an analogue signal. The class D amplifier modulates a low power analogue signal to a low power PWM signal which then is amplified using two big power MOSFETs. This large PWM signal can be filtered to get the analogue signal back but with increased magnitude. This working is displayed in figure 1.1

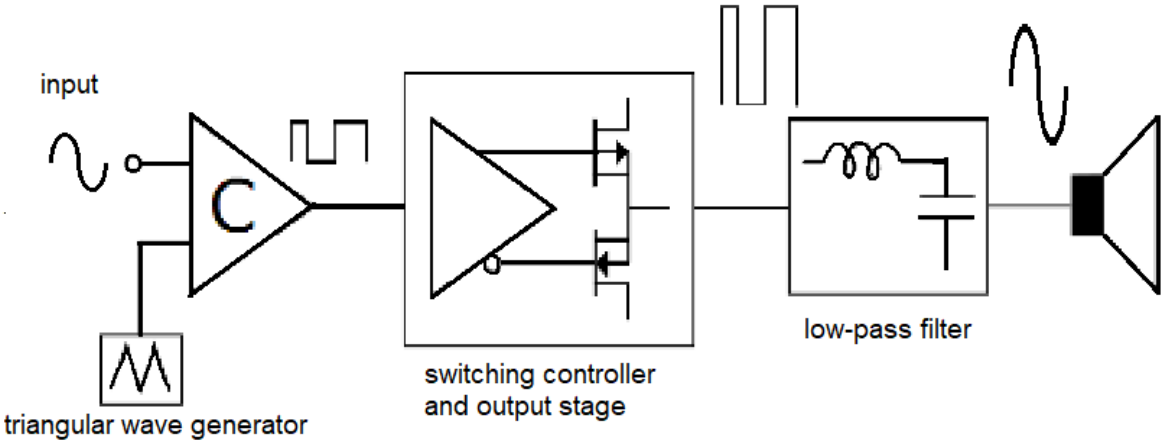


Figure 1.1: Circuit of a class D amplifier [2]

Because the oscillation occurs in the switching power circuit, the experiments will be done with only that part of the circuit, with a square wave generator as input to avoid any unnecessary interfacing errors.

1.3 Research question

Unfortunately this working does not happen flawlessly, as the amplification stage causes an oscillation somehow at the amplification output:

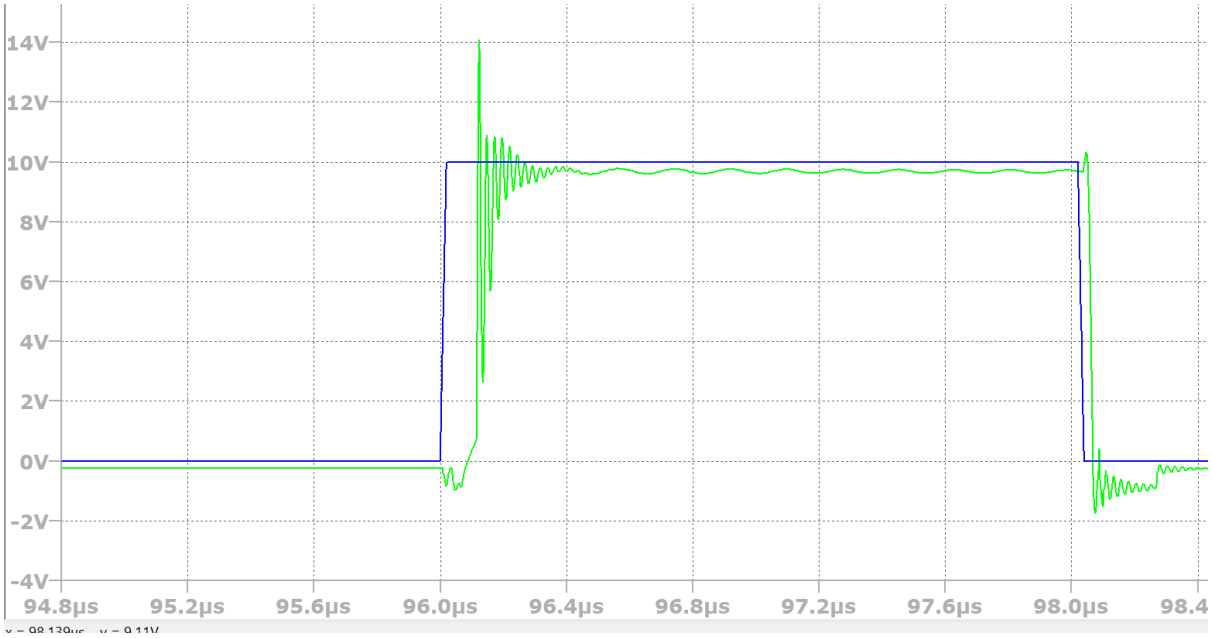


Figure 1.2: The blue waveform represents the theoretical waveform, the green waveform shows what happens in reality.

The EMI in figure 1.2 is generated by an oscillation which is caused by the combination of an initial energy input, an inductance and a capacitance. There are many parasitic inductances such as wires and many parasitic capacitances in the transistors. Combined with frequent voltage switching an oscillation occurs, it is unclear however which of these parasitics cause this effect. Insight into the oscillation loops would be helpful to find a solution to this problem. The main research question is formulated as follows: *What parasitic inductances and capacitances cause the ringing observed at the output of the power stage of a class D amplifier?*
To investigate this, a circuit will be built physically and one will be modeled in LTspice to compare the simulation with measurement results. After that the LC tanks will be identified by removing or adding extra inductors or capacitors.

1.4 Report outline

In this report it will be demonstrated which parasitic inductors and capacitors cause the ringing of a class D amplifier. In chapter 2 information will be gathered using LTspice to determine what to look for during the physical experiment. The realization of the circuit will be documented in chapter 3 and the experiments in 4. In chapter 5 the LTspice model will be matched to the observations to get insight into all parasitics. The whole report will be concluded in chapter 6.

1.5 Comments on the previous report

As mentioned in the introduction this research is based on the research performed earlier, the research paper [1] contained the same research question but did not manage to find the parasitic inductors and capacitors that cause the ringing. Although the solution to the problem was not found, it did have a good base to build the research further. A working model was already constructed which represents the class D amplifier quite well. The model will be reused in the modeling chapter to create an hypothesis, the values of the model will be reevaluated to be sure that the model is correct. The physical circuit analysis will be redone entirely, but will be done in a similar fashion, as it looked like the previous report was on the right track.

Chapter 2

LTspice modeling

2.1 Introduction

To find the parasitic oscillation, LTspice will be used. LTspice simulates circuit behaviour, so it is perfect for analysing which LC tank creates the oscillation. The parasitic inductances measured in the previous report [1] will be implented in the LTspice simulation, but the latest transistor models are used so those are different than those from the previous report.

2.2 The circuit

First of all, the circuit with all the parasitic inductances from the previous report [1] was rebuilt in LTspice which resulted in figure: 2.1 (note: the parasitic capacitances are already present in the transistor models).

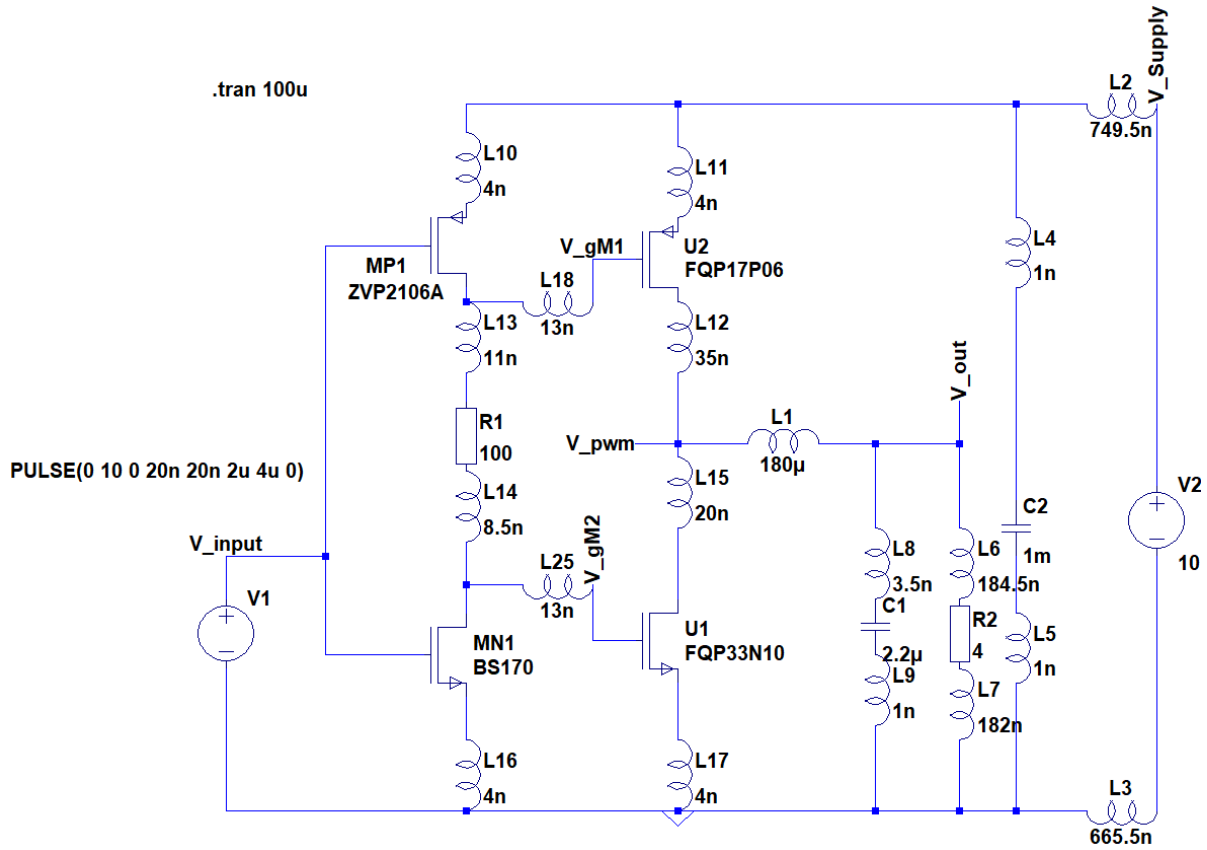


Figure 2.1: LTspice circuit of the class D amplifier with paracitics from the previous report [1].

The circuit works as follows: First a square wave is put in to the driver transistors which create a small time delay in the circuit to make sure that the supply is never shorted. Then, the square wave is amplified using the two powerMOSFETs. The amplified square wave is filtered and then put into the load to return the amplified decoded signal. Running a simulation of this circuit and displaying the V_pwm waveform clearly shows the oscillation problem. In figure 2.2 it can be seen that every time

Mosfets switch an oscillation is initiated. For this research it is irrelevant what the duty cycle is so it is kept at 50% for every experiment.

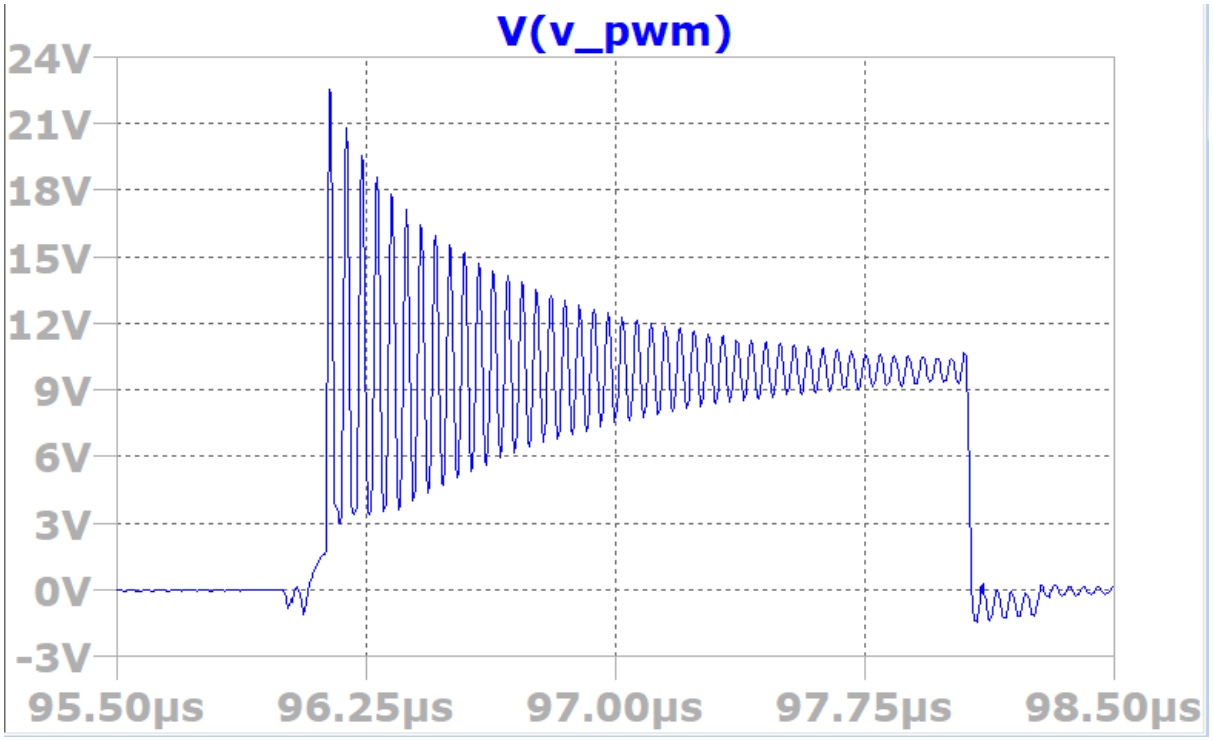


Figure 2.2: LTspice simulation of class D amplifier in figure 2.1

2.3 Rate of current change analysis

In the class D amplifier the MOSFET switching causes currents to change very rapidly. This rapid change induces a voltage, this voltage has a linear relation with the rate of change of the current through the inductor. The equation for an inductors voltage is:

$$V(t) = L\frac{dI}{dt} \tag{2.1}$$

To look for the inductors which cause the enormous ringing an analysis of all the current changes during the initial switch of The MOSFET is performed. Table 2.1 was created by checking the derivative of the current through every inductor and writing down the maximum value for each inductor. In this table it can be seen which inductors create big voltage changes.

Table 2.1: Analysis of Voltage changes during switching

stage	Inductor	current chage	inductor value	resulting voltage change	significance
Driver	L10	80MA/s	4n	0.3V	0
Driver	L13	25MA/s	11n	0.3V	0
Driver	L14	25MA/s	8.5n	0.2V	0
Driver	L16	160MA/s	4n	0.6V	0
Driver	L18	80MA/s	13n	1V	+
Driver	L25	370MA/s	13n	4V	++
Power	L11	370MA/s	4n	1.3V	+
Power	L12	370MA/s	35n	12V	++
Power	L15	370MA/s	20n	7V	++
Power	L17	370MA/s	4n	1.4V	+
Load	L8	26kA/s	3.5n	<0.1V	-
Load	L9	26kA/s	1n	<0.1V	-
Load	L6	17kA/s	184n	<0.1V	-
Load	L7	17kA/s	182n	<0.1V	-
Decoupling	L4+L5	420MA/s	2n	0.8V	0
Supply	L2	10kA/s	750n	<0.1V	-
Supply	L3	10kA/s	655n	<0.1V	-
Integrator	L1	27kA/s	180u	4.9V	++

These values give a strong indication that the oscillation is caused by the parasitic inductances of the power stage. Some current also flows trough the BS170 transistor via L16 and L18. Since the oscillation needs to go through a loop it is expected that it flows back via the decoupling capacitors as this path has the least impedance for a high frequency oscillation.

2.4 Determining the lowest impedance path

Now that there is an indication of which path to look for this hypothesis will be tested by looking at the impedances of all components and parasitics at 40MHz (the observed ringing frequency) and checking whether a clear path can be identified using this method. Because transistors cannot be modeled in this way an assumption is made: during the oscillation the BS170 and the FQP16P07 are on and the ZVP2106A and FQP33N10 are off. Transistor values are from their datasheets.

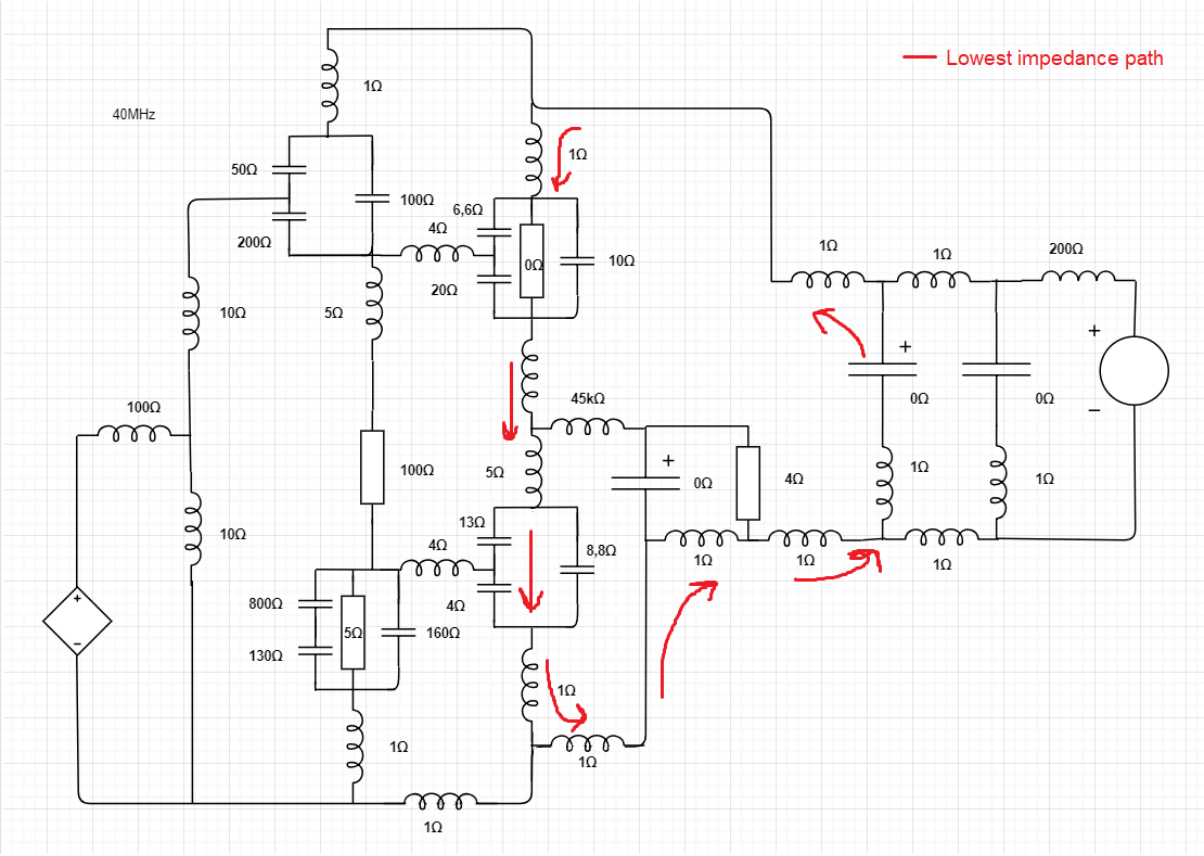


Figure 2.3: all components with their impedances

From figure 2.3 it can be seen that the impedance at 40MHz varies a lot between paths, this means that there are only a few possibilities for the oscillation loops. The two paths with the lowest impedance are also the paths which had the inductors with the highest induced voltages. The path with the lowest impedance is through the power stage.

2.5 Conclusion

Based on the experiments done in this chapter it follows that the oscillation is caused by inductors and capacitors in the main loop which is through the power stage and decoupling capacitors. There is another loop with a slightly higher impedance which could also influence the oscillation which goes through the driver NMOS. This hypothesis will be tested in chapter 4

Chapter 3

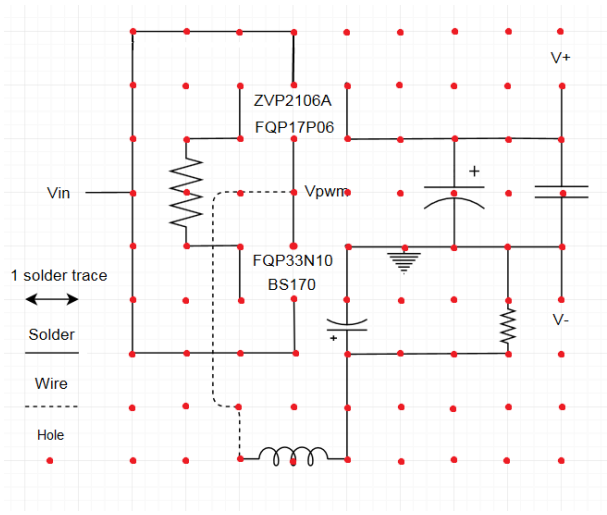
Circuit realization

3.1 Introduction

In order to test whether the behavior of the circuit is similar to the behavior model the circuit has to be created. The circuit will be soldered to an experimental through hole circuit board with thick solder traces to have reliable parasitic inductances. During inductance testing it was found that using wires instead of solder traces can yield different inductance results which should be avoided as much as possible as a slight change changes measurement results, exceptions have been made for a wire in series with the output filter inductor and the wires to the DC supply and function generator as they already have a very high series resistance.

3.2 The first circuit

A plan was made to solder the circuit with a minimal distance for the power stage, this plan can be seen in figure 3.1a. This circuit had a nice oscillation which was good to analyze with a small ground loop probe. The problem was that the small scale was impractical as there was no extra space for adding parasitics.



(a) Plan for soldering the circuit

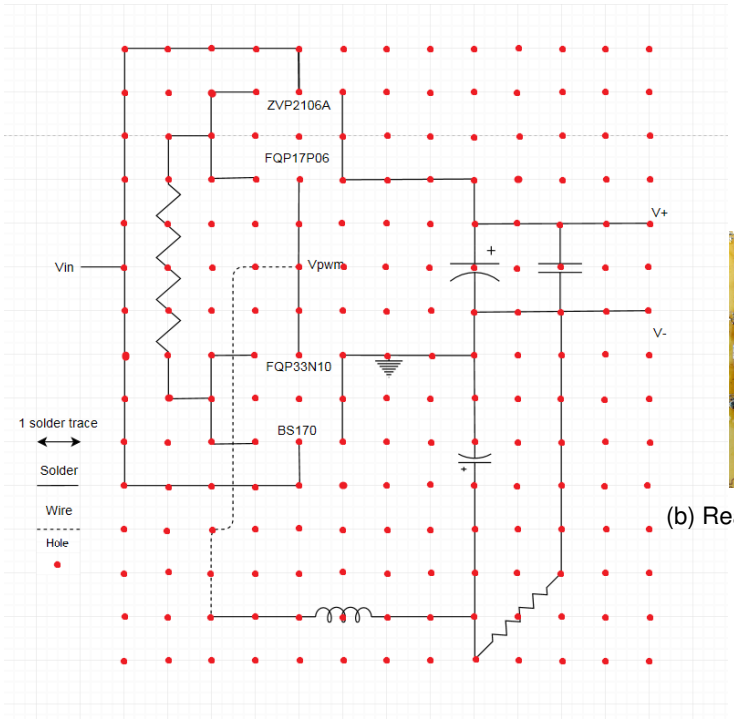
(b) Realization of the circuit

Figure 3.1: Plan and realization of the first circuit

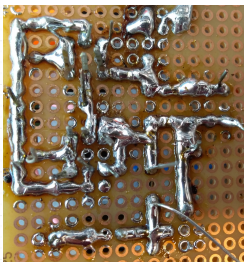
The soldering plan was made to plan what component is placed where. This plan was made to reduce the amount of soldering traces in the power stage. This was also an easy way to later define the inductance as an amount of soldering traces. A soldering trace is two holes connected by solder.

3.3 The second circuit

A second plan was set up to create a circuit where parasitics could be added easily everywhere and with an inductance which does not hinder the signal observation. The plan is shown in figure 3.2a.



(a) Plan for soldering the circuit



(b) Realization of the circuit

Figure 3.2: Plan and realization of the second circuit

The circuit was tested and a it was determined that the inductance was still small enough to see a practical waveform.

3.4 Conclusion

The circuits were almost built according to schematic (some ugly solder tracing). This means that the inductance of all the small connections should be predictable based on length. The second circuit in figure 3.2b will be used for the testing of the LC parasitics.

Chapter 4

Circuit testing

4.1 Introduction

In this chapter the circuit will be tested by hooking it up to the oscilloscope and checking the ringing. This ringing will be analyzed by measuring the frequency of the ringing and determine what parasitics influence this frequency. With this information a loop is identified through which the circuit oscillates.

4.2 Equipment

In order for this experiment to be reproducible, the used equipment is listed below:

- Oscilloscope - Rhode & Schwartz RTB2002 (2.5GSa/s)
- Probe - Rhode & Schwartz RT-ZP03 (C = 12pF R = 10MOhm at 10:1 setting)(15cm Ground wire)
- Power supply - Delta elektronika E030-1
- Function generator - Agilent 33220A (20MHz)

Note: It is important to use a decent function generator to create barely oscillating square waves, since the function generator drives dead time driver it is not required to have the best function generator. The main specifications to look at are the rise time which is only 13ns for the agilent 33220a with an overshoot of 2%. A function generator with a lot worse would do the job aswell. The oscilloscope also performs very well and can be downgraded. The probe should not be downgraded, it was tested with slightly higher input capacitance (80pF+) which will ruin the measurement, also increasing the ground wire length will reduce measurement accuracy severely. The setup was also tested with a keysight active probe of 3pF input capacitance with 1cm ground wire, the result did not differ from the measurement with the longer probe. Any power supply will do fine if it can output a steady 10V and deliver 1A.

4.3 Proving the hypothesis

In chapter 2 a hypothesis was formed that the circuit oscillates through the power and decoupling stage with a small path through the driver stage, this is illustrated in figure 4.1.

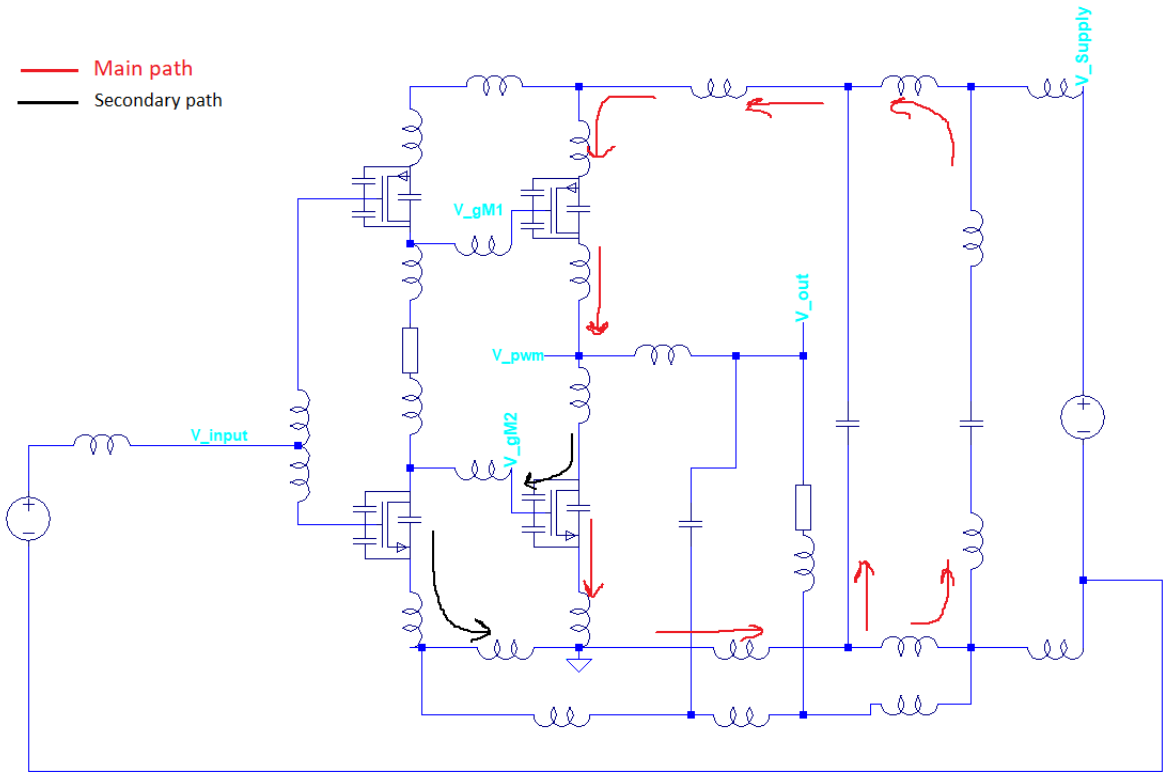
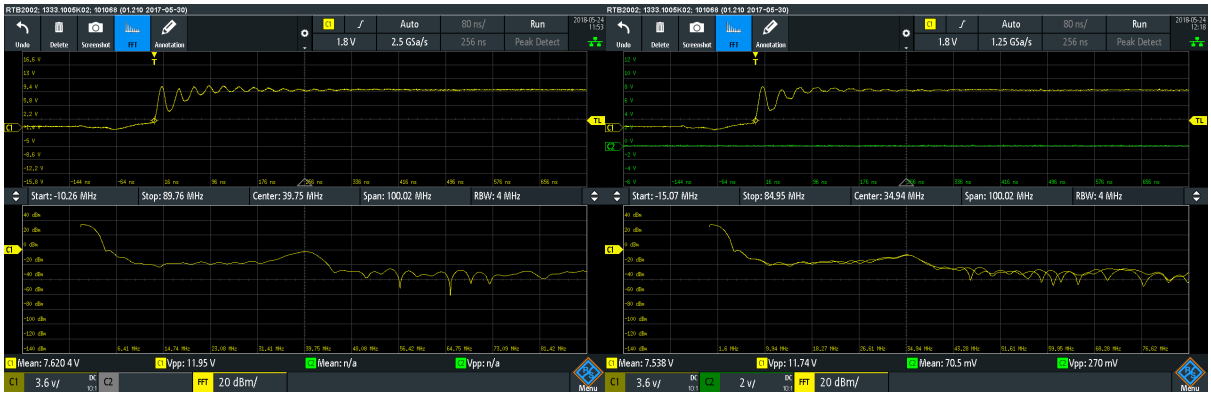


Figure 4.1: a circuit showing the two biggest oscillation paths

In order to prove that this is indeed the oscillation path the parasitic values will be changed to evaluate the effect the change has on the frequency. If a significant change is applied to a parasitic and the frequency changes it means that the loop goes through that parasitic element. The same can be said when a change does not result in an oscillation change, then the parasitic is not part of the loop.

4.4 The parasitic capacitance

The loop goes through two capacitors in the loop: the decoupling capacitor and the power-NMOS (FQP33N10) parasitic capacitor. Since these two stages are in series with each other it follows that the decoupling capacitor is insignificant in determining the frequency as it is orders of magnitude higher in capacitance. The parasitic capacitance of the mosfet is not simply one capacitor; It consists of three capacitors, at Vds = 10 the values are: Cgd = 300pF, Cds = 450pF and Cgs = 1nF. When the path runs from drain to source it can be seen as 450pF in parallel with 300pF and 1nF series resulting in a capacitance of around 680pF. When the path runs from drain to gate the capacitance is around 610pF. These values are read of the datasheet [3] and can vary quite a bit in practice. To test the effect of the parasitic on the circuit a capacitor was added in parallel to the drain and source of the power-NMOS.



(a) normal circuit (b) 300pF added in parallel to Cds

Figure 4.2: A figure with two subfigures

From figure 4.2 it can be seen that adding a capacitance decreases the frequency. this test was repeated with multiple values:

Default values:	Cds	Cgs	Cgd	loopinductance (nH)		
	450	1000	300	22		
Cdsadded (pF)	Frequency (MHz)	EffectiveCds (pF)	Cmainloop (pF)	Expected frequency (MHz)	Frequency error (MHz)	percentual error
0	39,8	450	681	41,1	1,3	3%
100	37,0	550	781	38,4	1,4	4%
300	35,0	750	981	34,3	0,7	2%
680	29,0	1130	1360	29,1	0,1	0%
1000	26,6	1450	1680	26,2	0,4	1%
1400	25,0	1850	2080	23,5	1,5	6%

Figure 4.3: effects of adding a capacitor parallel of Cds

The expected frequency was calculated with equation 4.1 and the default loopinductance. This inductance was calculated using estimates of the dimension of the loop with an online calculator [4].

In Table 4.3 it can be seen that the frequency of the oscillation decreases as the added capacitance increases, with these numbers it was calculated what the frequency needs to be in order to prove that equation 4.1 holds.

$$f = \frac{1}{2 * \pi * \sqrt{L * C}} \tag{4.1}$$

Table 4.3 and equation 4.1 together show that the inductance of the loop should be between 20nH and 24nH. Since these values are too small to be measured with an RLC bridge another method is used to check whether this is accurate: the inner and outer diameter of the loop is measured and the theoretical inductance is calculated. A square loop with a 10mm width, 10 mm length and 2 mm diameter results in an theoretical inductance of 12,2 nH [4]. The rest of the inductance is due to the legs of the transistor and decoupling capacitors. This also explains why the theoretical inductance is dropping slightly when bigger capacitors are added: The capacitor essentially shorts the transistor which has longer legs and therefore more inductance. The values of the frequency are read off and the capacitors can vary slightly from their labeled values so it cannot be proven nor disproven that these dropping inductances are due to this phenomena. What can be said that these inductances are in the right order of magnitude therefore it can be said that the FQP33N capacitances are the only significant factor in determining the frequency because otherwise equation 4.1 would not have held.

4.5 The parasitic inductances

In order to measure whether a path is in the parasitic loop a very long wire (20cm) is soldered to the circuit and replaces that soldering trace. This wire can then be shorted at any distance to change the parasitic inductance from 0 to approximately 135 nH . Based on the observed effect it can be determined whether the the inductance causes the oscillation. This ”vary-inductor” needs to be placed at a few spots to prove the path:

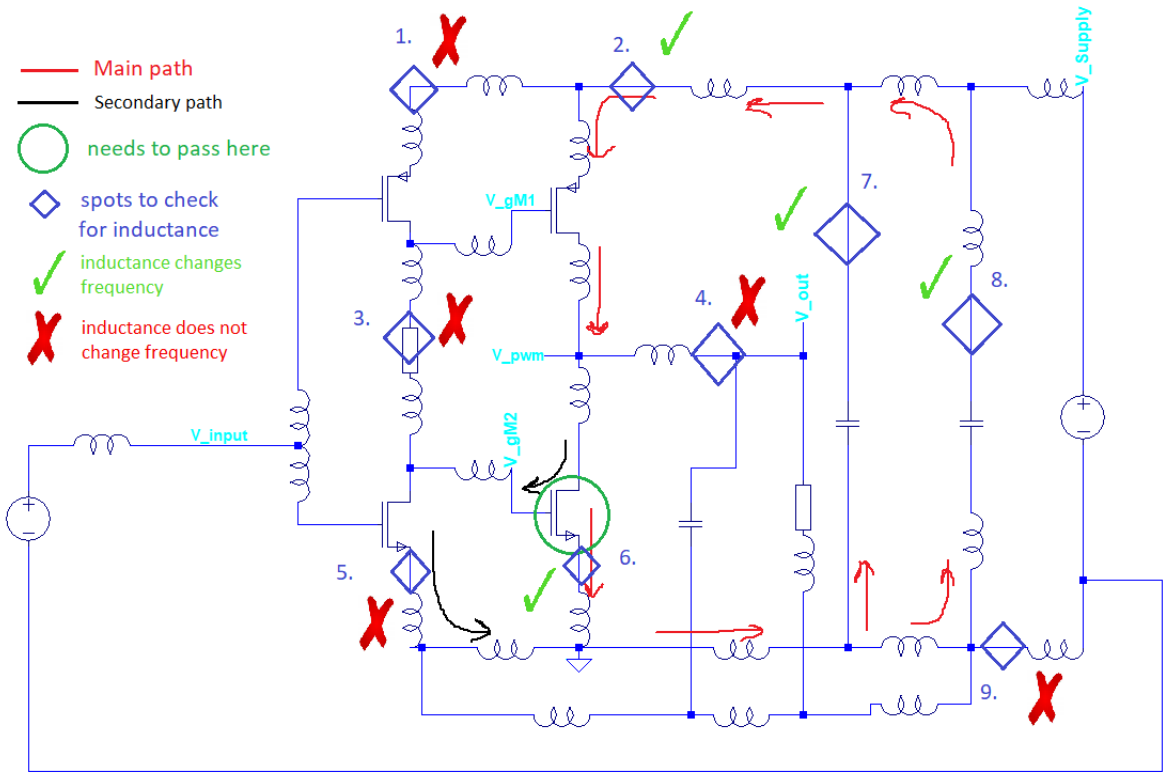


Figure 4.4: a circuit showing the two biggest oscillation paths with inductors

In figure 4.4 it can be seen that varying the inductance only has an effect on the frequency if the inductors are in the main path, during the measurements a few things were noticed: changing inductor 2 had the most significant effect, it caused a lot of overshoot while the others did not. The effect of inductor 6 is less noticable as the secondary path acts as a current divider when inductor 6 gets too large. When inductor 6 gets to large another frequency is present, presumably because the secondary path has a different parasitic capacitance (the inductor values are similar). Changing inductor 7 and 8 alters the frequency slightly, this is because they are in parallel. Inductor 7 and 8 were also tested together (increasing both at the same time), this had an effect like inductor 2. All other inductors did not have any effect at all.

Default values	wirethickness	loopheight	loop shape	Lcircuit (nH)	Effective Cds (pF)	
	0.6mm	5mm	rectangular	20	680	
Loop width(mm)	Ladded(nH)	Effective L (nH)	Frequency (MHz)	Expected frequency (MHz)	Frequency error (MHz)	Percentual error
0	0	20	40,4	43,2	2,8	7%
10	14	34	35,6	33,1	2,5	7%
20	25	45	28,9	28,8	0,1	0%
30	37	57	25,2	25,6	0,4	2%
40	48	68	22,5	23,4	0,9	4%

Figure 4.5: effects of adding a wire with known dimentions in series with the circuit

Because

In table 4.5 it is shown that when the inductance of inductor spot 2 is increasing the frequency decreases accordingly with equation 4.1.

There is a slight variation in the expected and observed frequency, this difference can be explained by the inaccuracy of the measurement as the values are read off the oscilloscope and datasheet and the inductance can easily vary by a few nH by bending slightly or soldering inaccurately. Because the error is still quite small it is determined that the oscillation is still in accordance with equation 4.1

4.6 Conclusion

The oscillation occurs due to the inductance in the power and decoupling stage and the capacitance of the FQP33N10. The frequency can be determined using equation 4.1 with an error less than 7%.

Chapter 5

Matching simulation with circuit

5.1 Introduction

For the purpose of designing class D amplifiers it is very useful to have a simulation which represents the workings in real life. This difference between simulation and realization most likely lies in the difference of parasitic values. In this chapter the LTspice simulation will be matched to the realized circuit. The matching will be successful when the frequency, damping and overshoot are similar and switching behavior stays normal. The LTspice simulation will be matched to the figure below:

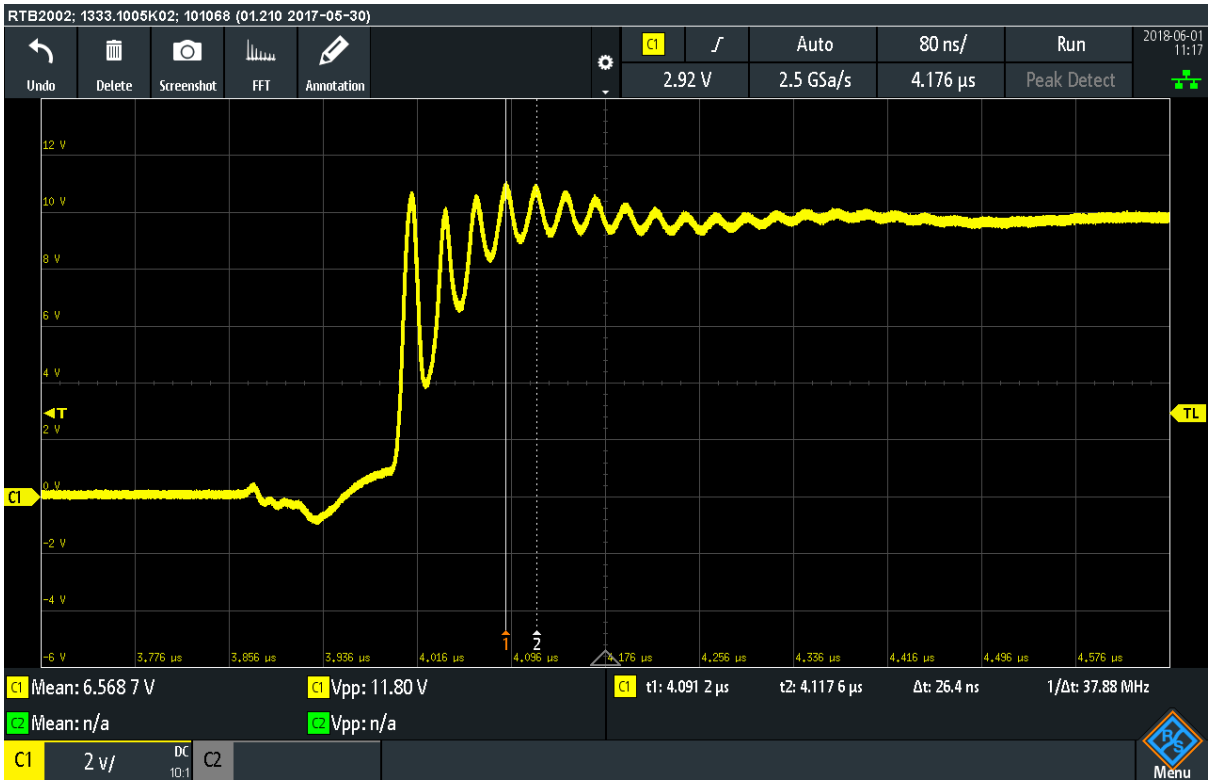


Figure 5.1: oscilloscope screenshot of measured ringing in normal circuit

5.2 The Frequency

The variation between the simulation and real life observations were very big in terms of frequency. For the same inductance loop the frequency was 70MHZ in simulation while it was 40MHz on the observed circuit. This difference is due to the capacitance between the drain and source of the FQP33N10. In order to prove that the observed capacitance between the drain and source is not equal to the model value in simulation a test setup was made:

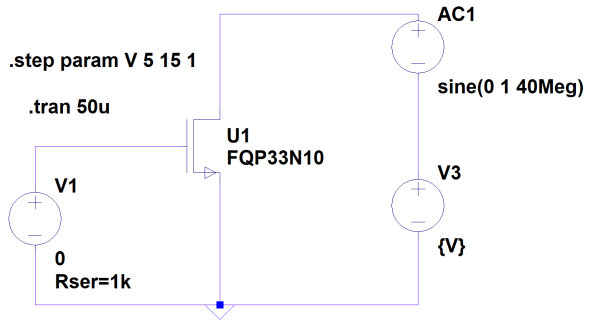


Figure 5.2: oscilloscope screenshot of measured ringing in normal circuit

Table 5.1: effective capacitance calculations

	freq (MHz)	40		
dc voltage	ac voltage	ac current (mA)	impedance (ohm)	capcitance (pF)
5	1	92	10,9	366
8	1	70	14,3	279
9	1	64	15,7	255
10	1	60	16,7	239
11	1	56	17,9	223
12	1	53	18,9	211
15	1	47	21,3	187

From the results in table 5.1 it can be concluded that the capacitance scales with Vds as it should, but it does not result in the value which was expected (680pF for Vds = 10V)

This test does not confirm however that the capacitance value is off because there is also a series resistance and inductance in the drain source connection, this does prove that the capacitance scales with Vds. To prove that the impedance measurement is fully determined by the capacitance an RC filter is built and the 45 degree point is found to find the capacitance:

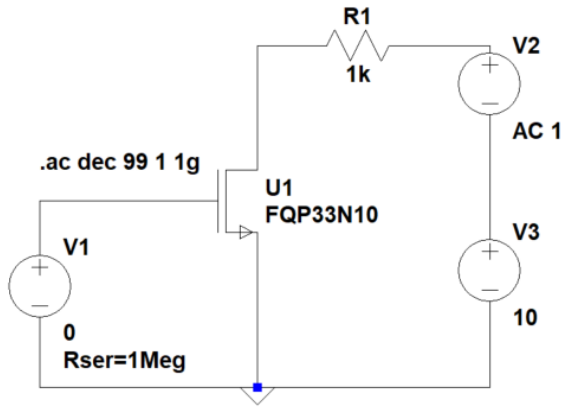


Figure 5.3: Test setup to measure the drain-source capacitance

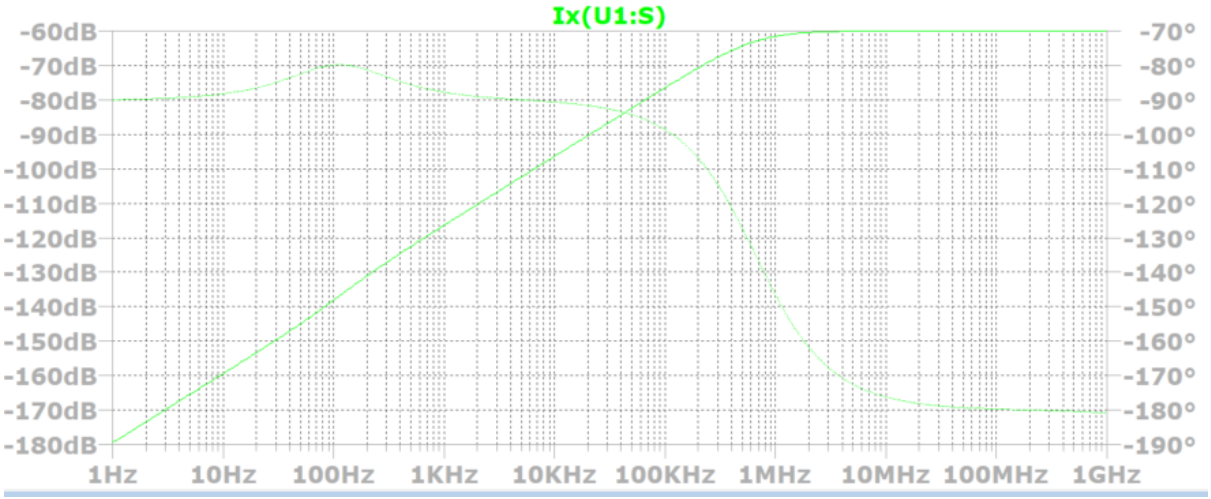


Figure 5.4: frequency sweep results to calculate the drain-source capacitance

A resistor of 1k in series was chosen to make sure that all the series resistance and inductance is irrelevant. The gate source resistor of 1Meg was added to make sure that the gate was not shorted to the source and all current flows from drain to source and nothing through the gate (shorting the gate and source results in the gate source capacitance being left out). At 660kHz the phase is at 45 degrees meaning the frequency at which equation 5.1 holds.

$$fc = \frac{1}{2\pi RC} \tag{5.1}$$

With the known resistance of 1k and known frequency of 660kHz the capacitance was calculated to be 241pF. To confirm the suspicion that the difference in simulation and reality is only due to this difference it is calculated whether the simulated frequency is in accordance with 4.1. The simulated 70MHz with a loop inductance of 22nH (the 22nH was read off LTspice model) results in a capacitance of 235pF, indicating that the problem solely lies with the mis-characterization of the simulation model.

5.3 Damping ratio

Since it is proven that the frequency can be determined accurately using equation 4.1 it is assumed that the circuit acts like a regular RLC circuit and therefore the other equations of an RLC circuit hold:

$$\alpha = \frac{R}{2L} \tag{5.2}$$

$$\zeta = \frac{\alpha}{\omega_0} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{5.3}$$

$$Q = 2\pi \frac{energy\ stored}{energy\ dissapated\ per\ cycle} = \frac{1}{2\zeta} \tag{5.4}$$

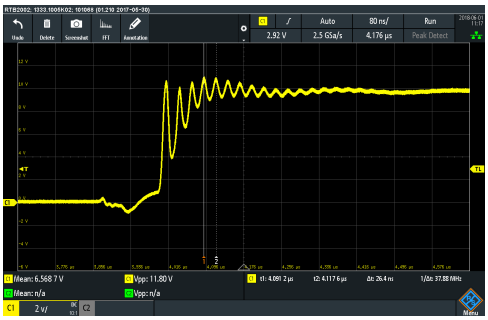
By combining these equations with the oscilloscope observations the loop resistance should be able to be found. Unfortunately the ringing is not the only component of the signal. This signal component does not instantly move from 0 to 10V, instead is slowly works its way up. in order to find the attenuation rate this signal should not be taken into account. In order to find the attenuation of the signal the voltage differences between each half oscillation are looked at. Using this method the signal will reduce to 72% of its previous signal each period. With this information it is determined that the damping ratio is equal to 0.04 and therefore the equivalent resistance is equal to 440 milliohm. In the simulation some resistance is already present in the transistor models so the rest of the resistance should probably be put in the decoupling capacitors as it is modeled as ideal and contains thin wires (the thick solder should have very little resistance).

5.4 Overshoot

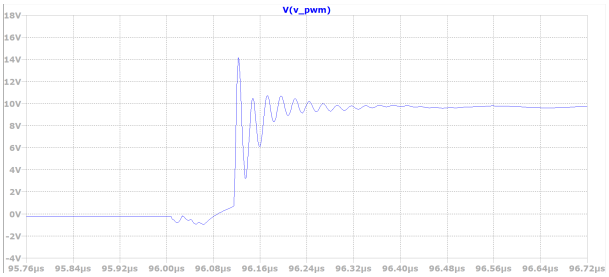
Since the initial voltage difference which causes the oscillation will not change the magnitude of the overshoot will always be connected to the damping ratio. So only the frequency and damping ratio need to be matched in order to have the overshoot match as well.

5.5 Matching

In order to match the LTspice model a capacitor of 440pF is added in the .LIB file of the FQP33N10 in parralel with the the existing diode (this solution works only for this voltage and it is recommended to fix this for all the DS voltages). Using equation 5.4 it was calculated that A loop resistance of 300m needed to be added to emulate its theoretical behavior based on the observation of figure 5.1. In the real circuit this 300m is spread over the solder traces, wires and the decoupling capacitors. The soldering traces were measured with an agilent 34401A. This was done by measuring a line of 20 soldering traces. The resulting Resistance is was 40 mOhm or 2 mOhm per trace. The shortest path contains 12 so thats 24mOhm. The 680uF decoupling cap has an ESR of 42 mOhm according to its datasheet. So the rest of the resistance has to be present in the FQP17P06 drain source connection when opened or between the FQP33N10 drain source parasitic capacitance if the capacitance and inductance are correct.



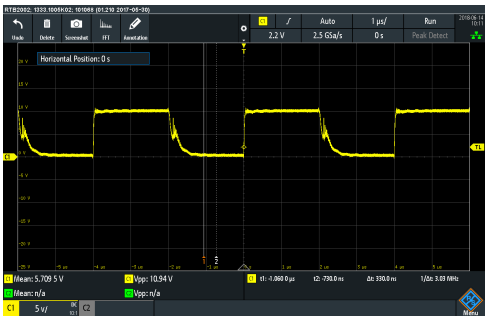
(a) oscilloscope observation



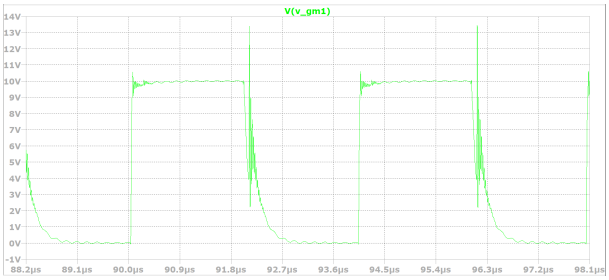
(b) LTspice observation

Figure 5.5: Oscillation difference when the loop components are matched

From the figure it was determined that the resistance needed to be slightly smaller to have the same damping ratio, so the added resistance was changed from 300m to 200m. the overshoot is still different however. Because the power stage should be matched a closer look was given to the driver stage. All nodes were measured and compared to its ltspice waveforms. One node stood out from the rest, the FQP17P06 gate node had a lot larger voltage swing when the FQP17P06 just reaches its threshold in simulation compared to the observed result.



(a) measurement of the FQP17P06 gate node



(b) simulation of the FQP17P06 gate node

Figure 5.6: Oscillation difference when the loop components are matched

Because this swing has a lot to do with the oscillation nodes overshoot this part was investigated. The swing is mainly caused by two components, the dead-time driver and the gate drain capacitor. The gate drain capacitors voltage changes very fast when the FQP17P06 reaches its threshold. the capacitor releases a current due to this effect through the dead-time resistor to ground. this current induces a voltage over the dead-time resistor which is visible in figure 5.6.

because the dead-time resistor is significant and it is easily measurable that its value is similar in simulation and measurement, this has to be caused by the parasitic capacitor. In figure 5.7 it can be seen what the change of this capacitor does to the slew rate. Which was the last thing that needed to be matched.

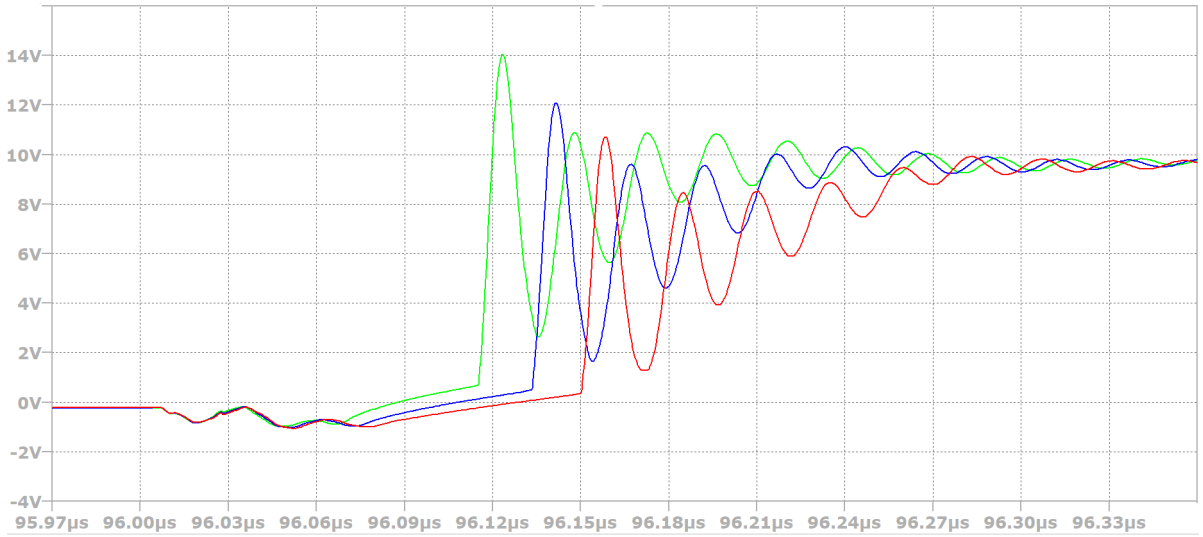
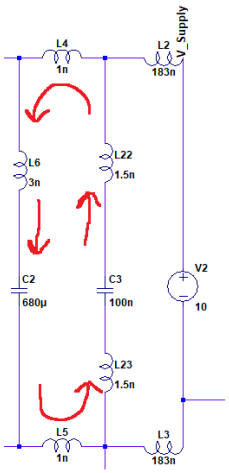


Figure 5.7: change in slew rate visualized when a capacitor is added between the gate and drain of the FQP17P06. green = 0pF added, Blue = 200pF added, red = 400pF added.

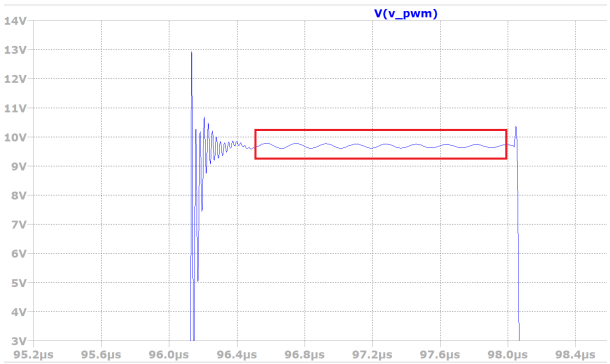
During the switching the drain source voltage is rapidly dropping and therefore the capacitance is also dropping so a quantitative analysis cannot be made of this oscillation. But a capacitance can be added to Cgd to decrease the slew rate to match the simulation with the measurements.

5.6 The small oscillation

The class D amplifier circuit also has a secondary oscillation. A 5MHz signal with a 0.2Vpp amplitude can be seen when the primary oscillation of 40MHz is damped. The components which cause this oscillation is the 100nF decoupling capacitor and all the inductance through the capacitor and back through the other big decoupling capacitor. The oscillation cause was verified by changing inductor and capacitor values and calculating the expected frequency and comparing that with the actual frequency. Equation 4.1 holds and the derived inductance is in accordance with the inductance calculator [4]. Because the frequency and amplitude of this oscillation is relatively small to the primary oscillation it was deemed unimportant to put a lot of effort into. This oscillation is very similar in simulation and measurement.



(a) oscillation path of the small oscillation



(b) visualization of the oscillation in question

Chapter 6

Conclusion&Discussion

6.1 Conclusion

The aim of this report was to answer the research question: *What parasitic inductances and capacitances cause the ringing observed at the output of the power stage of a class D amplifier?* From experimentation it was found that the parasitic capacitance consisted of only the parasitics of the FQP33N (power NMOS) transistor which value is equal to Cds + (Cgs//Cgd). The parasitic inductance was the loop through the power stage and the decoupling capacitors. It is possible to have another loop through the BS170 when the inductance of the FQP33N source is too big. The Frequency of the ringing can be characterized by equation 4.1.

6.2 Discussion

In this report the aim was to identify what parasitics cause the observed ringing in order to be able to remove the ringing all together. The overall approach was to change parasitic values in simulation and in realization in order to gain an understanding as to what influences the ringing and what does not, by looking for what and L's and C's change the frequency and therefore create the ringing it was found that the ringing is created by a loop of parasitic components. This observation fits perfectly with the existing literature as the frequency can be accurately predicted with equation 4.1. There is however a limitation to this study. The inductance values are calculated and not measured, as it is not possible to accurately measure small inductors and when soldered on the slightest bent can cause a deviation of a few nH. The capacitors that were added tightened the inductance loop as the were soldered inside the loop and had smaller legs. The frequencies were read of an FFT analysis of the oscilloscope and could be off by a maximum of 1MHz. Even though these things create some uncertainty the general predictable trend is good enough. In the future the research can be expanded by defining more properties of the ringing such as overshoot and damping. Or by defining the ringing when the power signal drops from 10V to 0V. To minimize the ringing the parasitics in question should be kept as small as possible.

References

[1] R. Haddad, “Electromagnetic interference analysis in class d amplifiers,” Master’s thesis, University of Twente, jun 2017.

[2] Bill McCulley, $http://low-powerdesign.com/article_mcculley_112409.htm$.

[3] Fairchild semiconductor, http://pdf1.alldatasheet.com/datasheet-pdf/view/52371/FAIRCHILD/FQP33N10.html, *FQP33N10 Datasheet*.

[4] EEweb, https://www.eeweb.com/tools/rectangle-loop-inductance, *RECTANGLE LOOP INDUCTANCE CALCULATOR*.