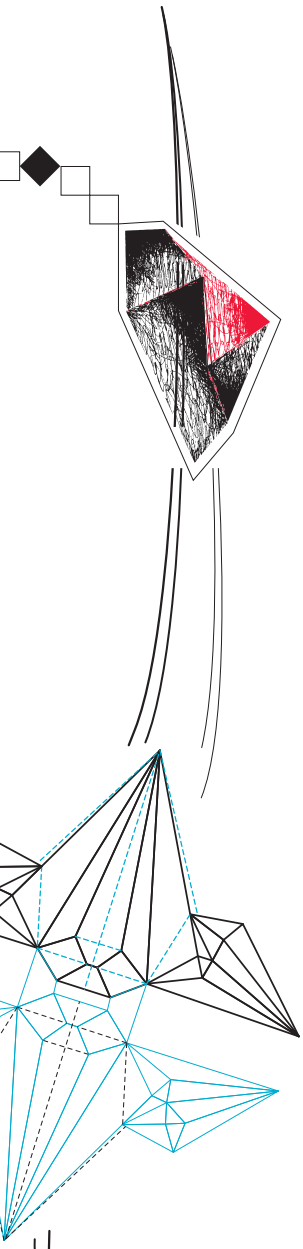

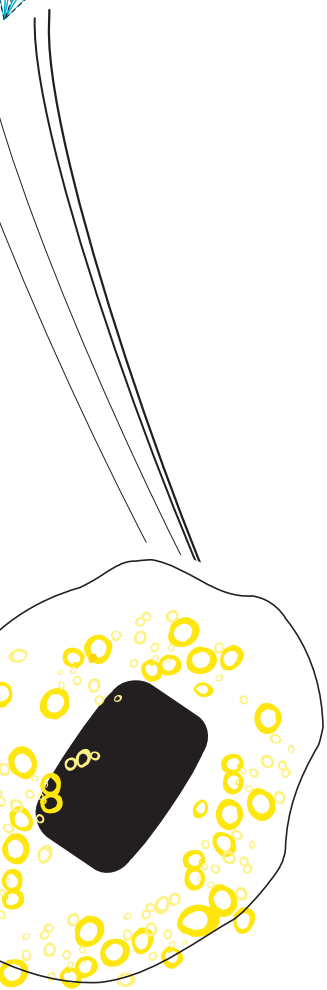

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Analysis of Phase Locked Loops with Enhanced Loop Bandwidth

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Master Thesis
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Abstract

The Phase-Locked Loop is an important building block in wireless transceivers, where it is used to synthesize wireless carriers and clocks. Strict phase noise requirements on the Phase-Locked Loop requires either a high-frequency reference or a high-quality Voltage-Controlled Oscillator.

This work presents a new Phase-Locked Loop architecture that makes it possible to have a larger loop-bandwidth with respect to the reference frequency than conventional Phase-Locked Loops. As a result, noisy ring-oscillators and low-frequency reference crystals can be used while still achieving good phase noise performance. An LPTV model and an event-based simulation environment are built to analyze the system's behavior and key performance aspects.

As a proof-of-concept, a system-level design of a fractional-N Phase-Locked Loop is presented which meets the Bluetooth Low-Energy requirements while using a cheap, low-power ring-oscillator. The loop has a bandwidth of 10 MHz, while a 20 MHz crystal reference is used. The Phase-Locked Loop exhibits an in-band phase noise of -104 dBc/Hz and has reference spurs less than -100 dBc.

Contents

Chapter 1

Introduction

The Phase-Locked Loop (PLL) is a key component in integrated systems. It is mainly used to synthesize radio frequency carriers that are used for wireless communications and to generate clocks. Since the wireless spectrum becomes more and more crowded, requirements on the spectral purity of these carriers increase. Besides this, there is an increasing interest in integrated solutions and Internet of Things, such that the demand for stable, cheap and low-power PLLs is higher than ever.

1.1 Basic Operation

A basic system overview of a PLL is given in Figure 1.1. The reference signal $s_{ref}(t)$ is a signal with known frequency f_{ref}. The output signal $s_{out}(t)$ is generated by a Voltage Controlled Oscillator (VCO). Using feedback, the VCO is tuned such that the phase of the output signal is synchronized with the input.

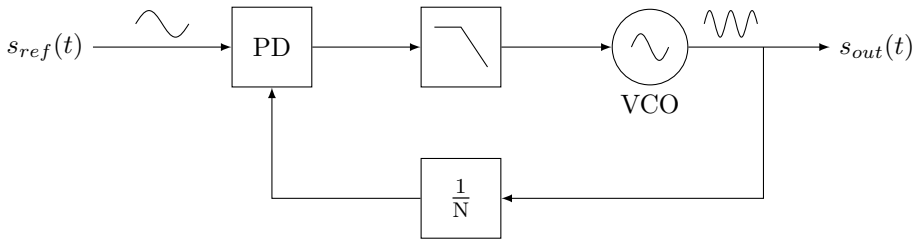

Figure 1.1: Basic PLL system overview

A frequency-divider divides the frequency of the output signal with factor N. This way, the output frequency can be configured by changing the divider value. PLLs with either an integer-N or fractional-N value exist. For integer-N PLLs, the divider ratio N is an integer number. Fractional-N PLLs also allow fractional divider ratios. This enables more flexibility in output frequency at the cost of increased system complexity.

The phase detector (PD) tracks the phase error between the frequency divided output signal and the reference signal. The loop-filter filters the phase difference measured by the phase detector and sets the loop bandwidth. Different type of loop-filter exist. A type-I PLL has only one integrator in the system, which is the VCO. This type of PLLs have a steady-state phase error between input and output. In a type-II PLL, another integrator is added to the loop-filter, which increases filtering and diminishes the steady-state phase error. Also higher order PLL loops exist.

The VCO is tuned according to the filtered phase error. This way an output signal can be generated with minimum phase noise and a frequency that is stable over temperature and other variations, provided that the reference signal has these properties.

1.2 Problem Definition

If we imagine an ideal PLL, it has three properties. Firstly, it has an infinite loop bandwidth. This allows the loop to cancel all the phase noise generated by the oscillator. Most PLLs use bulky LC-oscillators to achieve good phase noise performance. Ring-oscillators form a low-cost alternative to LC-oscillators, with the drawback of higher phase noise for the same power consumption [1]. Therefore it is important that the PLL can effectively suppress VCO phase noise over a large bandwidth, which enables the use of cheap oscillators.

The second property is its reference frequency. Many PLLs have a reference frequency in the order of 25 MHz. Decreasing the reference frequency decreases the power consumption and cost of the reference circuitry. Ideally, a 32.768 kHz real-time clock (RTC) crystal oscillator is used as a reference. Such a crystal is already available on most IoT systems as a time reference [2].

The last property of an ideal PLL is that the loop does not contribute to the phase noise of the output. When all these properties are achieved, the only phase noise contribution at the output is the noise that is already present in the reference clock.

The first and second property can however not be satisfied simultaneously. The bandwidth of a Type-II PLL is limited to one tenth of the reference frequency, which is commonly called Gardner's limit [3]. Therefore it is not possible to choose the loop bandwidth and reference frequency fully independently.

With the downsizing of CMOS technology, it becomes more attractive to solve analog problems in the digital domain. Besides technology improvements, the digital domain makes it easier to implement complex signal operations such as multiplications and wave generation. Therefore this project focuses on new PLL structures to increase the loop bandwidth using digital techniques. These structures are modeled and analyzed. The ultimate goal of this project is to create a PLL that has a loop bandwidth nearing or exceeding the reference frequency.

1.3 Outline

The remainder of this thesis is built up as follows. In the next chapter, an overview of current state-of-the-art PLLs is given and a solution to the stated problem is proposed. In Chapter 3, two different models are created to describe the PLLs behavior. Chapter 4 gives an analysis of the proposed PLL and discusses the key performance aspects.

In Chapter 5, a PLL is designed for a Bluetooth Low-Energy transceiver using the techniques described in this thesis. On the basis of this design, conclusions and recommendation with respect to high-bandwidth PLLs are made.

Chapter 2

System Proposal

In this chapter, first a review is given of current state-of-the-art PLLs and an analysis is done on their bandwidth limitations. After analysis of current technology, an idea is developed that does not have these bandwidth limitations. In the next sections, this idea is worked out and a system is proposed.

2.1 Current State-of-the-Art

State-of-the-art PLLs sample the oscillators phase error once every reference period. A system overview of a common PLL design can be found in Figure 2.1. The reference clock commonly is an analog waveform, generated by a crystal oscillator. A high-gain buffer digitizes this reference signal to create a digital clock. This clock triggers the phase detector to get an estimate of the output phase with respect to the reference, once every reference period. The phase-detector commonly is a lead-lag detector with charge-pump [3], or a sample-and-hold circuit for a Sub-Sampling PLL [4], or a Time-to-Digital converter for an All-Digital PLL [5].

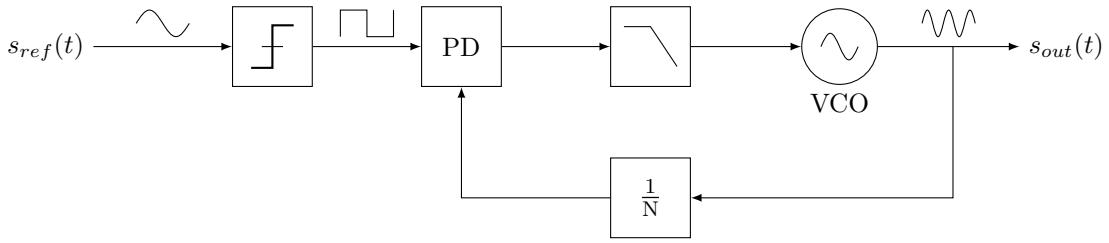

Figure 2.1: Common PLL with clocked phase detector

The disadvantage of these PLLs is that the bandwidth is limited to approximately one tenth of the reference frequency due to stability limitations. There have been recent attempts to push the loop bandwidth further. In [6], three clock buffers at different threshold levels have been added to create a total of six clock pulses per period from the analog reference clock. By alternating six clock divider settings, similar edges can be created from the output clock. This technique makes the effective reference frequency six times higher. The disadvantage is that calibration is required because the clock edges are not equidistant.

Another method is described in [7], where a type-I PLL loop is used. A type-I sampling PLL has a theoretical bandwidth limit of half the reference. A disadvantage of a type-I PLL with large loop bandwidth are large reference spurs because of inadequate filtering. Therefore the proposed PLL adds analog notch filters to suppress the reference spurs. The PLL is an Integer-N type, since the loop filter is not good enough to filter the noise from a delta-sigma fractional divider.

An improved fractional-N version of this PLL is proposed in [8]. The maximum bandwidth is a quarter of the reference frequency. An analog finite impulse response (FIR) filter is used to suppress the sigma-delta divider noise. This FIR filter is embedded in the phase detector.

2.2 Idea Development

All the PLLs described above sample the phase error using the reference clock. In early Analog PLL's (APLL), the phase detector was implemented in a different way. Instead of sampling the phase error once every reference period, the time-continuous reference clock and output clock are multiplied using an analog multiplier. A schematic overview of such a system is shown in Figure 2.2.

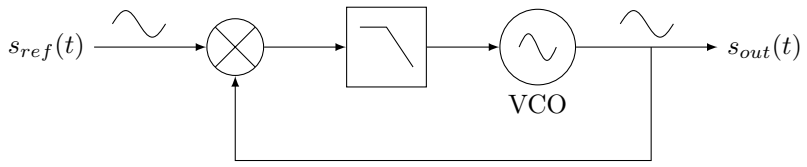

Figure 2.2: Analog PLL

The output of the multiplier is the down-converted phase error. An image at the double reference frequency is introduced here. When this image is filtered out using a low-pass filter, a time-continuous estimate of the phase error is left. Gardner's stability limit does not apply. The only bandwidth limiting factor is the low-pass filter required for filtering the image. Therefore the loop bandwidth can theoretically be extended up to the reference frequency.

This system has some drawbacks. Firstly, is difficult to implement good analog multipliers. Besides that, an analog frequency divider is required to get an output frequency that is different from the reference frequency. These problems are difficult to tackle in the analog domain, but can be solved in the digital domain. When this is done, the architecture of the APLL offers a possibility to achieve a high-bandwidth PLL.

2.3 Digital Phase-Locked Loop

Already before the adoption of the charge-pump PLL, research was done on digitizing PLL components. A survey on PLLs published in 1975 [9] lists different papers that propose a digital variant of the Analog PLL for demodulating Frequency Modulation (FM) signals. The FM signal is digitized using an Analog-to-Digital Converter (ADC). Using a digitally synthesized carrier and a digital multiplier, the FM signal is demodulated. No published circuit level implementation are found, presumably because of technology limitations.

With the downsizing of CMOS transistors, it becomes more attractive to implement functions digitally. Therefore we propose a PLL with a digital mixer. The architecture of this PLL is similar to the APLL. A system diagram is shown in Figure 2.3. The digital signals are approximated as continuous-time signals. The oscillators phase noise is shown as noise on the signals.

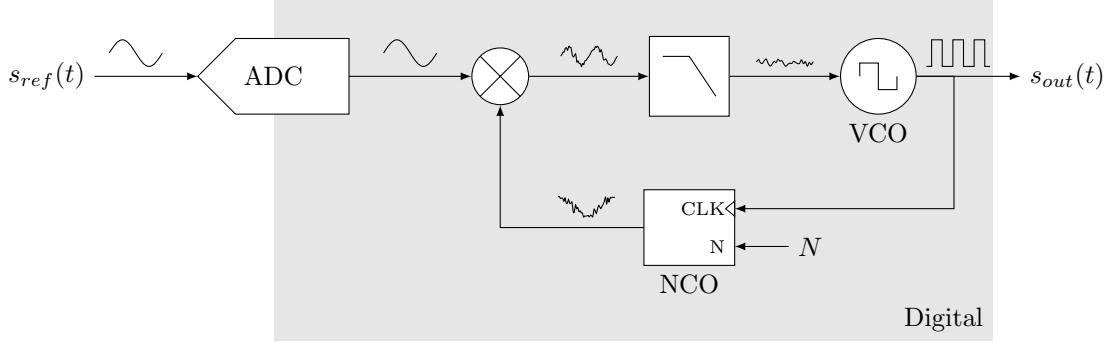

Figure 2.3: Digital PLL system diagram

The system is almost entirely digital, except for the ADC and the VCO. The VCO is digitally controllable such that the output of the loop-filter can be applied directly. The digital system is clocked on the VCO output clock.

The reference signal is digitized using an ADC. This signal is multiplied digitally with an sinusoid generated using a Numerically Controlled Oscillator (NCO). The NCO is a block that digitally synthesizes a sinusoid, where the number N determines the frequency of this signal. Since the NCO is clocked by the VCO, it also contains the phase information of the VCO. It is a digital equivalent of the frequency divider used in ordinary PLLs. An extra advantage over an analog frequency divider is that fractional spurs can be mitigated since an ideal NCO can generate arbitrary frequencies without spurs.

Another advantage of this structure is that the loop-filter is implemented digitally. This increases the flexibility of the PLL since digital loop-filters can be used. Therefore, the high-bandwidth of the Analog PLL and the flexibility of the All-Digital PLL are combined.

2.4 Digital Phase-Locked Loop with Crystal Embedded in Loop

The difference between the signal generated by the NCO and the reference signal is only minor. The largest part of these signals is the reference 'carrier'. A disadvantage of the system proposed in the previous section is that the dynamic range of the ADC must be very large to accurately detect the small phase errors.

This is illustrated in Figure 2.4. The spectrum describes the output of the NCO. The gray phase noise areas are very small compared to the large reference 'carrier', indicated with the arrow. When the frequency is locked, this large reference 'carrier' is identical to the reference signal. It is beneficial for the ADC requirements when only the phase error has to be digitized and the 'carrier' can be suppressed.

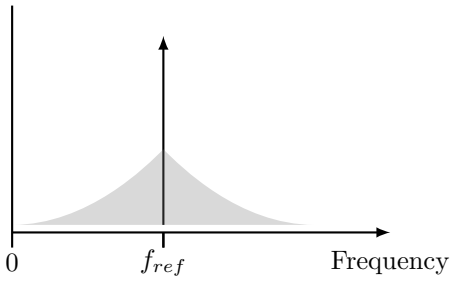

Figure 2.4: Schematic representation of the single-sided frequency spectrum of the NCO signal

This can be done by converting the NCO signal to the analog domain using a DAC. The NCO and DAC together form a Direct Digital Synthesizer (DDS). The reference signal can be subtracted in the analog domain, such that only the phase error information is left. A system that does so is presented in Figure 2.5. The reference signal is 'subtracted' from this signal using a crystal, which acts as a notch filter at its series resonance frequency. No structure like this is found in literature. The authors propose to call this system the Crystal Embedded Digital Phase-Locked Loop.

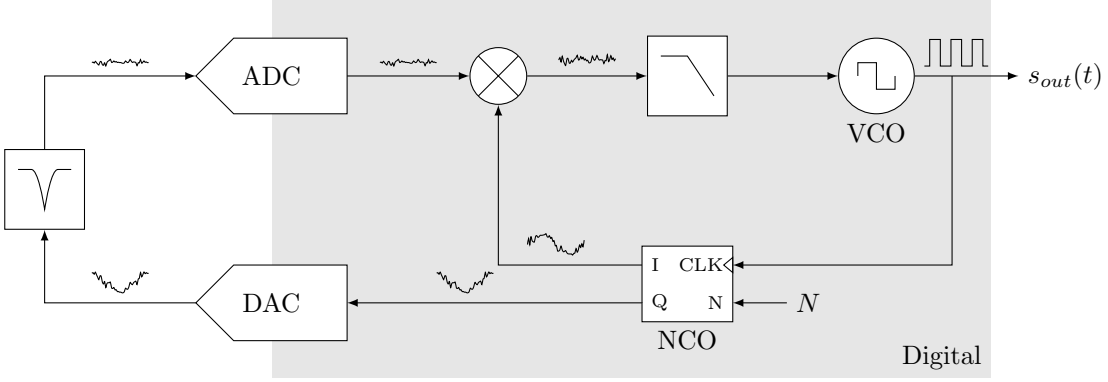

Figure 2.5: Crystal Embedded Digital Phase-Locked Loop

The small signal behavior of this system is similar to the system in Figure 2.3. No analog reference signal is used in this system. The frequency reference is the well-defined notch filter, which is implemented using a crystal resonator. An advantage of this structure is that the signal measured by the ADC is smaller, decreasing the Dynamic Range requirements of the ADC. The complexity is moved from the ADC to the DAC, which now has to convert the large reference 'carrier' to the analog domain. It is however easier to implement a good DAC since it offers more design flexibility.

2.5 Improved Bandwidth Mixer

The mixer used in the systems above introduces an image of the phase error around two times the reference frequency. This is illustrated in the middle row of Figure 2.6. This image limits the maximum bandwidth of the PLL to a maximum of the reference frequency. When the bandwidth is increased further, phase noise is added instead of removed due to the position of the image.

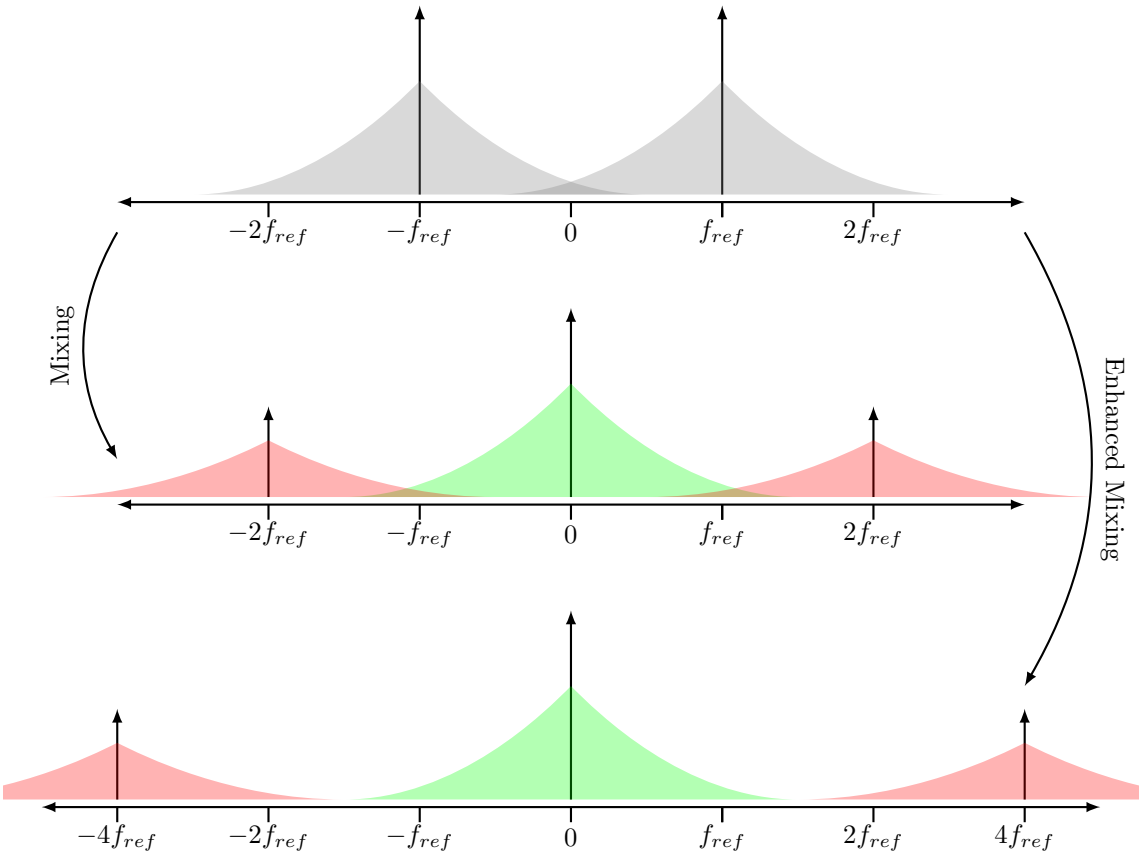

Figure 2.6: Frequency domain representation of mixer operation

When the output of the ADC is multiplied with a signal composed of multiple odd harmonics of the reference frequency, the maximum bandwidth of the PLL can be extended. This can be shown using the linearized DAC signal. more detailed signal descriptions will be derived in Chapter 3. In the case of the Crystal Embedded PLL, the linearized DAC signal is

$$s_{dac}(t) = \cos\left(\omega_{ref}t - \frac{1}{\mathrm{N}}\theta_{vco}(t)\right) \approx \cos\left(\omega_{ref}t\right) + \frac{1}{\mathrm{N}}\theta_{vco}(t) \cdot \sin\left(\omega_{ref}t\right). \tag{2.1}$$

It is assumed that the notch filter is perfect, such that the reference 'carrier' $\cos\left(\omega_{ref}t\right)$ is suppressed completely. The signal that is left and which is digitized by the ADC is

$$s_{adc}(t) = -\frac{1}{\mathrm{N}}\theta_{vco}(t) \cdot \sin\left(\omega_{ref}t\right). \tag{2.2}$$

When a sum of the fundamental and third harmonic of the reference frequency are used for mixing, the output of the mixer becomes

$$\begin{aligned} s_{mix}(t) &= s_{adc}(t) \cdot \left(\sin\left[\omega_{ref}t\right] + \sin\left[3\omega_{ref}t\right]\right) \\ &= -\frac{1}{2\mathrm{N}}\theta_{vco}(t)\left(1 - \cos\left[2\omega_{ref}t\right] + \cos\left[2\omega_{ref}t\right] - \cos\left[4\omega_{ref}t\right]\right) \\ &= -\frac{1}{2\mathrm{N}}\theta_{vco}(t)\left(1 - \cos\left[4\omega_{ref}t\right]\right). \end{aligned} \tag{2.3}$$

The mixer-image is now present at four times the reference frequency. This is shown in the bottom of 2.6. The theoretical maximum PLL bandwidth is now two times the reference frequency. By adding more odd harmonics to the mixer signal, the image can be shifted further. Adding up to the seventh harmonic shifts the image to $8f_{ref}$, and so forth. In order for this approximation to be true, the phase error must be small compared to a reference period such that the linearizion done in Equation 2.1 is accurate. The accuracy of this method is analyzed in Section 4.4.

2.6 Conclusions

In this chapter, a system is proposed that uses digital techniques to overcome bandwidth limitations present in state-of-the-art PLLs. Instead of sampling the output phase at the reference frequency, the reference signal is observed at a higher rate, ultimately the output frequency. This way, a much more broadband description of the phase error is available such that phase errors can be compensated over a large bandwidth. When special mixer signals are used, the bandwidth of the proposed PLL can be even larger than the reference frequency.

Chapter 3

System Modeling

The PLL that is proposed in the previous chapter uses an ADC and a digital mixer to detect the oscillator's phase error. These are time variant elements, as the ADC introduces aliases and the mixer translates signals in frequency. This makes regular Linear Time Invariant (LTI) system theory inadequate for analyzing the PLL.

Since the response of the PLL is periodic with the reference period and its behavior is approximately linear, it can be modeled as a Linear Periodically Time-Varying (LPTV) system. Basic LPTV analysis tools are described in Appendix A. These tools are used in Section 3.3 to create an LPTV model of the PLL. The model will primarily be used to give insight in the system. Besides this, it is used to estimate the systems response for a set of parameters without the need of extensive simulations.

Before the model is built, some assumptions and definitions are described in Section 3.1 and the systems large signal equations are derived in Section 3.2. Using the model, simplified algebraic expressions are derived in Section 3.4.

In addition to the LPTV model, an event-based simulation model is created. This model contains a more precise system description including non-linearities and uses stochastic processes to model noise. Transient effects can also be simulated using this model. The creation of this model is descried in Section 3.5. In Section 3.6, the LPTV model and event-based simulation model are compared and validity is discussed.

3.1 Definitions and Assumptions

In the process of building an LPTV model of the PLL, some assumptions are made. The first assumption is that aliasing effects can be neglected in this analysis since the ADC's sample frequency is much higher than the reference frequency. The frequencies of interest are around the reference frequency, such that the digital signals can be approximated as continuous-time signals.

Another assumption is that the phase errors in the system are small, such that the blocks can be linearized around their steady-state operating point.

Two 'perceptions' of time can be distinguished in the system. The first is the analog, continuous-time, view. In this view, the reference is a perfect sinusoid without any phase variations. The output of the VCO and the NCO have phase noise in this clock domain.

The other view is from the digital, discrete-time, controller. In this view, the output clock determines the discrete-time sampling points. A discrete-time system is not aware of the exact time positions of the samples. Therefore, the output clock is 'ideal' and has no phase variations. The ADC however samples the reference at time instances determined by this clock, such that the reference clock has phase variations.

The model is created with the first, analog point of view in mind. The digital systems are modeled as continuous-time signals, with phase variations set by the VCO. This choice is made because

the analysis methods are described for the continuous-time domain and because the point of view where the reference clock does not contain phase error seems more intuitive.

3.2 Large Signal Equations

In this section, a large signal description of the signals in the PLL are written down. A system diagram of the Crystal Embedded PLL, with annotated signal names can be found in Figure 3.1. The output of the VCO can be described as a sinusoid with angular frequency ω_{out} and phase variation $\theta_{vco}(t)$, given by

$$s_{out}(t) = \sin\left[\omega_{out}t + \theta_{vco}(t)\right] = \sin\left[\omega_{out}\left(t + \frac{\theta_{vco}(t)}{\omega_{out}}\right)\right]. \tag{3.1}$$

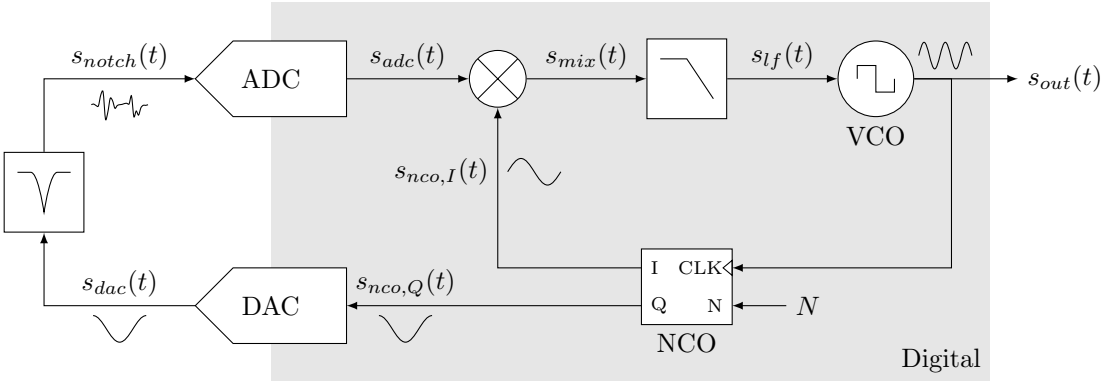

Figure 3.1: Crystal Embedded Digital Phase-Locked Loop

This signal is used as the time reference for the digital system, including the ADC, NCO and loop-filter. The NCO creates two quadrature phase sinusoids. The signal going to the mixer can be described as

$$s_{nco,I}(t) = \sin\left[\omega_{ref}\left(t + \frac{\theta_{vco}(t)}{\omega_{out}}\right)\right] = \sin\left[\omega_{ref}t + \frac{1}{\mathrm{N}}\theta_{vco}(t)\right], \tag{3.2}$$

where

$$N = \frac{\omega_{out}}{\omega_{ref}}. \tag{3.3}$$

This signal is used for down-converting the phase error information. The signal that is generated for the DAC is shifted by 90 degrees, and can be described as

$$s_{nco,Q}(t) = s_{dac}(t) = \cos\left[\omega_{ref}t + \frac{1}{\mathrm{N}}\theta_{vco}(t)\right]. \tag{3.4}$$

The notch filter removes the reference carrier from the signal generated by the DAC. It is assumed that the notch filter has an infinite quality factor, such that the complete carrier is suppressed. The carrier can be determined by setting $\theta_{vco}(t)$ to zero. By subtracting this carrier $\cos(\omega_{ref}t)$, an estimate of the signal after the filter can be estimated. This signal becomes, after a trigonometric simplification step,

$$\begin{aligned} s_{notch}(t) &\approx s_{dac}(t) - \cos\left[\omega_{ref}t\right] \\ &= -2\sin\left[\frac{1}{2\mathrm{N}}\theta_{vco}(t)\right] \cdot \sin\left[\omega_{ref}t + \frac{1}{2\mathrm{N}}\theta_{vco}(t)\right]. \end{aligned} \tag{3.5}$$

The ADC samples the filtered signal. Quantization errors and aliasing are neglected. Therefore

$$s_{adc}(t) = s_{notch}(t). \tag{3.6}$$

The mixer multiplies this signal with the signal generated in the NCO. The output of the mixer becomes

$$\begin{aligned} s_{mix}(t) &= s_{adc}(t) \cdot s_{nco}(t) \\ &= -2\sin\left[\frac{1}{2\mathrm{N}}\theta_{vco}(t)\right] \cdot \sin\left[\omega_{ref}t + \frac{1}{2\mathrm{N}}\theta_{vco}(t)\right] \cdot \sin\left[\omega_{ref}t + \frac{1}{\mathrm{N}}\theta_{vco}(t)\right] \\ &= -\sin\left[\frac{1}{2\mathrm{N}}\theta_{vco}(t)\right]\left(\cos\left[\frac{1}{2\mathrm{N}}\theta_{vco}(t)\right] + \sin\left[2\omega_{ref}t + \frac{3}{2\mathrm{N}}\theta_{vco}(t)\right]\right). \end{aligned} \tag{3.7}$$

The phase error component is multiplied with two terms, the first is approximately one and represents the phase error at baseband and the second the image around $2\omega_{ref}$. When the image at $2\omega_{ref}$ is filtered by the loop-filter, the output of the filter becomes approximately

$$s_{lf}(t) = \mathrm{LPF}\Big\{s_{mix}(t)\Big\} = -\sin\left[\frac{1}{2\mathrm{N}}\theta_{vco}(t)\right]\cos\left[\frac{1}{2\mathrm{N}}\theta_{vco}(t)\right] \approx -\frac{1}{2\mathrm{N}}\theta_{vco}(t). \tag{3.8}$$

This signal, representing the phase error, is fed in the oscillator to close the loop. In the next section, the input-output relation of the different blocks in the system are linearized and an LPTV model is created.

3.3 LPTV Model

The LPTV model is built in two steps. First the Harmonic Transfer Matrices (HTM) of the sub-blocks are derived. Afterwards the closed loop HTMs are obtained.

VCO

The output of the VCO is

$$s_{vco}(t) = \sin\left[\omega_{vco}t + \theta_{vco}(t)\right]. \tag{3.9}$$

The phase of the output of the VCO $\theta_{vco}(t)$ is influenced by two sources. The first source is the input tuning voltage. The phase relation with respect to the input can be described as

$$\theta_{tuning}(t) = 2\pi\mathrm{K_{VCO}}\int_{-\infty}^{t} s_{tuning}(t)dt. \tag{3.10}$$

$\mathrm{K_{VCO}}$ is the tuning sensitivity in [Hz/V]. Besides tuning, random phase variations also influence the output of the VCO. These are modeled as an addition input $\theta_{n,vco}$.

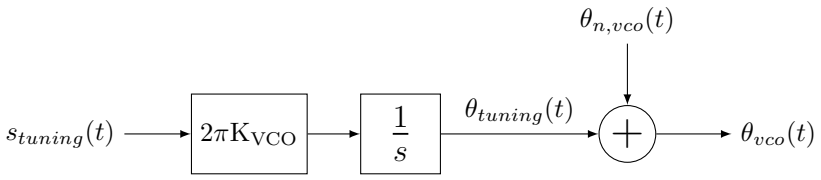

Figure 3.2: Small signal block diagram of the VCO

The common performance measure for oscillators and PLLs is the phase variation instead of the output voltage variation. Therefore the small signal phase variations are used as the output of the VCO. A schematic block diagram of the VCO can be found in Figure 3.2.

The VCO is time-invariant at the frequencies of interest, which is the reference frequency. There can however be high frequency time variant behavior. The output of the VCO is for example dependent on the time at which the input changes with respect to one output period. It is assumed that the VCO input is changed always at the same time with respect to an output period (e.g. during the zero crossings), such that this effect can be neglected.

Since the VCO is assumed to be time-invariant, it can be described as an LTI system. The transfer-function is found by transforming Equation 3.10 into the Laplace domain, which gives

$$\mathrm{H_{VCO}}(s) = \frac{\Theta_{vco}(s)}{S_{tuning}(s)} = \frac{2\pi \mathrm{K_{VCO}}}{s}. \tag{3.11}$$

Since this is an LTI transfer function, the HTM becomes a diagonal matrix. Its elements can be found using

$$\widetilde{\mathbf{H}}(s) = \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & H(s-j\omega_0) & 0 & 0 & \cdots \\ \cdots & 0 & H(s) & 0 & \cdots \\ \cdots & 0 & 0 & H(s+j\omega_0) & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{3.12}$$

NCO

The NCO synthesizes a sinusoid with a frequency corresponding to the reference frequency. Since the VCO is clocking the NCO, the phase error of the VCO is also present in this wave. An input-output relation for the NCO can be found in Equation 3.4. Linearizing this expression using a first order Taylor approximation gives

$$\begin{aligned} s_{nco,Q}(t) &= \cos\left[\omega_{ref} t + \frac{1}{\mathrm{N}}\theta_{vco}(t)\right] \\ &\approx \cos\left(\omega_{ref} t\right) - \frac{1}{\mathrm{N}}\theta_{vco}(t)\sin\left(\omega_{ref} t\right). \end{aligned} \tag{3.13}$$

The first term is the time periodic operating point. The second term is the linearized small signal variation. A block diagram representing the small signal flow can be found in Figure 3.3.

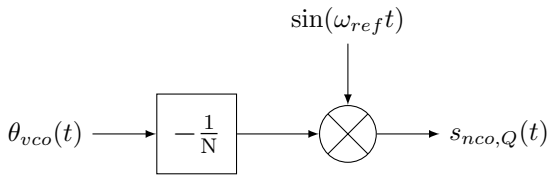

Figure 3.3: Small signal block diagram of the NCO

The multiplication with the signal $\sin(\omega_{ref}t)$ is an LPTV operation. This signal can be rewritten as

$$\sin(\omega_{ref}t) = \frac{e^{j\omega_{ref}t} - e^{-j\omega_{ref}t}}{2j}. \tag{3.14}$$

From this notation, the Fourier coefficients are visible. These are

$$S_n = \begin{cases} -\frac{1}{2j} & n = -1 \\ \frac{1}{2j} & n = 1 \\ 0 & \text{otherwise} \end{cases} \tag{3.15}$$

The HTM for the NCO is obtained using Equation A.19. The result is

$$\widetilde{\mathbf{H}}_{\mathbf{NCO}}(s) = -\frac{1}{\mathrm{N}} \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & 0 & -\frac{1}{2j} & 0 & \cdots \\ \cdots & \frac{1}{2j} & 0 & -\frac{1}{2j} & \cdots \\ \cdots & 0 & \frac{1}{2j} & 0 & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{3.16}$$

DAC

The DAC converts the digital NCO signal to an analog voltage. The input-output expression used for modeling this behavior is

$$s_{dac}(t) = \mathrm{K_{DAC}} \cdot s_{nco,Q}(t) + s_{n,dac}(t) \tag{3.17}$$

Since aliasing effects are neglected, this is a time invariant operation. An additional noise input is added which can be used for modeling DAC quantization noise. A block diagram describing the DAC can be found in Figure 3.4. The HTM is derived using Equation 3.12 and becomes

$$\widetilde{\mathbf{H}}_{\mathbf{DAC}}(s) = \mathrm{K_{DAC}} \cdot \mathbf{I}. \tag{3.18}$$

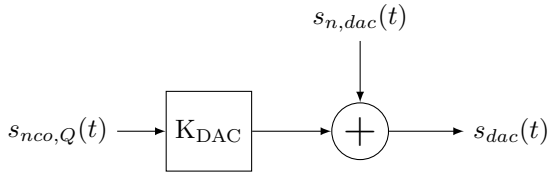

Figure 3.4: Small signal block diagram of the DAC

Notch Filter

The notch filter filters the carrier. But since the filter cannot be of infinite quality, the phase information is also altered. The HTM of the notch filter can be described from its LTI transfer function $\mathrm{H}_{\mathrm{notch}}(s)$ using Equation 3.12.

ADC

The ADC digitizes the phase noise signal. Like the DAC, it is assumed that no aliasing occurs. A noise input is added to the model such that the quantization noise transfer can be calculated. A block diagram of the small signals in the ADC can be found in Figure 3.5. The HTM is derived using Equation 3.12 and becomes

$$\widetilde{\mathbf{H}}_{\mathbf{ADC}}(s) = \mathrm{K}_{\mathrm{ADC}} \cdot \mathbf{I}. \tag{3.19}$$

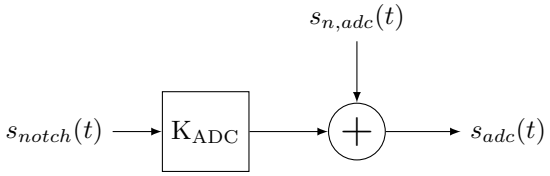

Figure 3.5: Small signal block diagram of the ADC

Mixer

The mixer multiplies the digital input signal, which comes from the ADC, with a signal coming from the NCO. As described in Section 2.5, different mixer signals can be used, where a sum of odd harmonics are added. A block diagram of the mixer with one harmonic can be found in Figure 3.6.

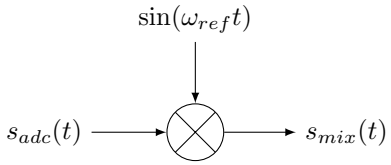

Figure 3.6: Small signal block diagram of the mixer

The mixer signal is generated by the NCO, such that the phase variations of the VCO are also present on the mixer signal. These phase variations introduce second order, nonlinear, effects, which are neglected in this analysis. Therefore it is assumed that the mixer signal has no phase variations.

The HTM of the mixer with only the fundamental mixer signal is

$$\widetilde{\mathbf{H}}_{\mathbf{MIX}}(s) = \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & 0 & -\frac{1}{2j} & 0 & \cdots \\ \cdots & \frac{1}{2j} & 0 & -\frac{1}{2j} & \cdots \\ \cdots & 0 & \frac{1}{2j} & 0 & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{3.20}$$

When the third harmonic is added, the signal becomes

$$\widetilde{\mathbf{H}}_{\mathbf{MIX,2}}(s) = \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \vdots & \vdots & \\ \cdots & 0 & -\frac{1}{2j} & 0 & -\frac{1}{2j} & 0 & \cdots \\ \cdots & \frac{1}{2j} & 0 & -\frac{1}{2j} & 0 & -\frac{1}{2j} & \cdots \\ \cdots & 0 & \frac{1}{2j} & 0 & -\frac{1}{2j} & 0 & \cdots \\ \cdots & \frac{1}{2j} & 0 & \frac{1}{2j} & 0 & -\frac{1}{2j} & \cdots \\ \cdots & 0 & \frac{1}{2j} & 0 & \frac{1}{2j} & 0 & \cdots \\ & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{3.21}$$

Extra harmonics can be added by adding the appropriate diagonals to the HTM.

Filter

The loop-filter can be modeled as an LTI system with transfer function $\mathrm{H}_{\mathrm{LF}}(s)$. Therefore the HTM follows from Equation 3.12. The HTM of the loop-filter is denoted as $\widetilde{\mathbf{H}}_{\mathbf{LF}}(s)$.

In a type-I PLL loop, the oscillator is the only integrator in the loop and the filter only has a static gain, such that

$$\mathrm{H}_{\mathrm{LF,I}}(s) = \alpha. \tag{3.22}$$

A type-II PLL loop contains a discrete-time integrator with a feed-forward path. This is approximated as

$$\mathrm{H}_{\mathrm{LF,II}}(s) = \alpha + \beta \frac{1}{1 - e^{-sT}}. \tag{3.23}$$

In the case of higher order loops or IIR filters, the HTM can be adjusted to the transfer-function of the specific loop-filter.

Discrete-time delays

The digital system uses some registers that introduce delays. These delays limit the stability of the loop and must be added to the model to properly predict the noise transfer at high loop bandwidths. A discrete time delay can be modeled as a shift in the time domain. The s-domain representation of a delay is

$$\mathrm{H}_{\mathrm{delay}}(s) = e^{-s \cdot n T_{clk}} \tag{3.24}$$

The value of T_{clk} is the digital clock period, and n is the number of clock periods delay that are made in the digital processing. The clock delay is an LTI operation, so the HTM follows from Equation 3.12. The HTM of the loop-filter is denoted as $\widetilde{\mathbf{H}}_{\mathbf{delay}}(s)$.

Closed loop expressions

From the HTMs of the different parts of the PLL, closed loop expressions can be derived. This is done using the method described in Section A.2. A block diagram containing all the functional blocks is shown in Figure 3.7.

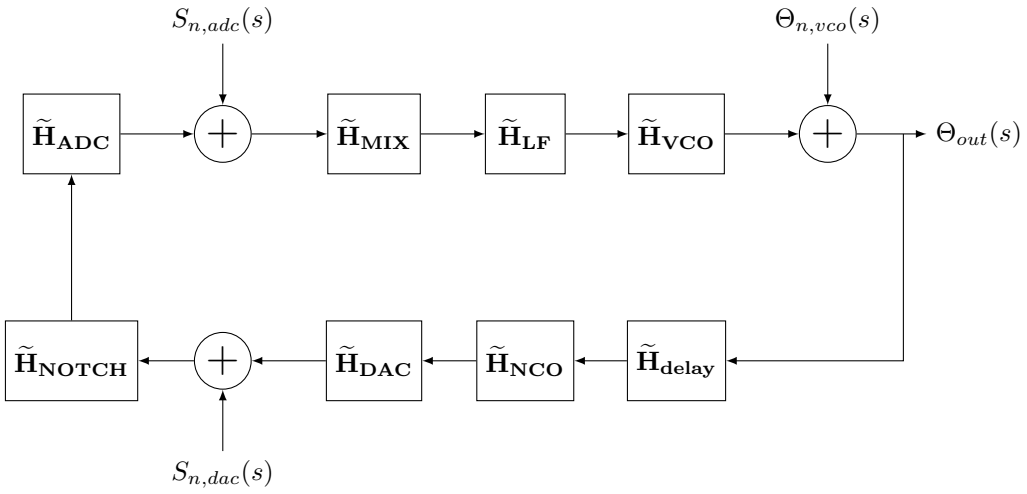

Figure 3.7: Block diagram of the PLL

Three different transfers are calculated, namely the transfer from the VCO phase noise to the output phase, ADC quantization noise to the output and from the DAC quantization noise to the output. The open loop gain of the PLL is

$$\widetilde{\mathbf{G}}(s) = \widetilde{\mathbf{H}}_{\mathbf{VCO}} \cdot \widetilde{\mathbf{H}}_{\mathbf{LF}} \cdot \widetilde{\mathbf{H}}_{\mathbf{MIX}} \cdot \widetilde{\mathbf{H}}_{\mathbf{ADC}} \cdot \widetilde{\mathbf{H}}_{\mathbf{NOTCH}} \cdot \widetilde{\mathbf{H}}_{\mathbf{DAC}} \cdot \widetilde{\mathbf{H}}_{\mathbf{NCO}} \cdot \widetilde{\mathbf{H}}_{\mathbf{delay}}. \tag{3.25}$$

Using this equation, the closed loop expressions can be calculated. These are listed in Equation 3.26.

$$\begin{aligned}
\Theta_{out,vco}(s) &= \left(\mathbf{I} + \widetilde{\mathbf{G}}(s)\right)^{-1} \cdot \Theta_{n,vco}(s) \\
\Theta_{out,adc}(s) &= \left(\mathbf{I} + \widetilde{\mathbf{G}}(s)\right)^{-1} \cdot \widetilde{\mathbf{H}}_{\mathbf{VCO}} \cdot \widetilde{\mathbf{H}}_{\mathbf{LF}} \cdot \widetilde{\mathbf{H}}_{\mathbf{MIX}} \cdot S_{n,adc}(s) \\
\Theta_{out,dac}(s) &= \left(\mathbf{I} + \widetilde{\mathbf{G}}(s)\right)^{-1} \cdot \widetilde{\mathbf{H}}_{\mathbf{VCO}} \cdot \widetilde{\mathbf{H}}_{\mathbf{LF}} \cdot \widetilde{\mathbf{H}}_{\mathbf{MIX}} \cdot \widetilde{\mathbf{H}}_{\mathbf{ADC}} \cdot \widetilde{\mathbf{H}}_{\mathbf{NOTCH}} \cdot S_{n,dac}(s)
\end{aligned} \tag{3.26}$$

Since matrix operations are required to calculate the inverse of an HTM, analytic expressions are not easily found and difficult to interpret due to their length. In the next section, some assumptions are made such that a coarse approximation can be made. Besides these approximations, the model is evaluated numerically using MATLAB with greater accuracy.

3.4 Approximate Analytic Expressions

When some assumptions are made, simplified expressions can be derived for important system parameters like the bandwidth and the effect of quantization noise. It is assumed that the loop bandwidth is much smaller than the reference frequency, such that the rank reduction method can be used with $R = 0$. This method is described in Appendix A.2. All the frequency transfers to frequencies beyond $f_{ref}/2$ are neglected. Besides this, the result is only valid for frequencies near DC.

For higher loop bandwidths, neglecting transfers beyond $f_{ref}/2$ will give errors. There can for example be a phase noise component that is first transferred from frequencies around $4f_{ref}$ to frequencies around $2f_{ref}$. Since the system with only a fundamental reference signal for the mixer has an image at $2f_{ref}$, this component can be mixed down to baseband during the next pass of the digital system. This leads to extra in-band phase noise, which is neglected with this method.

It is still expected that this approximation gives an rough estimate for in-band behavior. Exact behavior has to be verified with a numeric MATLAB solution.

In order to do the Rank-1 approximation, vector that is used for $\mathbf{P}$ is

$$\mathbf{P} = \begin{bmatrix} \vdots \\ 0 \\ 1 \\ 0 \\ \vdots \end{bmatrix}. \tag{3.27}$$

The open loop gain is shown in Equation 3.25. It is assumed that the loop delay is much smaller than the bandwidth of the system, such that this can be neglected. The notch filter is assumed to be perfect, such that the small signal transfer is unity. The loop filter that is used is a Type-I filter, with gain α. Using the HTMs derived in the previous section, the open loop gain becomes

$$\begin{aligned}\widetilde{\mathbf{G}}(s) =& 2\pi \mathrm{K_{VCO}} \cdot \mathrm{K_{DAC}} \cdot \mathrm{K_{ADC}} \cdot \alpha \\ & \cdot \frac{1}{\mathrm{N}} \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \vdots & & \\ \cdots & \frac{1}{2}\frac{1}{s-2j\omega_0} & 0 & -\frac{1}{4}\frac{1}{s-2j\omega_0} & 0 & 0 & \cdots \\ \cdots & 0 & \frac{1}{2}\frac{1}{s-j\omega_0} & 0 & -\frac{1}{4}\frac{1}{s-j\omega_0} & 0 & \cdots \\ \cdots & -\frac{1}{4}\frac{1}{s} & 0 & \frac{1}{2}\frac{1}{s} & 0 & -\frac{1}{4}\frac{1}{s} & \cdots \\ \cdots & 0 & -\frac{1}{4}\frac{1}{s+j\omega_0} & 0 & \frac{1}{2}\frac{1}{s+j\omega_0} & 0 & \cdots \\ \cdots & 0 & 0 & -\frac{1}{4}\frac{1}{s+2j\omega_0} & 0 & \frac{1}{2}\frac{1}{s+2j\omega_0} & \cdots \\ & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots \end{pmatrix}.\end{aligned} \tag{3.28}$$

For a Rank-1 reduction approximation, only the cell in the middle is used. It can be seen that the other rows in the HTM have terms $(s - nj\omega_0)$ in the denominator, which makes them much smaller than the middle row for $s \to 0$. The 1x1 sub-matrix becomes

$$\mathbf{G_P}(s) = 2\pi \frac{\mathrm{K_{VCO}}}{s} \cdot \frac{1}{2\mathrm{N}} \cdot \mathrm{K_{DAC}} \cdot \mathrm{K_{ADC}} \cdot \alpha \tag{3.29}$$

Similarly, the forward path from ADC to the output phase is

$$\widetilde{\mathbf{H}}_\mathbf{A}(s) = \widetilde{\mathbf{H}}_\mathbf{VCO} \cdot \widetilde{\mathbf{H}}_\mathbf{LF} \cdot \widetilde{\mathbf{H}}_\mathbf{MIX} = 2\pi \mathrm{K_{VCO}} \cdot \alpha \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & 0 & -\frac{1}{2j}\frac{1}{s-j\omega_0} & 0 & \cdots \\ \cdots & \frac{1}{2j}\frac{1}{s} & 0 & -\frac{1}{2j}\frac{1}{s} & \cdots \\ \cdots & 0 & \frac{1}{2j}\frac{1}{s+j\omega_0} & 0 & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{3.30}$$

Using Equation A.29, the approximated closed loop transfer becomes

$$\mathbf{\Theta_{out}}(\mathbf{s}) = \begin{bmatrix} \vdots \\ 0 \\ 1 \\ 0 \\ \vdots \end{bmatrix} \frac{2\pi\frac{\mathrm{K_{VCO}}}{s} \cdot \alpha}{1 + 2\pi\frac{\mathrm{K_{VCO}}\cdot\mathrm{K_{DAC}}\cdot\mathrm{K_{ADC}}}{s} \cdot \alpha \cdot \frac{1}{2\mathrm{N}}} \begin{bmatrix} \cdots & 0 & \frac{1}{2j} & 0 & -\frac{1}{2j} & 0 & \cdots \end{bmatrix} \mathbf{S_{n,adc}}(\mathbf{s}). \quad (3.31)$$

It can be seen that the ADC quantization noise is mixed from frequencies around the reference frequency into baseband. Quantization noise from baseband is not transfered to the baseband output in this rank-1 approximation. Using a higher-rank approximation, it can be shown that baseband noise is transfered to frequencies around the reference frequency.

The cut-off frequency of the transfer function is equal to

$$\omega_{-3dB} = 2\pi \cdot \mathrm{K_{VCO}} \cdot \mathrm{K_{DAC}} \cdot \mathrm{K_{ADC}} \cdot \alpha \cdot \frac{1}{2\mathrm{N}}. \quad (3.32)$$

Note that this expression is only valid for small bandwidth PLLs, as this assumption was made in the reduced rank method. The in-band phase noise due to the ADC quantization noise can be approximated by letting $s \to 0$. This is approximately

$$\frac{S_{\theta\theta,out}}{S_{nn,adc}} = 2\left(\frac{\mathrm{N}}{\mathrm{K_{DAC}} \cdot \mathrm{K_{ADC}}}\right)^2. \quad (3.33)$$

$S_{nn,adc}$ is the ADC quantization noise density around the reference frequency. The contributions of $-f_{ref}$ and f_{ref} are summed, which introduces the factor two. $S_{\theta\theta,out}$ is the in-band phase noise density at the output of the PLL. It can be seen that, similar to charge-pump PLLs, the quantization noise is multiplied with N^2. Since the carrier signal is filtered away, only the small error-signal is left. By adding gain before the ADC, the effect of the quantization noise of the ADC can be reduced.

The DAC quantization transfer is similar to the transfer of the ADC. For in-band signals, it is approximately

$$\frac{S_{\theta\theta,out}}{S_{nn,dac}} = 2\left(\frac{\mathrm{N}}{\mathrm{K_{DAC}}}\right)^2. \quad (3.34)$$

Similar analysis can be done for the transfer-function for VCO phase noise. Using the same Rank-1 reduction technique, this transfer becomes approximately

$$\mathbf{\Theta_{out}}(\mathbf{s}) = \begin{bmatrix} \vdots \\ 0 \\ 1 \\ 0 \\ \vdots \end{bmatrix} \frac{1}{1 + 2\pi\frac{\mathrm{K_{VCO}}\cdot\mathrm{K_{DAC}}\cdot\mathrm{K_{ADC}}}{s} \cdot \alpha \cdot \frac{1}{2\mathrm{N}}} \begin{bmatrix} \cdots & 0 & 0 & \frac{1}{2} & 0 & 0 & \cdots \end{bmatrix} \mathbf{S_{\phi,vco}}(\mathbf{s}). \quad (3.35)$$

A high-pass characteristic can be recognized, as expected from the PLL. Low frequency phase errors generated by the VCO are suppressed. In reality there are also transfers from frequencies around $2f_{ref}$ to baseband due to the mixer aliases. These transfers are neglected due to the rank-1 approximation. By using an improved bandwidth mixer as described in Section 2.5, this transfer is from four times the reference to baseband.

3.5 Event-Based Simulation Model

For the LPTV model, many assumptions have been made with respect to the system's behavior. The effect of non-linearities, rounding and stochastic variations can for example not be assessed using an LPTV model.

Therefore an event-based simulation model is built next to the LPTV model. In this model, all the PLL blocks are modeled behaviorally. This allows system simulations on a functional level, including nonlinear and stochastic effects. The model will be used to verify the accuracy and determine the shortcomings of the analytical LPTV model.

Event-Based Simulation

Most of the signals in the proposed PLL are in the discrete-time domain. Where the LPTV model assumes all signals to be in the continuous-time domain, the event-based model models them as discrete-time signals. The only continuous-time signals in the systems are the signals at the analog notch filter. These signals are approximated in the discrete-time domain using numerical integration techniques.

The time-step of the system is equal to the output period of the VCO. There are however minor variations in time-step due to phase variations of the VCO. The exact time at which the output clock rises is important, since the variations from the ideal clock are required to determine the systems phase noise.

When a fixed time-step simulator is used, the time-step must be much smaller than the expected time-variation. This results in long simulations and the system state is recalculated even when it has not changed. A event-based simulator does not have this problem since the systems state is only recalculated on an event basis. This event can be the rise of the output clock. This makes simulation possible with a variable time-step, where the time-step is set by the VCO.

VHDL can be used to do event-based simulations. The advantage of using VHDL for event-based simulations is that good simulators are available. Besides this, the digital system can directly be integrated into the model. The time-resolution in which events can be scheduled is 1 fs, which is accurate enough to simulate small levels of phase noise.

In the next subsections, a small introduction is given on how the VHDL models of key-components in the PLL are realized.

VCO

The VCO is the most important part in the event-based model. The VCO controls the time-instances on which the output clock rises and when events are launched. The time at which the clock rises next is based on two factors. The first factor is the tuning input of the VCO, which determines the nominal period.

The second factor is a stochastic variation representing the VCOs phase noise. This variation is based on Gaussian random variables, generated using a pseudo-random uniform number generator and the Box-Muller transform [10]. The Box-Muller transform can be used to generate two independent Gaussian random numbers given two uniformly distributed random numbers. Fixed seeds are used for the random number generator in order to get reproducible results.

The phase noise of the VCO can be expressed as two parts, a period deviation and an edge variation. Period deviations are accumulated edge variations, and specify the $1/f^2$ part of the

phase noise. Edge variations represent the 'white' phase noise. In [11], a method is described to calculate the standard deviation of these quantities for a given phase noise level.

Notch Filter

The notch filter can be simulated using two methods. The first method is a behavioral method, which subtracts a time continuous signal with the reference frequency from the analog signal generated by the DAC. The amplitude of the signals must match in order to suppress the carrier signal completely. By only subtracting the signal partly, the quality of the notch can be varied. This method is primarily used to analyze the system, since its simplicity helps in making the system understandable.

The second method implements a more realistic notch filter response. In Chapter 5, a circuit will be introduced which embeds a crystal resonator as a filter. In order to simulate this circuit, the crystal is modeled using its equivalent circuit model as seen in Figure 3.8. In order to calculate the discrete-time state of the circuit, the state space equations are written down. These equations are solved each system event using the fourth-order Runge-Kutta numerical integration method. A higher order differential equation solver is used because the system has a variable time-step. This makes the first-order Euler integration method not accurate enough.

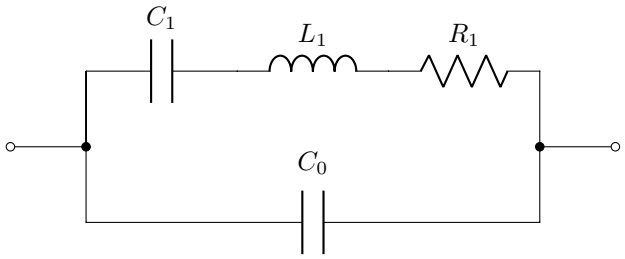

Figure 3.8: Equivalent circuit of a crystal resonator

DAC and ADC

For the DAC and ADC, two models are made. The first model is a simple model, that corresponds to the linear model. An additional Gaussian signal with a power equal to the mean square of the quantization error is added to the signal.

The second implementation rounds the signal to the actual quantization steps. This behavior corresponds more to a real ADC, since nonlinear effects of quantization are taken into account. When a feedback loop and discrete-time integrator are added, a noise shaping ADC can be simulated.

Phase Noise Processing

In order to estimate the output phase noise, the timestamps of the rising edges of the output clock are logged in an output file. In MATLAB, these timestamps are processed, yielding the phase deviation from the ideal output clock. From this phase deviation, the single-sided power spectral density is estimated using Welch's method. This methods averages different noise realizations in the frequency domain, such that the noise is reduced and a smoother spectrum is obtained. The phase noise is finally calculated using

$$\mathcal{L}(f) = \frac{S_{\theta\theta}(f)}{2} \tag{3.36}$$

When the phase noise for frequencies up to 10 kHz is simulated, a quarter of a million bins are required. Not all of these points can be plotted into this report. Therefore the results is subsampled. This is done on a logarithmic basis, such that more time resolution is obtained for lower frequencies and the amount of points at higher frequencies is reduced. Spurs are included to this

sub-set such that these are not lost during sub-sampling. This is checked by comparing the original datasets with the sub-sampled plot.

3.6 Validation

In order to validate the LPTV model, the noise outputs are compared to the values obtained from the event-based model. Three different simulations are performed. First a PLL with solely VCO phase noise is simulated. Secondly, ADC noise is added and in the last step also DAC quantization noise is added. Differences between the LPTV model and the simulations are discussed. In the next Chapter, the system is analyzed in more details and more attention is given to the exact behavior of the system.

An oscillator with high $1/f^2$ noise is simulated. At 100 kHz, the phase noise level is -80 dBc/Hz. The phase noise floor is -150 dBc/Hz. The loop-filter that is used is a type-II filter and the bandwidth of the PLL nears the reference frequency. A comparison of the LPTV model and the event-based simulation results are shown in Figure 3.9.

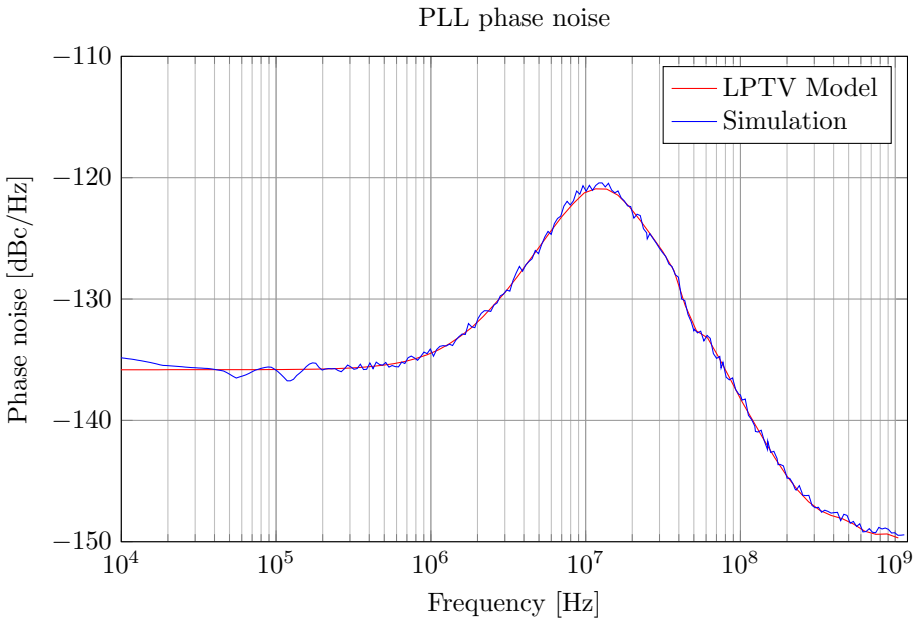

Figure 3.9: PLL phase noise without ADC quantization noise

It can be seen that the LPTV model closely matches the event-based simulation result. In another simulation, ADC quantization noise is added. Because there is no amplifier between the notch filter and ADC, the ADC input levels are very small. Therefore the quantization step must be taken very small in order to let the signal cross multiple quantization levels, otherwise major nonlinearities are introduced. In order to assess the linear behavior of the system, it is chosen to add additional white Gaussian noise to the ADC output instead of discrete quantization levels. The noise power that is chosen has an equivalent power of an 1 mV quantization step. The phase noise of the output can be found in Figure 3.10.

Like the previous simulation, the model and simulation model closely match. Using Equation 3.33, an estimate can be made of the in-band phase noise levels. For a 1 mV quantization step, $f_{out} = 2.4$ GHz and $f_{ref} = 25$ MHz, this level becomes

$$\mathcal{L}(\text{in-band}) = 10\log\left(\frac{\Delta^2}{12}\frac{2}{f_{out}}N^2\right) = -121.9\text{dBc/Hz}. \tag{3.37}$$

For low-frequencies, this corresponds to the phase noise obtained in simulation.

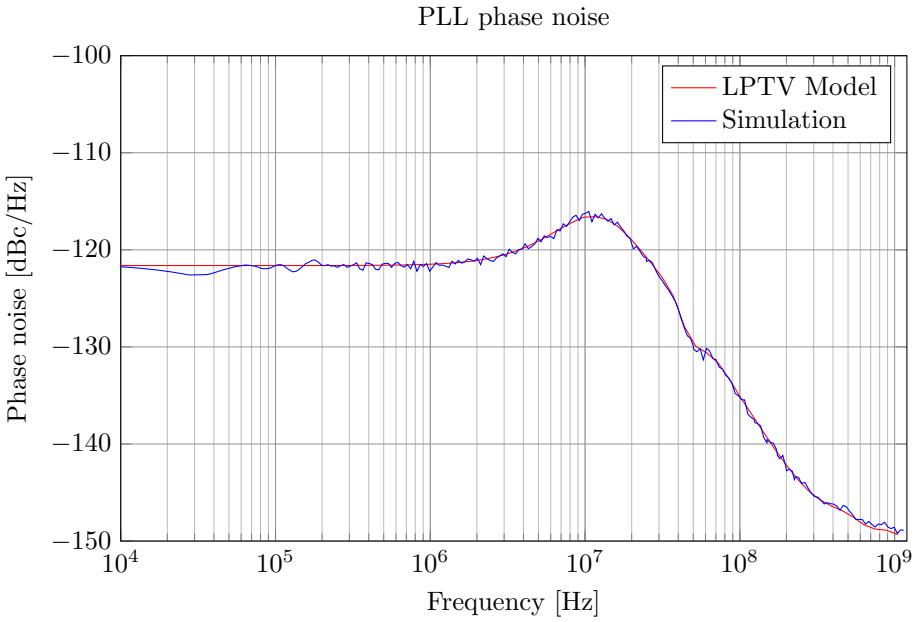

Figure 3.10: PLL phase noise with ADC quantization noise

The last simulation that is done for validating the models is by adding discrete quantization steps to the DAC in addition to the ADCs quantization noise and the VCO phase noise. Like the ADC, 1 mV quantization levels are simulated. For the DAC, this is done by actually rounding the output. This can be done since the DAC signal has a much larger swing. The output phase noise for the LPTV model and simulation and model can be found in Figure 3.11.

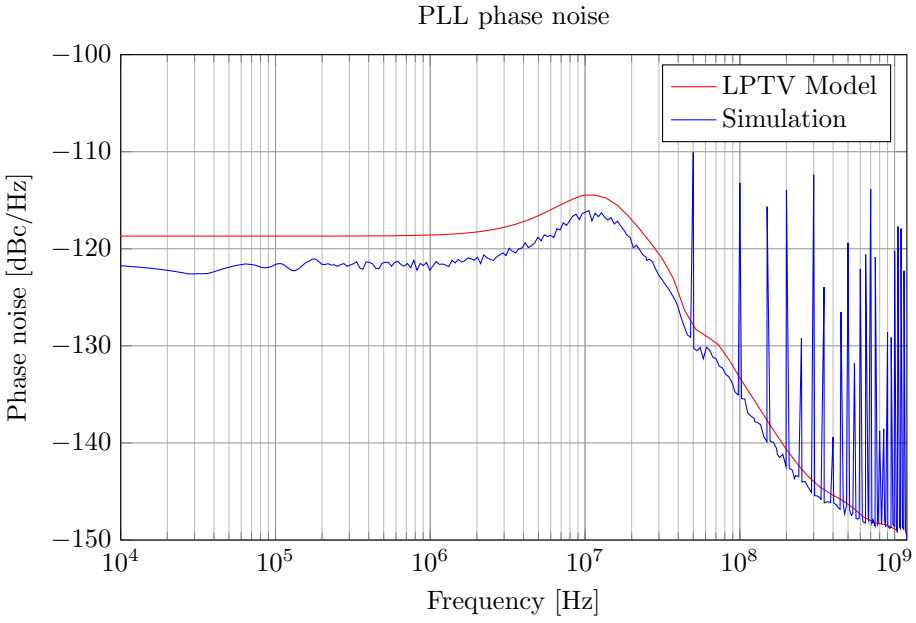

Figure 3.11: PLL phase noise with DAC and ADC quantization noise

In this situation there is a discrepancy between the simulation and model. It can be seen that spurs are present at multiples of $2f_{ref}$. This happens because the DAC signal is a repeating, periodic signal. Since an integer value of N is chosen, there fit an integer amount of sample in one reference period. Therefore the quantization errors repeat periodically, such that the quantization error is concentrated into spurs. This is non-linear behavior, which is not included into the LPTV model but can be simulated using the event-based model.

3.7 Conclusions

In this chapter, an LPTV model and a event-based model are built to describe the behavior of the Crystal Embedded Digital Phase-Locked Loop. The LPTV model can be used to get an analytic estimate of the phase noise due to a certain input noise spectrum. The event-based model can be used to more accurately describe nonlinear behavior of the system. It is verified that the LPTV model and event-based model closely match, as long as the system is approximately linear.

The event-based system simulations are considered as the most complete and form the most accurate description of what a 'real' system should look like. The event-based system description is behavioral, which is close to a real system's behavior. Therefore it is said that the event-driven model forms a realistic description of a real system for the aspects that are modeled.

Since the LPTV model is based on completely different assumptions, an error in the behavioral descriptions would lead to discrepancies with the LPTV model. These discrepancies can be explained if no modeling error is involved. An example are the spurs which show up when an actual quantizer is used for the DAC, which are due to the periodic repetition in quantization errors.

In the current event-based model, system aspects such as ADC DNL errors, crosstalk and VCO $1/f^3$ noise are not taken into account, which means that there will be a difference between the simulation results and a silicon prototype or transistor-level simulations. These effects can however be added to the event-based simulation model if desired.

Chapter 4

System Analysis and Simulation

In this chapter, the Crystal Embedded Digital Phase-Locked Loop is analyzed. This is done using the LPTV model and the Event-Based Simulation Model described in the previous chapter. The analysis is done in different steps. First, the effect of VCO phase noise is analyzed. Different loop-filter configurations are used. After this, the effect of ADC and DAC quantization noise is analyzed. Different ADC topologies are simulated, including a noise shaping ADC. In the last section, the impact of the enhanced mixer proposed in Section 2.5 on the system is qualified.

For all the simulations, unless otherwise noted, the parameters listed in Table 4.1 are used. The phase noise levels of the VCO are comparable to the phase noise of the oscillator used in [8]. The DAC and ADC are modeled as an unity gain block without quantization noise. The notch filter is modeled as an adder which subtracts the 'carrier' signal completely.

f_{out}	2.4 GHz
f_{ref}	25 MHz
$\mathcal{L}_{\text{vco},1/f^2}$(100 kHz)	-80 dBc/Hz
$\mathcal{L}_{\text{vco}}$	-150 dBc/Hz
K_{ADC}	1
K_{DAC}	1
K_{VCO}	f_{out}

Table 4.1: Common system parameters

4.1 VCO Phase Noise

The first system aspect that is analyzed is the VCO phase noise. The phase noise of the free-running VCO is shown in Figure 4.1. This result is obtained by setting the transfer of the loop-filter to zero in the discrete-event model and the LPTV model.

It can be seen that the phase noise has a -20 dB/dec slope as expected from an oscillator. The phase noise crosses-80 dBc/Hz at 100 kHz. The phase noise floor is -150 dBc/Hz. These values are in correspondence with Table 4.1.

In the next subsections, the closed loop behavior of the PLL is analyzed with regard to the VCO phase noise. Two different loop-filters are used. First a type-I filter with different gains are compared. After that type-I and type-II loop-filters are compared.

Type-I

A type-I loop-filter only has a constant gain α. Three values for α are used, namely 1.0, 0.5 and 0.1. The simulation results for these values of α can be found in Figure 4.2.

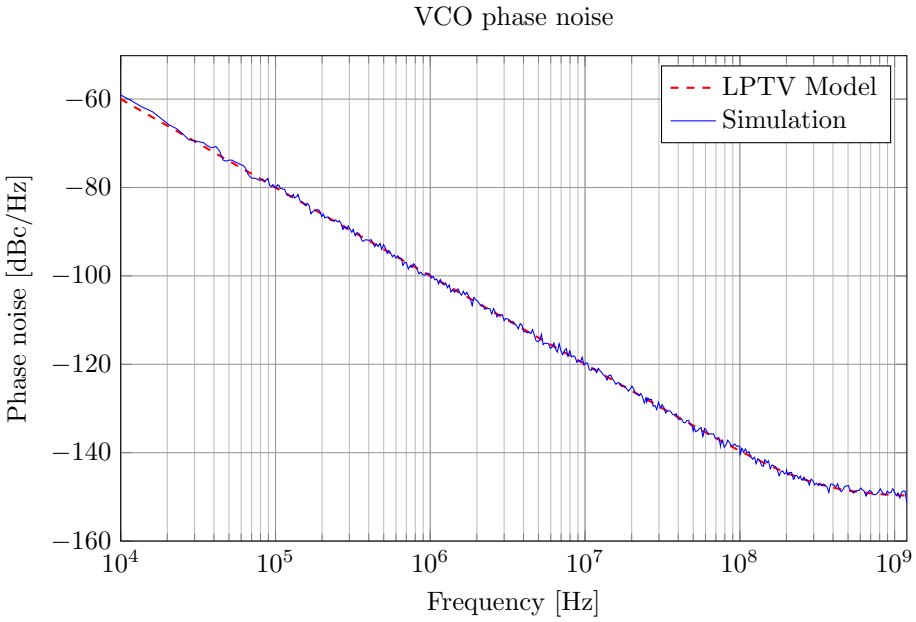

Figure 4.1: Free-running VCO phase noise spectrum

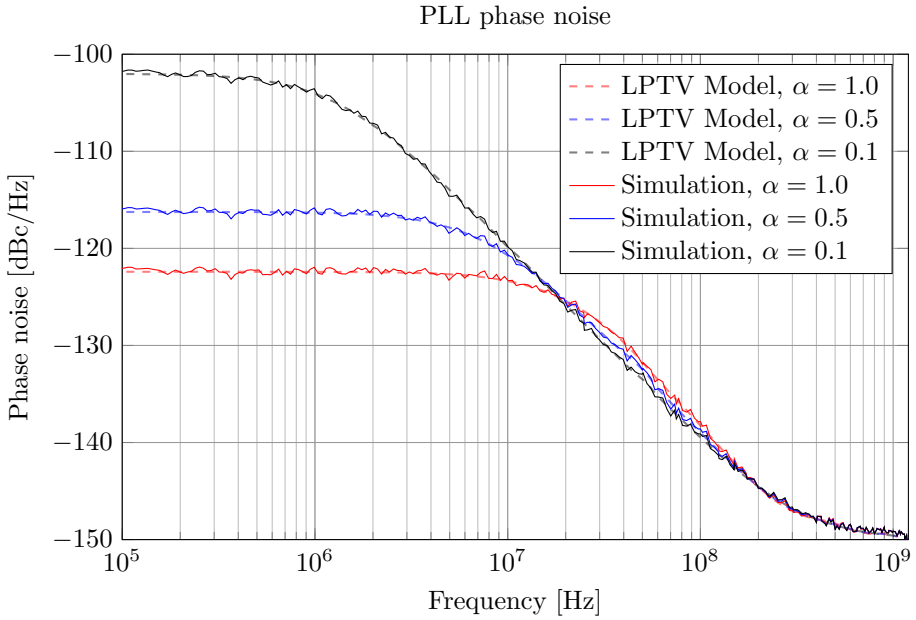

Figure 4.2: PLL phase noise due to VCO with type-I loop-filter

The first thing that can be observed is that the model and simulation results closely match. This means that the LPTV model is sufficiently accurate to describe the systems behavior. The -3dB bandwidth of PLL can be estimated from the simulation results. These estimation are shown in Table 4.2. The expected value from Equation 3.32 is also shown.

The simulated bandwidth is higher than the approximations made using Equation 3.32, especially for higher bandwidths. The main reason is that the approximation does not include the loop delay. These loop delays become more important for large values of α. The current implementation has six clock cycles delay in the feedback loop, which degrades the phase-margin of the loop. This results in added phase noise for frequencies near cut-off, which shifts the -3dB point to a higher frequency. By decreasing the number of digital delays in the design, this effect can be minimized.

α	f_{-3dB} (Simulation)	f_{-3dB} (Equation 3.32)
0.1	1.3 MHz	1.25 MHz
0.5	7.5 MHz	6.25 MHz
1.0	20 MHz	12.5 MHz

Table 4.2: System bandwidth

This is shown in Figure 4.3. Here the VCO noise output for the LPTV model is shown for $\alpha = 1.0$. There are two lines, one with inclusion of digital delays and one without digital loop delay. For the model without digital delay, the loop bandwidth is approximately 12.5 MHz, which is in line with the value obtained using Equation 3.32. The in-band phase noise for the delay-less loop is 0.8 dB higher due to the decreased loop bandwidth.

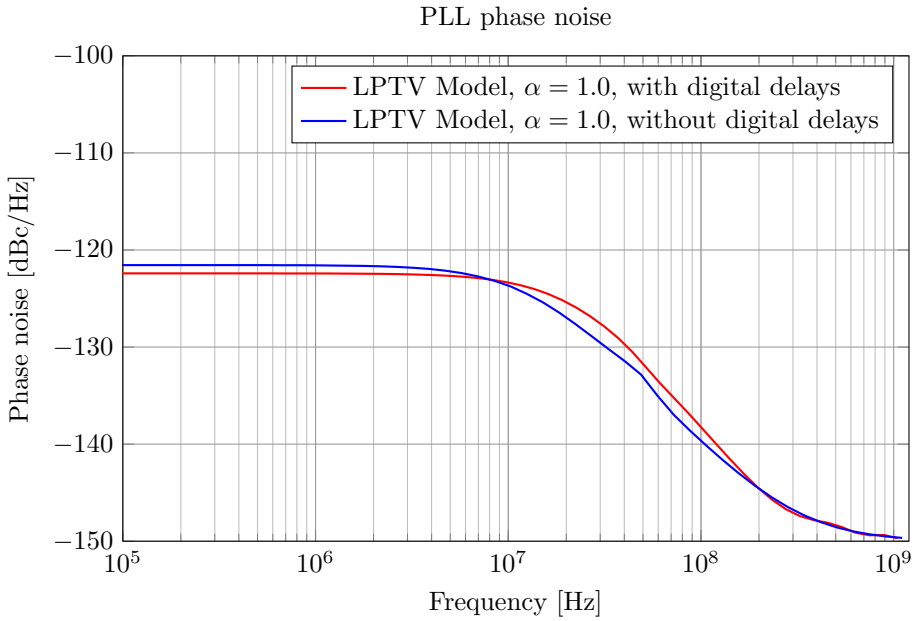

Figure 4.3: PLL phase noise due to VCO with Type-I loop-filter. With and without model of digital delays

Type-II

Another simulation is performed for a type-II loop. The mathematical description of the loop-filter can be found in Equation 3.23. The value of β is set to 0.02 and α is set to 1.0, such that the loop is approximately critically damped. The results of the simulation and model can be found in Figure 4.4, along with the result of the type-I PLL with $\alpha = 1.0$.

Low frequency phase noise from the VCO is suppressed more since an extra integrator is present in the loop. This makes that the loop has slope of 40 dB/dec for in-band frequencies, such that the phase noise increases with 20 dB/dec. For frequencies below 1 MHz, this attenuation is not visible since the dominant phase noise contribution is the phase noise mixed down from frequencies around $2f_{ref}$.

The phase noise at 50 MHz ($2f_{ref}$) is -132 dBc/Hz. The phase noise at low offset frequencies is -135.8 dBc/Hz, which is approximately 3 dB lower than the phase noise from 50 MHz. This is due to the mixing gain of 0.5, which introduces a 3 dB attenuation.

At frequencies around cut-off, the phase noise levels are higher than the phase noise in the type-I PLL. This is the case because the extra integrator decreases the phase margin, which introduces

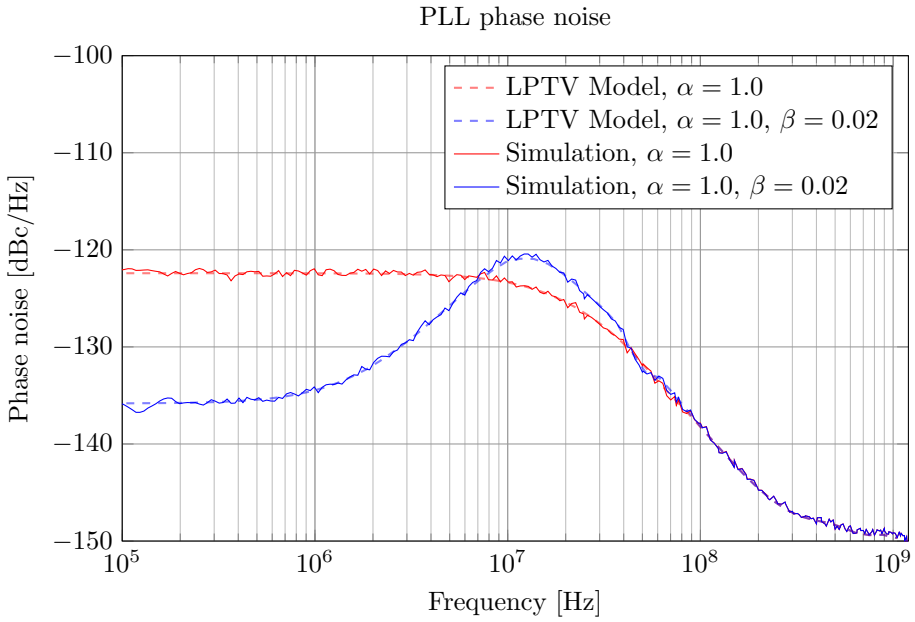

Figure 4.4: Type-I and type-II PLL comparison

slight peaking around cut-off. Decreasing the value of β reduces this effect, but this increases phase noise at low frequencies. Another way to decrease the peaking is to decrease the amount of digital delays in the loop.

4.2 ADC Quantization Noise

The next aspect that is analyzed is the quantization noise performance of the ADC. First a Nyquist ADC will be simulated, after which a noise-shaping ADC is simulated.

Nyquist ADC

For the first simulations an ADC with a quantization step of respectively 1 mV and 10 mV is used. In the Event-Based simulation, the ADC is modeled as a linear gain with an addition of white noise. A type-I loop is used with $\alpha = 1.0$. The VCO does not produce any phase noise in this analysis, such that the ADC quantization can be analyzed exclusively. The simulation and modeling result is shown in Figure 4.5.

Using Equation 3.33, an approximation of the phase noise due to ADC quantization noise can be made. An quantization step of 10 mV gives a double sided quantization noise power of $\frac{0.010^2}{\sqrt{12} f_{out}} = -144.6$ dB/Hz. The gain of the ADC and DAC is equal to 1 and $N = \frac{2.4\text{GHz}}{25\text{MHz}} = 96$, such that the in-band phase noise is approximately -101.9 dBc/Hz. This corresponds to the value obtained using simulation and the LPTV model.

It can be seen that the in-band phase noise for the ADC with 1 mV quantization step is 20 dB lower than the 10 mV ADC. This is as expected, since the system is approximately linear and the quantization noise power is proportional to the square of the quantization step.

Around 50 MHz, an increase in the phase noise with respect to an ideal -20 dB/dec slope can be noticed. This is an image of the baseband phase noise, which is up-converted by the NCO and mixer. Since this image is filtered by the loop-filter, the noise level is almost 15 dB lower. When the order of the loop-filter is increased, this image can be suppressed further.

The simulated phase noise around 1 GHz is higher than the modeled phase noise. It is expected that this is due to aliasing in the ADC. This behavior is not modeled in the LPTV model, but

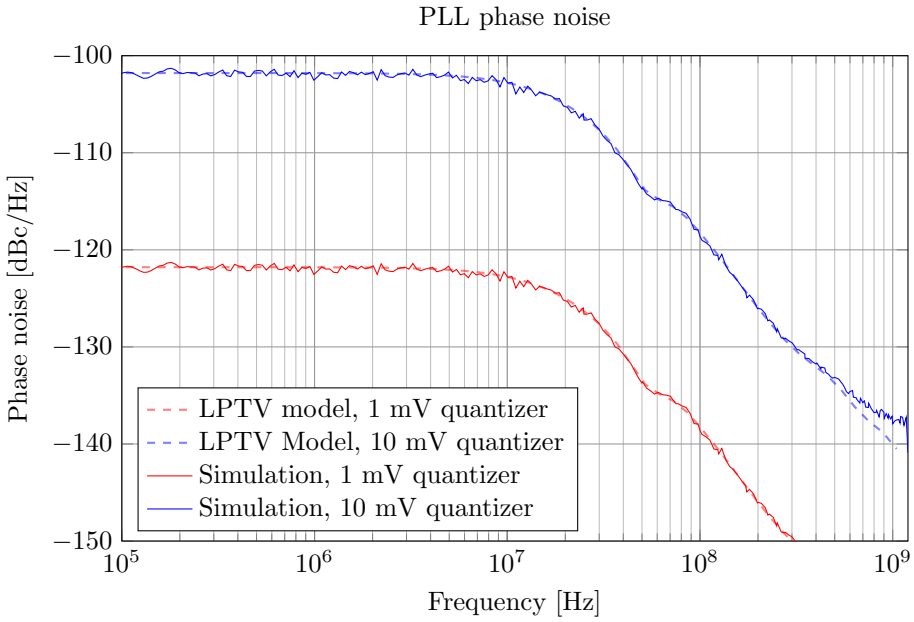

Figure 4.5: PLL phase noise due to ADC quantization noise

sampling is done in the Event-Based simulation model. Since this effect is small and at high frequencies which are not of primary interest, this aliasing is not added to the LPTV model.

Noise shaping ADC

Next to the Nyquist ADCs, first and second-order sigma-delta ADCs are simulated. Perfect discrete-time integrators are assumed and one-bit quantizers are used. Before the first-order ADC, a voltage gain of 100 is introduced to amplify the small signal levels. A gain of 10 is used for the second-order ADC.

In addition to a type-II loop filter with $\alpha = 0.5$ and $\beta = 0.0025$, a 20 MHz second-order IIR low-pass filter is added to filter high frequency quantization noise. The VCO produces phase noise with the levels listed in Table 4.1. This is required for the sigma-delta converter to function correctly. When no noise source is present in the system, the sigma-delta converter will exhibit limit-cycles and other nonlinear behavior since it only has its own quantization noise on the output.

In the LPTV model, an ideal noise-transfer function is used with a slope of respectively 20 dB/dec and 40 dB/dec for the first and second-order ADC for shaping the ADC noise. The quantizer quantization noise power is set to 1. The simulation and model results can be found in Figure 4.6.

From the Noise Transfer Function (NTF) of the ADC, an estimate of the in-band phase noise can be made. In Equation 3.31, it can be seen that the ADC quantization noise is mixed from frequencies around f_{ref} to baseband. The phase noise at 10 MHz is therefore the sum of the quantization noise at $f_{ref} + 10$ MHz and $f_{ref} - 10$ MHz. This is illustrated in Figure 4.7.

When it is assumed that the NTF equals one at $f_s/6$, an estimate of the phase noise can be made. The reference frequency and output frequency are respectively 25 MHz and 2.4 GHz in this simulation. This means that the NTF is approximately -21 dB and -27 dB at respectively 35 MHz and 15 MHz assuming a 20 dB/dec NTF. The quantization noise power is approximately $\frac{1}{f_{out}}$, such that the phase noise at 10 MHz is approximately -114 dBc/Hz for the first order sigma-delta ADC. This is approximately 2 dB lower than the value expected from the LPTV model and 6 dB lower than the simulated value. It is expected that that the quantizer gain is not exactly equal to one, such that the assumption that the NTF equals one at $f_s/6$ is not true. This method can however be used to give a coarse estimate.

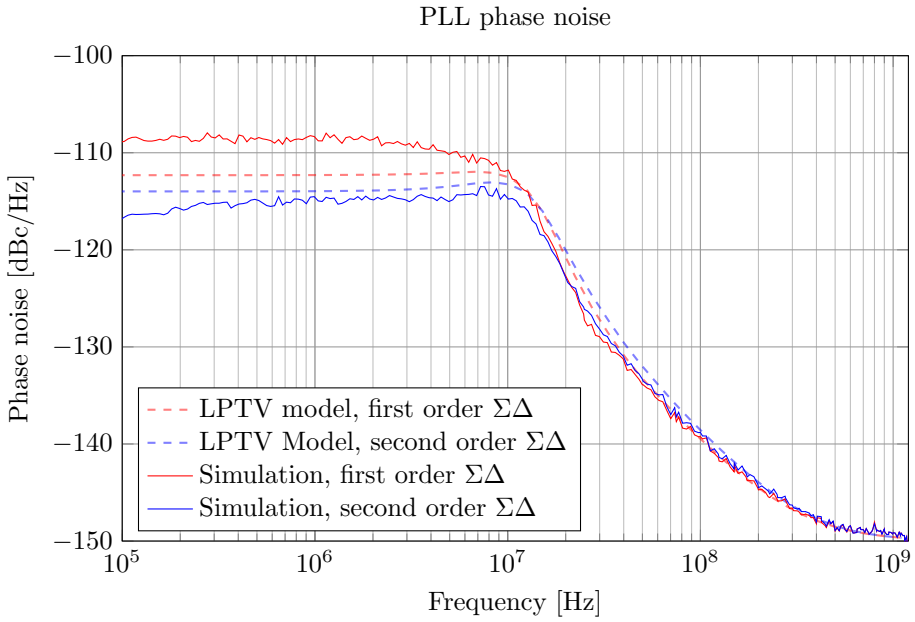

Figure 4.6: PLL phase noise with a noise shaping ADC

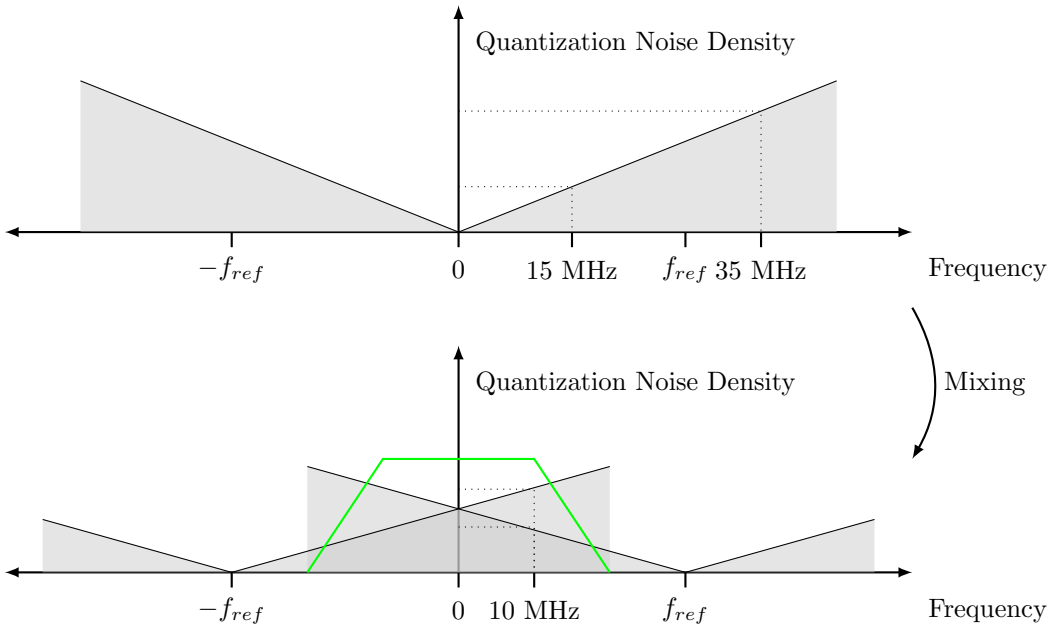

Figure 4.7: Frequency domain representation of the mixing of first-order sigma-delta quantization noise for $f_{ref} = 10$ MHz and a bandwidth of 10 MHz. The loop-filter is indicated in green.

There is a larger difference between model and simulation as in the previous simulations. For the second-order model, the phase noise level is slightly lower than expected by the LPTV model. It is expected that the quantization noise power is slightly lower than 1, such that less phase noise is produced than used in the model. The simulation result of the first-order ADC has more phase noise than the model. It is expected that this is due to nonlinear effects and that the quantizer gain is smaller than one, which are common effects in first-order sigma delta ADCs.

4.3 Limited Crystal Notch Depth

When the quality-factor of the crystal is not infinite, the depth of the notch is not zero. Therefore the reference 'carrier' is not completely suppressed and some residue of the reference 'carrier' is

left on the ADC input signal. Simulations are performed to assess the effect.

As explained in Section 3.2, the behavioral model of the notch filter is described as the subtraction of the reference carrier. A notch filter which does not fully suppress this carrier due to limited Q is simulated by only partially subtracting the reference carrier. Simulations are performed with a notch filter that only has a notch depth of 20 dB, such that 10% is left of the carrier is left.

In the LPTV model, the gain of the notch filter is set to 0.9 instead of 1.0, since the usable phase noise information is attenuated due to the limited 'carrier' suppression. A type-II PLL with only VCO phase noise is used for this analysis. This PLL is similar to the configuration used for analyzing the VCO phase noise in Figure 4.4. The simulation and model results can be found in Figure 4.8.

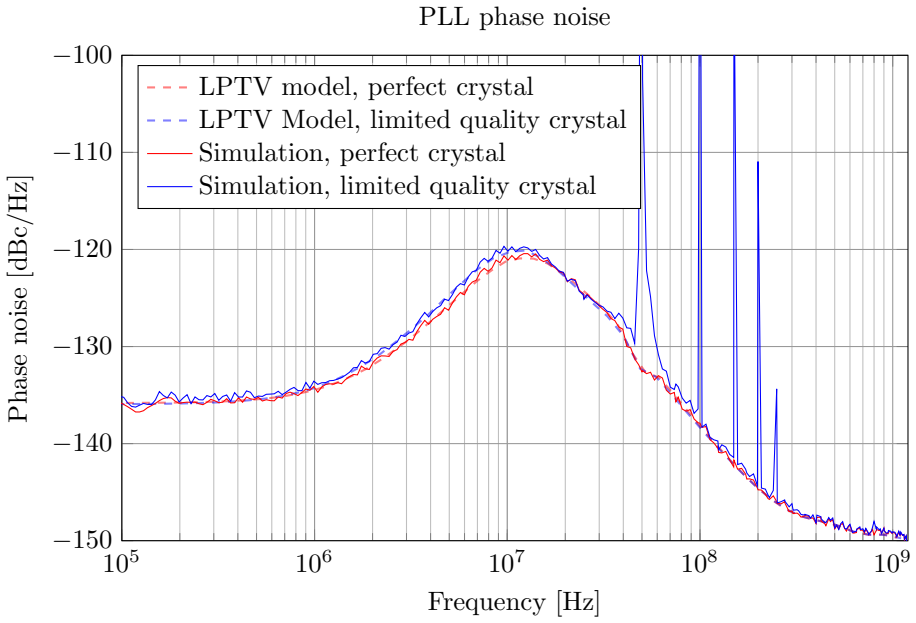

Figure 4.8: PLL phase noise with limited crystal quality-factor

The first thing that can be noticed is that large spurs are present at $2f_{ref}$ and harmonics. This is because the residue of the reference 'carrier' is mixed to DC and $2f_{ref}$. The spurs at multiples of $2f_{ref}$ are images that are introduced by multiple passes through the system. These spurs can be mitigated by placing a high-quality digital notch filter at $2f_{ref}$ in addition to the type-II loop filter.

Another effect that can be observed is that the loop bandwidth of the system with limited crystal quality is slightly smaller than the system with the perfect notch. This is due to the gain of 0.9 that is present in the PLL with limited notch quality. This attenuates the phase noise information, such that the loop-bandwidth is decreased. This can be compensated by adding gain in the loop-filter.

4.4 Enhanced Mixer

In this section, the effect of the enhanced mixer as described in Section 2.5 is analyzed. First simulations are done for determining the effect on VCO phase noise, next the effect on ADC quantization noise is analyzed.

VCO Phase Noise

The first set of simulations use a type-II loop-filter with the same specifications as in 4.1. Only the VCO produces phase noise, the ADC and DAC are noiseless. The simulation and model results can be found in Figure 4.9.

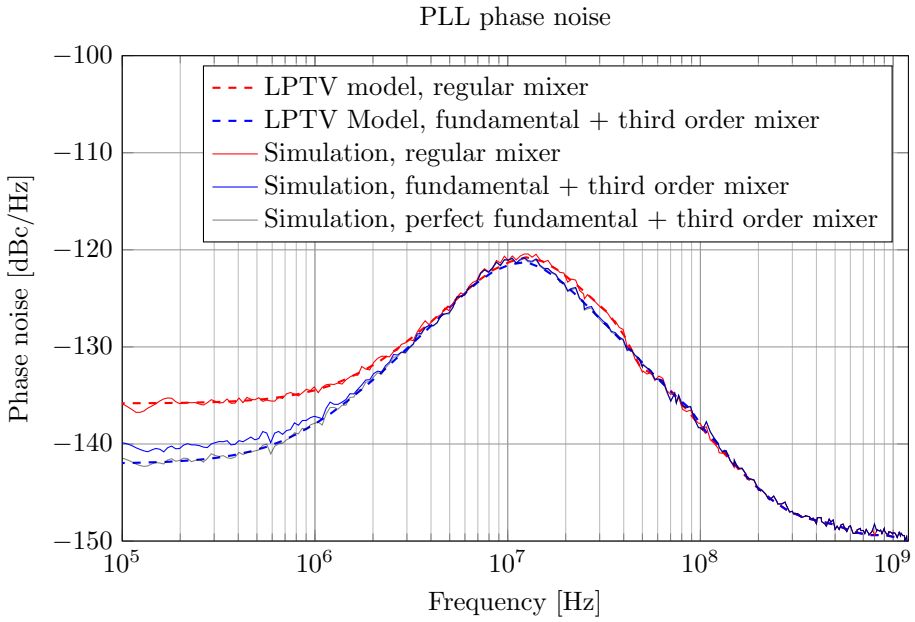

Figure 4.9: PLL phase noise with noisy VCO and different mixer signals

Two observations are made. The first is that the in-band noise around 100 kHz decreases. The LPTV model predicts a decrease of 6 dB. This can be explained by the fact that the mixer image is at $4f_{ref}$ for the enhanced mixer, instead of $2f_{ref}$ for the regular mixer. The phase noise at $4f_{ref}$ is 6 dB lower than the VCO phase noise at $2f_{ref}$, since the VCO $1/f^2$ phase noise has a 6 dB/octave slope.

The decrease in phase noise at 100 kHz is slightly less than 6 dB for the simulated system. It is expected that this is due to nonlinear effects. The derivation of the enhanced mixer signal assumed that the signals used for the mixer are perfect. In reality these contain the phase noise of the oscillator. A more exact description of the fundamental plus third harmonic of the reference generated by the NCO can be written as

$$s_{mix}(t) = s_{adc}(t) \cdot \left(\sin\left[\omega_{ref}t + \frac{1}{\mathrm{N}}\theta_{vco}(t)\right] + \sin\left[3\omega_{ref}t + \frac{3}{\mathrm{N}}\theta_{vco}(t)\right]\right). \tag{4.1}$$

The phase variations of the mixer signals lead to second order effect, such that the phase noise at $2f_{ref}$ is not completely canceled. It can be verified that perfect mixing signals do not have this effect. A simulation result with phase noise free mixer signals is added to Figure 4.9 in gray. This system however not be realized in reality, since in a normal system this exact time is not available.

The second observation that can be made is that the phase noise around $2f_{ref}$ slightly decreases when the enhanced mixer is used. The phase noise around $2f_{ref}$ is an image of the in-band phase noise, which is illustrated in Figure 2.6. For the enhanced mixer, this image is shifted to $4f_{ref}$. It cannot be observed in the simulation results since this contribution is too small.

ADC Quantization Noise

Next to the VCO phase noise, the effect of the enhanced mixer on ADC quantization noise is analyzed. A Nyquist ADC is used, where the quantization noise is modeled as additional Gaussian white noise. The ADC quantization step is set to 1 mV, $\alpha = 1.0$ and $\beta = 0.02$. The simulation and model results for a regular and a mixer with the fundamental and third order harmonic are shown in Figure 4.10.

It can be observed that the in-band quantization noise increases with 3 dB. This can be explained

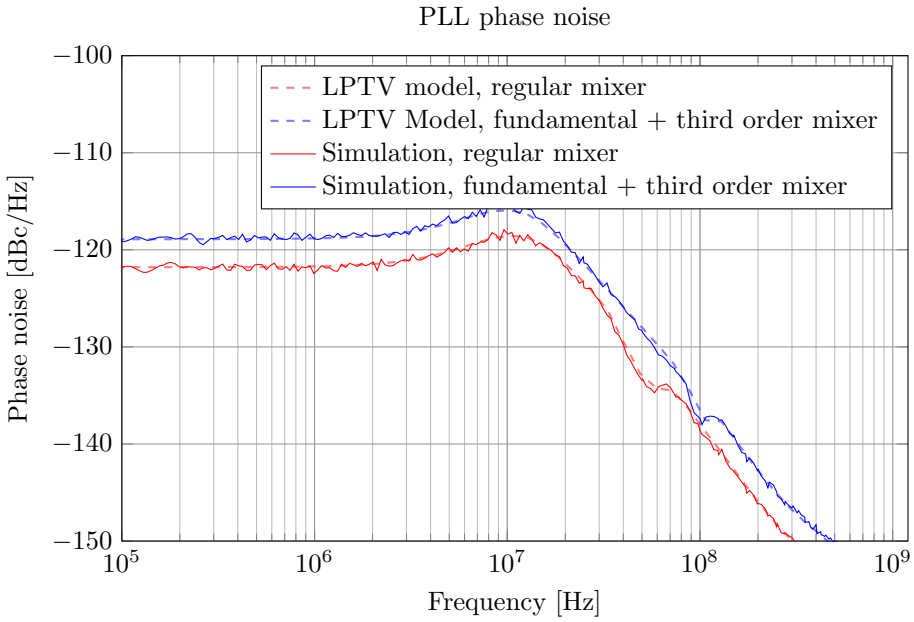

Figure 4.10: PLL phase noise with ADC quantization noise and different mixer signals

by the fact that ADC quantization noise is now mixed from frequencies around f_{ref} and $3f_{ref}$ into baseband. Since these values are uncorrelated, these add up as a 3 dB increase of in-band phase noise. This is a major disadvantage when a noise shaping ADC is used. The quantization noise power of an ideal first-order noise shaping ADC is 9.5 dB higher at $3f_{ref}$ compared to f_{ref}, such that the in-band quantization noise increases with approximately 10 dB when the enhanced mixer is used.

The image of the in-band phase noise is shifted from $2f_{ref}$ to $4f_{ref}$ when the enhanced mixer is used, which was also observed for the VCO phase noise.

4.5 Conclusions

From the analysis done in this chapter, a few conclusions can be drawn. The first conclusion is that the Crystal-Embedded Phase-Locked Loop architecture allows loop-bandwidths up to f_{ref} or beyond. This allows the use of noisy ring-oscillators as a VCO, which can lower the cost and area consumption of PLLs.

The quantization noise of the ADC in the system has a big impact on the phase noise performance of the system. It is amplified proportional to N^2, such that lower reference frequencies increase this effect. Noise-shaping can offer a way to decrease the quantization noise at low frequencies, such that a one-bit quantizer suffices. Another possibility is the use of a notch filter, such that the dynamic range requirement of the ADC can be decreased.

The enhanced mixer architecture can help to shift the phase noise image introduced by the mixer, but it also increases the demands of the ADC. This is especially true for a noise-shaping ADC, since high-frequency quantization noise is mixed in-band.

Chapter 5

Crystal Embedded Digital Phase-Locked Loop Design

In this chapter, a PLL is designed that can be used for a Bluetooth Low-Energy (BLE) radio. The design is based on the Crystal Embedded Digital Phase-Locked Loop, which is analyzed in the previous chapters.

In the first section, the PLL is described in more detail and some architectural choices are made. Next, some fundamental limitations are analyzed. Then the requirements of the PLL are set-up from the BLE specifications and a design is proposed. In the last sections, the design is verified using simulation and conclusions are drawn.

5.1 System Overview

As explained in Section 2.4, one of the most critical parts of the proposed digital PLL is the ADC. It has to convert a large reference signal with a great accuracy in order to accurately measure the oscillators phase error. The Crystal-Embedded PLL incorporates a DAC and notch filter to suppress the large signal carrier and relax the ADC requirements.

In order to minimize the phase noise contribution of the ADC, the quantization noise around the reference frequency must be low. This quantization noise is mixed down to low frequencies by the mixer, where it appears as phase noise. This is shown in Section 3.4, where an analytic expressions are derived for the in-band phase noise.

There are different ways to minimize the quantization noise of an ADC. Firstly, low quantization noise can be achieved by oversampling the signal. This way, the quantization noise is spread over a broader frequency range, which decreases the quantization noise in the band of interest. Another method is noise-shaping, which is a method to push the quantization noise to higher frequencies, out of the frequency band of interest.

Since the band of interest is of relatively low frequency with respect to the frequency of the VCO, these techniques can help to design an ADC for the system. In order to include noise shaping in the Crystal-Embedded PLL, some minor changes are made. A new system diagram of the DAC, notch filter and ADC can be found in Figure 5.1.

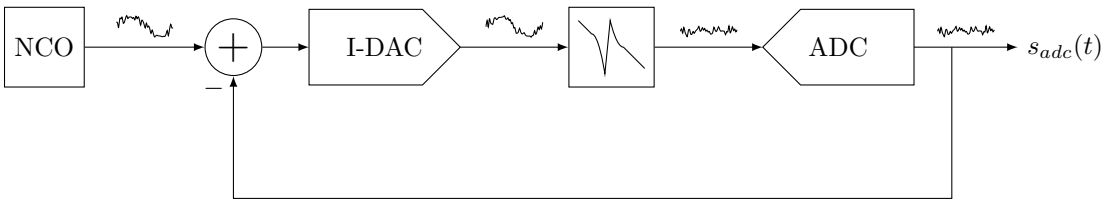

Figure 5.1: Noise shaping in the Crystal Embedded PLL

The first change with respect to the original system is that the DAC is replaced with a Current-steering DAC (I-DAC), whose output is a current instead of a voltage. The second change is that the notch filter is implemented as a crystal resonator. An equivalent circuit diagram is shown in Figure 5.2. For most frequencies, the impedance of the crystal is capacitive, determined by the parallel capacitance C_0. At the series resonance frequency, determined by C_1 and L_1, the crystal is a real impedance given by R_1. Close near the series resonance, the crystal is in parallel resonance where the impedance is very high. This point is determined by the parallel resonance of C_1, C_2 and L_1.

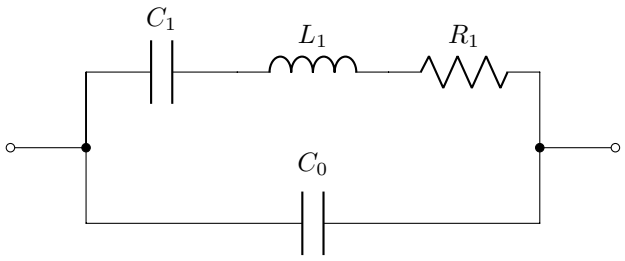

Figure 5.2: Equivalent circuit of a crystal resonator

Together with the current-output of the DAC, this crystal acts as an integrator for most frequencies. At the series resonance, the crystal acts as a filter to suppress the reference 'carrier' coming from the NCO. The ADC digitizes the voltage on the crystal and this voltage is feed-back using the DAC to close the noise-shaping loop.

5.2 ADC Modeling

In this section, the behavior of the noise-shaping ADC is modeled. The model is used in the next sections to make the design choices for a Bluetooth Low-Energy radio. First a crystal is characterized using measurements. From these measurements, a model of the crystal is made. Next, the noise transfer function (NTF) and signal transfer function (STF) of the noise-shaping ADC are derived. Finally, quality of the notch filter is determined from the STF.

Crystal Characterization

A crystal resonator can be modeled as a series RLC circuit. The equivalent circuit is shown in Figure 5.2. In order to characterize the crystal and use a proper model in simulations, a 20 MHz crystal is measured using the Keysight E5061B impedance analyzer. The measurement result can be found in Figure 5.3. By fitting the lumped element model of Figure 5.2, the values of R_1, L_1, C_1 and C_0 are determined. The approximate values of these elements are listed in Table 5.1.

R_1	5.8 Ω
L_1	4.03 mH
C_1	15.7 fF
C_0	5.31 pF

Table 5.1: Element values for the crystal model

From the measurement results, the series resonance frequency can be determined. This value is 19.99 MHz. The quality factor can be calculated using the lumped element values and is equal to

$$Q = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} = 8.5 \cdot 10^4. \tag{5.1}$$

This value is in-line with the usual quality factor of crystal resonators, which is in the order of $1 \cdot 10^5$. In Figure 5.3, it can be seen that the crystals response containes multiple spurious modes.

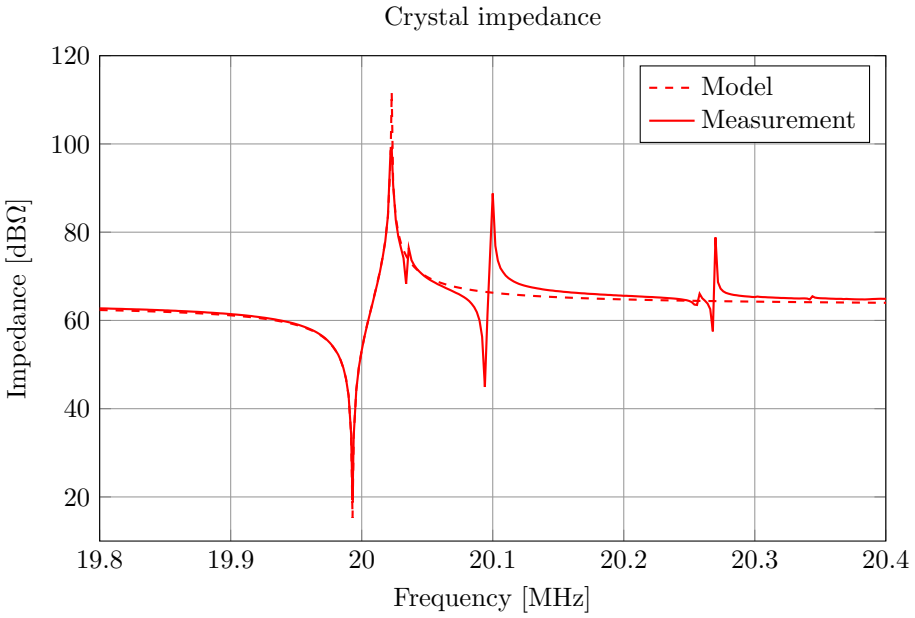

Figure 5.3: Measured and modeled crystal impedance

The most prominent spurious tones are at approximately 20.09 MHz and 20.27 MHz. Besides these spurious tones, odd harmonics of the fundamental resonance are present, which are not visible in this measurement. These extra tones can be added to the model using extra parallel RLC branches. In this research, the effect of these tones is neglected to reduce the complexity of the system. Analysis of the effect of these tones on the system is left for further research.

Another assumption that is made is that the parallel capacitance behaves capacitive for high frequencies around the sample frequency. Since the crystal is connected off-chip, the crystal is expected to show inductive behavior at high frequencies due to the interconnect wiring. This effect is not taken into account. In a real design, this effect can be mitigated by placing an extra on-chip capacitor parallel to the crystal if needed.

Linearized Transfer Functions

A block diagram of the noise shaping ADC can be found in Figure 5.4. Two transfer functions can be distinguished, the signal transfer function (STF) from $s_{in}(t)$ to $s_{out}(t)$ and the noise transfer function (NTF) from the ADC quantization noise $s_{n,q}(t)$ to the output $s_{out}(t)$.

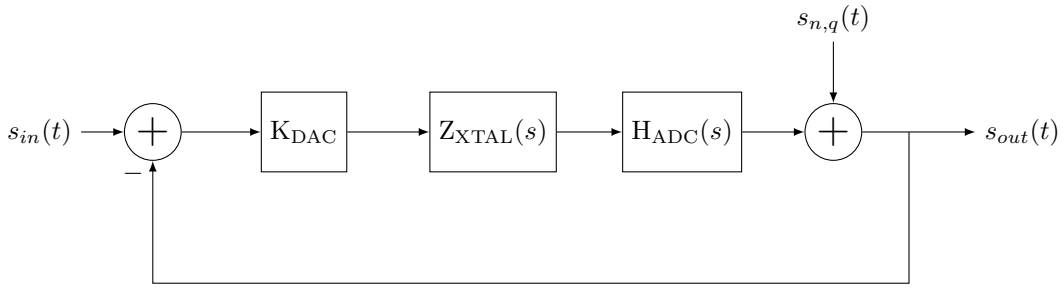

Figure 5.4: Block diagram of the ADC

The I-DAC is modeled as a linear gain with a gain K_{DAC}. It is assumed that the DAC has a gain that is constant over frequency. Since the output of the DAC is a current, the unit of the gain is [1/A]. The ADC is also modeled as a linear gain. When an one-bit quantizer is used, the gain will settle at a value such that the NTF is approximately one at $f_s/6$. For a multi-bit quantizer, the gain is equal to the linearized input-output relation.

The impedance of the crystal is represented as $Z_{XTAL}(s)$. The impedance is modeled using the lumped element model shown in Figure 5.2. Using MATLAB, the closed loop NTF and STF responses are determined. These can be found in Figure 5.5.

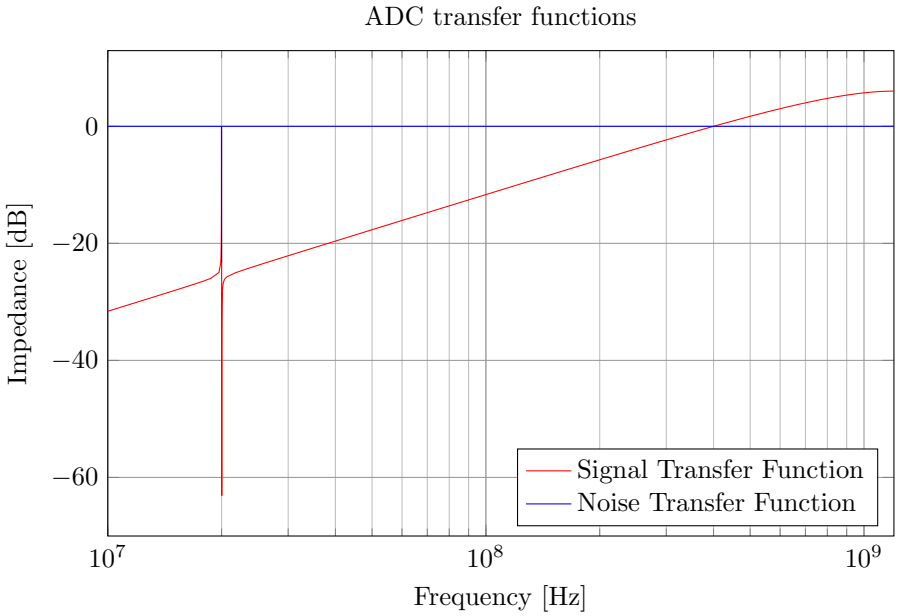

Figure 5.5: STF and NTF of the noise shaping ADC

It can be seen that the NTF is 0 dB at $f_s/6$, which is 400 Mhz. The NTF has a slope of 20 dB/dec. The STF is 0 dB. In Figure 5.6, a zoom-in is shown around the reference frequency. It can be seen that the STF has a notch at the series resonance of the crystal. The NTF increases at series resonance. This is the case because the crystal does not behave as an integrator at series resonance, which degrades the NTF. At parallel resonance, the impedance of the crystal is very high, which creates a notch in the NTF. In the next subsection, the deepness of the Notch is determined.

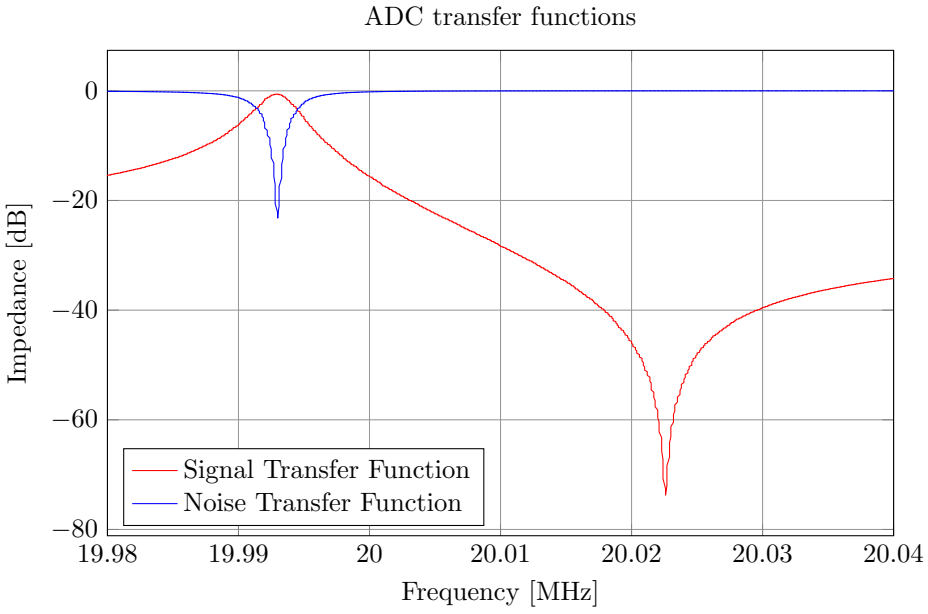

Figure 5.6: Zoomed STF and NTF of the noise shaping ADC

Notch Quality

The deepness of the notch filter in the STF can be estimated using the lumped element values in Table 5.1. The value of the capacitor C_0 is approximately 5.31 pF. The value of the resistor R_1 is approximately 5.8 Ω. In the case of an one-bit, first order sigma-delta ADC, the gain of the comparator stabilizes to a value such that the open loop gain is approximately 1 at $f_s/6$.

The impedance of the crystal at $f_s/6$ is primarily determined by the value of parallel capacitance C_0. At series resonance, the impedance is primarily determined by R_1. When the gain of the DAC and ADC are frequency independent, the ratio between the impedance of C_0 at $f_s/6$ and R_1 determine the deepness of the notch. This is illustrated in Figure 5.7. This ratio is

$$A_{notch} = \frac{R}{\left|\frac{6}{j2\pi f_s C_0}\right|} = \frac{2\pi R C_0 f_s}{6}. \tag{5.2}$$

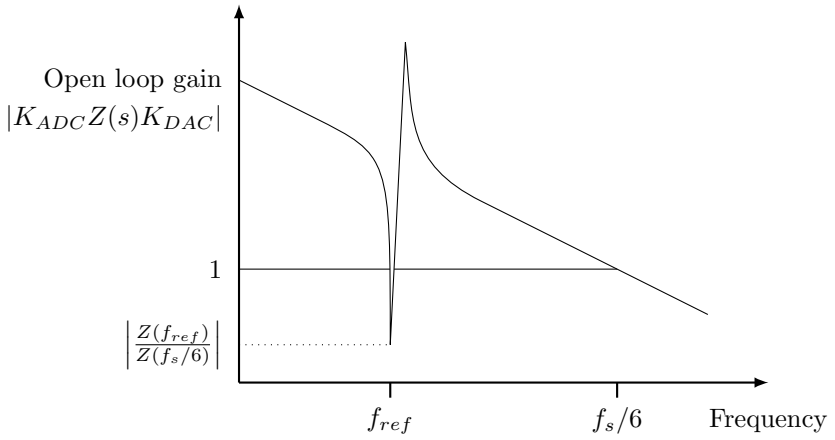

Figure 5.7: Illustration of the open loop gain of the noise shaping ADC and the corresponding STF. The notch depth is illustrated

For the characterized crystal, the maximum notch depth is approximately 22 dB when f_s is 2.4 GHz. When the sample frequency is lowered, the quality of the notch can be increased. Halving the sample frequency improves the notch by 6 dB. The noise performance of the first order ADC will however degrade by 9 dB, such that the net loss in the dynamic range of the ADC is 3 dB.

5.3 Bluetooth Low Energy Specifications

The phase noise performance of a PLL is important for a receivers performance. The output of the PLL is often used for a mixer to down-convert a receiver signal. When strong interferer are present, this interferer is partially mixed into the wanted channel due to the oscillators phase noise.

The Bluetooth Low-Energy (BLE) specification does not include a specification for the PLL phase noise, but these can be derived from the maximum interference levels. The Bluetooth specifications listed in the book of Masuch [12] are used.

The required Carrier-to-Interference (CIR) levels are listed in the second column of Table 5.2. The CIR is defined as the ratio of the average power in the wanted frequency channel to the average power in the interfering channel. The bandwidth of a Bluetooth channel is 1 MHz. It can be seen that the maximum allowable interference level becomes larger for higher offsets.

The minimum Signal-to-Noise Ratio (SNR) of the baseband signal of a BLE receiver must be 11 dB in order to achieve the required Bit Error Rate (BER) of 0.1. Since the PLL phase noise is not the only source of noise, a margin is taken in these calculations, such that the required SNR is set to 15 dB.

Offset [MHz]	CIR [dB]	Phase noise [dBc/Hz]
0	N/A	-75
1	15	-60
2	-17	-92
≥3	-27	-102

Table 5.2: Carrier-to-Interference Ratios for Bluetooth Low Energy and the resulting phase noise requirements

In order to achieve this SNR, the maximum phase noise levels can be calculated. It is assumed that the phase noise density is constant over the respective band. The average maximum allowable phase noise can be calculated using the following equation:

$$\mathcal{L}(\Delta f) = -\text{SNR} + \text{CIR}(\Delta f) - 10\log(\text{BW}) \tag{5.3}$$

These values are listed in the third column of Table 5.2. A graphical representation of the required phase noise levels can be found in Figure 5.8.

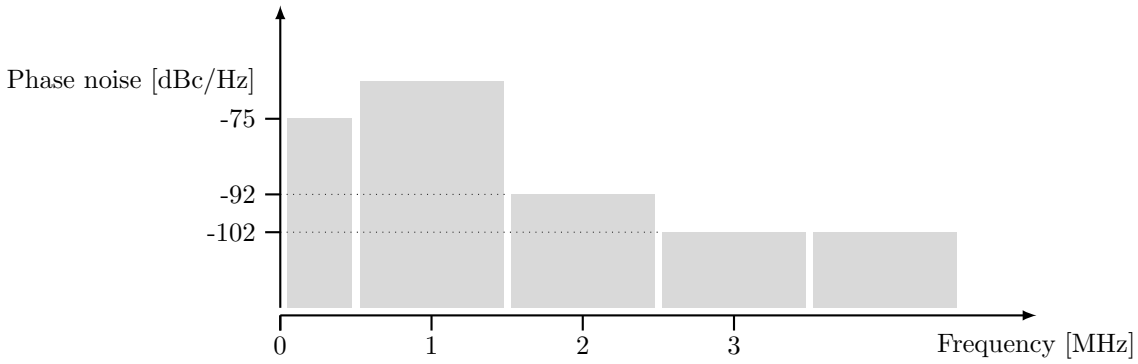

Figure 5.8: PLL phase noise requirement

5.4 Design

From the PLL requirements the loop bandwidth, oscillator requirements and ADC quantization noise can be determined. The PLL will be built around a ring oscillator, which consumes a small area compared to an LC-oscillator. A comparable large-bandwidth PLL with ring-oscillator for BLE is presented in [8]. The ring-oscillator in that PLL has -80 dBc/Hz of $1/f^2$ phase noise at 100 kHz. In the PLL that is designed in this work, a ring oscillator with 10 dB more phase noise is assumed, such that the $1/f^2$ phase noise is -70 dBc/Hz at 100 kHz. A high PLL bandwidth is required to achieve the BLE specifications.

The phase noise of the oscillator falls down with 20 dB/dec in the $1/f^2$ region. The loop bandwidth of the PLL must be at least 4 MHz in order to achieve an in-band phase noise level of -102 dB/Hz, which is required by the specification for frequencies larger then 2.5 MHz. In order to have some margin, it chosen to set the loop bandwidth to 10 MHz. The resulting in-band phase noise due to the VCO is approximately -110 dBc/Hz.

A crystal with a frequency of 20 MHz is used as reference. This is the same crystal as characterized in Section 5.2. This means that the loop-bandwidth is half the reference frequency, which is not presented in literature for a type-II PLL. The sample frequency for the ADC is set to 2.4 GHz, equal to the output frequency of the VCO. According to Equation 5.2, this means that a maximum reference 'carrier' attenuation of 22 dB can be achieved.

The amplitude of the NCO signal that is send to the DAC is chosen to be 5.0. This means that the residual amplitude of the reference 'carrier' is approximately 400 mV. This is small enough to make sure that the first-order sigma delta ADC does not saturate. The large signal amplitude helps in achieving good phase noise performance, as the signal-to-quantization-noise ratio is improved by $20 \log 5 = 14$ dB.

A type-II loop filter is chosen, such that no steady-state phase error exist and low-frequency phase noise is attenuated with 40 dB/dec. In order to filter the high frequency quantization noise, a second-order IIR low-pass filter is added. The cut-off frequency of this filter is set to 30 MHz. Another second order notch filter with high quality factor is added to filter reference image at 40 MHz. The value of α can be calculated using Equation 3.32. For a 10 MHz bandwidth, it has to be 0.2. The value of β is set to $4.0 \cdot 10^{-4}$ to allow enough phase margin. This is done experimentally using the LPTV model.

The last design choice that has to be made is whether an one-bit or a multi-bit quantizer is used in the sigma-delta ADC. Using Equation 3.33, an approximation of the ADC quantization noise requirement can be made. K_{DAC} is set to 5.0 to take the large amplitude of the NCO into account.

The phase noise at 10 MHz is determined by the sum of the quantization noise power at 10 MHz and 30 MHz, as explained in Figure 4.7. For a noise-shaping ADC, the largest contribution is the quantization noise at 30 MHz. It is assumed that the quantization noise at 10 MHz can be neglected, since it is approximately 10 dB lower. The factor 2 in Equation 3.31 can be ignored, since it accounts for the quantization noise image. The in-band phase noise must be lower than -102 dBc/Hz. A 3 dB margin is taken to allow other contributors. In order to achieve -105 dBc/Hz phase noise at 10 MHz, the quantization noise power at 30 MHz must be lower than

$$\begin{aligned} S_{nn,q}(30\text{ MHz}) &= \mathcal{L}(10\text{ MHz}) - 20\log\left(\frac{N}{\mathrm{K_{ADC}K_{DAC}}}\right) \\ &= -105 - 20\log\frac{2.4\mathrm{GHz}}{20\mathrm{MHz}} - 14 = -133\mathrm{dB/Hz} \end{aligned} \tag{5.4}$$

The NTF is equal to approximately -22.5 dB at 30 MHz for $f_s = 2.4$ GHz. Therefore the quantization noise power must be lower than -110 dB/Hz. This corresponds to a quantization step (Δ) of maximum 500 mV. It is chosen to take a multi-bit quantizer with a quantization step of 400 mV. A single-bit quantizer does not meet specification since the quantization noise power is approximately -94 dB/Hz.

The DAC has a larger quantization noise requirement than the quantizer. In order to have -110 dBc/Hz in-band phase noise due to the DAC, the quantization noise power of the DAC must be -140.6 dB/Hz around 20 MHz. This corresponds to a quantization step of approximately 14 mV with a $\pm$ 5.0 V output at a sample frequency of 2.4 GHz, which is 9.5-bits when a Nyquist architecture is used. This corresponds to an SNR of 81.5 dB over a 20 MHz bandwidth between 10 and 30 MHz. Possibly a lower resolution DAC can be used when the DAC's input signal can be noise-shaped. These fictive voltages have to be scaled to a current, since a current-steering DAC has to be used. The scaling factor is dependent on the thermal noise of the DAC.

5.5 Simulation Results

In this section the system is simulated and the results are discussed. The first simulation that is performed simulates the system with the parameters mentioned above. A phase noise plot is shown in Figure 5.9. The expected phase noise from the model is included in this diagram, including the contributions of individual system parts.

Both the LPTV model and the simulation have less phase noise density than the minimum of -102 dBc/Hz required for a BLE receiver. The simulated PLL has approximately -105 dBc/Hz phase noise. The simulated phase noise is within approximately 4 dB of the result from the LPTV model.

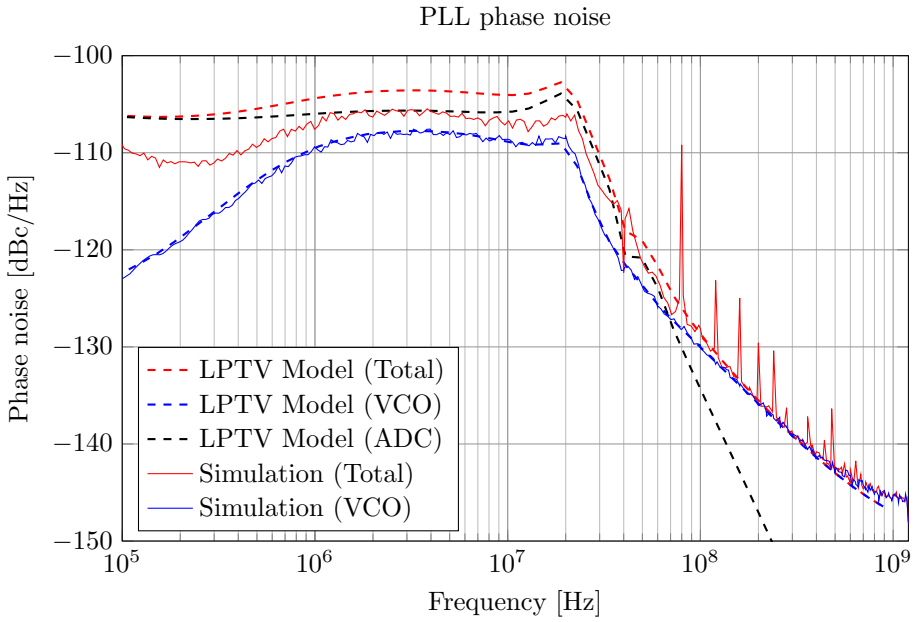

Figure 5.9: Crystal Embedded PLL with 400 mV quantization step

For in-band frequencies, the phase noise is lower than expected. For frequencies out of the PLL bandwidth, the simulation and model are approximately the same. The most notable difference is the presence of spurs at even multiples of 40 MHz.

An additional simulation is carried out where the quantizer is replaced with a linear gain. This simulation is added to Figure 5.9 under the label 'Simulation (VCO)'. It can be seen that the output phase noise now closely corresponds to the modeled VCO contribution. The spurs are not present now. Therefore it is expected that the differences between model and simulations in the full system are mainly due to second-order and nonlinear behavior of the ADC.

The difference for high frequencies is mainly the existence of spurs at even multiples of 40 MHz. At 40 MHz, no spur is present thanks to the digital IIR notch filter. The spur at 80 MHz has a power less than -100 dBc. It is expected that these spurs are due to nonlinearities in the ADC, since they are not present in simulation when an ideal quantizer is used. Third-order nonlinearity in the ADC for example produces a 60 MHz harmonic from the reference residue at 20 MHz. This harmonic is mixed to a spur at 80 MHz by the mixer.

The in-band phase error is approximately 4 dB lower than expected. There are multiple possible explanations for this. One option could be that the quantization noise power is lower than the RMS estimate of $\Delta^2/12$.

Another possible explanation is that the loop exhibits second order noise shaping behavior for low frequencies. At first sight, the only discrete-time integrator in the system is the crystal in combination with the I-DAC, but the VCO and the type-II loop filter also act as integrators. Low frequency quantization noise coming from the ADC can take this path, back to the input of the ADC, such that it is possible that this quantization noise achieves additional suppression. In order to verify and fully understand this behavior, more advanced models have to be built.

Fractional-N Effects

In addition to the integer-N simulation, a fractional-N configuration is tested. As noted in the crystal characterization done in Section 5.2, the crystals series resonance frequency is not exactly 20 MHz but approximately 19.99 MHz. In order to get an output frequency of exactly 2.4 GHz, the value of N has to be adjusted to approximately 120.042. The simulated phase noise of the PLL is shown in Figure 5.10.

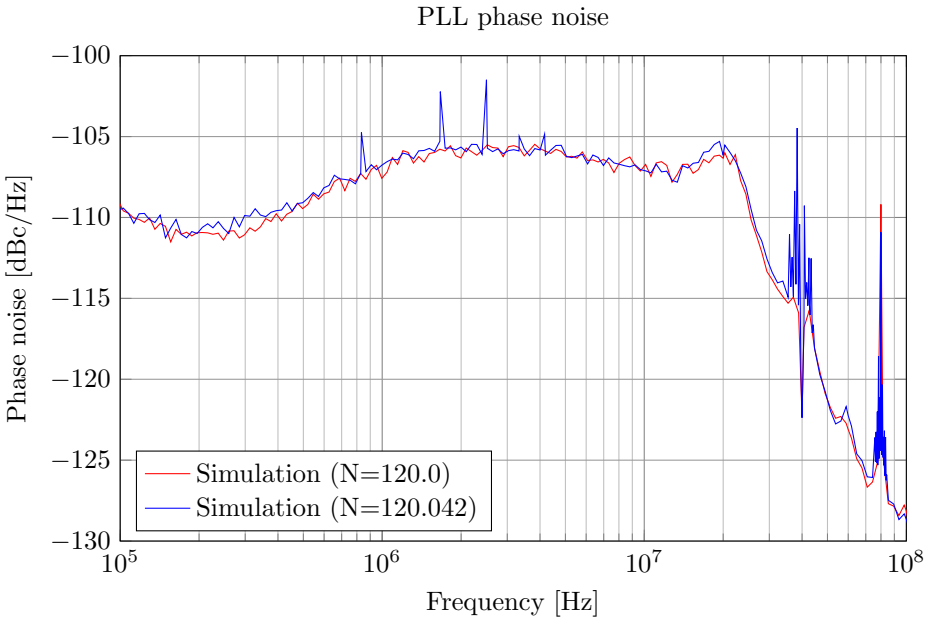

Figure 5.10: Crystal Embedded PLL, fractional-N and integer-N comparison

The fractional spurs are present at multiples of 830 MHz. This is at the place as expected, as fractional spurs are normally found at

$$f_{spur} = n \cdot (N - \text{round}(N)) \cdot f_{ref} \tag{5.5}$$

The same spurs are also present around $2f_{ref}$ and $4f_{ref}$. The energy in the largest spur is approximately -100 dBc. Fractional spurs are generally arising when periodic errors are made. No spurs are expected from the digital part of the PLL, since it uses double precision floating point numbers to represent internal signals and the NCO produces more-or-less ideal signals using the VHDL sin and cos functions.

It is therefore expected that the spurs are coming from the ADC. This is verified by simulating the system using an ideal quantizer with very small quantization step. With this configuration, no fractional spurs are present. In another experiment, a small random noise signal (with an RMS value of 0.05Δ) is added to the quantizer input. This also makes the fractional spurs disappear. Therefore it is expected that the fractional spurs are originating from the periodic repetition of quantization errors. Since a real design incorporates comparator noise and other forms of electrical noise in the sigma-delta loop, it is expected that this mechanism does not introduce reference spurs.

It is theoretically possible to design a fractional-N PLL without significant fractional spurs, but great care must be taken in the design because small periodicity in rounding or quantization errors can already produce spurs. This is also expected to happen when less accurate integer or fixed-point numbers are used for the digital signals. Techniques like dithering and noise-shaping can be used to break the periodicity in these errors and reduce the level of the spurs.

Close-In Phase Noise

Two additional simulations have been carried out, one with the 400 mV quantizer as described above and one with a 200 mV quantizer. The PLL is simulated for a long time (100 ms), such that close-in phase noise can be estimated. The result of these simulations are shown in Figure 5.11.

It can be seen that the phase noise and spur levels are smaller for the PLL with smaller quantizer step, as expected. For the ADC with 200 mV quantizer, the phase noise performance is mainly determined by the VCOs contribution. Besides this, it can be seen that the phase noise rises for

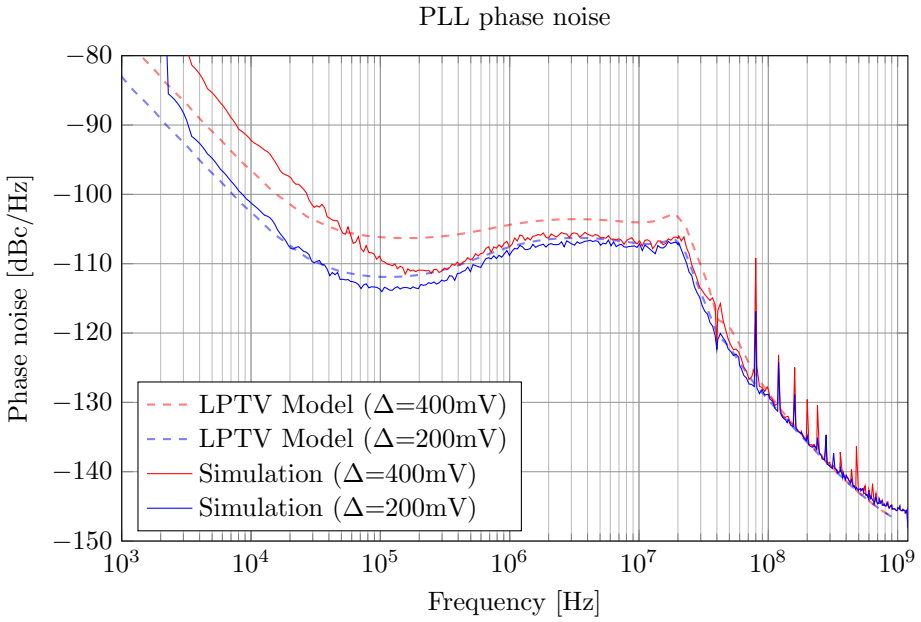

Figure 5.11: Crystal Embedded PLL, comparison of 200 mV and 400 mV quantizer

low frequency offsets. This has two reasons. The first is that the NTF equals almost one at series resonance, as shown in Section 5.2. This results in additional phase noise at low offset frequencies.

The second reason is that the STF of the ADC has a notch filter characteristic. The quantization noise at these frequencies is amplified by the loop. This is illustrated in the simplified system diagram in Figure 5.12. The quantization noise is boosted by the large gain of the VCO. For most frequencies, this quantization noise is fed-back using the ADC, such that the gain from the quantization noise to the output is limited. At the frequencies where the STF behaves as a notch filter, the quantization noise is amplified.

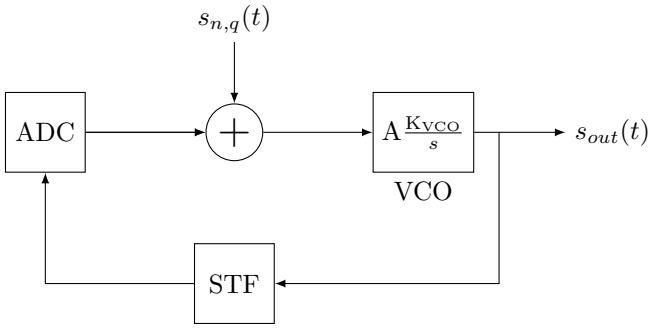

Figure 5.12: Approximate loop for quantiation noise

Non-ideal DAC

As a last step in the system's verification, the DAC is implemented as a real discrete level quantizer. In simulation, the DAC's output values are rounded to the nearest quantization level. A quantization step of 0.014 is used at a full-range of 5.0, as described in the last part of Section 5.4. A Gaussian distributed noise signal with a RMS power of 0.05 LSB is added to the signal before the quantizer, which acts as a dithering signal. For the rest of the system, the same configuration is used as used for the results in Figure 5.9.

The results from simulation and model can be found in Figure 5.13. It can be seen that the performance degradation due to the non-ideal DAC is minimal with respect to the system with ideal DAC. In-band the phase noise is increased by approximately 2 dB to a maximum of -104

dBc/Hz. It is lower than expected from the LPTV model. This difference is expectedly due to interference between the NTF of the ADC and the feedback via the VCO, as described earlier in this results section.

At out-of-band frequencies, the phase noise performance is comparable. Only the reference spurs are slightly larger. It is expected that this is due periodic rounding errors in the DAC. These spurs can be suppressed by adding more dithering to the DAC input.

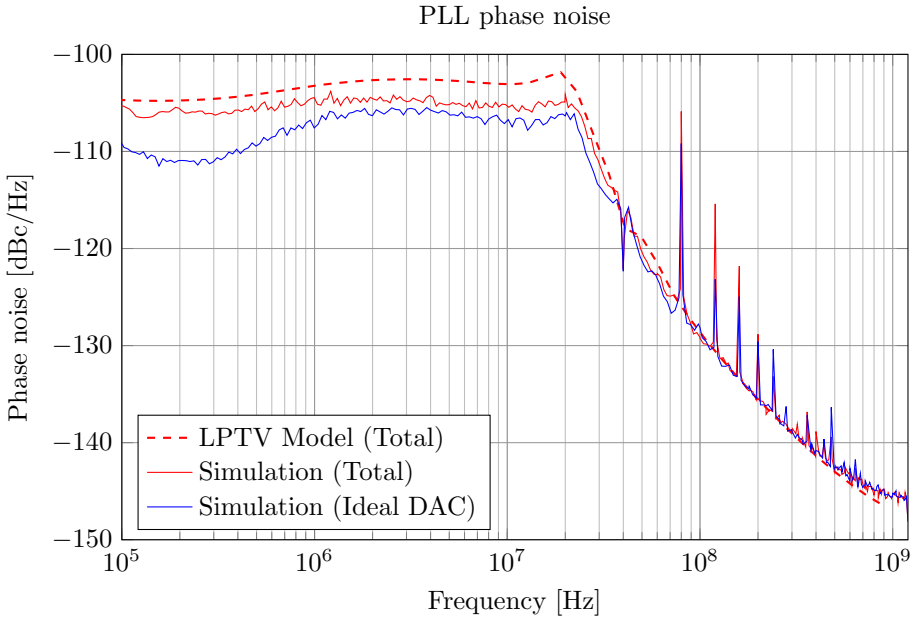

Figure 5.13: Crystal Embedded PLL with 400 mV quantization step and non-ideal DAC

5.6 Conclusions

A system-level design of a Phase-Locked Loop is presented that can serve as a frequency reference for Bluetooth Low-Energy transceivers. Discrete-level models are used for the DAC as well as for the ADC. WIth this configuration, the system has successfully met the phase noise requirements imposed by the BLE specifications. The in-band phase noise is less than -104 dBc/Hz and the largest reference spurs are smaller than -100 dBc. Fractional spurs are only minor, due to the digital nature of the PLL.

The architecture shows high close-in phase noise. This is a drawback of embedding the crystal in the sigma-delta loop of the ADC. When the phase noise is integrated over a complete channel, the phase noise is still lower than the BLE specification. Reference oscillator circuits will also exhibit much close-in phase noise, so the performance might be comparable to PLLs with a regular crystal oscillator as reference.

There is still much room for optimization. Firstly, the current design does all digital operations at the output frequencies. High-speed digital circuitry is required which is possibly difficult to implement. Besides this, the ADC and DAC are also clocked on this high sample rate. The feasibility of this high sample frequency must be researched, and when necessary, ways must be found to lower the sample frequency.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

In this thesis, a new Phase-Locked Loop architecture is presented with the potential of having a loop bandwidth nearing or even exceeding the reference frequency. This has a major advantage, since it allows the use of cheap, low-area ring-oscillators without compromising much on the PLL's phase noise performance.

In order to understand and characterize this PLL, a frequency-domain model is built based on Linear Periodically-Time Varying system theory. This model accurately describes the contribution of the system's most important noise sources to the output phase noise.

Besides the LPTV model, a discrete-event simulation environment is realized. Noise sources are modeled as stochastic sources and the simulation can also describe non-linear system effects. The model can be used to understand certain time-domain effects and to benchmark the validity and shortcomings of the LPTV model.

In the final chapter of this thesis, a PLL that can serve as a frequency reference for Bluetooth Low-Energy transceivers is designed on system-level. A high-phase-noise ring-oscillator is used as a basis. The bandwidth of the PLL is 10 MHz with a 20 MHz crystal reference. The in-band phase noise is below -104 dBc/Hz and the PLL allows almost spur-less fractional-N operation. This PLL successfully meets the phase noise requirements for a Bluetooth Low-Energy transceiver.

6.2 Recommendations for Further Research

There is still a lot of work to do before this PLL architecture can be turned into a transistor-level circuit and real measurements can be performed. In this section, a few recommendations are given.

The first recommendation is to make the basic system analysis more complete. The effect of spurious tones present in a crystal has for example not been researched. Besides this, the effect of settling and initial frequency locking has to be determined.

The PLL design for a Bluetooth Low-Energy radio can be worked out further to a transistor-level circuit. In order to do so, it must be researched if the system-level choices are realistic or if for example the sample frequency of the DAC and ADC has to be decreased. Also the possibility of creating a higher-order sigma-delta converter can be investigated.

If the in-band quantization noise has to be decreased for more demanding applications and the current architecture does not allow good enough quantization noise performance, another direction can be researched. A possible direction is to implement the mixer in the analog domain using digital, discrete-time techniques. This way, the phase noise information is mixed to base-band. Noise-shaping ADCs can be used more efficiently now since the relevant phase information is at much lower frequencies.

Appendix A

Linear Periodically Time-Varying Systems

In this appendix, a basic summary of LPTV system analysis techniques is given. The theory is based on the PLTV theory described in the book of Sansen, Gielen and Vanassche [13]. A short overview of the parts relevant for creation of the model for this PLL is given. It is tried to give an intuitive understanding, such that it can help to understand the effects that occur in the proposed PLL.

A.1 Harmonic Transfer Function

An LPTV system with input $x(t)$ and output $y(t)$ is shown in Figure A.1. LPTV systems respond to signals in a periodic manner. In order words, when the input $x(t)$ is delayed an integer number of periods T, the response $y(t)$ is, besides the delay, unaltered. Mathematically, this can be written as

$$y(t - nT) = H_{\text{LPTV}}\left[x(t - nT)\right] \ \forall \ t \in \mathbb{R}, n \in \mathbb{Z}. \tag{A.1}$$

Figure A.1: LPTV system

A consequence is that the impulse response of LPTV systems is time dependent. This is illustrated in Figure A.2. The time when the impulse is launched is $v = t - \tau$, and the time when the impulse is observed is t. Due to the periodic behavior of the system, the impulse response repeats itself in t with period T. The impulse response is therefore called the periodic impulse response.

Like for LTI systems, the output of the LPTV system can be written as a convolution of the input with the periodic impulse response. The output of the system is

$$y(t) = \int_0^\infty h(t, \tau)x(t - \tau)d\tau. \tag{A.2}$$

Since the periodic impulse response $h(t, \tau)$ is periodic in t, it can be written as a Fourier series. The Fourier representation is

$$h(t, \tau) = \sum_{n=-\infty}^{\infty} h_n(\tau)e^{jn\omega_0 t}, \tag{A.3}$$

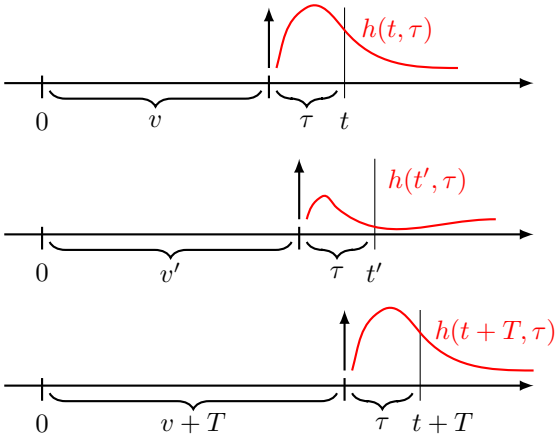

Figure A.2: Impulse response for an LPTV system at three different time instances

with coefficients

$$h_n(\tau) = \frac{1}{T}\int_0^T h(t,\tau)e^{-jn\omega_0 t}dt. \tag{A.4}$$

The fundamental frequency is $\omega_0 = 2\pi f_0 = \frac{2\pi}{T}$. Combining Equation A.2 with Equation A.3 and rewriting the exponentials gives the input-output relation

$$\begin{aligned} y(t) &= \int_0^\infty \sum_{n=-\infty}^{\infty} h_n(\tau)e^{jn\omega_0 t}\cdot x(t-\tau)d\tau \\ &= \sum_{n=-\infty}^{\infty}\int_0^\infty h_n(\tau)e^{jn\omega_0\tau}\cdot x(t-\tau)e^{jn\omega_0(t-\tau)}d\tau. \end{aligned} \tag{A.5}$$

Doing a Laplace transform gives the expression

$$Y(s) = \sum_{n=-\infty}^{\infty} H_n(s-jn\omega_0)X(s-jn\omega_0), \tag{A.6}$$

where $H_n(s)$ is the Harmonic Transfer Function. In Figure A.3, an graphical time-domain interpretation of this expression is given. The input signal $x(t)$ is led through an infinite number of LTI systems with transfer-function $H_n(s)$. The outputs of these systems are frequency translated and summed, resulting the output $y(t)$ of the system.

Equation A.6 can alternatively be expressed using matrices. If $X(s-jn\omega_0)$ is written as a vector $\mathbf{X}(s)$ with elements

$$X_n(s) = X(s+jn\omega_0), \tag{A.7}$$

and $Y(s-jn\omega_0)$ is written as $\mathbf{Y}(s)$ in similar way, then Equation A.6 becomes

$$\mathbf{Y}(s) = \widetilde{\mathbf{H}}(s)\mathbf{X}(s). \tag{A.8}$$

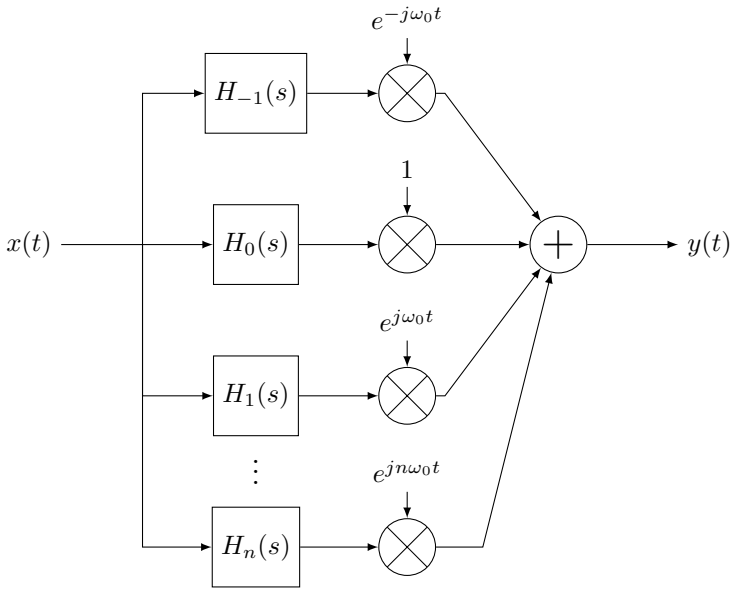

Figure A.3: LPTV system

The matrix $\widetilde{\mathbf{H}}(s)$ is called the Harmonic Transfer Matrix (HTM). The HTM is a doubly infinite matrix, and contains frequency shifted copies of the harmonic transfer function. It has the structure as shown in Equation A.9 with elements according to Equation A.10.

$$\widetilde{\mathbf{H}}(s) = \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & \widetilde{H}_{-1,-1}(s) & \widetilde{H}_{-1,0}(s) & \widetilde{H}_{-1,1}(s) & \cdots \\ \cdots & \widetilde{H}_{0,-1}(s) & \widetilde{H}_{0,0}(s) & \widetilde{H}_{0,1}(s) & \cdots \\ \cdots & \widetilde{H}_{1,-1}(s) & \widetilde{H}_{1,0}(s) & \widetilde{H}_{1,1}(s) & \cdots \\ \cdots & \widetilde{H}_{2,-1}(s) & \widetilde{H}_{2,0}(s) & \widetilde{H}_{2,1}(s) & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{A.9}$$

$$\widetilde{H}_{n,m}(s) = H_{n-m}(s + jm\omega_0). \tag{A.10}$$

$x(t)$ and $y(t)$ can alternatively be written in an sum of band-limited and frequency translated baseband signals $x_n(t)$ and $y_n(t)$. If the bandwidth of the baseband signals is $[-\omega_0/2, \omega_0/2]$, then $x(t)$ is equal to

$$x(t) = \sum_{n=-\infty}^{\infty} x_n(t) e^{jn\omega_0 t}. \tag{A.11}$$

The output $y(t)$ can be written in similar way. The Laplace transform of $x_n(t)$ is written as $X_n(s)$. Using Equation A.6 and the property that all the signals $X_n(s)$ are band limited to $(-\omega_0/2, \omega_0/2]$,

the output baseband signal $Y_n(s)$ can be calculated. This relation becomes

$$\begin{aligned} Y_n(s) &= Y(s + jn\omega_0) \\ &= \sum_{m=-\infty}^{\infty} H_m(s - j(m-n)\omega_0)X(s - j(m-n)\omega_0) \\ &= \sum_{m'=-\infty}^{\infty} H_{n-m'}(s + jm'\omega_0)X(s + jm'\omega_0) \\ &= \sum_{m'=-\infty}^{\infty} \widetilde{H}_{n,m'}(s)X_{m'}(s). \end{aligned} \tag{A.12}$$

Since $X_{m'}(s)$ is band-limited, the transfer $\widetilde{H}_{n,m'}(s)$ can also be band-limited. Rewriting this expression using matrices, again the expression in Equation A.8 is found. There are however advantages of this representation.

The most important advantage is that this notation gives an intuitive look at the mixing in the system. The element $H_{n,m}$ from the HTM describes the transfer from the m-th input frequency band to the n-th output frequency band. This is illustrated in Figure A.4. This way, the transfers between different frequency bands (mixing) can be analyzed individually.

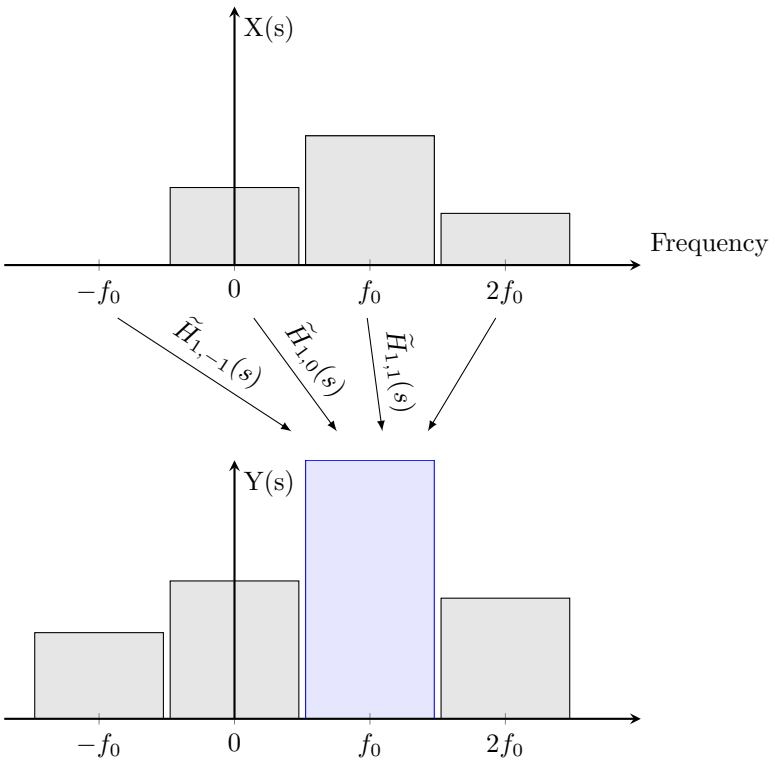

Figure A.4: Mixing in an LPTV system

Besides the intuitive look, the band-limited HTMs offer computational benefits when numerical approximations are done, since the Laplace operator s has to be evaluated only in the interval $(-j\omega_0/2, j\omega_0/2]$.

A.2 System Properties

In this section, different LPTV system and HTM properties are given that can be used for system analysis.

Series and Parallel

In Figure A.5, parallel and series connections of LPTV systems are shown. The input-output relations for these parallel and series connections become respectively

$$\mathbf{Y_P}(s) = \left(\widetilde{\mathbf{H}}_\mathbf{A}(s) + \widetilde{\mathbf{H}}_\mathbf{B}(s)\right)\mathbf{X}(s) \quad \text{and} \tag{A.13}$$

$$\mathbf{Y_S}(s) = \widetilde{\mathbf{H}}_\mathbf{B}(s)\widetilde{\mathbf{H}}_\mathbf{A}(s)\mathbf{X}(s). \tag{A.14}$$

Important is that the HTM multiplication used for the series connection in Equation A.14 is non-commutative. The order in which systems are placed does matter for LPTV system, contrary to LTI systems.

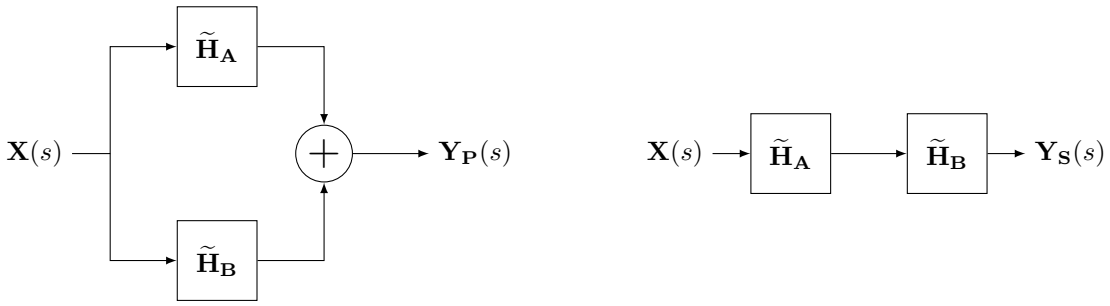

Figure A.5: LPTV series and parallel connections

LTI Systems

The HTM can be used to describe an LTI system. The impulse response of an LTI system is constant over time, which means that only $H_0(s)$ of the harmonic transfer function is nonzero. From Equation A.10, it can be observed that only the diagonal elements in the HTM are therefore nonzero. The HTM for an LTI system $H(s)$ is shown in Equation A.15.

$$\widetilde{\mathbf{H}}(s) = \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & H(s-j\omega_0) & 0 & 0 & \cdots \\ \cdots & 0 & H(s) & 0 & \cdots \\ \cdots & 0 & 0 & H(s+j\omega_0) & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{A.15}$$

Mixing

In Figure A.6, a system is shown that multiplies the input with a signal $s(t)$. This signal must be periodic in T to make it an LPTV system. When $s(t)$ is written as a Fourier series, the result becomes

$$s(t) = \sum_{n=-\infty}^{\infty} s_n e^{jn\omega_0 t}. \tag{A.16}$$

The periodic impulse response becomes

$$h(t,\tau) = s(t) \cdot \delta(t-\tau). \tag{A.17}$$

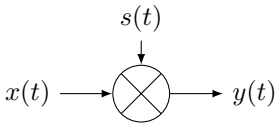

Figure A.6: LPTV system with a multiplier

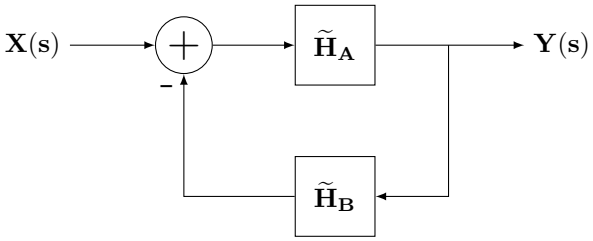

Figure A.7: LPTV feedback system

Using Equation A.4, it can be rewritten as

$$h_n(\tau) = s_n \delta(\tau). \tag{A.18}$$

Applying the Laplace transformation and applying Equation A.10 gives the HTM

$$\widetilde{\mathbf{H}}(s) = \begin{pmatrix} \ddots & \vdots & \vdots & \vdots & \\ \cdots & S_0 & S_{-1} & S_{-2} & \cdots \\ \cdots & S_1 & S_0 & S_{-1} & \cdots \\ \cdots & S_2 & S_1 & S_0 & \cdots \\ & \vdots & \vdots & \vdots & \ddots \end{pmatrix}. \tag{A.19}$$

Feedback

An feedback system is given in Figure A.7. The input-output relation is

$$\begin{aligned} \mathbf{Y}(s) &= \widetilde{\mathbf{H}}_{\mathbf{A}}(s)\mathbf{X}(\mathbf{s}) - \widetilde{\mathbf{H}}_{\mathbf{A}}(s)\widetilde{\mathbf{H}}_{\mathbf{B}}(s)\mathbf{Y}(\mathbf{s}) \\ &= \left(\mathbf{I} + \widetilde{\mathbf{G}}(s)\right)^{-1} \widetilde{\mathbf{H}}_{\mathbf{A}}(s)\mathbf{X}(\mathbf{s}), \end{aligned} \tag{A.20}$$

where

$$\widetilde{\mathbf{G}}(s) = \widetilde{\mathbf{H}}_{\mathbf{A}}(s)\widetilde{\mathbf{H}}_{\mathbf{B}}(s). \tag{A.21}$$

Equation A.20 requires the inversion of the HTM

$$\mathbf{I} + \widetilde{\mathbf{G}}(s). \tag{A.22}$$

Since an HTM is a doubly infinite matrix, it is impossible to calculate its inverse. There are different methods for solving this problem. The simples method is to just truncate the HTMs to finite size.

Another method is the rank-reduction approximation. This method assumes that the HTM can be approximated by its rows around $n = 0$. The other columns are set to zero, which results in a HTM with finite rank. The approximation can be made with the expression

$$\widetilde{\mathbf{H}}(s) \approx \mathbf{P}(\mathbf{P}^T\widetilde{\mathbf{H}}(s)), \tag{A.23}$$

where the matrix $\mathbf{P}$ has the structure

$$\mathbf{P} = \begin{pmatrix} \vdots & \vdots & \vdots \\ 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \\ \vdots & \vdots & \vdots \end{pmatrix}. \tag{A.24}$$

The number of columns is $N = 2R + 1$. Using Equation A.23, the feedback expression from Equation A.20 can be written as

$$\begin{aligned} \mathbf{Y}(s)\mathbf{X}^{-1}(s) &= \left(\mathbf{I} + \widetilde{\mathbf{G}}(s)\right)^{-1} \widetilde{\mathbf{H}}_{\mathbf{A}}(s) \\ &= \left(\mathbf{I} + \mathbf{P}(\mathbf{P}^T\widetilde{\mathbf{G}}(s))\right)^{-1} \mathbf{P}(\mathbf{P}^T\widetilde{\mathbf{H}}_{\mathbf{A}}(s)) \\ &= \left(\mathbf{I} + \mathbf{P}\mathbf{V}(s)^T\right)^{-1} \mathbf{P}\mathbf{V}_{\mathbf{in}}(s)^T. \end{aligned} \tag{A.25}$$

The matrices

$$\mathbf{V}(s)^T = \mathbf{P}^T\widetilde{\mathbf{G}}(s) \tag{A.26}$$

and

$$\mathbf{V}_{\mathbf{in}}(s)^T = \mathbf{P}^T\widetilde{\mathbf{H}}_{\mathbf{A}}(s) \tag{A.27}$$

are infinite matrices with N columns. The Sherman-Morisson-Woodbury formula states that

$$(\widetilde{\mathbf{Z}} + \mathbf{U}\mathbf{V}^T)^{-1} = \widetilde{\mathbf{Z}}^{-1} - \widetilde{\mathbf{Z}}^{-1}\mathbf{U}\left(\mathbf{I} + \mathbf{V}^T\widetilde{\mathbf{Z}}^{-1}\mathbf{U}\right)^{-1}\mathbf{V}^T\widetilde{\mathbf{Z}}^{-1}, \tag{A.28}$$

where $\widetilde{\mathbf{Z}}$ is a square invertible matrix and $\mathbf{U}$ and $\mathbf{V}$ have a limited number of columns N. Using

this formula in Equation A.25 gives

$$\begin{aligned}
\mathbf{Y}(s)\mathbf{X}^{-1}(s) &= \left(\mathbf{I}^{-1} - \mathbf{I}^{-1}\mathbf{P}\left(\mathbf{I} + \mathbf{V}(s)^T\mathbf{I}^{-1}\mathbf{P}\right)^{-1}\mathbf{V}(s)^T\mathbf{I}^{-1}\right)\mathbf{P}{\mathbf{V_{in}}}^T(s) \\
&= \mathbf{P}{\mathbf{V_{in}}}^T(s) - \mathbf{P}\left(\mathbf{I} + \mathbf{V}(s)^T\mathbf{P}\right)^{-1}\mathbf{V}(s)^T\mathbf{P}{\mathbf{V_{in}}}^T(s) \\
&= \mathbf{P}{\mathbf{V_{in}}}^T(s) - \mathbf{P}\left(\mathbf{I} + \mathbf{G_P}(s)\right)^{-1}\mathbf{G_P}(s){\mathbf{V_{in}}}^T(s) \\
&= \mathbf{P}\left(\mathbf{I} + \mathbf{G_P}(s)\right)^{-1}\left(\mathbf{I} + \mathbf{G_P}(s)\right){\mathbf{V_{in}}}^T(s) - \mathbf{P}\left(\mathbf{I} + \mathbf{G_P}(s)\right)^{-1}\mathbf{G_P}(s){\mathbf{V_{in}}}^T(s) \\
&= \mathbf{P}\left(\mathbf{I} + \mathbf{G_P}(s)\right)^{-1}\left({\mathbf{V_{in}}}^T(s) + \mathbf{G_P}(s){\mathbf{V_{in}}}^T(s)\right) - \mathbf{P}\left(\mathbf{I} + \mathbf{G_P}(s)\right)^{-1}\mathbf{G_P}(s){\mathbf{V_{in}}}^T(s) \\
&= \mathbf{P}\left(\mathbf{I} + \mathbf{G_P}(s)\right)^{-1}{\mathbf{V_{in}}}^T(s).
\end{aligned} \tag{A.29}$$

The matrix

$$\mathbf{G_P}(s) = \mathbf{V}(s)^T\mathbf{P} = \mathbf{P}^T\widetilde{\mathbf{G}}(s)\mathbf{P} \tag{A.30}$$

is an $N \times N$ square sub-matrix of $\widetilde{\mathbf{G}}(s)$. The inversion that has to be performed is of a $N \times N$ matrix.

Due to the approximations, there are no transfers to frequency bands beyond $R\omega_0$. Besides this, the approximation is only valid for frequencies where the approximation made in Equation A.23 is justified.

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