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Faculty of Electrical Engineering,
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ADC for Passive Mixer First Radio Receiver Architectures

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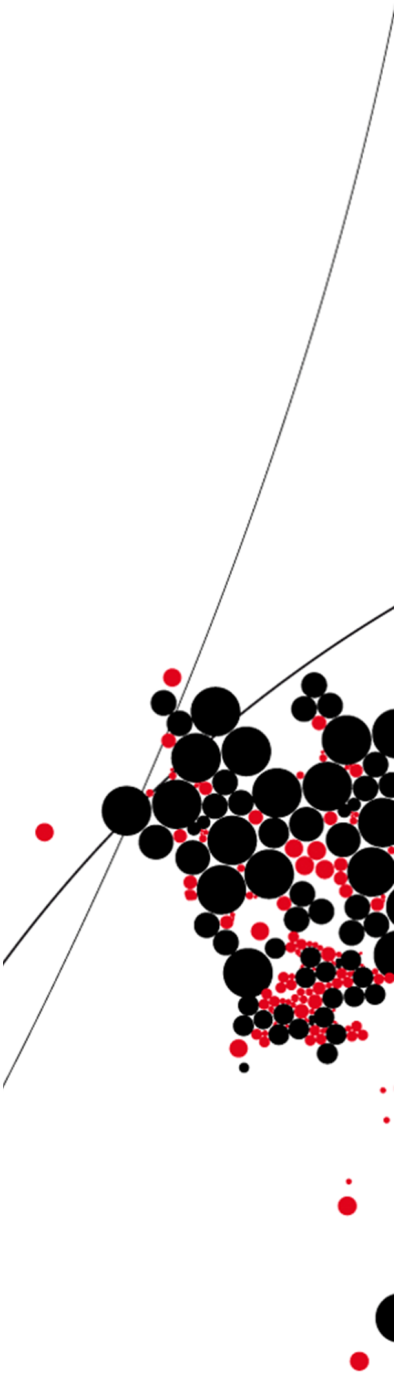

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Abbreviations

AAF anti-aliasing filter

ADC analog-to-digital converter

DAC digtigal-to-analog converter

DSP digital signal processing

ENOB effective number of bits

FDSOI fully-depleted silicon on insulator

FIR finite impulse response

GF22nm 22nm FDSOI technology (by GLOBAL FOUNDARIES)

IIR infinite impulse response

IoT internet of things

LNA low noise amplifier

LSB least significant bit

MSB most significant bit

NB-IoT narrow-band IoT

NS-SAR noise shaping SAR

NTF noise transfer function

OSR oversampling ratio

RF radio frequency

SAR successive approximation register

SINAD signal to noise and distortion ratio

SNR signal to noise ratio

STF signal transfer function

TT typical-typical (corner)

$\Sigma\Delta$ sigma-delta modulator

1 Abstract

In recent years the internet of things has been a growing field of interest. Low signal levels and a hostile environment with large interferers put tough requirements on the RF circuitry of IoT radio receivers. Not only is linearity a key point, the low signal levels seem to require significant amplification to be detected. A key question is whether this amplification is really that necessary. If an RF front end can achieve sufficiently high linearity and enough dynamic range on the part of the ADC one might be able to do without a lot of amplification. This thesis seeks to explore this notion.

Targeted is a mixer first architecture without active amplification in the receive chain. This relies on passive amplification provided by the mixer and high dynamic range at low signal levels in the ADC. For this project the mixer was provided, it being the UTPASS from the PhD research of V.K. Purushothaman.

For IoT applications battery life is critical, so circuitry should use little energy. In terms of energy consumption the SAR architecture is a logical choice for the ADC. SAR accuracy is limited by comparator noise, however. Added to is that the fact that signal levels are low, so the SAR ADC is likely not going to achieve the requirements. The noise shaping SAR may prove to be a solution to this problem. This architecture combines the energy efficiency of SAR and the noise shaping of $\Sigma\Delta$ modulators to achieve higher accuracies. An interesting property that will be explored in this work.

Goals of this thesis are twofold. Studying the feasibility of a fully passive mixer first receiver architecture with only a mixer and an ADC and exploring the possibilities and limitations of the noise shaping SAR ADC architecture.

2 Problem Definition

The internet of things (IoT) aims to connect many devices, sensors and other items to the internet. Typically, the devices are meant to be cheap standalone devices with long battery life. Naturally, the circuitry that is used for this type of wireless communication should be energy efficient and as a result, signal levels are typically low. The projec targets narrow-band IoT (NB-IoT), as part of a NB-IoT mixer first receiver with the UTPASS as mixer. The desire is to not only go for a mixer first architecture, but make it fully passive as well. There will be little gain and high linearity, which has implications for the ADC specifications, discussed in section 3. The ADC of this receiver is the focus of the research project.

2.1 Mixer first architecture

To elaborate on the choice of a mixer first architecture, the architecture is explained. Figure 1 shows the architecture, where the anti-aliasing filter (AAF) is assumed implicit in the ADC block. It differs from conventional radio frequency (RF) front-ends in a distinct way: the low noise amplifier (LNA) is removed from the receive chain, leaving the mixer as the first block in the front-end. This has a few implications. The LNA amplifies the received signals and adds relatively little noise. Amplification relaxes the noise requirements of the subsequent blocks, but also increases the linearity requirements of said blocks.

2.1.1 Mixer

In a mixer first architecture the first step is down conversion. The mixer is part of a PhD research and its architecture and specifications were provided for this project. The mixer is the UTPASS, a switched capacitor network implemented in FDSOI GF22nm by Purushothaman [1]. It utilizes a 1 GHz clock with 25% duty-cycle to generate four phases, allowing differential I and Q signals to be generated. Figure 2 shows the top-level architecture of the mixer.

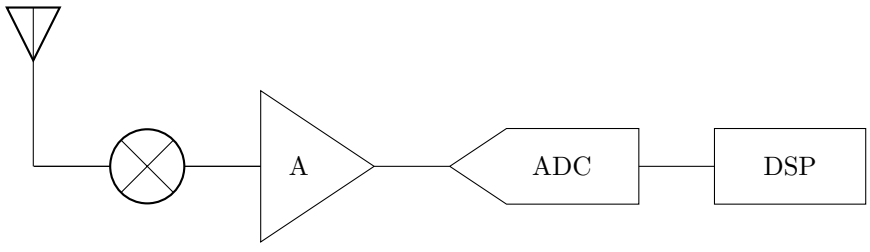


Figure 1: Conventional mixer first architechture (note: AAF is assumed implicit to the ADC block)

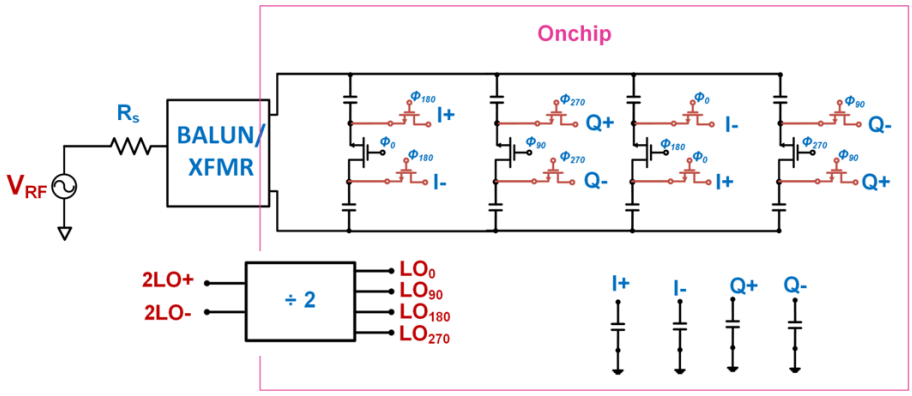


Figure 2: Top-level architecture of the UTPASS

The mixer specifications are listed in table 1. Of particular interest to this project are the gain and noise figure that are achieved by the mixer, because these affect the signal and noise levels at the input of the ADC. Note that in the ideal case 16 dB voltage gain is provided, however post-layout at typical-typical (TT) corner only 11.5 dB is provided. Ultimately, this drop in voltage gain will lead to tougher noise requirements for the ADC. Measured performance achieves a gain of 14 dB, but at the cost of a lower noise figure of 6 dB.

Target specification	
Gain	16 dB
Clock	1 GHz
Duty-cycle	25%
Post-layout performance	
Gain / BW	11.5 dB / 14.7 MHz
Noise figure	5 dB
Output noise @ 1 MHz	4.2 nV/$\sqrt{Hz}$
Measured performance	
Gain	14 dB
Noise figure	6 dB

Table 1: Provided mixer specifications

2.1.2 Baseband amplifier

The baseband amplifier serves a similar function as the LNA in a typical RF front-end. It amplifies the signals to increase the signal levels and relaxes the noise requirements of the subsequent block, the ADC. The question is whether the amplifier is required or if it's consuming power to relax requirements on the

ADC unnecessarily. This question is critical for the project, as an attempt is made to create an ADC that can achieve the tougher ADC specifications that arise when the amplifier is left out (figure 3).

2.1.3 Digital signal processing

The output of the ADC is a digital signal which has to be processed by the digital signal processing (DSP) block. Typically, the first digital block in the chain is a decimation filter. This filter reduces all the noise and unwanted signals outside the band of interest and reduces the sample rate to the Nyquist rate. The subsequent blocks attempt to reduce the noise inside the band to increase the signal to noise ratio (SNR) by means of crosscorrelation. [2].

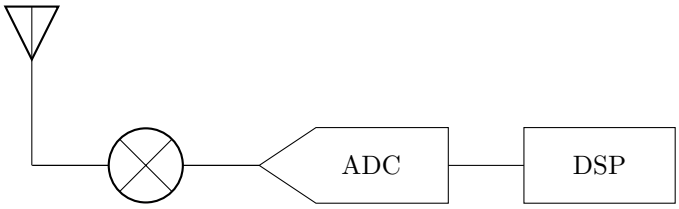


Figure 3: Mixer first architecture without baseband amplifier (note: AAF is assumed implicit in the ADC block)

2.2 ADC architectures

For the IoT application a bandwidth of 1.4 MHz is required at an accuracy of 14 bits, so a number of ADC architectures come to mind: the successive approximation register (SAR), the sigma-delta modulator ($\Sigma\Delta$) and the recent development of the noise-shaping SAR (NS-SAR).

2.2.1 Successive Approximation Register

The SAR is an architecture that is used for medium resolution, medium bandwidth applications. Typical numbers for state of the art SARs are 10 to 12 bit ENOB with 100MS/s to 150MS/s sampling rates [3, 4]. The input signal is sampled onto a binary weighted capacitor array. The capacitors are switched sequentially and compared to a reference to determine whether the switch should stay connected or be disconnected. The SAR architecture is power efficient, because it is charge based. Using small capacitors, a small amount of charge is required to change the voltages on the capacitors and thus little current is required to do so. The speed of this architecture is limited by the fact that each bit is decided sequentially, so N bits require N clock cycles with a clocked comparator. The accuracy of this architecture is limited by noise at the comparator input and capacitor array mismatch. Accuracy can be improved by applying majority voting [5], though this technique can not be applied to high speed SAR ADCs,

because extra conversion cycles are required at the LSB levels. Calibration to reduce the mismatch between the capacitor array and the digital codes can be applied to improve accuracy as well, either analog or digital [6, 7]. A coarse-fine architecture is another solution, where flash is used for the MSB levels. This allows fast MSB decisions and removes a large portion of the input capacitance (the MSB capacitors contribute a lot to the total capacitance of the array) [8, 9].

The limited accuracy is the bottleneck for this architecture, because it suits the requirements of this project in terms of bandwidth and power consumption.

2.2.2 Sigma-Delta Modulator

The $\Sigma\Delta$ is an architecture that employs oversampling and noise shaping to achieve high dynamic range for small bandwidth applications. $\Sigma\Delta$ ADCs of 24 bit accuracy have been reported and typical bandwidths are in the order of a few kHz. $\Sigma\Delta$ ADCs with lower accuracy requirements can range into the medium bandwidth application with bandwidths from 10 up to 40 MHz at with 10 to 12 bit accuracies [10, 11, 12, 13, 14, 15].

The $\Sigma\Delta$ ADC consists of a loop filter, a 1- or multi-bit quantizer and a 1- or multi-bit DAC. Nyquist ADCs sample at twice the bandwidth of the system, but in a $\Sigma\Delta$ ADC oversampling is used in combination with a digital decimation filter. The loopfilter and feedback allow noise to be shaped to the higher frequency ranges, i.e. the parts removed by the decimation filter, thus the noise inside the signal bandwidth is effectively reduced. The SNR improvement depends on the loop filter order and oversampling ratio (OSR). For detailed analysis of $\Sigma\Delta$ modulators the interested reader is referred to [16].

This architecture is limited mostly by the need for oversampling, which limits the bandwidth and/or ENOB that can be achieved. In terms of power efficiency SAR performs better compared to $\Sigma\Delta$.

2.2.3 Noise-Shaping SAR

The noise-shaping SAR is a relatively recent development that combines SAR with some features of the $\Sigma\Delta$ to bridge the gap between the two architectures. It applies low OSRs in the range of 8 to 32 and noise shaping to increase the accuracy to roughly 14 to 16 bits, keeping the SAR's benefits of low power consumption and medium bandwidth [17, 18].

The implementation of the loop filter is done with FIR and IIR filters and [18] utilizes a buffer to fix some issues presented in [17]. With tough noise requirements these blocks may become critical in terms of power consumption, which could negate the benefits that are maintained by using the SAR structure, compared to going for a $\Sigma\Delta$.

2.3 Research question

The main question for this thesis is as follows: is it feasible and beneficial to implement a mixer first architecture with just a mixer and an ADC? Does this result in a higher energy efficiency and/or better linearity compared to the traditional receiver?

The initial research will comprise system level calculations to derive the specifications of the ADC and an evaluation of possible ADC architectures. After that an indepth analysis of one of these architectures is done, including circuit implementation of critical blocks to study the feasibility of these blocks.

The thesis is structured as follows. First the system calculations are discussed in chapter 3. This chapter presents the signal and noise levels at the ADC input and discusses the choice of ADC architecture. Chapter 4 focuses on the noise shaping SAR ADC architecture, reviewing literature and presenting simulations on a system level. In chapter 5 transistor level implementations and simulations of two critical blocks of the loop filter are discussed. Conclusions are drawn in chapter 6, along with recommendations for future work.

3 System Calculations

The UTPASS and mixer first receiver of this project target NB-IoT. With the specifications of NB-IoT and the specifications of the UTPASS system calculations can be performed to derive the requirements for the ADC. This chapter covers the IoT standards, the system calculations and the ADC requirements.

3.1 IoT standard

Two NB-IoT standards will be be considered, CAT-M1 and CAT-NB1 and ideally the receiver can handle both standards. Table 2 provides details about the standards that operate in the ISM band at 915 MHz [1].

	CAT-M1	**CAT-NB1**
Bandwidth	1.4 MHz	200 kHz
Channels	6x 200 kHz	1x 200 kHz
Sensitivity	$-103\ dBm \Leftrightarrow$ $-164.5\ dBm/Hz$	$-108.2\ dBm \Leftrightarrow$ $-161.2\ dBm/Hz$
In-band blocker rejection profile	45 dB @ 2 MHz - 4 MHz 57 dB @ 4 MHz - 11 MHz 67 dB @ 11 MHz and above	45 dB @ 8 MHz - 13 MHz 57 dB @ 13 MHz and above
Out-of-band blocker profile	Rejection > 60 dB @ 15 - 60 MHz offset Absolute < -30 dBm @ 60 - 85 MHz Absolute < -15 dBm @ 85 MHz and above	

Table 2: Specifications for CAT-M1 and CAT-NB1

3.1.1 Out-of-band blockers

Out-of-band blockers can be detrimental to a system if they are not considered. Usually they are taken care of by filtering, because they are located outside of the band. For the IoT standards an out-of-band blocker profile was specified, giving the blocker levels that need to be tolerated by an IoT targeted system. The out-of-band blocker profile is given in table 2 and visually represented in figure 7. Note that the specification is the same for both standards, but the figure also shows the in-band blocker profile of CAT-M1 for reference. For the remainder of this project it is assumed that out-of-band blockers can be taken care of by the UTPASS and as a result the out-of-band blockers do not affect the ADC specifications.

3.1.2 In-band blockers

Unlike the out-of-band blockers, the in-band blockers cannot be neglected, because they cannot be filtered out. Instead, the analog front end has to be able to detect small signals in the presence of these blockers. The in-band blocker profile is specified relative to the sensitivity, as given in table 2. Figure 5 shows

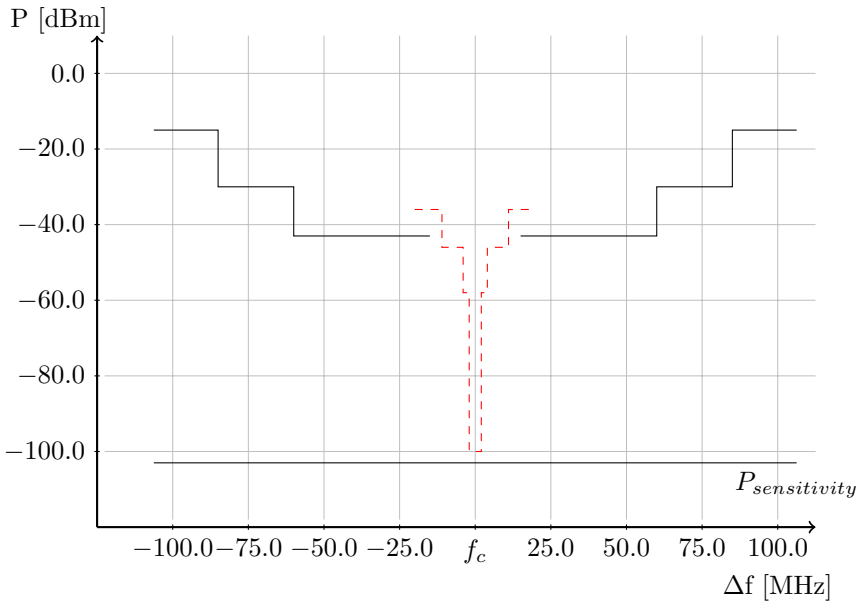


Figure 4: Out-of-band blocker profile around the carrier frequency for CAT-M1 and CAT-NB1. Dashed red line represents the in-band blocker profile for CAT-M1, for reference

the in-band blocker rejection profile around the carrier frequency for CAT-M1. Figure 6 shows the profile for CAT-NB1. The system should be able to handle any blocker that is below the given values, so the system should be able to handle a maximum input power of -36 dBm and -57.2 dBm for CAT-M1 and CAT-NB1 respectively. These numbers set the upper bound for the dynamic range of the ADC at -36 dBm.

3.2 Signal levels throughout the system

Ideally the system would comply to both the NB-IoT standards, thus it should be able to handle the lowest of the sensitivity levels and the highest of the in-band blockers. This sets the sensitivity at -108.2 dBm, coming from CAT-NB1, and the maximum in-band blocker at -36 dBm, set by CAT-M1. Combining the two requirements leads to a dynamic range for the system from -36 dBm to -108.2 dBm, i.e. 72.2 dB dynamic range (figure 7).

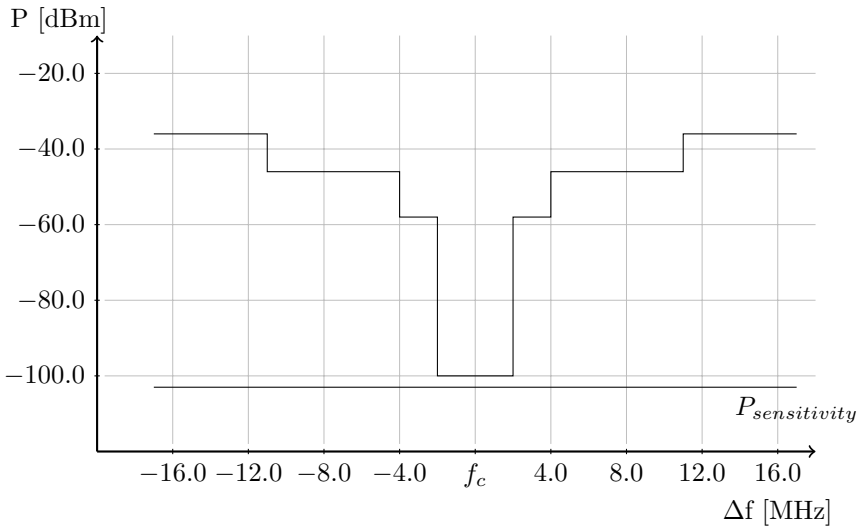


Figure 5: In-band blocker profile around the carrier frequency (900 MHz) for CAT M1

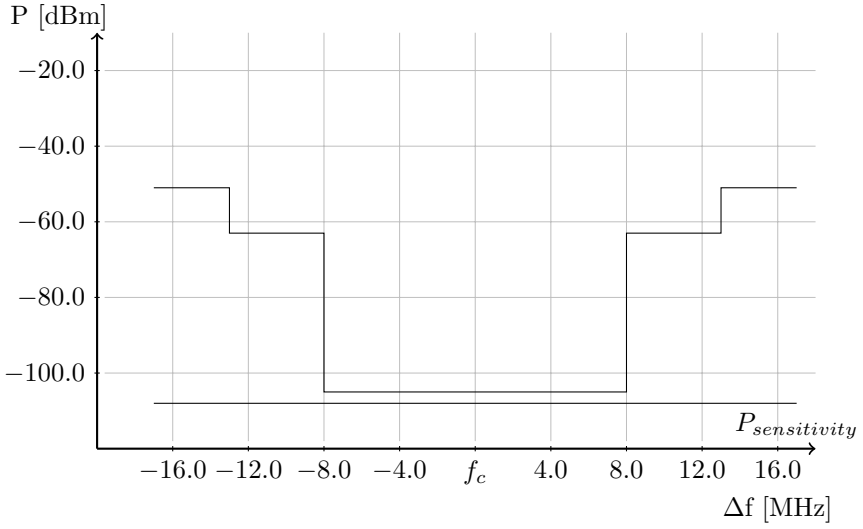


Figure 6: In-band blocker profile around the carrier frequency (900 MHz) for CAT NB1

3.2.1 Impedance levels

It is important to realize that after the antenna (figure 3) the impedance levels will be undefined, because after the mixer the receiver operates in the voltage

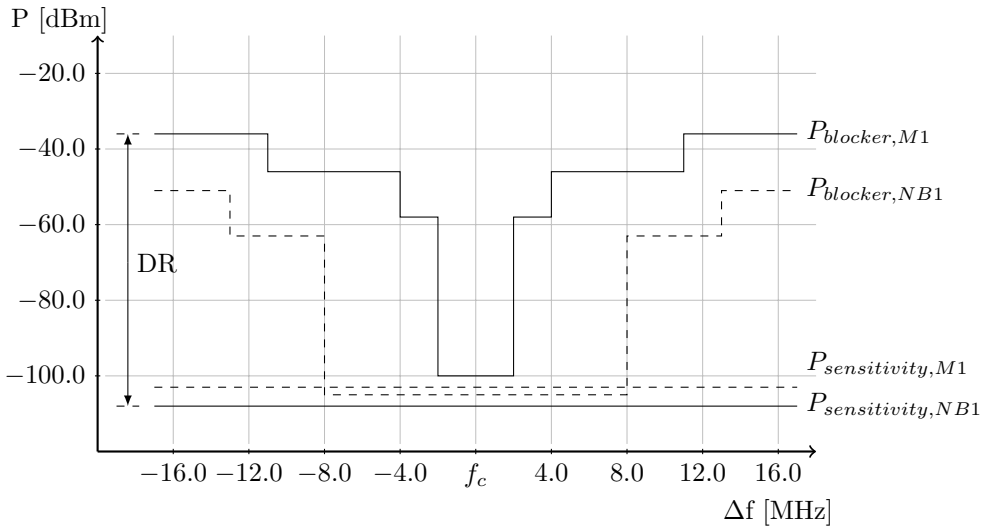


Figure 7: Dynamic range of the input signals as specified by the NB-IoT standards

domain, where high input impedances and low output impedances are typically present. At the antenna, however, it can be assumed 50Ω, so it is convenient to convert the dBm values to dBV at this point in the receiver chain. Table 3 shows the signal and noise levels at the antenna and the associated dBV values and rms voltage levels. These were converted from dBm in 50Ω using the following math.

$$P[dB] = P[dBm] - 30\ dB \tag{1}$$

$$P_{RX}[W] = 10^{\frac{P[dB]}{10}} \tag{2}$$

$$V_{rms}[V] = \sqrt{P_{RX}[W] \cdot R} = \sqrt{10^{\frac{P[dB]}{10}} \cdot 50\Omega} \tag{3}$$

$$V_{RX}[dBV] = 20 \cdot log\left(V_{rms}[V]\right) \tag{4}$$

	P_{dBm}	V_{rms}	V_{RX}
Max. blocker	-36 dBm	3.54 mV	-49 dBV
Min. signal level	-108.2 dBm	0.87 μV	-121.2 dBV
Noise floor	-120.8 dBm	0.203 μV	-133.8 dBV

Table 3: Antenna input range for CAT-M1

3.2.2 ADC input requirements

The receiver front end (antenna, matching network and mixer) provides 16 dB voltage gain with a noise figure of 5 dB [1]. These figures determine the signal and noise levels at the input of the ADC. Table 4 gives these levels. The numbers were derived using the equations below:

$$V_{ADC} = V_{RX}[dBV] + 16dB \tag{5}$$

$$V_{rms} = 10^{V_{ADC}/20} \tag{6}$$

$$V_{n,ADC} = V_{n,RX}[dBV] + 16dB + 5dB \tag{7}$$

	V_{RX}	V_{ADC}	$V_{rms}[V]$
Max. blocker	-49 dBV	-33 dBV	22.4 mV
Min. signal level	-121.2 dBV	-105.2 dBV	5.50 μV
Noise floor	-133.8 dBV	-112.8 dBV	2.04 μV

Table 4: ADC input range

An SNR of 10 dB is required from the ADC for reliable detection and demodulation of the NB-IoT signal. One could argue that to achieve 10 dB SNR for the smallest signal two bits accuracy is required. This would lead to a 12 dB SNR requirement at the lowest signal level. Table 5 gives the resulting ADC input requirements.

It might seem that 10 dB SNR cannot be achieved regardless of the ADC, because from table 4 it can be seen that the SNR at the ADC input is 7.6 dB. This is solved in the digital domain however, by means of cross correlation using two receive paths. The details need not be known for the design of the ADC, but the interested reader can find them in [2].

	rms value	rms value
Max. blocker	-33 dBV	22.4 mV
Min. signal level	-105.2 dBV	5.50 μV
ADC noise	-117.2 dBV	1.38 μV

Table 5: ADC input range and noise requirements

The required SINAD, derived from table 5, is 84.2 dB for 2 bit accuracy at the minimum signal level. Applying this SINAD to equation (9) yields a required ENOB of 13.7.

$$SINAD = 6.02 \cdot N + 1.76 \tag{8}$$

$$ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB} = \frac{84.2\ dB - 1.76\ dB}{6.02\ dB} = 13.7 \tag{9}$$

At the minimum signal level a 2 bit accuracy is required. The minimum signal level is 5.50 μV and 4 signal levels are required, so V_{LSB} is equal to 1.38 μV.

$$V_{LSB} = \frac{5.50\ \mu V}{4} = 1.38\ \mu V \tag{10}$$

3.3 Noise at the ADC input

Analog to digital conversion consists of two steps: sampling the time-continuous input signal to a time-discrete signal and quantizing the continuous amplitude to discrete amplitude levels. Both of these operations generate noise. Sampling will generate kT/C noise ($v_{n,kT/C}$) in a frequency band from 0 to $f_s/2$ [19]. The ADC block also suffers from quantization noise ($v_{n,Q}$) and comparator noise ($v_{n,comp}$). Noise caused by clock jitter is not considered.

3.3.1 kT/C noise

The sampling operation is usually performed by a switch and a capacitor. An input signal is sampled onto the capacitor when the switch is closed and held on the capacitor when it is open. The switch is controlled by a clock with frequency F_s, i.e. the sampling frequency. Noise generated by this operation is a white noise spread from 0 to $f_s/2$. The noise power is given by (11), from which it is clear that the size of the capacitor determines the noise power. A smaller capacitor produces more noiser.

$$v_{n,kT/C}^2 = \frac{kT}{C} \tag{11}$$

To achieve the noise requirement of 1.38 μV a capacitor of 2.17 nF is required.

$$C = \frac{kT}{v_{n,kT/C}^2} = \frac{4.14 \cdot 10^{-21}\ J}{(1.38 \cdot 10^{-6}\ V)^2} = 2.17nF \tag{12}$$

The value of this capacitor matters, because sampling is the first operation in many ADC architectures. The sampling capacitor connects to the output capacitor on the UTPASS, which is only 8 pF. Charge sharing will occur between the two, illustrated by figure fig:1.4, where the charge stored on C_1 and C_2 will be shared between C_1 and C_2 after the switch closes. Assume there is Q_2 charge on C_2 due to voltage V_2 stored in the previous cycle. The voltage on the capacitors when the switch closes, V_{closed} is given by (14).

$$V_1 = \frac{Q_1}{C_1} \qquad\qquad V_2 = \frac{Q_2}{C_2} \tag{13}$$

$$V_{closed} = \frac{Q_1}{C_1 + C_2} + \frac{Q_2}{C_1 + C_2} = V_1 \frac{C_1}{C_1 + C_2} + V_2 \frac{C_2}{C_1 + C_2} \tag{14}$$

$$\frac{\partial V_{closed}}{\partial V_1} = \frac{C_1}{C_1 + C_2} \qquad\qquad \frac{\partial V_{closed}}{\partial V_2} = \frac{C_2}{C_1 + C_2} \tag{15}$$

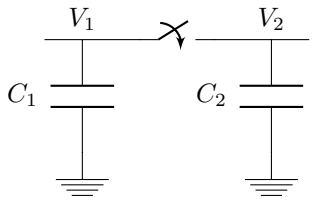


Figure 8: Illustration of charge sharing between two capacitors

Ideally, the voltage V_{closed} depends only on V_1 and not on V_2. This occurs when $C_1 \gg C_2$. The opposite, however, is also true. If $C_1 \ll C_2$ the voltage V_{closed} is mostly determined by V_2. If C_1 is 8 pF and C_2 is 2.17 nF then $C_1 \ll C_2$ and the charge sharing causes an attenuation of the input signal (V_1 in this case) of 272 times. The signal level becomes too low to be detected, so the value of C_2 should be reduced somehow. Oversampling allows the value of C_2 to be reduced while maintaining the noise level. Paragraph 3.4 discusses oversampling and its implications.

3.3.2 Quantization noise

Quantization noise is the error that arises from the difference between an analog signal and its digital representation. The digital representation has an accuracy limited by the number of bits. More bits yield higher accuracy and a smaller error. This noise is modeled as white noise from 0 to $f_s/2$. It is important to note that this noise is **not** white noise, but rather a deterministic signal dependent noise that can generate significant spurious tones. The white noise model has the noise power given by (16) [19, p. 98] and is accurate for systems above 6 bits [19, p. 97].

The LSB level of the has been derived to be $1.38\mu V$ previously. Inserting this value into (17) yields $v_{n,Q} = 0.40\mu V$, so the quantization noise will not be limiting in this project.

$$v_{n,Q}^2 = \frac{V_{LSB}^2}{12} \tag{16}$$

$$v_{n,Q} = \frac{V_{LSB}}{\sqrt{12}} = \frac{1.38\ \mu V}{\sqrt{12}} = 0.40\ \mu V \tag{17}$$

3.3.3 Comparator noise

The comparator is an integral part of any ADC, regardless of the architecture used. The function of the comparator is to take decisions based on a reference level, thus quantizing the continuous amplitude input signal. The comparator creates two types of noise, the first one being the quantization noise that was discussed prevoiusly. Secondly, the comparator creates noise, mainly coming from the pre-amplifier that is in it.

For this thesis the use of the dynamic bias latch-type comparator is assumed [20]. The paper describes an impementation in 65-nm CMOS with 0.4 mV input noise, however, an implementation in FDSOI GF22nm by Bindra can achieve 0.18 mV input noise [21].

3.4 Oversampling

Oversampled systems use a higher sampling rate than is strictly necessary according to the Nyquist theorem, i.e. $f_s > 2 \cdot B$, and is especially relevant for low bandwidth systems. The oversampling ratio (OSR) is defined as the ratio of the sampling frequency to the Nyquist rate, so $OSR = {}^{f_s}/_{2 \cdot B}$. The main purpose of oversampling is to spread noise from 0 to ${}^{f_s}/_2$, effectively reducing the noise inside the bandwidth B, thus increasing the SNR inside this bandwidth. Note that this does require a decimation filter after the ADC to remove the unwanted noise outside the bandwidth.

Two types of noise were mentioned previously that are spread from 0 to ${}^{f_s}/_2$, the two being quantization noise and kT/C noise. Paragraph 3.3.2 showed that quantization noise will not be limiting for this project, so the focus will be on kT/C noise. Every factor two OSR spreads the noise power over double the frequency range, thus reducing the in band noise by a factor 2. Assuming perfect decimation filtering, this improves the SNR by a factor 2, or 3 dB.

Equation 12 derives the required capacitor value for the case of Nyquist sampling. The value was derived for a given SNR, so improving the SNR is not required. Instead, it is possible to decrease the value of C when oversampling is applied. A factor 2 oversampling allows a factor 2 smaller capacitor while maintaining the in band SNR. Table 6 gives the minimum allowed capacitance for a given OSR at a constant noise level of 1.38 μV.

OSR	f_s [MHz]	C [pF]
1	3.00	2170
2	6.00	1085
..	..	..
32	96.0	67.81
64	192	33.91
128	384	16.95
256	768	8.477

Table 6: Minimum capacitor values for a noise level of 1.38 μV at certain OSR values

Table 6 shows some important numbers. First of all it shows that decreasing the capacitor size comes at the cost of sampling frequency. 768 MHz might not seem out of question, but in the case of a SAR ADC the clock frequency is effectively

multiplied by N, where N is the number of bits that have to be resolved in one sampling time. Secondly, it gives a range of input capacitor values, which is important with regard to the charge sharing problem from 3.3.2.

Most importantly, table 6 confirms the observation that was made previously, that oversampling is not optional, due to charge sharing between the UTPASS output capacitance and the input sampling capacitance of the ADC.

3.5 ADC architecture

Choice of the ADC architecture is based mainly on the noise requirement for the lowest signal level and the need for an energy efficient converter. As mentioned previously, the SAR architecture is limited by comparator noise. This is especially true in this particular case, because the LSB level is at 1.38 μV. Comparator noise would have to be much lower than this to not corrupt the LSB decision levels. Given the need for oversampling, the relatively high bandwidth and the accuracy required, techniques like majority voting cannot be applied. The comparator by H.S. Bindra [21] achieves 0.18mV noise, so by impedance scaling the power consumption would be so large that it would negate the energy efficiency that SAR is known for.

Research into the noise shaping SAR has shown promising results, where performance of SAR ADCs is improved with noise shaping techniques from the $\Sigma\Delta$ architecture. Compared to the $\Sigma\Delta$ architecture the NS-SAR should have better performance in terms of energy efficiency. Added to that the fact that this is an opportunity to expand the knowledge in the ICD group with a new ADC architecture, the choice was made to go for noise shaping SAR.

4 Noise Shaping SAR

The noise shaping SAR was first introduced by Fredenburg and Flynn [17]. It is an architecture that intends to bridge the gap between low bandwidth, high precision ΣΔ ADCs and medium bandwidth, medium precision SAR ADCs.

Comparator noise can be a limiting factor for SAR ADCs, especially if the comparator operates at high frequencies [22]. Similar to a ΣΔ, noise shaping, combined with oversampling provides a means to shift the noise to frequencies that are outside the bandwidth of interest. In order to do noise shaping, one needs to feed back the noise, so a means to capture this noise is discussed first.

4.1 Residue generation

In a SAR the noise that is added during the successive approximation operation is the quantization noise and comparator noise during the last cycle. For a regular SAR the last bit decision is not fed back to the DAC, but instead the cells are reset. This reset discards all the information from the previous cycle, making it impossible to feed back the quantization noise. Instead, as proposed in [17], the final bit decision should be fed back to the DAC. What is left on the capacitors is the difference between the input signal and its digital representation, i.e. the quantization noise, and the input referred comparator noise comparator noise.

The residue that is generated by the extra switching of the LSB can be stored on a small capacitor to ensure that it is not affected by a reset or sampling of input voltage of the next cycle. This can however be incorporated in the loop filter, because a FIR filter is typically present in the loop filter (L(z) in figure 9), which is implemented with switches and capacitors to create delay elements, as demonstrated in [17] and [18]. To prevent large signal swings on the input of the loop filter a switch can be added (s_1 in figure 9 that is only enabled when the residue voltage is present on the SAR capacitors. This is especially relevant when the first stage of the loop filter is a buffer that can not tolerate large signals on its input.

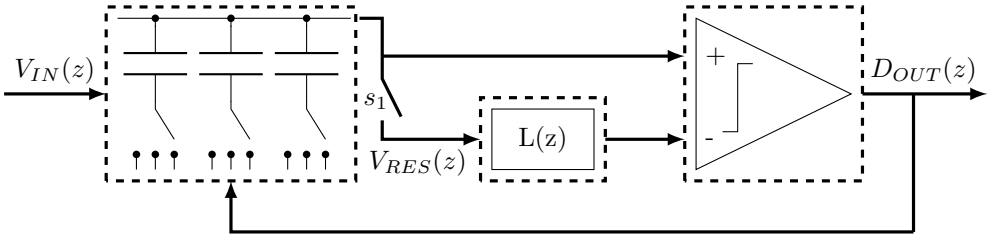


Figure 9: Noise shaping SAR architecture, similar to [17, fig.6]. Switch s_1 is enabled when the SAR sequence has finished

4.2 Modeling the NS-SAR

Based on figure 9 and the transfer functions from [17] and [18] a model was made in Simulink. The signal flow diagram is as figure 27. Starting with $V_{in}(z)$, which is the sampled version of the input at the sampling rate of the converter, F_s. This V_{in} represents the value that is sampled onto the capacitor bank of the SAR and thus should contain kT/C noise as well.

The residue voltage, the difference between V_{in} and the digital representation of V_{in}, is modeled as a subtraction of V_{in} and D_{out}, implying an ideal DAC feedback. This value is meaningful at the end the SAR cycle, which is when it is captured onto a capacitor using the method of [17], which is implemented in the loop filter as part of the FIR filter.

A loop filter with transfer function L(z) is used to model the transfer functions implemented in [17] and [18]. It is a combination of a FIR filter (delay elements, which will capture the residue voltage) and an IIR filter, which acts as an integrator. In the case of [18] a buffer is added in the loop filter, but this does not change the model, merely the transfer function of L(z).

The input voltage V_{in} and filtered residue voltage are added before the comparator block. This comparator block is implemented as a multi-bit quantizer to represent the SAR operation that would be present in the real NS-SAR. The output of this quantizer is the final value of the SAR algorithm, the bit level that is closest to V_{in}. The quantization operation is performed by this block, so the quantization noise is intrinsic to this block and does not have to be added separately. It has been added in figure 10 though, to enable the derivation of noise transfer functions.

The feedback branch incorporates the DAC, which was modeled as perfectly linear. In the case that the DAC is not perfectly linear or there is some form of mismatch between the capacitors, this could be modeled in the feedback branch.

The models provided in [17] and [18] all follow the structure of figure 10. From

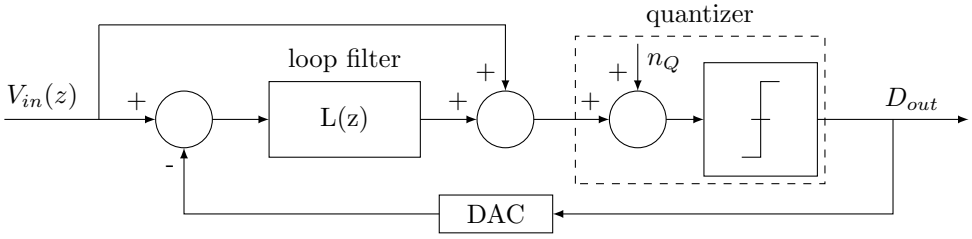


Figure 10: Signal flow diagram of the NS-SAR ADC

the signal flow diagram the transfer function (20) and the noise transfer function can be derived (21). It is important to note that the derivation of the noise transfer function holds **only** for the noise generated in the comparator, i.e. comparator and quantization noise. The equations illustrate that the loop filter can be used to shape the noise without affecting the signal transfer function (STF), which is a useful property.

$$D_{out}(z) = V_{in}(z) \cdot (1 + L(z)) - D_{out}(z) \cdot L(z) + n_Q(z) \tag{18}$$

$$D_{out}(z) = V_{in}(z) + n_Q(z) \cdot \frac{1}{1 + L(z)} \tag{19}$$

$$TF(z) = 1 \tag{20}$$

$$NTF(z) = \frac{1}{1 + L(z)} \tag{21}$$

4.3 Noise transfer functions

Because the signal transfer function is not affected by the loop filter, the filter can be used to optimize for the noise transfer function (NTF). In [17] a number loop filters are presented, whereas [18] presents an improved loop filter based on [17]. These loop filters and their resulting NTF have been validated using MATLAB.

Fredenburg [17]

The paper by Fredenburg and Flynn proposes a number of loop filters based on a delay element and an integrator. Ideally, the loop filter has the transfer function L(z) from equation 22. The NTF that is produced by this filter is given in equation eq:4.5 and its magnitude response plotted in figure 11.

$$L(z) = z^{-1} \cdot \frac{1}{1 - z^{-1}} \tag{22}$$

$$NTF(z) = 1 - z^{-1} \tag{23}$$

From figure 11 it is evident that there is a high pass behaviour, i.e. the noise is high at frequencies near $f_s/2$ and low for small frequencies. The way this graph can be interpreted is as follows: with increasing OSR the bandwidth of interest becomes a smaller fraction of $f_s/2$, so the bandwidth moves to the left on the curve and thus the noise level in that bandwidth decreases.
The approach of using an ideal integrator leads to issues when it is implemented with an OpAmp (as it is done in [17]), due to non-idealities in the OpAmp and capacative losses in the form of charge sharing. Finite gain of the opamp and

capacitive losses between the delay element and the integrator are modeled with a quality factor κ_A.

$$L(z) = z^{-1} \cdot \frac{\kappa_A}{1 - \kappa_A z^{-1}} \tag{24}$$

$$NTF(z) = 1 - \kappa_A z^{-1} \tag{25}$$

Figure 12 shows the NTF for three values of κ_A, where $\kappa_A = 1$ is the ideal case from before. It is clear that this issue limits the performance of the noise shaping, as low frequency suppression is limited.

FIR-IIR implementation

Instead of the implementation above with a delay element and an OpAmp integrator, another impementation is proposed in the paper by Fredenburg and Flynn using a FIR-IIR filter cascade. The IIR filter is still implemented with an OpAmp, so the non-unity κ_A remains, but by using a FIR filter in front the overall transfer function of the loop filter is altered.

The FIR filter has a second delay element and a transfer function of $\alpha_1 z^{-1} + \alpha_2 z^{-2}$. where $\alpha_1 = 3$ and $\alpha_2 = 1$. The IIR filter has the same transfer function as the integrator used before, equation 24. The cascaded FIR and IIR create the loop filter transfer function given by equation 26. Taking this transfer function, putting it into equation 21 and simplifying yields the NTF in equation 27.

$$L(z) = \frac{\kappa_A \alpha_1 z^{-1} + \kappa_A \alpha_2 z^{-2}}{1 - \kappa_A z^{-1}} \tag{26}$$

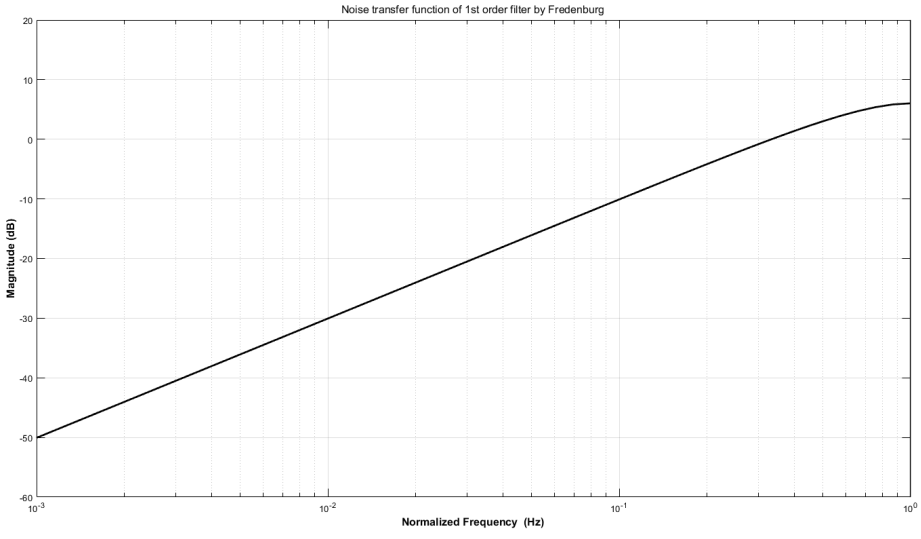


Figure 11: NTF for a loop filter with a delay element and an ideal integrator

$$NTF(z) = \frac{1 - \kappa_A z^{-1}}{1 + \kappa_A (\alpha_1 - 1) z^{-1} + \kappa_A z^{-2}} \tag{27}$$

The NTF from equation 27 has the magnitude response of figure 13, where $\kappa_A = 0.64$[1]. Compared to the magnitude responses of $\kappa_A = 0.8$ in figure 12 there is a 4.2 dB improvement for high OSR and compared to $\kappa_A = 0.6$ there is a 10.2 dB improvement.

An interesting thing to note is that using $\kappa_A = 1$ would result in an unstable filter.

Shu [18]

Based on Fredenburg's concept, Shu published a paper that proposes a NS-SAR with some additional features [18]. Here the FIR-IIR cascade is used as well, however, an input buffer is added to avoid loss in the passive sampling in [17]. The buffer is combined with a 46 dB simulated OpAmp DC gain to solve the quality factor issue that prevents high suppression high OSRs in [17]. The proposed transfer function in [18] is given in equation 28, equation 29 provides the resulting NTF. From figure 14 it is clear that the NTF has improved compared to the ideal $1 - z^{-1}$ NTF, an improvement of 8.5 dB.

$$L(z) = 2\frac{z^{-1} + \frac{1}{3}z^{-2}}{1 - z^{-1}} \tag{28}$$

[1] no justification for this value is given in [17]

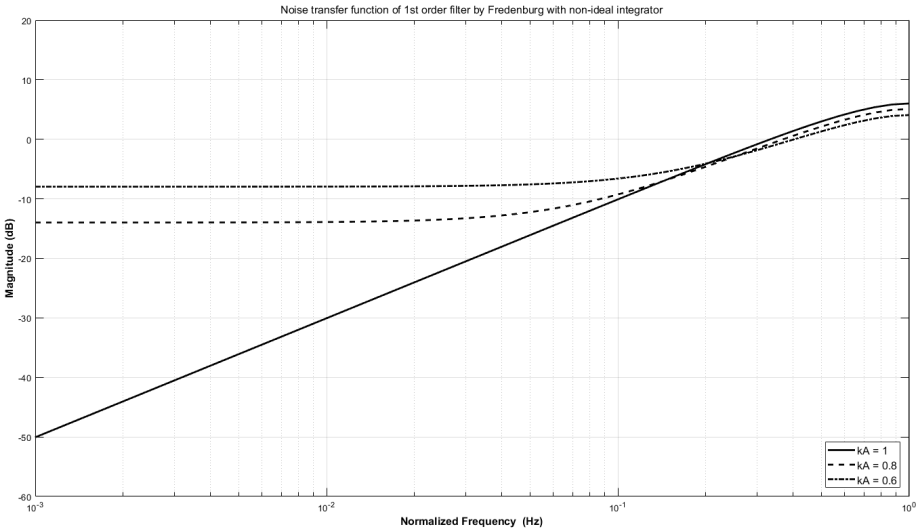


Figure 12: NTF for a loop filter with a delay element and a non-ideal integrator

$$NTF(z) = \frac{1 - z^{-1}}{1 + z^{-1} + \frac{2}{3}z^{-2}} \tag{29}$$

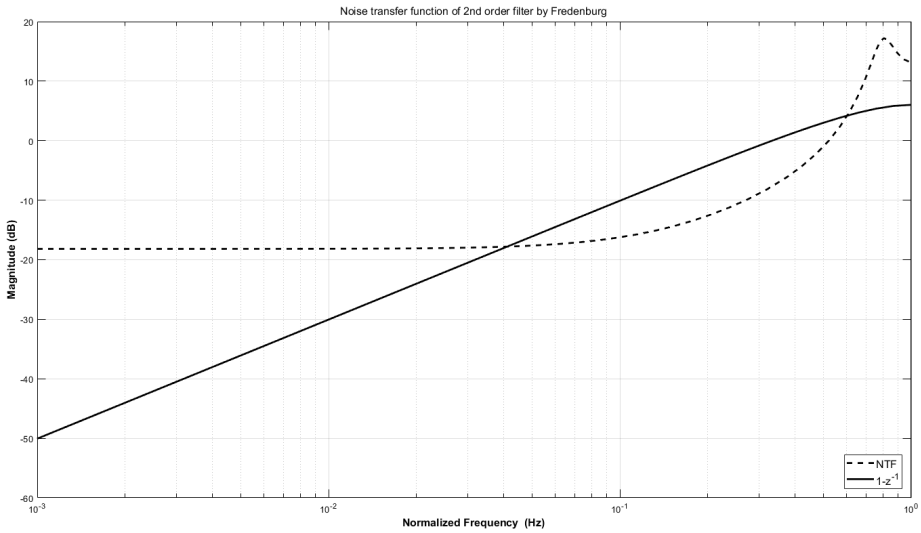


Figure 13: NTF for a loop filter with a FIR-IIR cascade (non-ideal integrator)

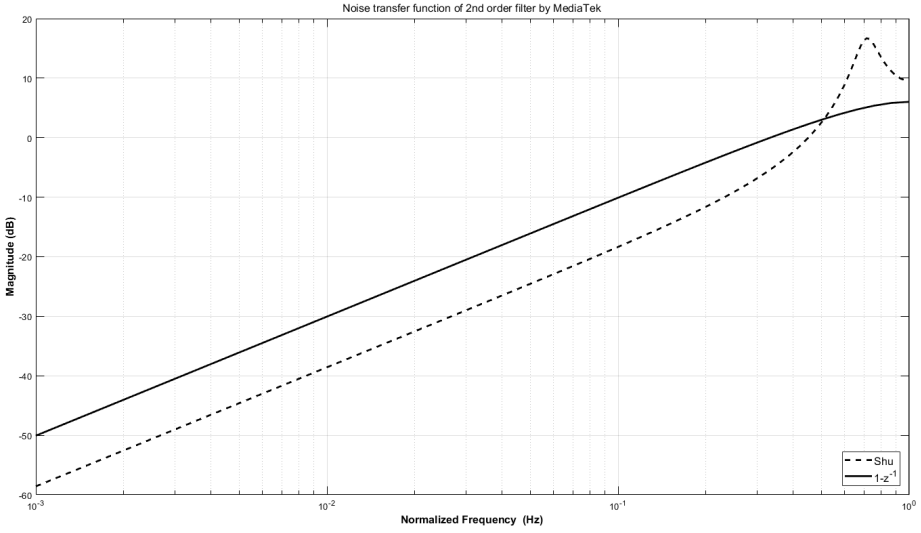


Figure 14: NTF for a loop filter with a buffer-FIR-IIR cascade (non-ideal integrator) proposed in [18]

Results

The NTFs show how noise can be shaped from 0 to $f_s/2$ and thus what the noise levels are inside the band on interest. As OSR increases, the point on the NTF moves to the left. For example, an OSR of 4 yields $f_{BW} = f_s/(2 \cdot 4) = 0.125 f_s$. Figures 11, 12, 13 and 14 are normalized plots with respect to f_s, so one simply has to find 0.125 on the logarithmic axis for OSR = 4.

MATLAB was used to evaluate the magnitude of each of the NTFs at OSRs ranging from 1 to 256. Tables 7, 8 and 9 show the values for equations 25, 27 and 29 respectively.

OSR	1	2	4	8	16	32	64	128	256
$\kappa_A = 0.6$	4.08	1.34	-2.91	-6.00	-7.37	-7.80	-7.92	-7.95	-7.96
$\kappa_A = 0.8$	5.11	2.15	-2.94	-7.91	-11.5	-13.1	-13.8	-13.9	-14.0
$\kappa_A = 1.0$	6.02	3.01	-2.32	-8.17	-14.2	-20.2	-26.2	-32.2	-38.2

Table 7: Magnitude [dB] of NTF from equation 25 at certain OSRs

OSR	1	2	4	8	16	32	64	128	256
$\kappa_A = 0.64$	13.2	-0.98	-10.8	-15.4	-17.3	-18.0	-18.1	-18.2	-18.2

Table 8: Magnitude [dB] of NTF from equation 27 at certain OSRs

OSR	1	2	4	8	16	32	64	128	256
	9.54	2.55	-9.13	-16.3	-22.6	-28.7	-34.7	-40.7	-46.7

Table 9: Magnitude [dB] of NTF from equation 29 at certain OSRs

It is worth noting that oversampling as a process adds additional suppression, i.e. 3.01 dB per factor 2 for quantization noise. Quantization noise was not limiting anyways though.

Previously it was derived that noise shaping should provide an attenuation of the noise of at least 43 dB. Shu's implementation can reach this, but only with an OSR of 256.

In the case that non ideal behaviour occurs from finite OpAmp gain, a κ_A of 0.986 is required. This translates to a required OpAmp gain of 70.4 (37.0 dB), by solving equation 30.

$$\kappa_A = \frac{A}{1+A} = 0.986 \tag{30}$$

4.4 Loop filter

So far it was assumed that the loop filter is ideal in the the sense that no noise is added. The loop filter is not an ideal block when it is implemented on chip though. Assuming an implementation like the one in [18] it comprises a buffer, FIR filter and IIR filter. Each of these blocks generates noise at a different point in the loop and thus each will have a different NTF compared to the comparator noise. Figure 15 shows the loop filter components inside the system. Input referred noise will be used to derive each NTF.

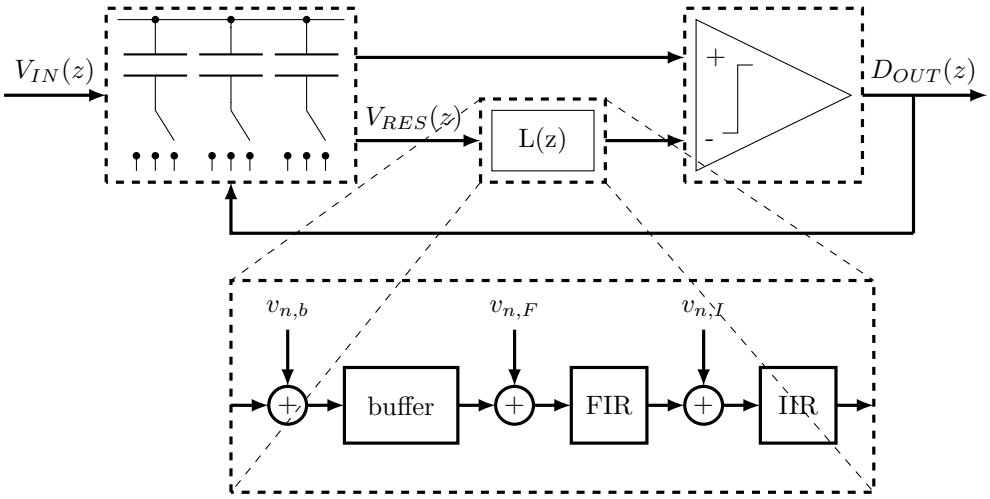


Figure 15: Noise shaping SAR architecture, similar to [17, fig.6]

4.4.1 Buffer noise

Input referred noise from the buffer sees the NTF given by (31), which is derived in appendix A.2. A magnitude plot is given in figure 16, which shows that there is no attenuation of the noise, no matter the OSR. Consequently, the buffer noise needs to be very low and this block is critical in terms of noise.

$$NTF_b = \frac{\partial D_{OUT}}{\partial v_{n,b}} = \frac{L(z)}{1+L(z)} = \frac{2\left(z^{-1}+\frac{1}{3}z^{-}2\right)}{1+z^{-1}+\frac{1}{3}z^{-2}} \tag{31}$$

In the bandwidth of 1.5 MHz there is a requirement of 1.38 μV noise. The allowed noise density is given by (32). A very low number, which will lead to a large amount of power dissipated in the buffer to achieve. If only a single channel is demodulated the bandwidth reduces to 200 kHz and the noise requirement

becomes like (33). This is the requirement used in section 5.

$$\frac{1.38\ \mu V}{\sqrt{1.5\ MHz}} = 1.127\ nV/\sqrt{Hz} \tag{32}$$

$$\frac{1.38\ \mu V}{\sqrt{0.2\ MHz}} = 3.086\ nV/\sqrt{Hz} \tag{33}$$

4.4.2 FIR noise

The FIR filter is located behind the 2x buffer, so intuitively one would say that the noise is attenuated by 6 dB compared to the buffer noise. Equation 34 (derived in appendix A.2) and figure 16 show that this is indeed the case.

$$NTF_F = \frac{\partial D_{OUT}}{\partial v_{n,F}} = \frac{\frac{1}{2}L(z)}{1+L(z)} = \frac{\left(z^{-1}+\frac{1}{3}z^{-}2\right)}{1+z^{-1}+\frac{1}{3}z^{-2}} \tag{34}$$

Because the FIR filter is based on switches and capacitors, the noise that is introduced will be kT/C based. That means that oversampling will help to reduce it, thus the noise of this block is less critical. The required capacitor values will be in the same range as the total capacitor array of the SAR (appendix A.1).

4.4.3 IIR noise

The IIR filter is implemented in [18] as an integrator based on an OpAmp. The noise generated by this block gets attenuated slightly, because it is behind the FIR filter, compared to the FIR noise. Mathematical derivation (in

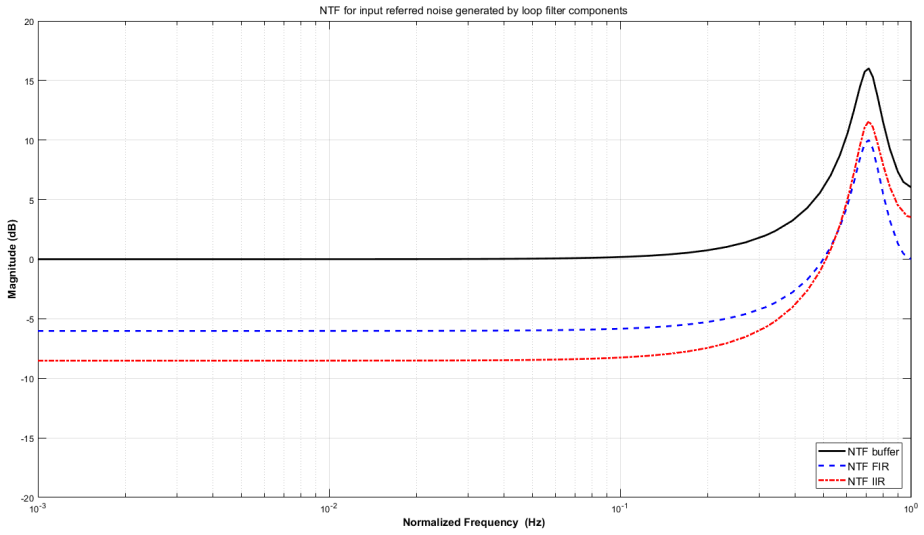


Figure 16: NTF for separate loop filter components

appendix A.2) shows that the noise transfer function is as in (35).

$$NTF_F = \frac{\partial D_{OUT}}{\partial v_{n,I}} = \frac{1}{1 + z^{-1} + \frac{1}{3}z^{-2}} \tag{35}$$

IIR noise stems mostly from the OpAmp. Again, numbers are derived for a bandwidth of 1.5 MHz and 200 kHz. Similar to the buffer noise, the figure for 200 kHz bandwidth is used for the transistor level simulations.

$$\frac{1.38\ \mu V}{\sqrt{1.5\ MHz}} \cdot 10^{\frac{-8.51}{20}} = 3.00\ nV/\sqrt{Hz} \tag{36}$$

$$\frac{1.38\ \mu V}{\sqrt{0.2\ MHz}} \cdot 10^{\frac{-8.51}{20}} = 8.22\ nV/\sqrt{Hz} \tag{37}$$

4.4.4 Input signals

In [18] it is mentioned that input signals of the loop filter are small, because these are residue voltages, and thus linearity is not regarded as a problem. Indeed the difference between the difference between the sampled continuous amplitude input signal and the digital representation of it should be in the order of an LSB (1.38 μV). The comparator noise (0.18 mV) contributes much more, assuming 3σ it would be 0.54 mV maximum. This value is relevant when looking at the linearity of the buffer, which is examined in 5.2.2.

4.5 Simulink model

The derived transfer functions require verification and as such, simulations were done to do so. The simulink model of figure 17 was used to for this purpose. The figure shows the general architecture, similar to that of figure 15.

The first block (figure 18a) contains a signal generator, limiter and a zero-order hold block to set the sampling rate of that signal. The frequency and amplitude of the input signal can be set using the signal generator block, while the sampling rate of this signal can be set in the zero-order hold block. In the UTPASS the outputs are at a sampling rate of 1 GHz, so this is the frequency that is set for simulations. The limiter ensures that the maximum input range is not violated. If the maximum input range is violated however, which could happen if the limiter was left out, then it would cause clipping in the quantizer.

Block two (figure 18b) contains another zero-order hold, representing the sampling moment of the input signal onto the capacitor array of the NS-SAR. This sampling generates kT/C noise, which is added by a random number generator, where the mean and variance can be set.

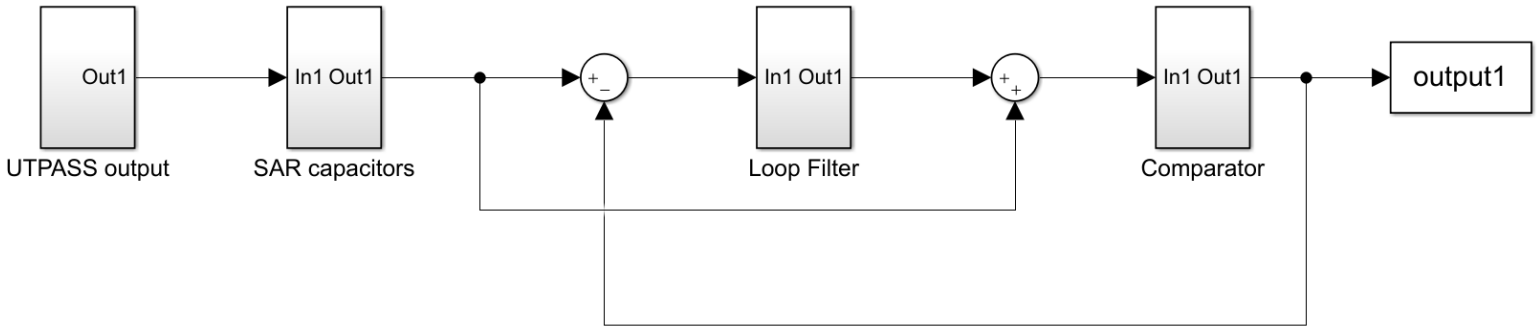
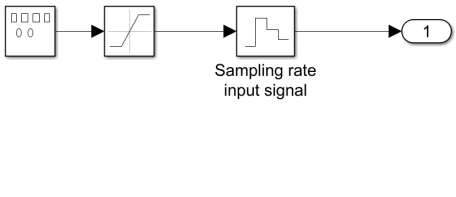
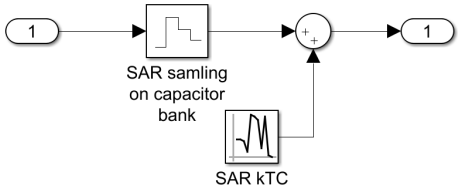


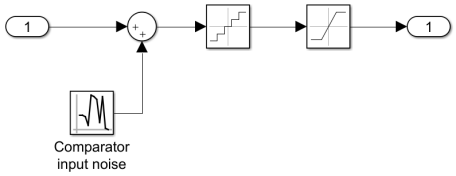
Figure 17: Simulink model of the noise shaping SAR



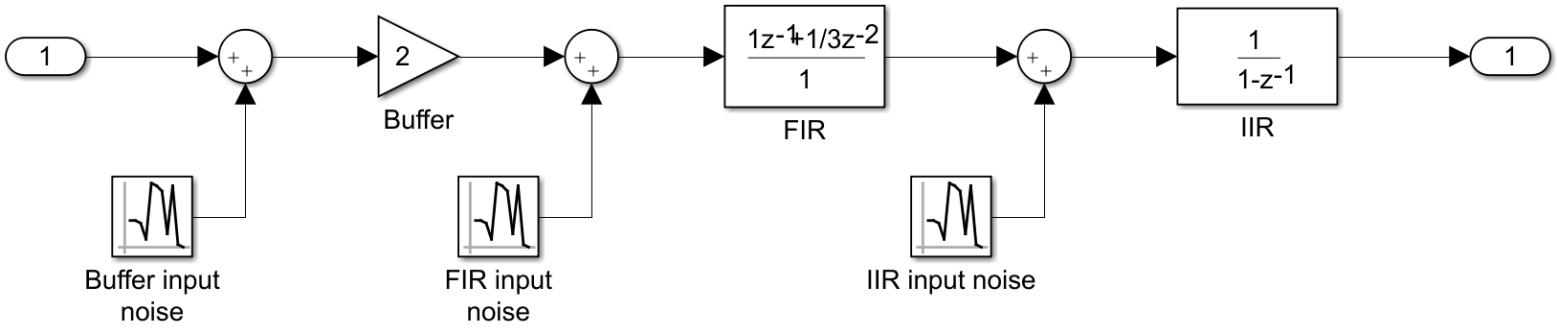
(a) UTPASS output model



(b) Sampling capacitors model



(c) Comparator model



(d) Loop filter model

Figure 18: Simulink model subblocks

Third is the loop filter. As discussed in section 4.4 each of these blocks has an input referred noise, which is added in a similar fashion as the kT/C noise (as all of these are modeled as white Gaussian noise). As for the blocks themselves, these are modeled as ideal, though it is technically possible to add a κ_A factor to the IIR block.

The last block is the comparator. It has an input referred noise block, an N-bit quantizer, where the LSB value can be set. To ensure that it is indeed an N-bit quantizer with the given LSB step a limiter should be used. This limiter sets the full scale range of the comparator. If for any reason there would be a violation of the maximum input range, then this limiter will cause clipping similar to what would happen in an ADC. The output of the comparator is exported to MATLAB.

4.6 Simulations

Simulations done in order to verify the NS-SAR behaviour are as follows. First a simulation was done where all noise sources are set to 0. Thus this simulation will only have an input signal and the quantization noise generated by the quantization process. The input signal is a 47.635 kHz[2] sine wave with an amplitude of $0.31 \cdot 10^{-3}$. The result of this simulation is figure 19, which shows the noise shaping effect that the quantization noise is expected to benefit from. At low frequiencies side lobes of the input signal are visible, caused by the FFT. At high frequencies the noise is higher than these side lobes and roughly shows the behaviour as expected from the noise transfer function (figure 14).

A note on dBs in the figures. The exact values are unknown to me, as I have limited experience with how MATLAB defines these values. Each noise source uses the same seed and power, however, so relative to one another the effects can be seen.

Next step is characterizing the noise source that will be used. Each simulation will use a noise source with mean 0 and a variance of $1 \cdot 10^{-3}$. The seed used for this noise source is 2016. Figure 20 shows the spectrum of the noise, hovering around -75 dB. From here on, each time one noise source will be activated.

First the kT/C noise source is activated with the noise mentioned above. The result is figure 21, which shows the same noise level as figure 20. This is the expected behaviour. Only towards $f_s/2$ the noise starts to drop, but an explanation for this behaviour has not been found.

Next is the buffer noise, figure 22. Expected is that the noise is the same as characterized noise, except for the high frequency portion near $f_s/2$. Indeed

[2] A rather arbitrary number, however, one must take care to not pick a frquency that is an integer ratio of the sampling frequency. Failure to do so can lead to strong correlation between the input signal and the quantization noise when performing the FFT operation [26].

there is a slight upswing near this point as expected from the noise transfer function. The drop that was seen for kT/C noise is present in this simulation as well, but not expected.

Now the FIR noise is made active (and buffer noise is deactivated). Compared to the buffer noise a drop of 6 dB is expected, due to noise transfer function. In figure 23 some of the recognizable peaks have indeed dropped by this amount, indicating that the FIR noise is indeed attenuated by 6 dB. Towards $f_s/2$ the noise goes up as expected. When the IIR noise is examined, figure 24, again the behaviour is as expected. Noise at low frequencies has gone down, but the peaking near $f_s/2$ is higher.

Finally the comparator noise is enabled. This is the most interesting simulation, because it can showcase the performance of the NS-SAR. Figure 25 shows the simulation result. It clearly shows that the comparator noise is shaped as expected according to the noise transfer function.

4.7 Conclusion

Throughout these simulations there is one problem that kept arising: the trend at the high end of the frequency spectrum does not seem to match. Due to time constraints no further investigation of this phenomenon was possible. Simulations do prove that the noise shaping SAR can definitely improve the accuracy of a SAR by reducing the effect of comparator noise inside the signal bandwidth.

The noise requirements in this project are quite stringent, however, especially for the loop filter components. As such, a transistor level design was done of the buffer and OpAmp that are to be used in an implementation such as [18]. This will allow an evaluation of the feasibility of said implementation under the given requirements.

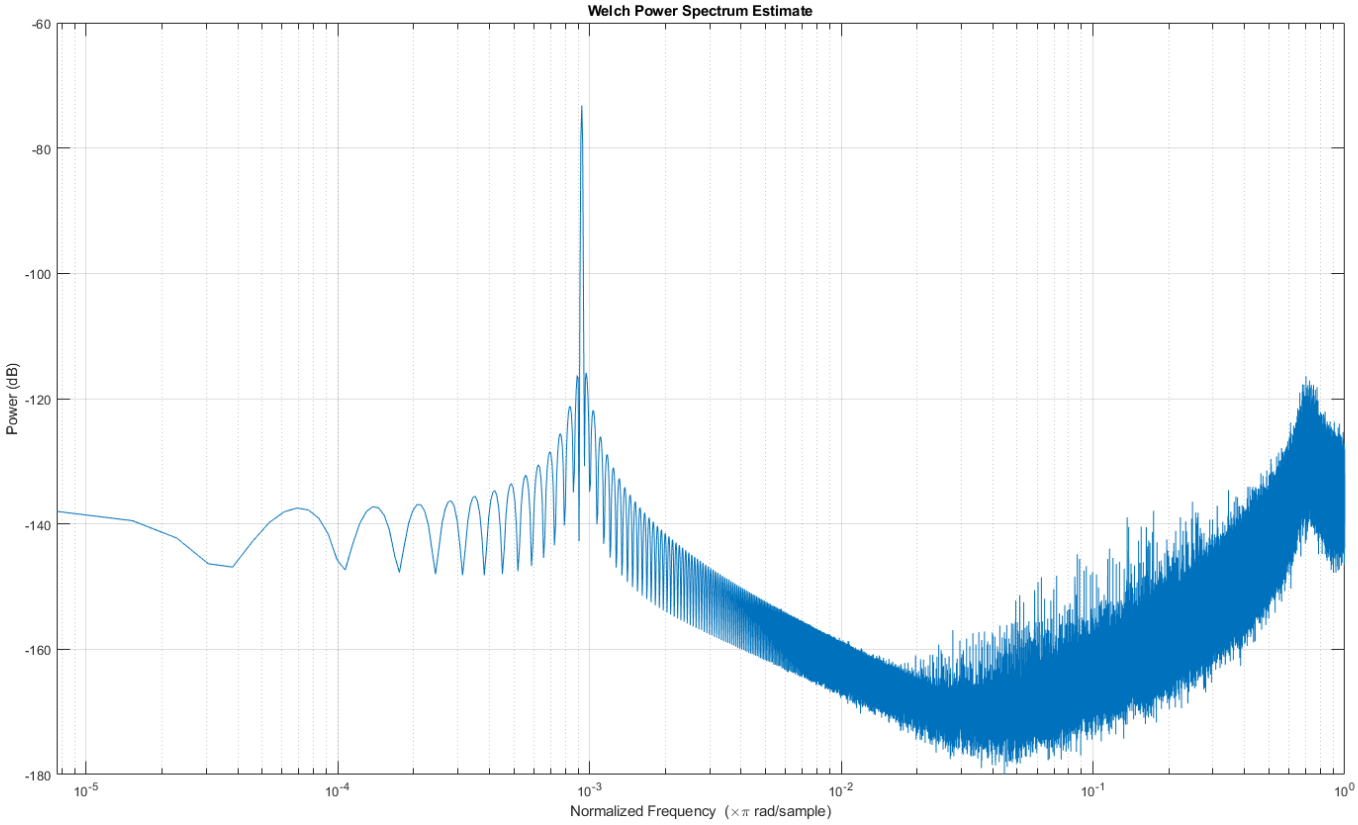


Figure 19: Simulation of simulink model (figure 17) without active noise sources

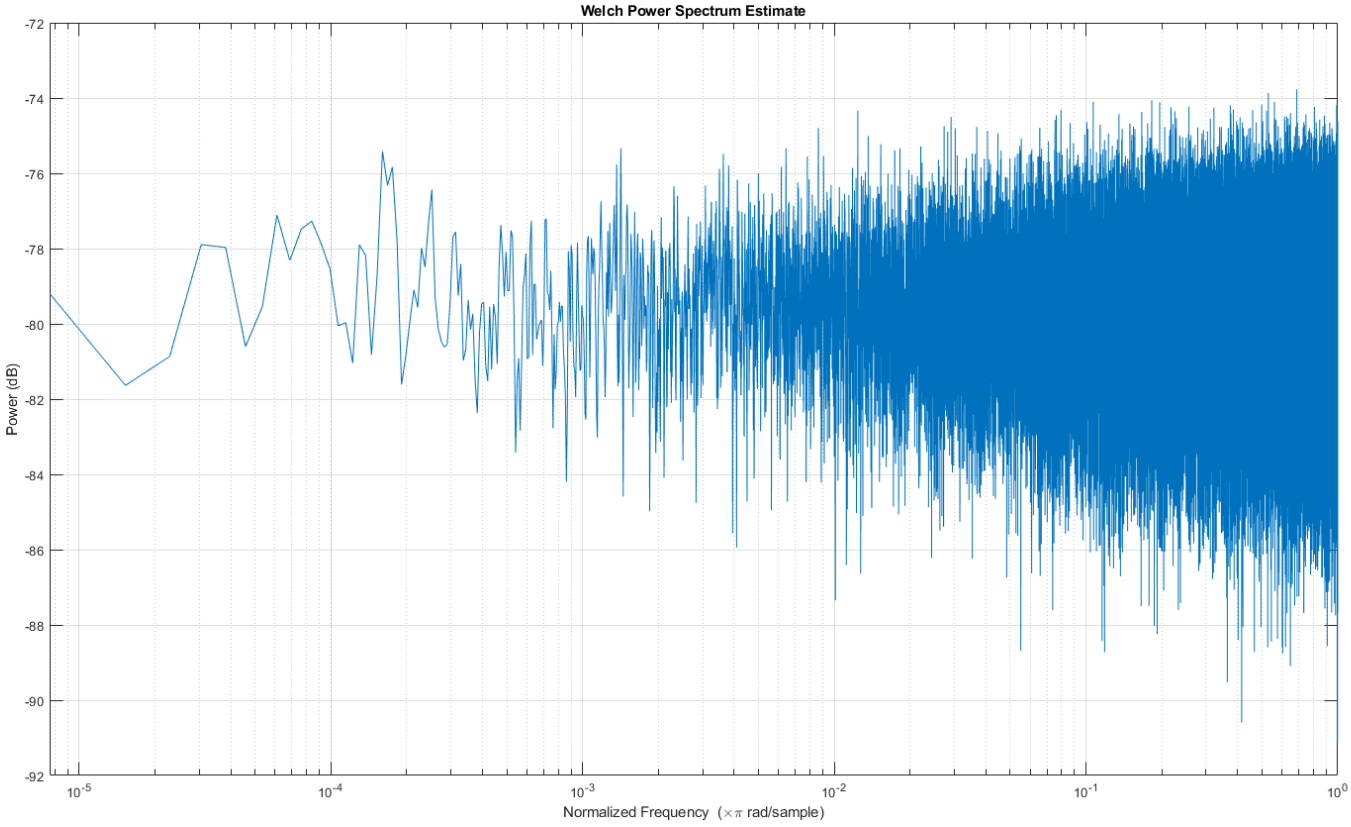


Figure 20: Spectrum of noise source used in simulations

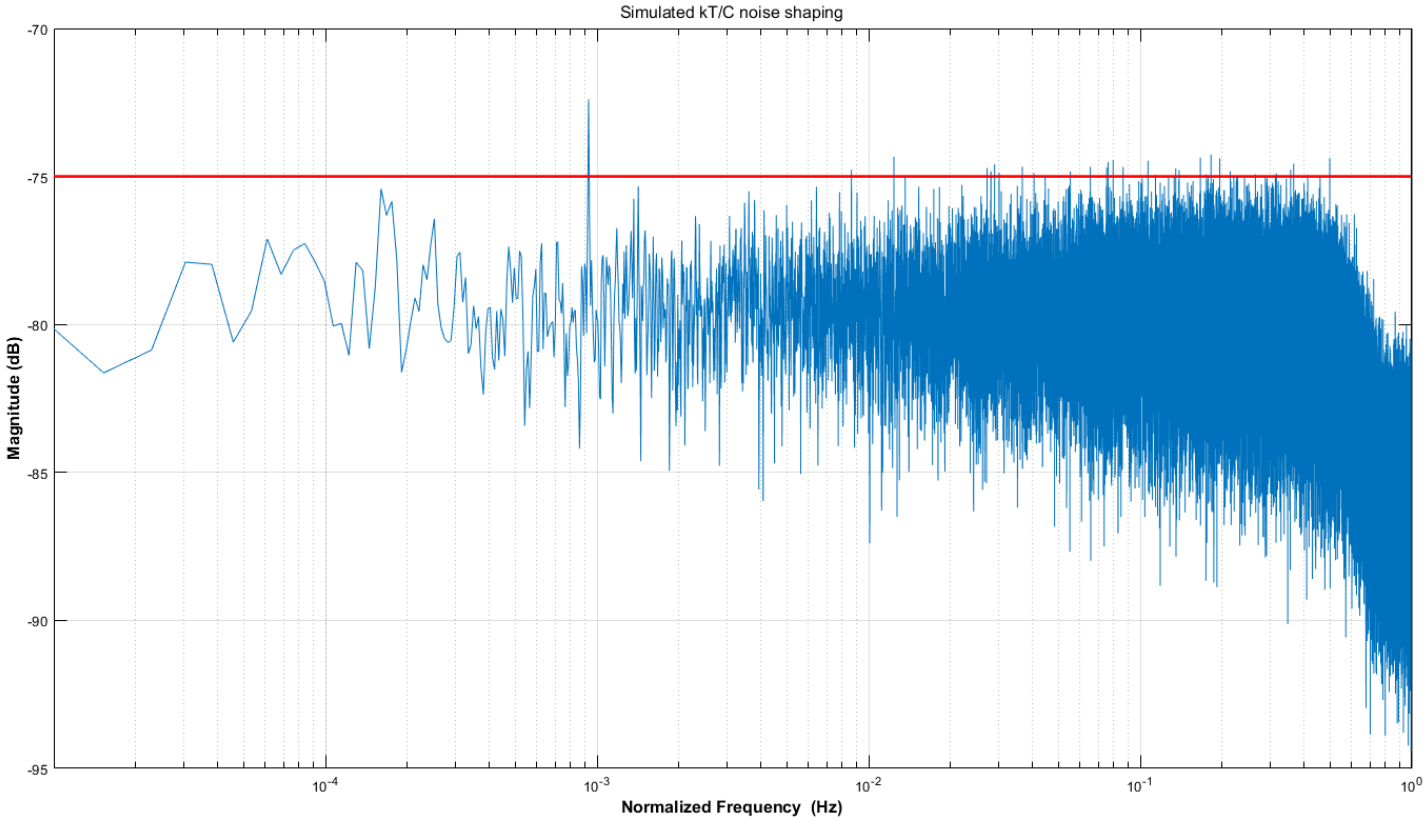


Figure 21: Simulation of simulink model (figure 17) with kT/C noise

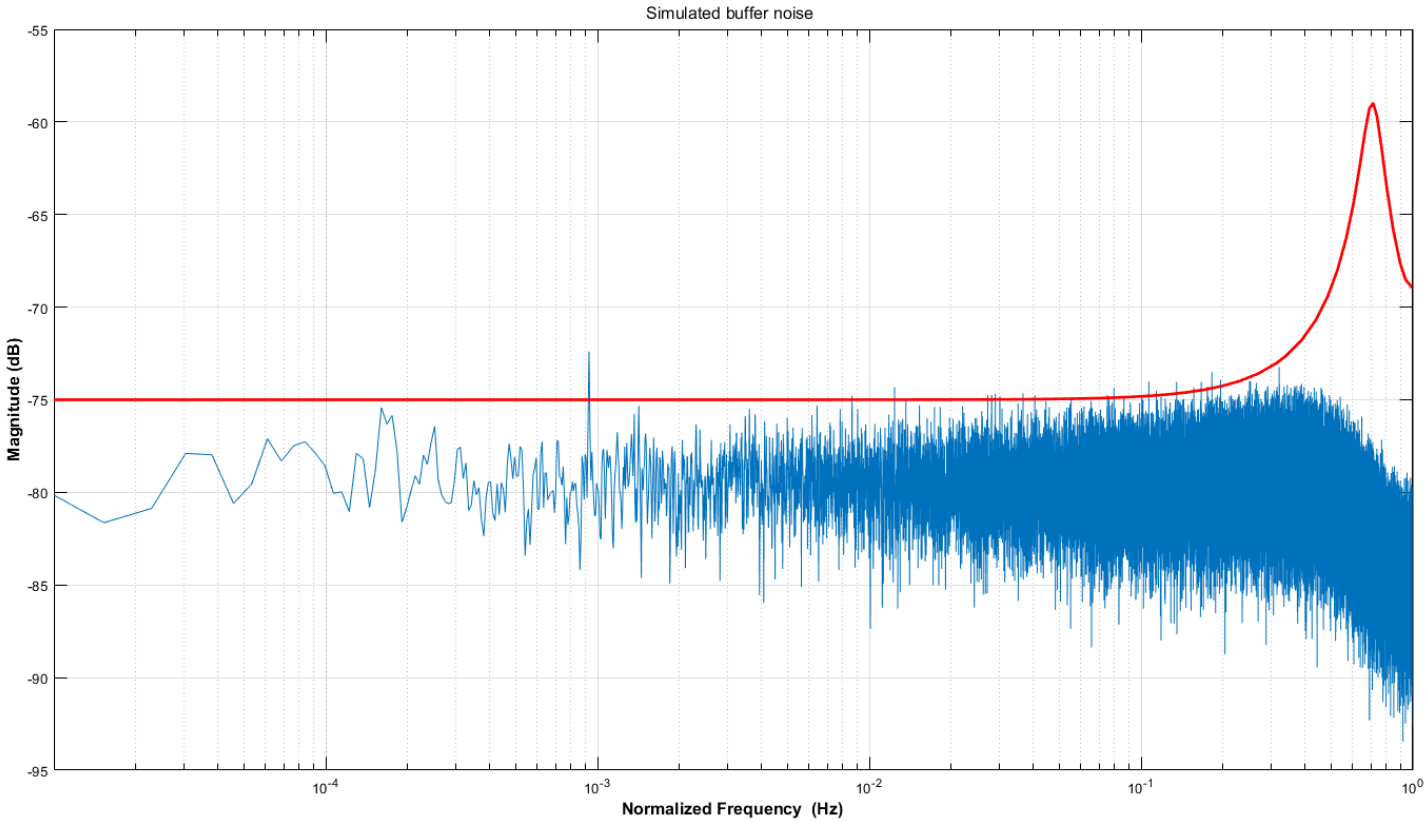


Figure 22: Simulation of simulink model (figure 17) with buffer noise

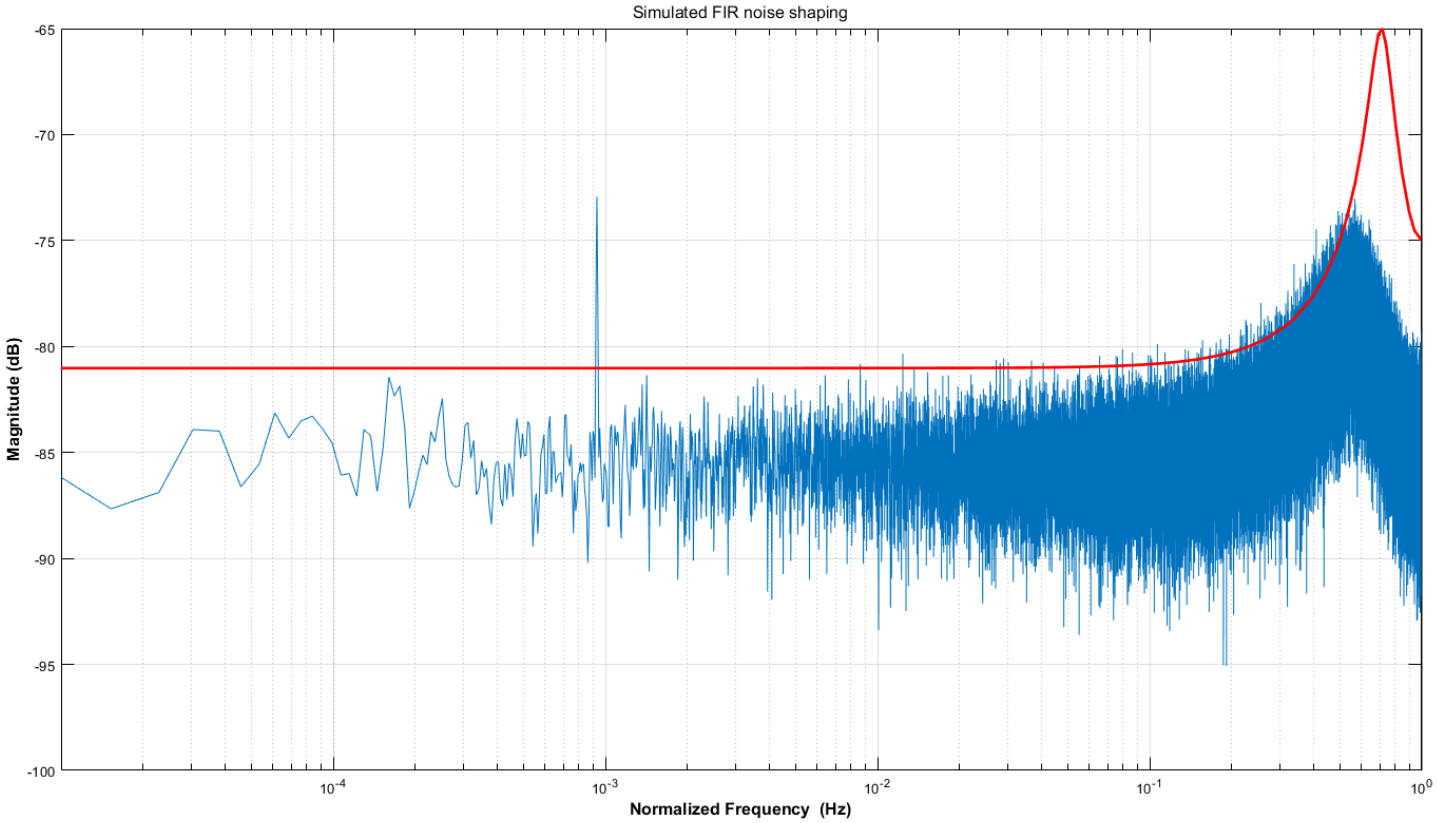


Figure 23: Simulation of simulink model (figure 17) with FIR noise

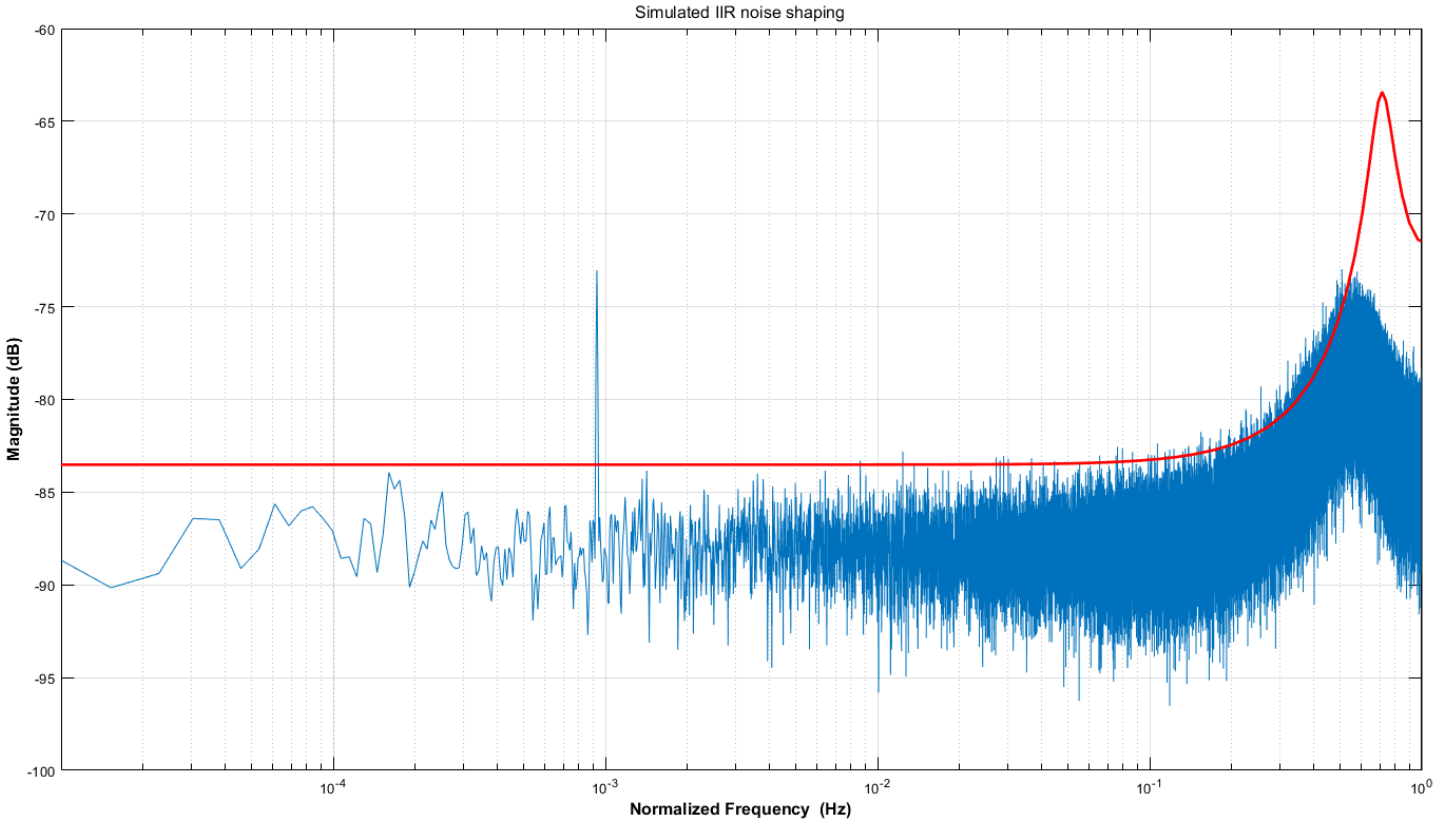


Figure 24: Simulation of simulink model (figure 17) with IIR noise

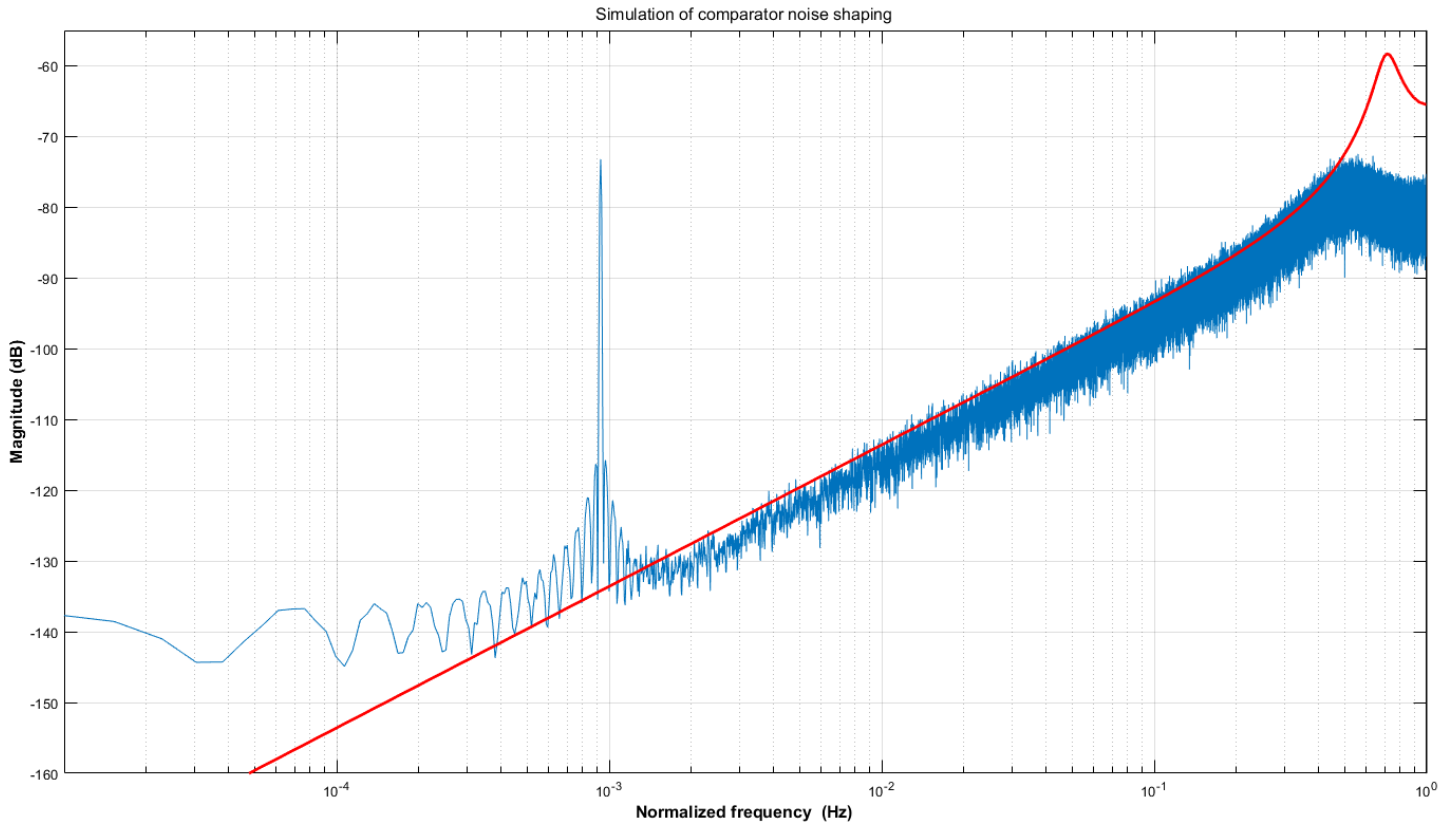


Figure 25: Simulation of simulink model (figure 17) with comparator noise

5 Transistor Level Simulations

Despite the desire for an all passive ADC some experimentation was done with a buffer and an OpAmp. Especially the buffer plays an important role in [18].

5.1 Buffer Schematic

The initial schematic of the buffer is a differential pair with diode connected load, as in figure 26, where the ratio of the transconductances of the nmos and pmos determines the small signal gain (38), derived in appendix A.3.

$$\frac{v_{out}^{+} - v_{out}^{-}}{v_{in}} = \frac{g_{m,N}}{g_{m,P}} \tag{38}$$

A gain of 2 is desired, so the transistors should be biased such that $g_{m,P} = 2g_{m,N}$.

5.1.1 Common mode levels

Due to the desire to use the buffer in a setting like in [18], thus in a system with feedback, the common mode levels should be well defined. The choice was made to set all the common mode levels (both input and output) at 400mV, which is half of the supply voltage.

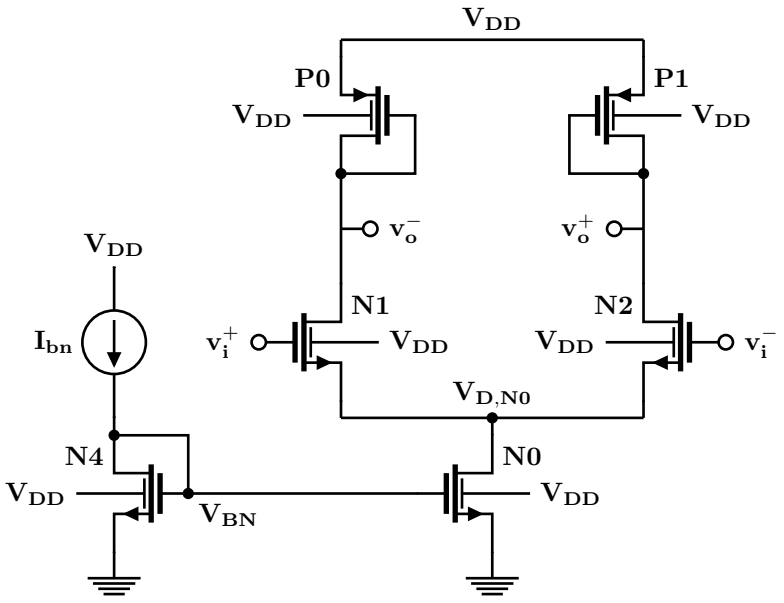


Figure 26: Buffer schematic

5.1.2 Biasing

As mentioned previously, the input and output nodes will be biased such that there is 400mV common mode level, assuming that there is no common mode variation. N0 will require roughly 100mV to 150mV $V_{DS,N0}$ to provide sufficient bias current, so both $V_{GS,N1}$ and $V_{DS,N1}$ will range from 250mV to 300mV, with the same voltages for N2. For P0 (and P1) $V_{GS,P0}$ and $V_{DS,P0}$ are both 400mV.

Under these circumstances both the NMOS and PMOS devices operate in weak inversion and it turned out to be impossible to get a ratio of 2 between $g_{m,N1}$ and $g_{m,P0}$, even with variation of the body bias. To resolve this issue a bleeding current source can be added to the circuit (figure 27), on both sides, to reduce the current through the PMOS. This helps, because under given biasing, the ratio of g_m and I_D is set. Less current through P0 and P1 means lower $g_{m,P0}$ and $g_{m,P1}$, thus allowing a ratio of 2 between NMOS and PMOS.

5.1.3 DC operating points

For this design the approach was to ensure certain voltage drops at the nodes and find W and L to generate a certain amount of current under those bias conditions. This is convenient, because g_m/I_D depends on V_{GS} and increasing the current through a branch will not change the ratio between $g_{m,N}$ and $g_{m,P}$. The tail current is used to scale the design to a certain noise level, discussed

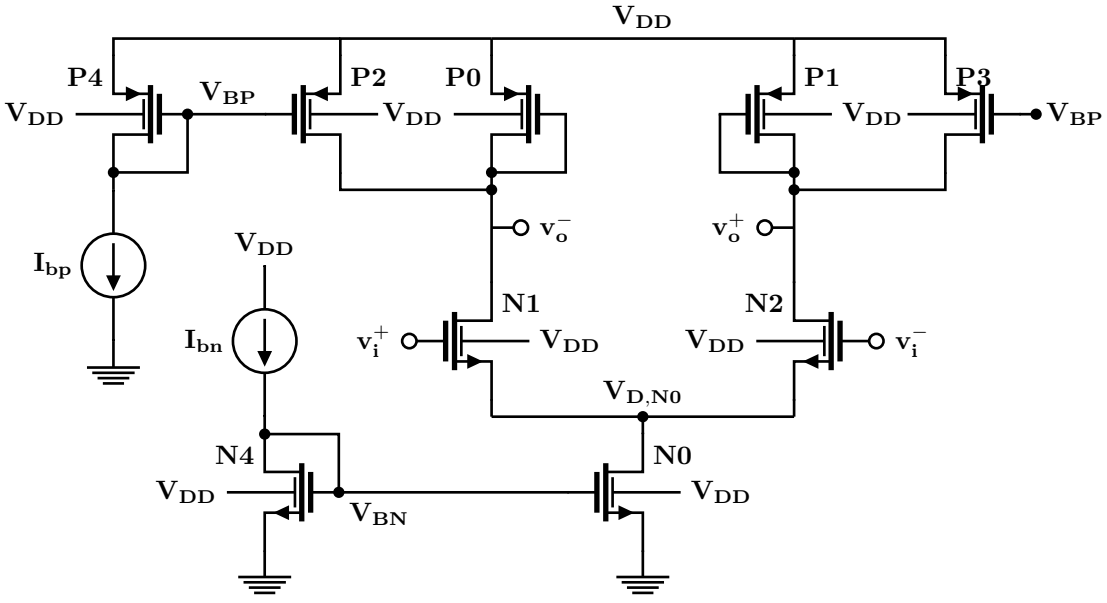


Figure 27: Complete buffer schematic, including current mirrors

in 5.2.4, so the approach proved useful.

As mentioned before V_i and V_o will be at 400mV DC common mode level, so V_i^+, V_i^-, V_o^+ and V_o^- are all at 400mV. $V_{D,N0}$ was set at 125mV, which allows N0 to operate in weak inversion and still generate sufficient current.

Given in table 10 are the DC operating points for the final design. The currents through N4 and P4 were deliberately kept small, so as to not draw large static currents. Of course, in a real design these currents would depend on the golden reference that is available for use in current mirrors, or another method to generate a stable DC voltage could be used to bias the tail current source.

	$\mathbf{V_{GS}}$	$\mathbf{V_{DS}}$	$\mathbf{V_{TH}}$	$\mathbf{I_D}$	$\mathbf{g_m}$	$\mathbf{g_{ds}}$	$\mathbf{g_m/I_D}$	**reg**
N0	300	125	355.7	405.0	7.738m	557.3u	19.1	WI
N1/N2	275	275	351.9	202.5	5.125m	25.13u	25.3	WI
P0/P1	-400	-400	-408.9	-144.1	2.502m	14.48u	17.4	WI
P2/P3	-300	-400	-444.8	-58.5	1.544m	16.34u	26.4	WI
N4	300	300	333.9	0.5	10.97u	34.83n	21.9	WI
P4	-300	-300	-446.3	-0.25	7.169u	94.52n	28.7	WI

Table 10: Buffer DC operating points. Voltages in mV, currents in μA, transconductances in S.

5.1.4 Sizing

The first step in sizing the transistors was using minimum length. While applying bias voltages with voltage sources on the specified nodes to set the gate-source and drain-source voltages a sweep was done over W to find the right W/L ratio to get the I_D specified in table 10. It turned out, however, that small variations (sub nm range) in W would cause significant discrepancies in the node voltages when the voltage sources were removed and the transistors connected. Instead, the length of each transistor was increased by some power of 2.

At this point it is interesting to look at second order effects in the buffer, most notably that of N0, N1 (and N2) and P0 (and P1). The small signal gain when R_{DS} is taken into account changes to (39), derivation in A.4. Ideally $g_{ds,N1} \ll g_{m,N1}$, $g_{ds,P0} \ll g_{m,P0}$ and $g_{ds,P2} \ll g_{m,P0}$, which means that L should be taken relatively large, because R_{DS} increases with L [23, p.34]. Filling in the numbers from table 10 into equation 63 yields 2.004 gain.

So far it was assumed that the branchs are perfectly balanced. In case of an imbalance, for example in the input voltages, $R_{DS,N0}$ will start to play a role, because the imbalance in currents produces a residue current at $V_{D,N0}$ that needs to be sinked to ground through N0. This happens through $R_{DS,N0}$, so from

a first look it would seem that $R_{DS,N0}$ should be small, such that the voltage swing due to this residue current at $V_{D,N0}$ is small. Analysis in appendix A.5 confirms this suspicion. To keep $R_{DS,N0}$ small L should not be too large. In the case that this proves to be an issue in the circuit, a possible solution would be to add a capacitor to ground at node $V_{D,N0}$, which allows the circuit to sink any AC residue current at this node to be sinked to ground. Note: this has not been tested.

Listed in table 11 are the W and L values for the final design, where all transistors use a single finger. These values were reached using the method described above, taking into account the contraints mentioned.

A short note concerning transistor type and body bias. It was recommended to use either LVT or SLVT devices from the GF22nm technology. The choice was made to use the SLVT devices. Reverse body bias was applied to the PMOS devices to increase VT[3], preventing the PMOS devices from entering strong inversion. Strong inversion is not desired, because the noise is lower in weak inversion. In hindsight, LVT may have been a better option in this case, given the inherently higher threshold voltage.

	W [um]	**L [nm]**	**W/L**	**m**	**type**	**V_{BB}**
N0	3.588	80	44.85	9	SLVT	V_{DD}
N1/N2	8.737	160	54.61	9	SLVT	V_{DD}
P0/P1	6.703	320	20.95	9	SLVT	V_{DD}
P2/P3	7.448	80	93.10	9	SLVT	V_{DD}
N4	0.184	320	0.575	1	SLVT	V_{DD}
P4	0.342	80	4.275	1	SLVT	V_{DD}

Table 11: Buffer device dimensions

5.2 Buffer simulations

In order to verify the behaviour of the buffer, simulations were performed. First the DC characteristics are determined by large signal simulations using a DC sweep. Then the AC behaviour is characterized with small signal simulations at the specified bias point. Last is a noise simulation to determine whether the noise specifications are met.

5.2.1 Large signal

The DC characteristics of the circuit are determined by sweeping the differential input voltage from -800 mV to +800 mV. Due to the differential nature of the circuit a characteristic similar to that of [23, p. 104] is expected. There

[3]Possible because the NMOS are biased at V_{DD} as well, thus no junctions are put in forward if the wells are touching each other.[24]

is one major difference though: the book ([23, p. 104]) uses a resistor as load, whereas a diode connected load is used here in conjunction with a bleeding current source. The effect of this difference will become clear.

A sweep was done to determine the behaviour of the circuit over a large range of input signals, characterizing the DC behaviour of the buffer. Figure 28 shows the result of a DC sweep where V_{in} goes from -0.8 V to 0.8 V (horizontal axis), showing the voltages at the output nodes V_o^- (red), V_o^+ (blue) and $V_o^+ - V_o^-$ (purple). The difference with [23, p. 104] now becomes clear, because the output nodes do not have an odd symmetry like in [23, p. 104].

V_o^- starts at +800 mV, with both P0 and P2 turned off completely. As the differential input voltage (horizontal axis) increases, the branch will have to start conducting. Because P2 is biased at a V_{GS} of 400 mV it will start conducting before P0 does. V_o^- will drop slightly to follow an increasing current through the branch (because V_{DS} of P2 has to rise to do so). At some point V_{DS} surpasses V_{DSsat} for P2, after which its current is nearly constant. P0 starts switched off, but eventually enters weak inversion when V_o^- starts to drop. $|V_{GS,P0}|$ has to increases rapidly when $V_{DS,P2} = V_{DSsat,P2}$ is satisfied to match the rapidly increasing current through the branch.

At equilibrium ($V_{in} = 0\ mV$) V_o^- is at its common mode voltage of 400 mV. For a still increasing input voltge V_o^- will converge towards a stable value. V_{GS} of N0 continues to increase, but the current cannot follow, because it is limited by the tail current. On top of that, V_o^- cannot continue to drop, because V_{DS} of N0 and N1 should be sufficient to stay in saturation. Therefore, if V_o^- cannot drop further, the current through P0 cannot increase.

Verifying the behaviour of P0 and P2 as described above was done by plotting the relevant voltages and current through the transistor separately, figure 29. Note that the behaviour of P1 and P3 is similar, but mirrored around $V_{in} = 0.0\ mV$. The figure confirms the suspicion that $|V_{GS,P0}|$ (purple) quickly needs to increase to follow the increasing current in the branch after $V_{DS,P2} = V_{DSsat,P2}$ (purple, orange) is satisfied. As V_{GS} continues to rise it will eventually surpass V_{TH} (green) and push P0 into strong inversion.

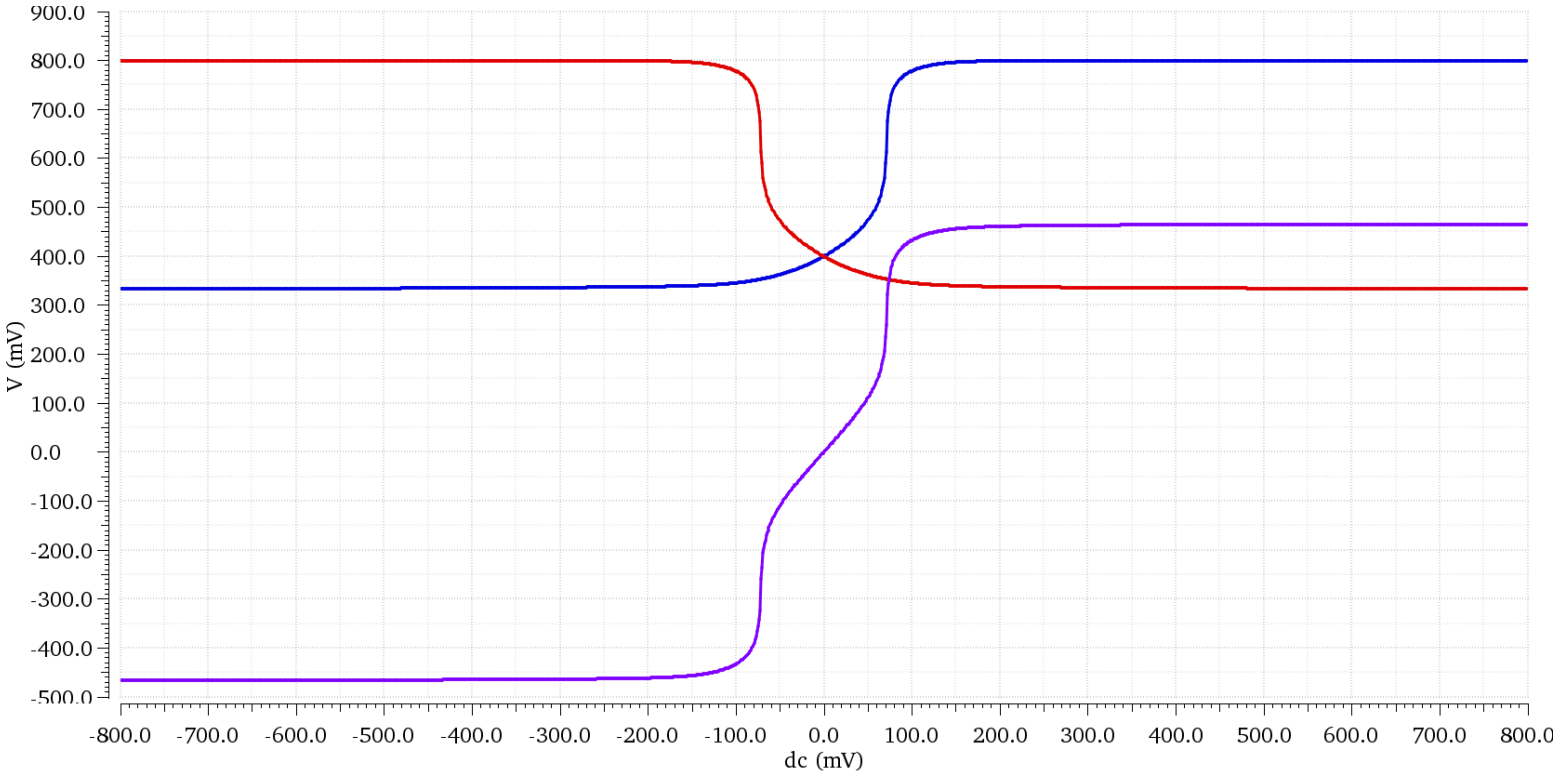


Figure 28: Large signal behaviour of the output nodes of the buffer. Red: V_o^-, blue: V_o^+, purple: $V_o^+ - V_o^-$.

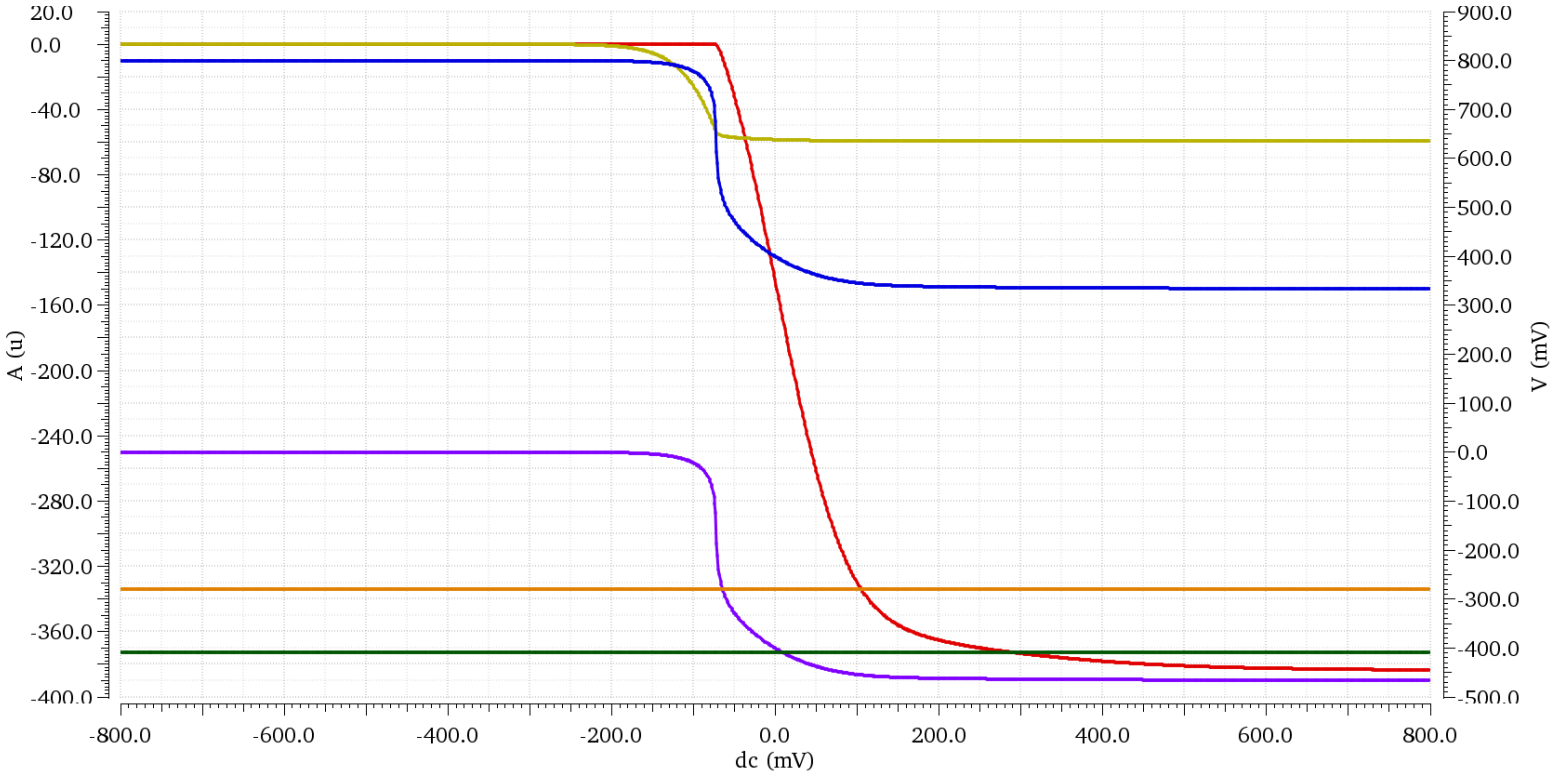


Figure 29: Large signal behaviour of the PMOS (P0) of the buffer. Red: $I_{D,P0}$, blue: V_o^-, purple: $V_{DS,P2} = V_{DS,P0} = V_{GS,P0}$, orange: $V_{DSsat,P2}$, green: $V_{TH,P0}$, yellow: $I_{D,P2}$.

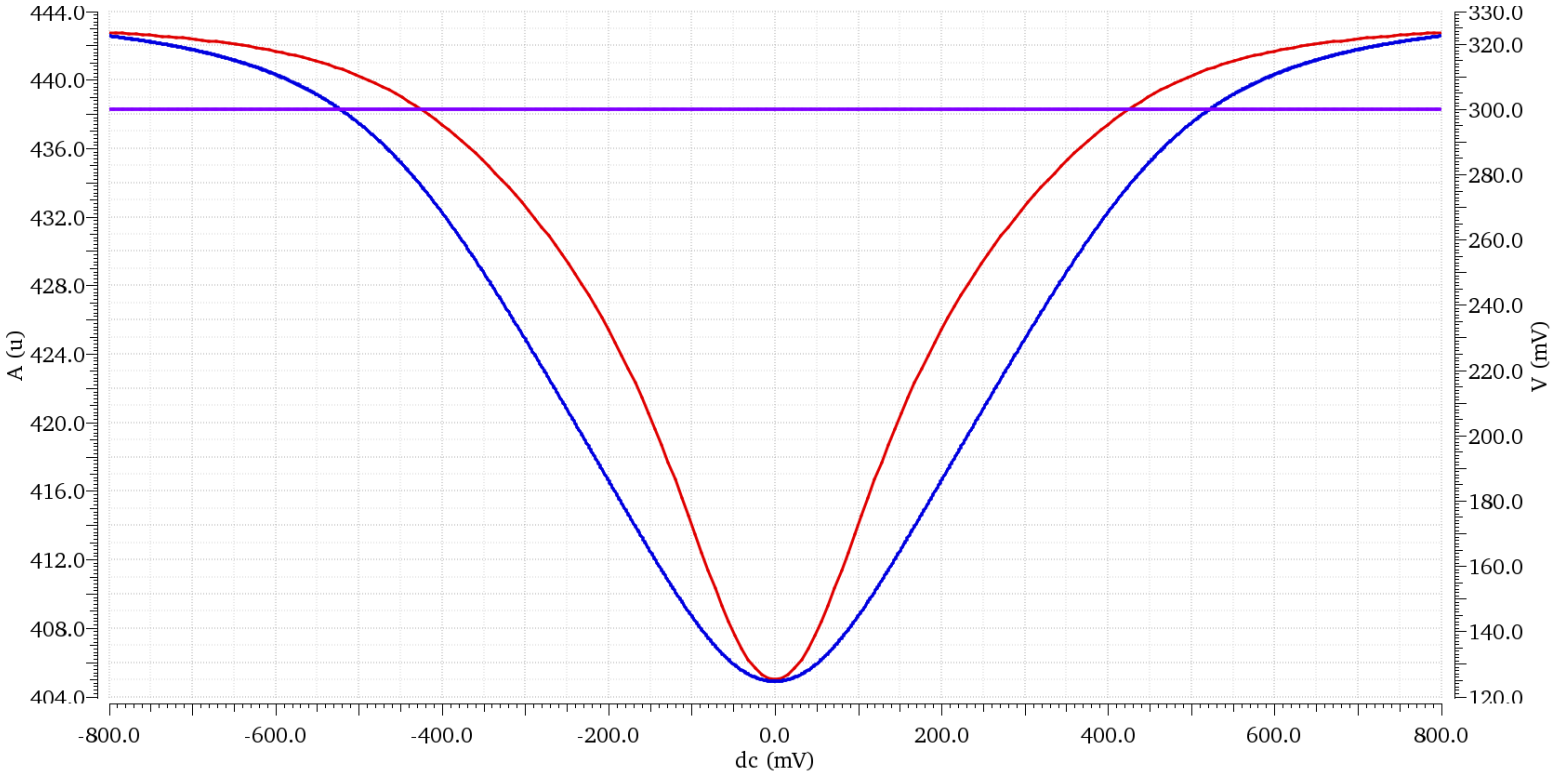


Figure 30: Large signal behaviour of tail NMOS (N0) of the buffer. Red: I_D, blue: V_{DS}, purple: V_{GS}.

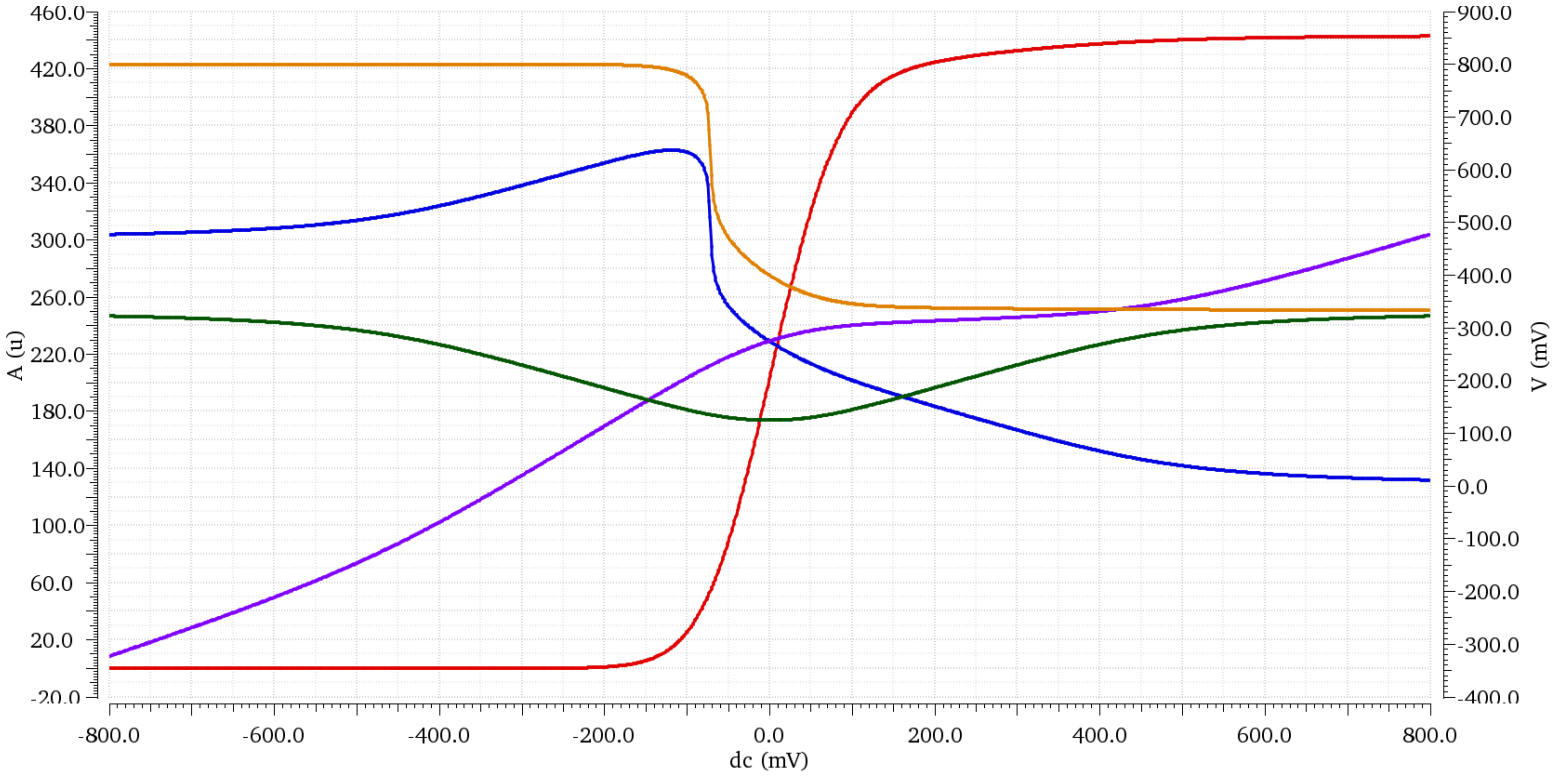


Figure 31: Large signal behaviour of the differential pair NMOS (N1) of the buffer. Red: I_D, blue: V_{DS}, purple: V_{GS}, orange: $V_D = V_o^-$, green: $V_S = V_{DS,N0}$.

Figure 30 shows the large signal behaviour of N0. It confirms the prediction that the tail current rises due to increasing V_{DS}. This effect is most prevalent around the bias point.

More interesting than the behaviour of N0 is that of the NMOS differential pair. Figure 31 shows the large signal behaviour of N1, which is in the same branch as P0. Again, the behaviour of N2 is similar, but mirrored.

Figure 31 displays the relevant signals for transistor N1. N1 starts switched off due to the a negative V_{GS} (purple), as the source voltage V_S (green) is larger that the gate voltage (which starts at 0 mV and ends at 800 mV). V_{DS} (blue) is sufficiently high, so the transistor can start conducting once V_{GS} surpasses 0 mV. V_o^- (orange) is the drain voltage V_D and is plotted for reference.

As the differential input voltage moves towards 0 mV V_{DS} swings up before going down rapidly. The upswing is caused by the drop of V_S, caused by the drop in $V_{DS,N0}$. The rapid drop in V_{DS} is caused by the drop in V_o^-, which was explained previously. I_D (red) doesn't seem to start conducting when V_{GS} becomes larger than 0 mV. The transistor is still deep in weak inversion and thus the current is too small to be visible on this scale. Due to the exponential nature of I_D in weak inversion, it soon becomes visible and I_D starts to rise. It does not seem to be affected by the rapid drop in V_{DS}, which is likely due to the fact that $V_{DS} > V_{DSsat}$ is still satisfied and because R_O is large.

As the differential input voltage moves away from 0 mV, $V_{DS,N0}$ starts to rise, thus increasing V_S for N1. The increase of V_{GS} is temporarily negated and V_{DS} starts to drop. As a result, I_D moves towards a stable value. V_S continues to rise until at some point V_{DS} drops V_{TH} below V_{GS}, at which point N1 enters triode.

In figure 32 the currents at node V_o^- are plotted, confirming that the sum of the currents through P0 and P2 is equal to the current through N1.

In the bias point a gain of 2.007 was measured (figure 33), which is close to the predicted value of 2.004.

5.2.2 Linearity

Derived in appendix A.4 is the linearity of the buffer around its bias point, using figure 33. The figure shows differential output voltage $v_{out}(v_{in})$ (red) and the differential with respect to the differential input voltage $\frac{\partial v_{out}}{\partial v_{in}}$, in other words the gain of the circuit. The derivation shows that an IIP3 of -13.56 dBV is achieved. The input voltage is at a maximum of 0.54 mV or -65.35 dBV. These numbers show that linearity of the buffer is not a limitation.

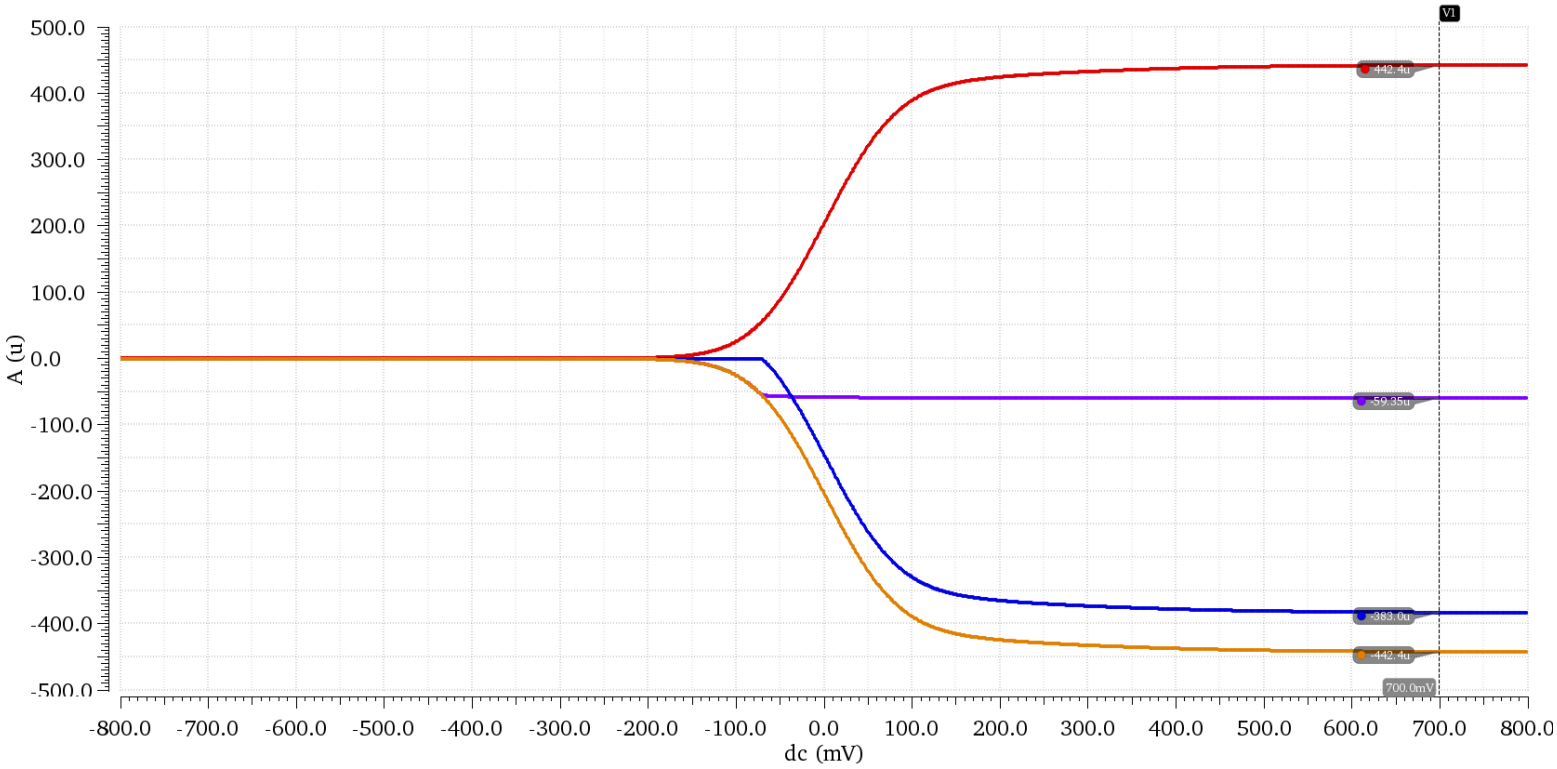


Figure 32: Currents through N1, P0 and P2 against differential input voltage. Red: $ID, N1$, blue: $I_{D,P0}$, purple: $I_{D,P2}$, orange: $I_{D,P0} + I_{D,P2}$.

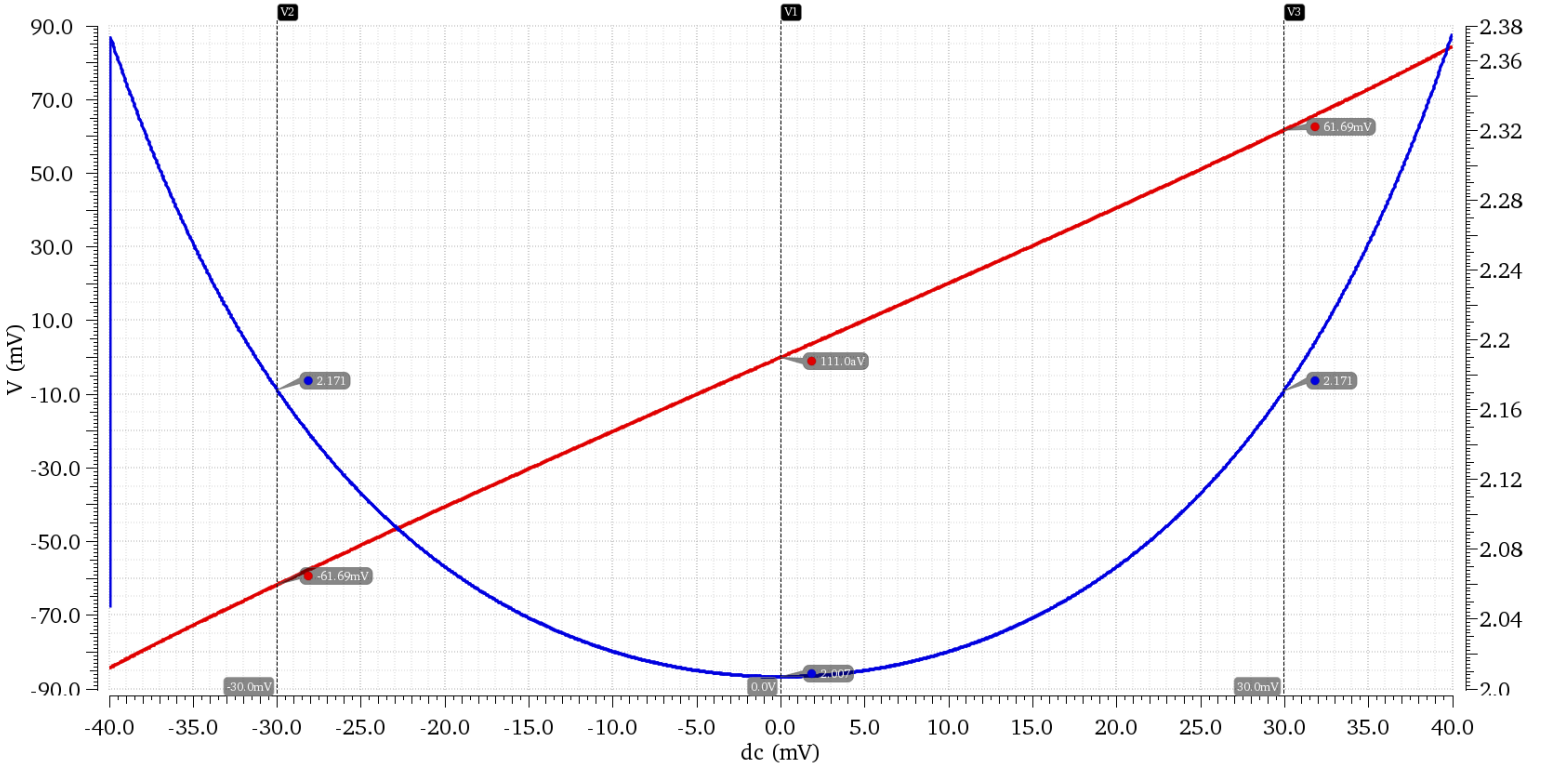


Figure 33: Differential output voltage (red) and gain (blue) around the bias point, against differential input voltage. Used for linearity calculations.

5.2.3 AC

The AC response of the buffer is expected to be flat up to a certain point, where it will start to drop due to the parasitic capacitances at the output nodes. Figure 35 confirms this behaviour. The -3dB point was measured to be at 1.89 GHz, which should be sufficient for this design as the ADC operates in baseband.

The design of [18] uses choppers to move the 1/f noise out of baseband. A similar approach is necessary in this case, because 1/f noise would be limiting the noise performance otherwise. For the buffer there is a large frequency range that can be used. In terms of gain, the range is a bit arbitrary. If, say, a gain deviation of 0.03 dB is allowed from the ideal 6.02 dB (2x gain), then the range is from DC up to 220 MHz.

5.2.4 Noise

Buffer noise is a cricital parameter in the design. As discussed in section 4.4.1, the noise should be below 3.086 $nV/\sqrt{Hz}$. Figure 36 shows the noise simulation, where the noise is plotted on a logarithmic axis. Chopping should move signal bandwidth out of the 1/f noise region, which ends somewhere between 1 MHz and 10 MHz.

In terms of the noise requirement of 3.086 $nV/\sqrt{Hz}$, that constraint is satisfied between 4.1 MHz and 7.6 GHz. A wide range, which has overlap with the previously mentioned range. A chopping frequency between 4.1 MHz and 220 MHz should be selected, taking into account that the bandwidth is 0.2 MHz.

Figure 34 shows the noise summary for the buffer. From this summary it can be concluded that the differential input pair is the main contributor for the noise, with the diode connected PMOS pair coming in second. This is as expected for a differential amplifier such as this buffer. It also demonstrates that the thermal noise is dominant at this point and that 1/f (flicker) noise is but a fraction of the total noise.

5.2.5 Results

A buffer was designed that achieves the tough noise requirement and a gain of 2. It achieves sufficient linearity for the given, relatively small input range. It does however consume a significant amount of static power. The bias tail current is 405 μV at a supply voltage of 0.8 V, equating to 324 μW power consumed in a buffer that is always active. This is a large power consumption compared to the 15.7 μW used by the entire ADC in [18]. In fact, state of the art baseband amplifiers with good linearity are available in the range of 100 to 200 μW [1], which could help reduce the noise requirements of the ADC significantly, allowing the use of an energy efficient one.

The above shows that the desire for an all passive approach, even in the ADC, is justified. The use of a buffer in [18] was a good option there, but in the case of this project it is not feasible, due to the power consumption that comes with it. If a passive solution for the noise shaping SAR were to be found it would be much more appealing.

Device	Param	Noise Contribution	% Of Total
/N2	therm_sid	1.15765e-06	18.85
/N1	therm_sid	1.15765e-06	18.85
/P1	therm_sid	9.11175e-07	11.68
/P0	therm_sid	9.11175e-07	11.68
N2.rgres	rn	8.62332e-07	10.46
N1.rgres	rn	8.62332e-07	10.46
/P3	therm_sid	6.59512e-07	6.12
/P2	therm_sid	6.59512e-07	6.12
P3.rgres	rn	3.29409e-07	1.53
P2.rgres	rn	3.29409e-07	1.53
P0.rgres	rn	2.65691e-07	0.99
P1.rgres	rn	2.65691e-07	0.99
/N2	therm_Rs	1.10661e-07	0.17
/N1	therm_Rs	1.10661e-07	0.17
/N2	flicker	8.75743e-08	0.11
/N1	flicker	8.75743e-08	0.11
/P0	flicker	4.45359e-08	0.03
/P1	flicker	4.45359e-08	0.03
/P3	flicker	4.07756e-08	0.02
/P2	flicker	4.07756e-08	0.02

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 2.66641e-06
Total Input Referred Noise = 1.33073e-06
The above noise summary info is for noise data

Figure 34: Noise summary of the buffer around 102 MHz, in a 200 kHz bandwidth

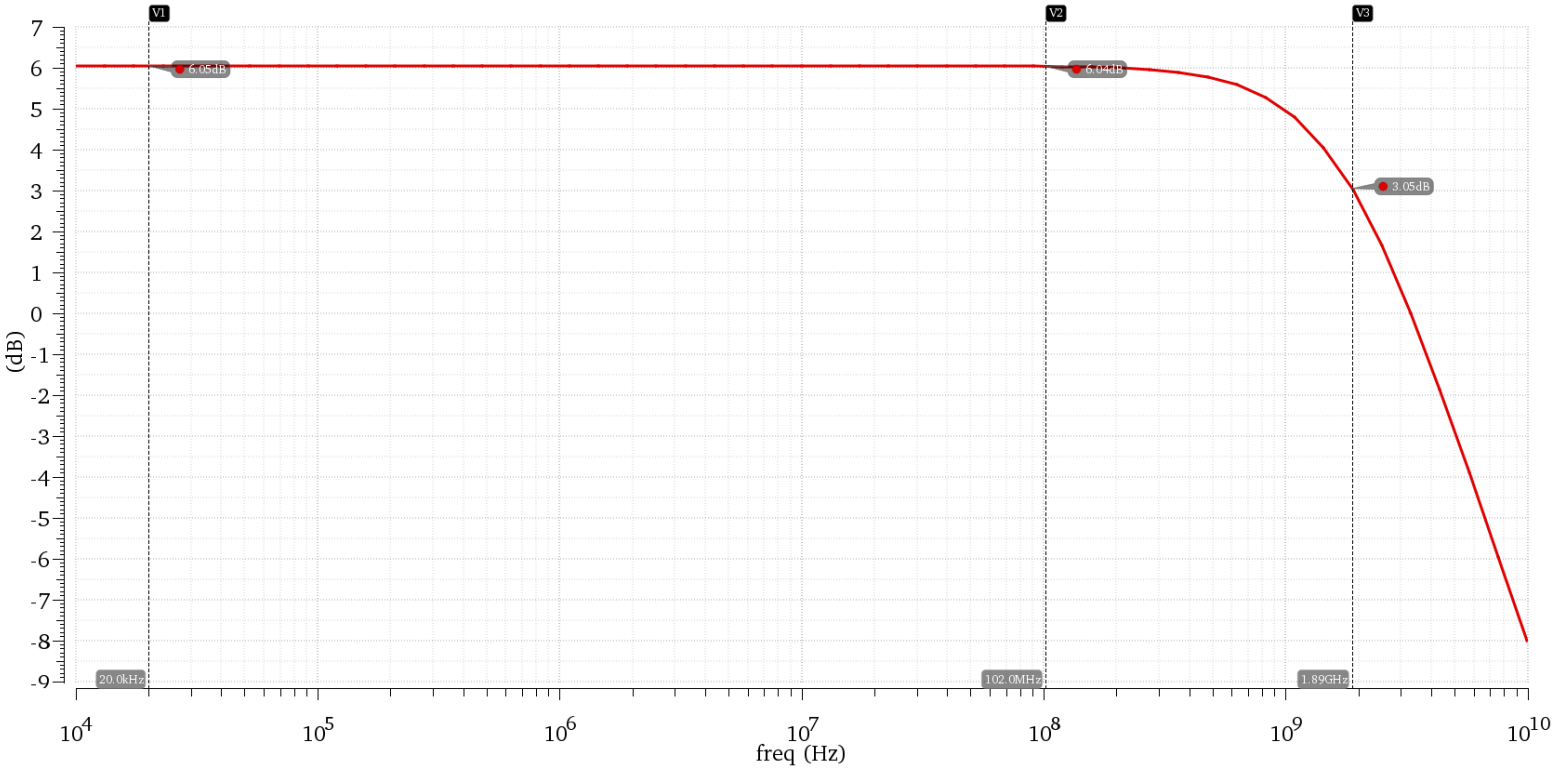


Figure 35: Buffer small signal simulation

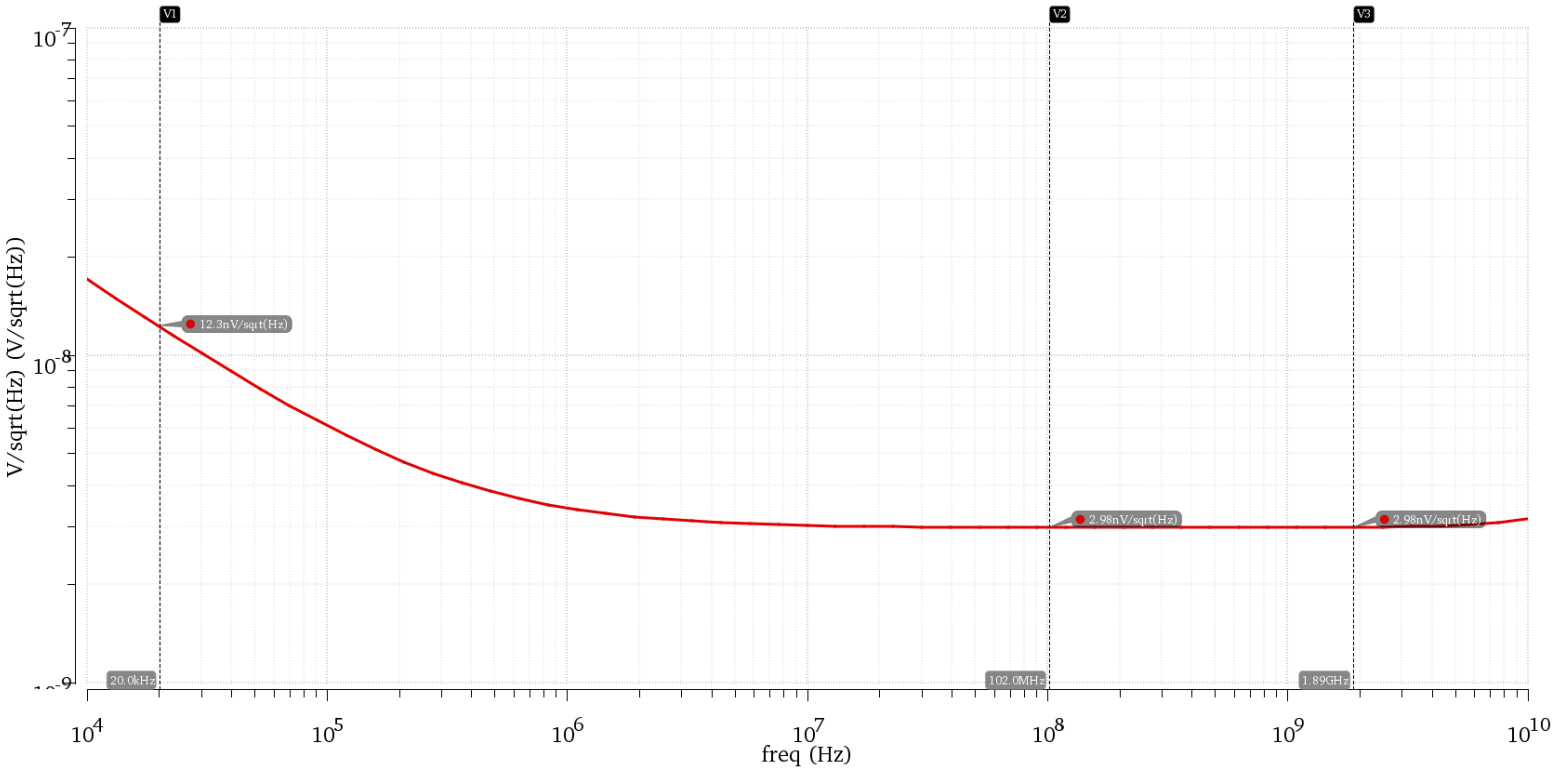


Figure 36: Noise simulation of the buffer

5.3 OpAmp schematic

Like the design of the buffer, the OpAmp design is also based on [18]. It uses a cascoded differential pair with active load, however, in the GF22nm headroom is smaller and R_{DS} is higher [**?**], so the use of a cascode is not necessary. Figure 37 displays the OpAmp design that was used. The small signal gain of this circuit is given by (39), derived in appendix A.7. From this equation two contraints can be deduced: $g_{m,N} \gg g_{ds,N}$ and $g_{m,N} \gg g_{ds,P}$, which should be kept in mind when biasing the transistors.

$$\frac{v_{out}^{+} - v_{out}^{-}}{v_{in}} = \frac{g_{m,N}}{g_{ds,N} + g_{ds,P}} \tag{39}$$

A gain of 37 dB is required, so:

$$\frac{g_{m,N}}{g_{ds,N} + g_{ds,P}} > 70.4 \tag{40}$$

5.3.1 Common mode levels

Similar to the buffer, the common mode levels of the OpAmp need to be well defined, input and output should be at 400 mV. The output of the OpAmp is used to drive the comparator, so any deviation in this level could lead to errors in at the comparator. In fact, the circuit requires a common mode feedback

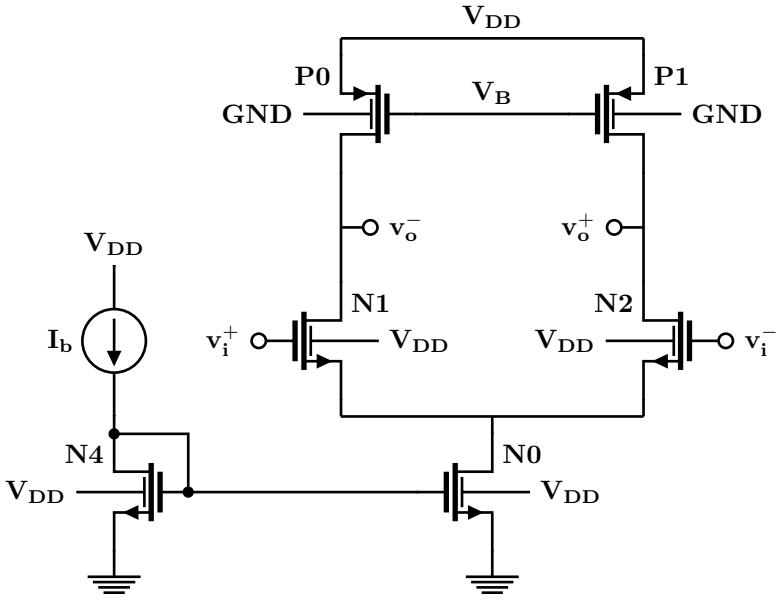


Figure 37: Behavioural model of the ADC architecture

from the output nodes to the PMOS bias voltage, such that the common mode level is stable. The common mode feedback circuit is outside the scope of this project, instead it is assumed that a stable common mode level can be generated at the output nodes.

5.3.2 Biasing

Biasing of the OpAmp was done is a similar fashion as the buffer. The tail transistor requires a V_{DS} roughly between 100 mV and 150 mV and the output nodes need to be at 400 mV. Ideally, the input NMOS pair is quite deep into weak inversion, such that a high g_m/I_D is achieved. For this reason the tail was designed for 150 mV V_{DS}. Given the input common mode level of 400 mV $V_{GS,N1}$ and $V_{GS,N2}$ well below the threshold voltage.

From equation 40 it can be deduced that R_{DS} should be high for both the NMOS and the PMOS. This is intrinsically the case for GF22nm, but can be improved by scaling L. Drawback in this case is that the capacitances should stay small to achieve sufficient bandwidth. As such, the scaling of L wasn't done to the extent as it was done in the buffer.

5.3.3 DC operating points

Given in table 12 are the DC operating points of the transistors in the OpAmp circuit. Most notable is the high g_m/I_D of N1 and N2, which was a design choice. Not only is weak inversion region beneficial for the g_m/I_D, but it also helps the noise, as that is lowest for transistors in weak inversion. The current was scaled to achieve the noise requirements. The output nodes are not exactly at 400 mV, but as mentioned before there should be a common mode feedback from the output to the PMOS gates, which should take care of that issue.

Filling in the numbers from table 12 into equation 39 yields an expected voltage gain of 61.22, or 35.74 dB. This falls short of the 70.4 or 37 dB that was required. $\kappa_A = 0.984$ is achieved in this case, resulting in a suppression of 42.4 dB at 256 times oversampling, where 43 dB was required.

	$\mathbf{V_{GS}}$	$\mathbf{V_{DS}}$	$\mathbf{V_{TH}}$	$\mathbf{I_D}$	$\mathbf{g_m}$	$\mathbf{g_{ds}}$	$\mathbf{g_m/I_D}$	**reg**
N0	300	150	355.6	48.02	929.7u	39.93u	19.36	WI
N1/N2	250	251.2	367.4	24.02	652.4u	7.003u	27.16	WI
P0/P1	-400	-398.6	-367.3	-24.01	344.7u	3.654u	14.36	SI
N4	300	300	333.9	0.5	10.97u	34.83n	21.9	WI

Table 12: OpAmp DC operating points. Voltages in mV, currents in μA, transconductances in S.

5.3.4 Sizing

For the OpAmp it was necessary to keep L closer to minimum length compared to the buffer. The NMOS were scaled to 80 nm, PMOS to twice this size. In order to satisfy contraints for the current through the transistors and the node voltages, W was sized by performing a sweep with the given node voltages and finding W for the right current. Table 13 gives an overview.

	W [um]	**L [nm]**	**W/L**	**m**	**type**	**V_{BB}**
N0	1.249	80	15.61	3	SLVT	V_{DD}
N1/N2	2.500	80	31.25	3	SLVT	V_{DD}
P0/P1	0.693	160	4.331	3	SLVT	GND
N4	0.184	320	0.575	1	SLVT	V_{DD}

Table 13: OpAmp device dimensions

5.4 OpAmp simulations

Verifying the behaviour of the OpAmp was done is a similar fashion as the buffer simulations. First the DC characteristics are determined by large signal simulations using a DC sweep. Next is a transient simulation to determine the settling behaviour. Then the AC behaviour is characterized with small signal simulations at the specified bias point. Last is a noise simulation to determine whether the noise specifications are met.

5.4.1 Large signal

Being a differential amplifier with active load it is expected that behaviour is similar to [p. 104][23]. P0 starts switched in triode, with V_o^- at 800 mV. As current starts flowing into the branch V_o^- drops, eventually switching on the PMOS. At some point $|V_{DS}| > |V_{GS} - V_{TH}|$, so P0 and P1 will go into strong inversion (as $|V_{GS}| > |V_{TH}|$ is always satisfied). At this point the current through the branch depends on R_{DS} and thus the increasing current will rapidly increase the voltage drop over P0, until it is limited by the headroom that the NMOS transistors N1 and N0 require.

N1 starts switched off, but gradually starts conducting current as it is in weak inversion. Around the bias point the voltage drop over P0 increases rapidly, eventually pushing N1 into triode. As the differential voltage increases even N0 gets pushed into triode, because the current cannot increase, as that would require V_o^- to drop further.

Figure 38 shows the DC sweep from -800 mV to 800 mV differential input voltage. A zoom around the bias point is provided in figure 39. The figures display the steep slope around the bias point, but also show the limited voltage

swing that can be applied to the input.

Measured was a gain of 35.73 dB, which is close to the expected value of 35.74 dB gain.

5.4.2 Linearity

The maximum input of the OpAmp is twice as large as that of the buffer, i.e. 0.108 mV (-59.33 dBV). This is still a very small number, so linearity should not be an issue. Regardless, the linearity of the OpAmp is derived in appendix A.7. Clearly a highly non-linear OpAmp was designed, because an IIP3 of only -38.42 dBV was achieved. Due to the low input voltages there is still roughly 20 dB margin and linearity should not be a problem.

5.4.3 Transient

In order to determine the settling behaviour of the OpAmp it was presented with an input step of 10 mV. From figure 41 it can be seen that settling happens between 5-10 ns after the input step. Similarly, it takes around the same amount of time to reach equilibrium after the step is removed. Rise and fall time of the input signal are 1 ps. The gain at a 10 mV input step is only 31.9 though, so it has dropped significantly at that point.

5.4.4 Small signal

The small signal gain is plotted in figure 42. The DC voltage gain is 35.7 dB, with a -3 dB point at 287 MHz. For the OpAmp it is necessary to employ chopping to circumvent 1/f noise as well. At 102 MHz the gain deviates 0.5 dB from the DC gain, so it is adviced to keep the chopping frequency below this when looking at the gain.

5.4.5 Noise

The result of noise analysis is given in figure 43. 1/f noise dominates up to roughly 10 to 100 MHz. According to the specification in 4.4.3 the noise should be below 8.22 $nV/\sqrt{Hz}$, which is easily satisfied by the OpAmp. The tail current could theoretically be reduced (resulting in higher noise), however, optimizing the performance of the OpAmp is not inside the scope of the project.

5.4.6 Conclusion

An OpAmp was designed to match the gain and noise requirements specified previously. In order to achieve these a static current of 48 μA was required at 0.8 V supply, leading to a static power consumption of 38.4 μW. This is a much more respectable number than that of the buffer, which is definitely the bottleneck in this design.

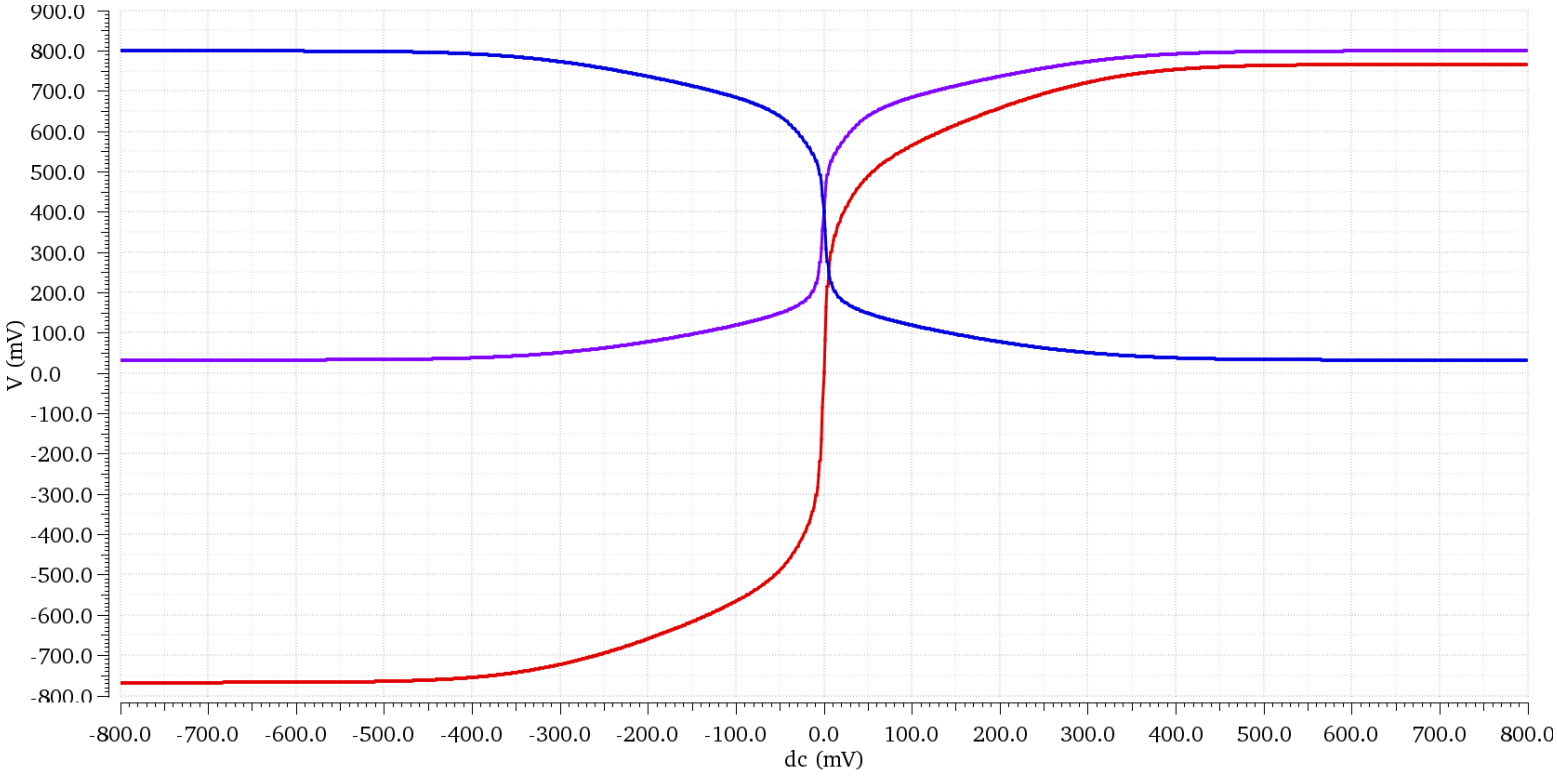


Figure 38: Large signal behaviour of the output nodes of the OpAmp. Red: $V_o^+ - V_o^-$, blue: V_o^-, purple: V_o^+.

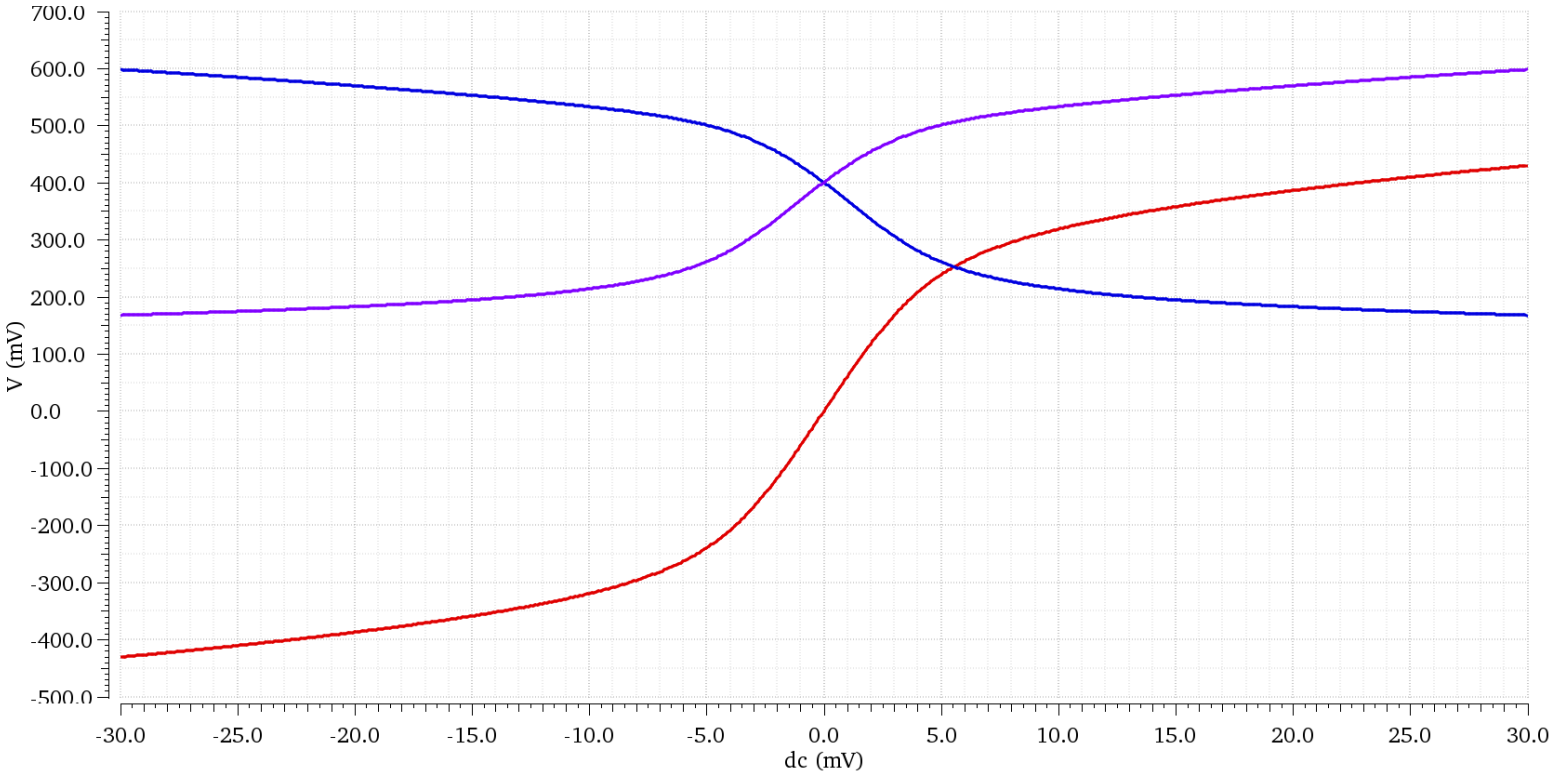


Figure 39: Large signal behaviour of the output nodes of the OpAmp around the bias point. Red: $V_o^+ - V_o^-$, blue: V_o^-, purple: V_o^+.

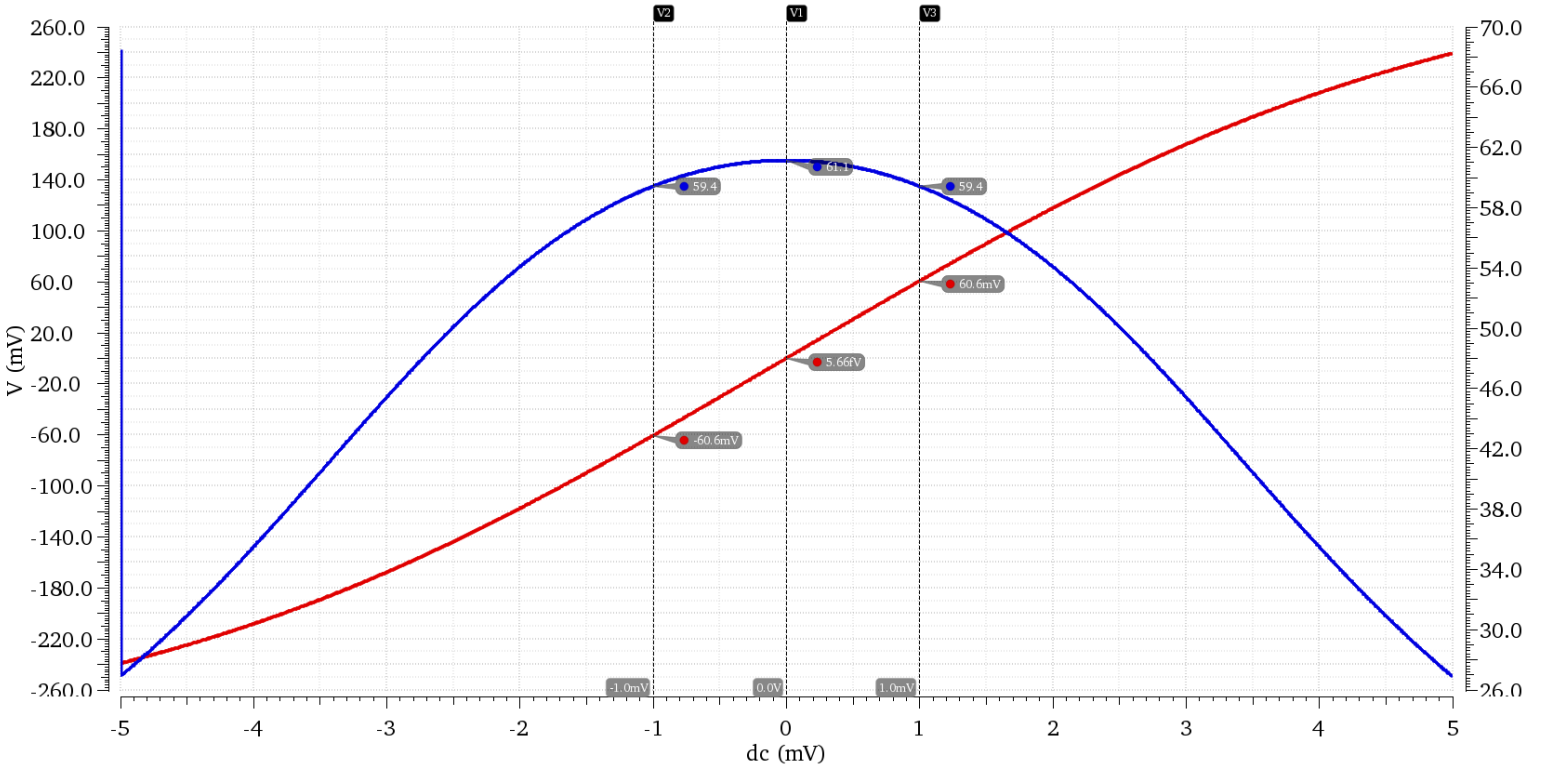


Figure 40: Differential output voltage (red) and gain (blue) around the bias point. Used for linearity calculations.

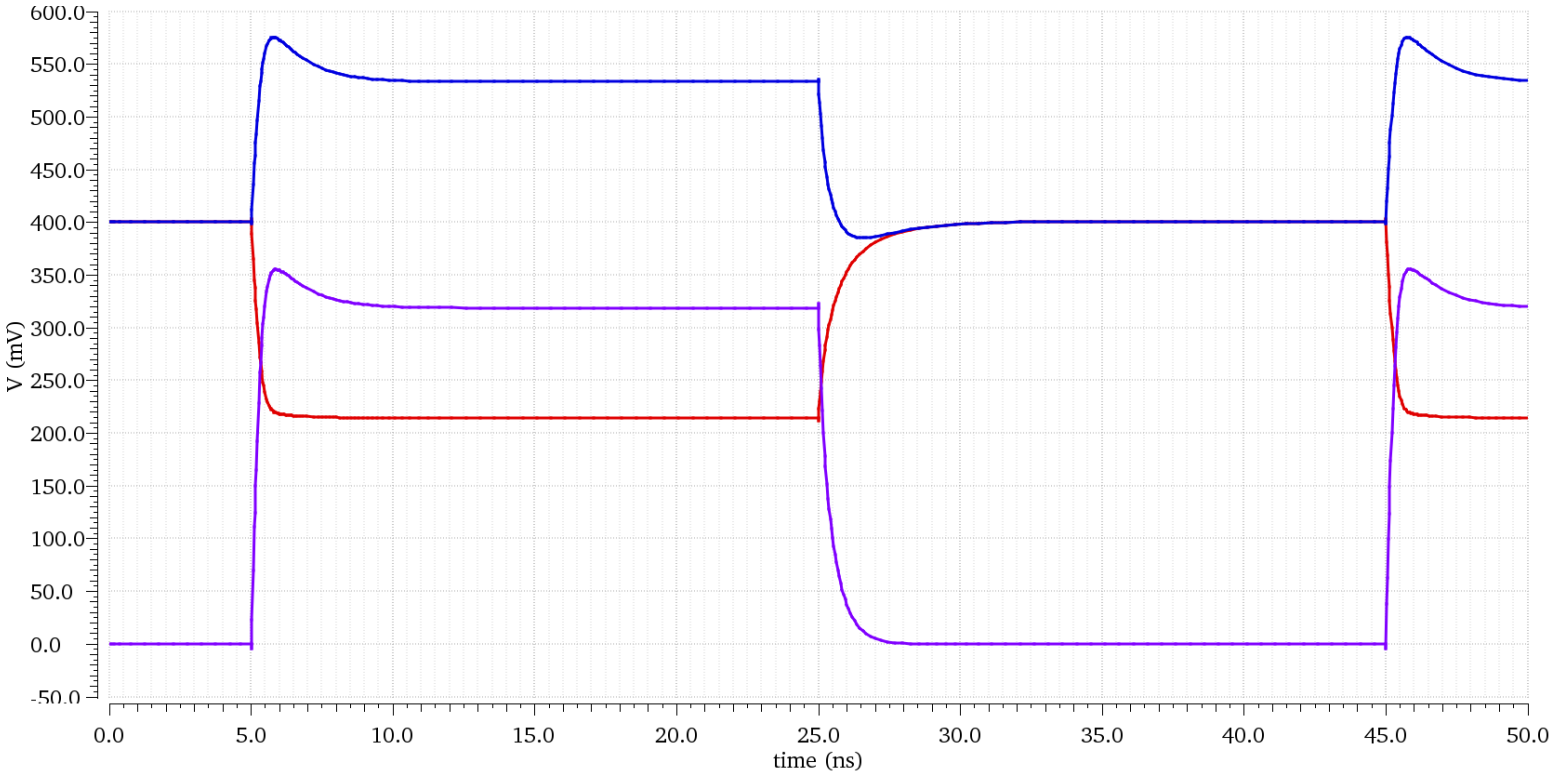


Figure 41: OpAmp settling behaviour when presented with an input step. Red: V_o^-, blue: V_o^+, purple: $V_o^+ - V_o^-$.

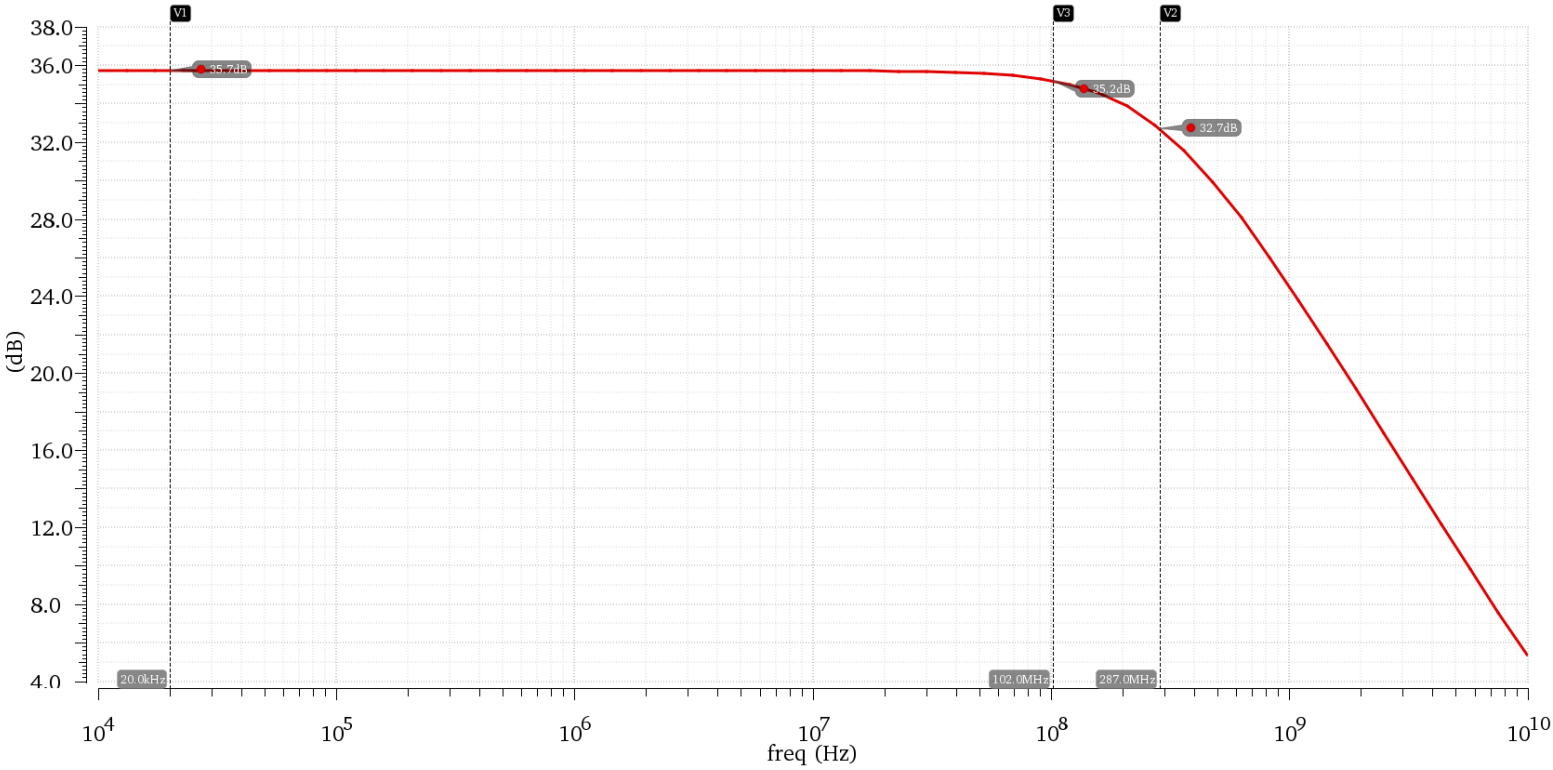


Figure 42: OpAmp small signal gain.

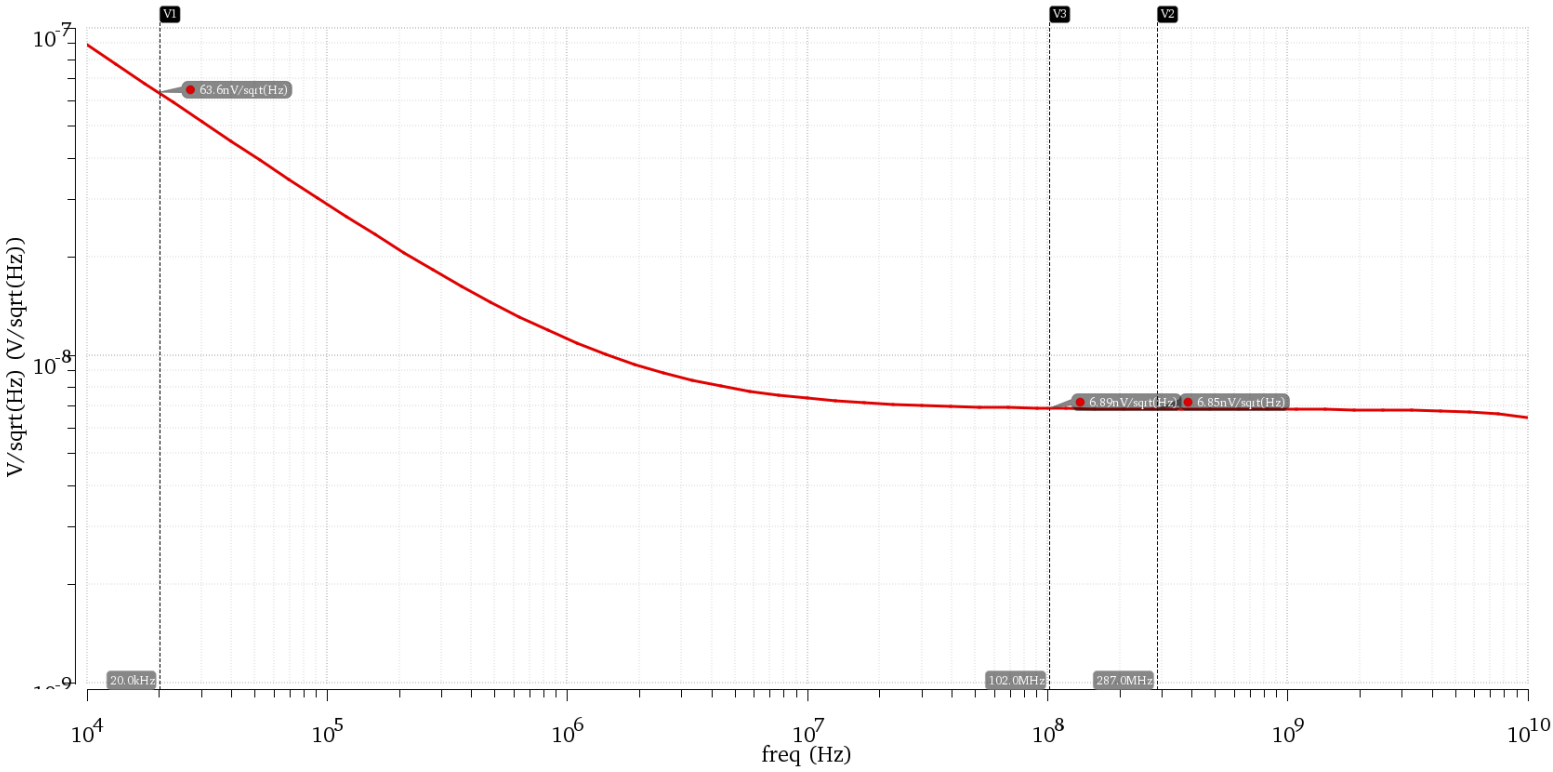


Figure 43: OpAmp input referred noise

6 Conclusions & Recommendations

Two main goals were set for this thesis. The first being a feasibility study of a mixer first receiver architecture with only a mixer and an ADC, preferably all passive. The context of this receiver was IoT applications, which leads to low signal levels and high interferer levels. With limited amplification in the receiver chain the requirements for the ADC turned out to be tough, especially on the part of noise. Ultimately, this led to the choice of the noise-shaping SAR architecture.

The second goal was to explore the noise-shaping SAR architecture, looking at the merits and drawbacks. System level analysis was performed, backed up by a transistor level implementation of the buffer and OpAmp blocks of the loop filter. These proved critical in terms of power consumption for the ADC, especially on the part of the buffer, due to the tough noise requirements.

In terms of feasibility the main conclusion was that although tough, the reuirements for the ADC are not impossible to achieve. The choice was made to go for a noise shaping SAR ADC, because it combines the energy efficiency of SAR and the noise shaping of the $\Sigma\Delta$ architectures. Combining a high OSR with noise shaping was theoretically sufficient to reduce comparator noise below the level of 1.38 μV in a 1.5 MHz bandwidth and allow a small input sampling capacitor to be used to circumvent detrimental charge sharing between the mixer output and the ADC input, which would negate the passive gain made in the mixer.

Upon further investigation of the noise shaping SAR it turned out that the active components in the loop filter are a bottleneck in the design due to the noise created in these blocks. The noise transfer functions of these individual blocks proved to benefit a lot less, if at all, from the noise shaping. As a result the buffer and OpAmp blocks had to achieve 3.086 $nV/\sqrt{Hz}$ and 8.22 $nV/\sqrt{Hz}$ respectiyvely. Transistor level simulations showed that a power consumption of 324 μW is required to achieve this level, which is high a supposedl energy efficienct ADC architecture. As such a passive solution for the loop filter is definitely desired, so further research into this would be recommended.

Linearity played a minor part in the design of the active components of the loop filter. Signal levels at the input are low, so high linearity is not necessary. Both the buffer and OpAmp reached sufficient linearity for the application.

A Appendix: Mathematical Derivations

A.1 FIR filter noise and capacitor size

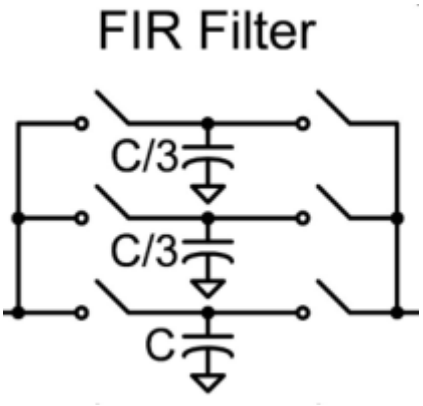


Figure 44: FIR structure, from [18]

Figure 44 shows the FIR filter as it is implemented in [18]. The structure is made up of three separate capacitors, each of which produces kT/C noise (which is affected by oversampling). The top two capacitors produce noise power equal to 3kT/C, while the bottom one produces kT/C. Assuming the noise is uncorrelated (it is, because each switch has a different clock input) the noise powers can be added up, leading to 7kT/C as total noise. This demonstrates that the size of C should be 7 times the size of that of the total SAR DAC capacitance.

The above derivation neglects the fact that the FIR noise is attenuated by the buffer, by a factor 2 (see 4.4.2), so in fact a factor 3.5 would suffice.

A.2 Loop filter noise transfer functions

From figure 45 equation 41 can be derived (where quantization and comparator noise are left out for clarity). After that the NTF for each noise component is derived by simply rewriting and taking partial derivatives.

$$D_{OUT} = V_{IN} + V_{IN}L(z) - D_{OUT}L(z) + v_{n,b}L(z) + v_{n,F}\frac{1}{2}L(z) + v_{n,I}\frac{1}{1-z^{-1}} \tag{41}$$

$$D_{OUT}(1 + L(z)) = V_{IN}(1 + L(z)) + v_{n,b}L(z) + v_{n,F}\frac{1}{2}L(z) + v_{n,I}\frac{1}{1-z^{-1}} \tag{42}$$

$$D_{OUT} = V_{IN} + v_{n,b}\frac{L(z)}{(1 + L(z))} + v_{n,F}\frac{\frac{1}{2}L(z)}{(1 + L(z))} + v_{n,I}\frac{\frac{1}{1-z^{-1}}}{(1 + L(z))} \tag{43}$$

$$NTF_b = \frac{\partial D_{OUT}}{\partial v_{n,b}} = \frac{L(z)}{1 + L(z)} = \frac{2\left(z^{-1} + \frac{1}{3}z^{-2}\right)}{1 + z^{-1} + \frac{1}{3}z^{-2}} \tag{44}$$

$$NTF_F = \frac{\partial D_{OUT}}{\partial v_{n,F}} = \frac{\frac{1}{2}L(z)}{1 + L(z)} = \frac{\left(z^{-1} + \frac{1}{3}z^{-2}\right)}{1 + z^{-1} + \frac{1}{3}z^{-2}} \tag{45}$$

$$NTF_F = \frac{\partial D_{OUT}}{\partial v_{n,I}} = \frac{\frac{1}{1-z^{-1}}}{(1 + L(z))} = \frac{1}{1 + z^{-1} + \frac{1}{3}z^{-2}} \tag{46}$$

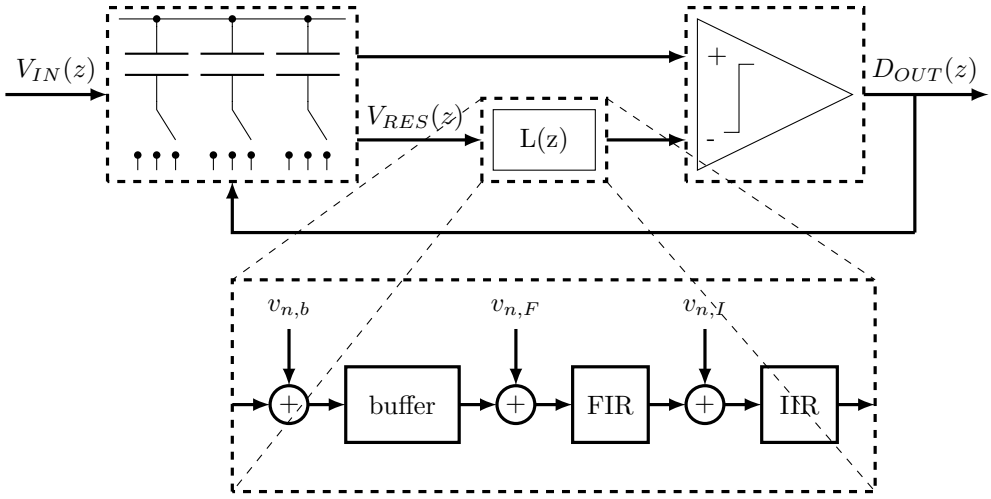


Figure 45: Noise shaping SAR architecture, similar to [17, fig.6]

A.3 Buffer small signal gain

Given in figure 46a is the simplified buffer schematic, i.e. without the current mirror. For this analysis it is assumed that the sides are balanced, so node V_X can be viewed as a virtual ground node. The branchs can be analyzed separately, where one side is excited by $+v_{in}/2$ and the other half by $-v_{in}/2$.

The small signal equivalent circuit of one branch is given in figure 46b. From this figure the following equations can be derived, where $v_{in}^{+} = +v_{in}/2$.

$$i_{P0} = -(v_{G,P0} - v_{S,P0}) \cdot g_{m,P0} \tag{47}$$
$$= -v_{out}^{-} \cdot g_{m,P0} \tag{48}$$

$$i_{N1} = (v_{G,N1} - v_{S,N1}) \cdot g_{m,N1} \tag{49}$$
$$= v_{in}^{+} \cdot g_{m,N1} = \frac{1}{2} v_{in} \cdot g_{m,N1} \tag{50}$$

Knowing that i_{P0} and i_{N1} must be equal, a transfer function from input to output can be derived.

$$-v_{out}^{-} \cdot g_{m,P0} = \frac{1}{2} v_{in} \cdot g_{m,N1} \tag{51}$$

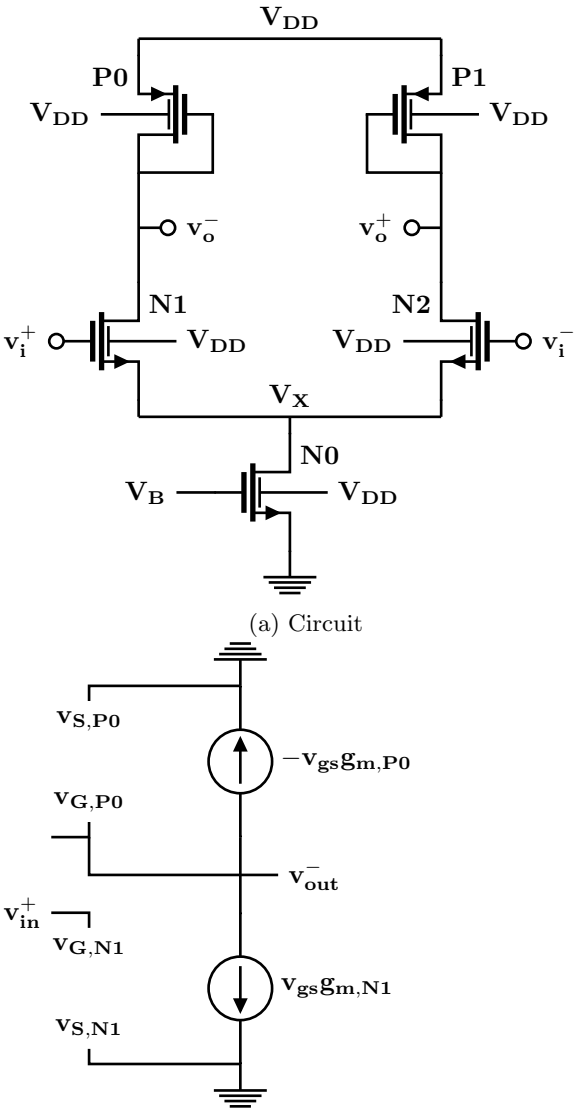
$$\frac{v_{out}^{-}}{v_{in}} = -\frac{1}{2} \cdot \frac{g_{m,N1}}{g_{m,P0}} \tag{52}$$

A similar derivation can be done for the other branch, resulting in (53).

$$\frac{v_{out}^{+}}{v_{in}} = \frac{1}{2} \cdot \frac{g_{m,N2}}{g_{m,P1}} \tag{53}$$

Knowing that the sides are balanced: $g_{m,N1} = g_{m,N2} = g_{m,N}$ and $g_{m,P0} = g_{m,P1} = g_{m,P}$.

$$\frac{v_{out}^{+} - v_{out}^{-}}{v_{in}} = \frac{1}{2} \cdot \frac{g_{m,N2}}{g_{m,P1}} - \left(-\frac{1}{2} \cdot \frac{g_{m,N1}}{g_{m,P0}} \right) \tag{54}$$
$$= \frac{g_{m,N}}{g_{m,P}} \tag{55}$$



(a) Circuit

(b) Small signal equivalent

Figure 46: Simplified buffer schematic

A.4 Buffer small signal gain with output resistances

Figure 47 shows the small signal equivalent of figure 46a, with one difference compared to figure 46b: the output resistance of the transistors is now included. This means that the output resistance of the bleeding current source should be considered as well, which in P2 in the case of figure 47. Derivation is similar to the one in the previous section.

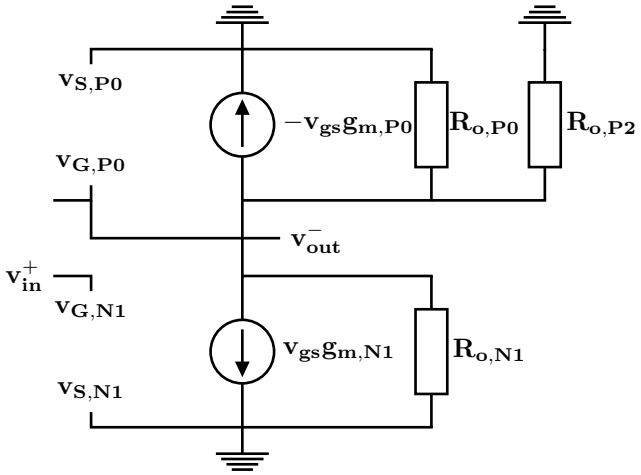


Figure 47: Small signal equivalent

$$i_P = -(v_{G,P0} - v_{S,P0}) \cdot g_{m,P0} - \frac{v_{out}^-}{R_{o,P0}} - \frac{v_{out}^-}{R_{o,P2}} \tag{56}$$

$$= -v_{out}^- \cdot (g_{m,P0} + g_{ds,P0} + g_{ds,P2}) \tag{57}$$

$$i_{N1} = (v_{G,N1} - v_{S,N1}) \cdot g_{m,N1} + \frac{v_{out}^-}{R_{o,N1}} \tag{58}$$

$$= v_{in}^+ \cdot g_{m,N1} + v_{out}^- \cdot g_{ds,N1} = \frac{1}{2} v_{in} \cdot g_{m,N1} + v_{out}^- \cdot g_{ds,N1} \tag{59}$$

Again, i_P and i_{N1} must be equal, so the transfer function on one branch can be derived.

$$-v_{out}^- \cdot (g_{m,P0} + g_{ds,P0} + g_{ds,P2}) = \frac{1}{2} v_{in} \cdot g_{m,N1} + v_{out}^- g_{ds,N1} \tag{60}$$

$$-v_{out}^- \cdot (g_{m,P0} + g_{ds,P0} + g_{ds,P2} + g_{ds,N1}) = \frac{1}{2} v_{in} \cdot g_{m,N1} \tag{61}$$

$$\frac{v_{out}^-}{v_{in}} = -\frac{1}{2} \cdot \frac{g_{m,N1}}{(g_{m,P0} + g_{ds,P0} + g_{ds,P2} + g_{ds,N1})} \tag{62}$$

Through the same reasoning as in the previous section the final transfer function becomes (63), where $g_{ds,PB}$ is comes from the bleeding current sources P2 and P3.

$$\frac{v_{out}^+ - v_{out}^-}{v_{in}} = \frac{g_{m,N}}{(g_{m,P} + g_{ds,P} + g_{ds,PB} + g_{ds,N})} \tag{63}$$

A.5 Buffer linearity

Linearity of the buffer is derived. Markers in figure 33 show that at the bias point there is a gain of 2.007 and at ±30 mV there is a gain of 2.171. A quadratic relation is assumed for the sake of this derivation, i.e. it is assumed that there is only third order distortion present in this simulation. v_{out} is given by (64).

$$v_{out} = \alpha_1 v_{in} + \alpha_3 v_{in}^3 \tag{64}$$

$$\frac{\partial v_{out}}{\partial v_{in}} = \alpha_1 + 3\alpha_3 v_{in}^2 \tag{65}$$

It is obvious that α_1 should be 2.007. At 30mV input voltage the gain deviates 0.164 from α_1, so:

$$3\alpha_3 \cdot 0.03^2 = 0.164 \tag{66}$$

$$\alpha_3 = \frac{0.164}{3 \cdot 0.03^2} = 60.74 \tag{67}$$

At the IIP3 the wanted signal and the third order term are equal, as in (69) [25, p. 40].

$$20log(\alpha_1 A) = 20\log\left(\frac{3}{4}\alpha_3 A^3\right) \tag{68}$$

Rearranging and solving for A yields (70)

$$A = \sqrt{\frac{4 \cdot 2.007}{3 \cdot 60.74}} = 0.210 \tag{69}$$

$$20\log(A) = 20\log(0.210) = -13.56\ dBV \tag{70}$$

Thus the IIP3 of the buffer is -13.56 dBV.

A.6 OpAmp small signal gain

Given in figure 48a is the simplified OpAmp schematic, i.e. without the current mirror. For this analysis it is once again assumed that the sides are balanced, so node V_X can be viewed as a virtual ground node.

The small signal equivalent circuit of one branch is given in figure 48b. It is easy to see that $R_{ds,P0}$ and $R_{ds,N1}$ are in parallel. Given that $v_{in}^{+} = {}^{v_{in}}/_{2}$, the following equations can be derived.

$$v_{out}^{-}\left(\frac{1}{R_{ds,P0}} + \frac{1}{R_{ds,N1}}\right) = -\frac{1}{2}v_{in}^{+} \cdot g_{m,N1} \tag{71}$$

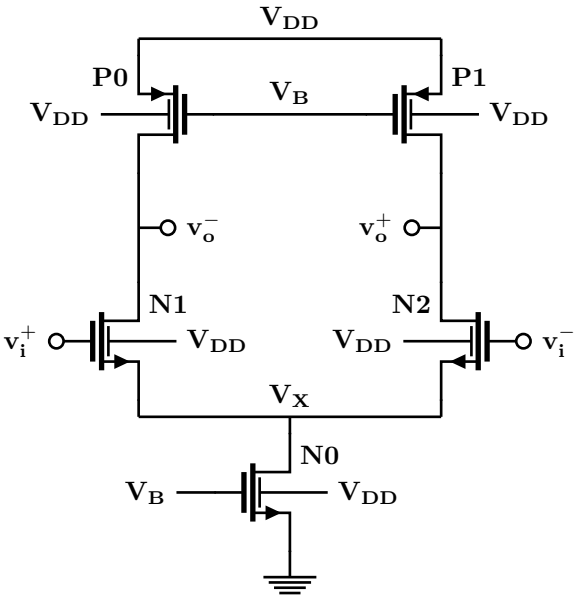
$$\frac{v_{out}^{-}}{v_{in}} = -\frac{1}{2} \cdot \frac{g_{m,N1}}{g_{ds,N1} + g_{ds,P0}} \tag{72}$$

A similar derivation can be done for the other branch, resulting in (73).

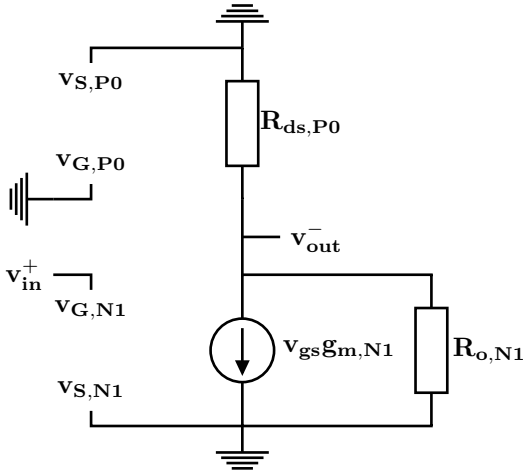
$$\frac{v_{out}^{+}}{v_{in}} = \frac{1}{2} \cdot \frac{g_{m,N1}}{g_{ds,N1} + g_{ds,P0}} \tag{73}$$

Knowing that the sides are balanced:

$$\frac{v_{out}^{+} - v_{out}^{-}}{v_{in}} = \frac{g_{m,N}}{g_{ds,N} + g_{ds,P}} \tag{74}$$



(a) Circuit



(b) Small signal equivalent

Figure 48: Simplified OpAmp schematic

A.7 OpAmp linearity

A similar derivation as that in appendix A.5. It is once again assumed that only third order distortion is present. From the markers in figure 40 the following numbers can be read. At the bias point (0 mV) there is a gain of 61.1, while at ±1 mV the gain is 59.4. The equations are similar to (**??**) and (65), though in this case there is a negative coefficient.

$$v_{out} = \alpha_1 v_{in} - \alpha_3 v_{in}^3 \tag{75}$$

$$\frac{\partial v_{out}}{\partial v_{in}} = \alpha_1 - 3\alpha_3 v_{in}^2 \tag{76}$$

α_1 equals 61.1, while at 1 mV the gain deviates -0.7 from it.

$$-3\alpha_3 \cdot 0.001^2 = -1.7 \tag{77}$$

$$\alpha_3 = \frac{1.7}{3 \cdot 0.001^2} = 5.67 \cdot 10^5 \tag{78}$$

At the IIP3 the wanted signal and the third order term are equal, as in (79) [25, p. 40].

$$20log(\alpha_1 A) = 20\log\left(\frac{3}{4}\alpha_3 A^3\right) \tag{79}$$

Rearranging and solving for A yields (80)

$$A = \sqrt{\frac{4 \cdot 61.1}{3 \cdot 5.67 \cdot 10^5}} = 0.012 \tag{80}$$

$$20\log(A) = 20\log(0.012) = -38.42\ dBV \tag{81}$$

Thus the IIP3 of the buffer is -38.42 dBV.

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