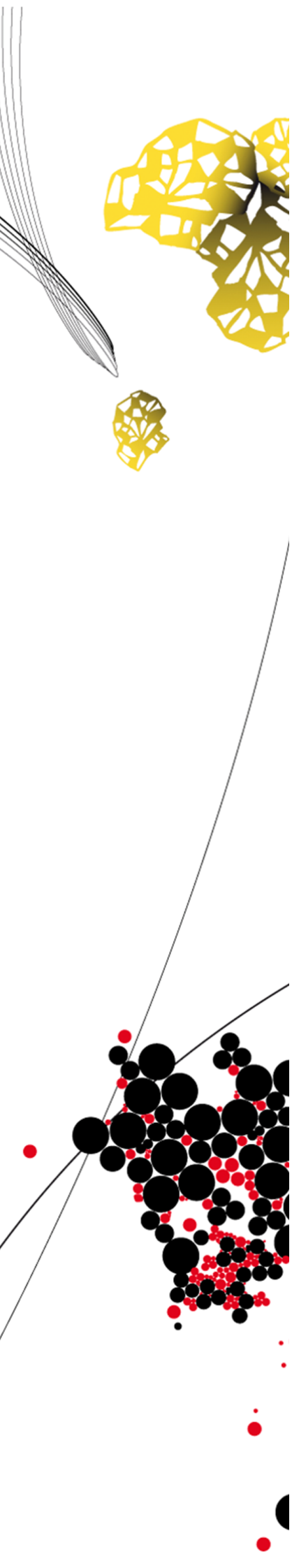

UNIVERSITY OF TWENTE.

Faculty of Electrical Engineering, Mathematics & Computer Science

Comparison of divide-by 2 circuits for clocks used in mixers

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B.Sc. Thesis

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Preface

Clock generation circuits can be made in a variety of ways. The IC-Design group of the University of Twente made multiple designs in FDSOI technology. The goal of this project is to compare two divide-by 2 circuits of clocks used in mixers. These circuits have been designed for different objectives such as the frequency of operation, power and phase noise. The main goal is to analyze which circuit is the most up-and-coming for low-power RF front-ends. The end result will give a fair comparison of the strengths and weaknesses and will be useful for future implementations of these circuits. I would like to thank Vijay Purushothaman and Eric Klumperink for helping me by providing information and giving insight to the topic.

Bachelor Assignment Committee

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Summary

Many mixers in radio receivers use quadrature mixers with 25% duty cycle clock inputs with ideally no overlap. Two clock generation circuits capable of making these desired clock inputs used within the IC-Design group can be split up in 3 stages which are shown below:

- Amplification and clipping stage
- Divider stage
- 25% duty cycle stage

The purpose of this thesis is to compare the two divider stages of both implementations. These two dividers can be distinguished based on their implementation. One is called the static divider and the other is called the dynamic divider. The names come from the use of either static or dynamic latches. One circuit is a flip-flop with static latches and the other one uses a shift register with dynamic latches. The dividers are designed for certain objectives such as operating frequency range, power consumption and phase noise. Due to time limitations only power consumption and operating frequency range are discussed. The circuits are used in RF front-ends so they have to meet certain boundary conditions. The boundary conditions for the clock generation circuit are set so that the output signals have to be full swing and the duty cycle has to be between 23% and 26%.
Circuit theory is used to analyse the circuits. To determine the power consumption of a circuit the load capacitance has to be known. The MOSFET capacitance model is used to determine the in- and output capacitances of the circuits. Adding the in- and output capacitances of the circuits will end up in the load capacitance of a stage. Because these implementations behave differently a comparison method has to be developed. First the amplification/clipping stage should be the same such that only the input capacitance of the divider is influencing the load of the amplification/clipping stage. Also the 25% duty cycle stage should have the same input capacitance. This will cause the divider to always have the same load capacitance. The load capacitance is determined by splitting up the circuit into multiple smaller circuits.
It's determined that the dynamic divider has a bigger input capacitance than the

static divider which means that it is a bigger load capacitance for the amplification/clipping stage demanding for more power from the source. Also the output capacitance of the dynamic divider is bigger such that it has to charge more load capacitance. This means that the dynamic divider has more power consumption in the circuit. The power consumption of the stages is also simulated and verifies the found conclusions. The ratio found for the load capacitances between the circuits only differs less than 8% from the power consumption ratio.
Also operating output frequency range is compared using the boundary conditions. Where the static divider consumes less power it will only work to 6.5 GHz where the dynamic divider implementation works up to 10GHz.

Contents

Chapter 1

Introduction

1.1 Motivation

Many mixers in radio receivers use quadrature mixers with 25% duty cycle clock inputs with ideally no overlap. Two implementations of this divide-by 2 circuit are made by the IC-Design group. These circuits uses different implementations and are designed for different objectives. This bachelor assignment targets to find a way to to make a fair comparison between the circuits and draw meaningful conclusions on power dissipation and operating frequency range. Using the PHD thesis about 'Switched-RC Beamforming Receivers in Advanced CMOS' [1] of Michiel Soer and the theory of the book 'Digital Integrated Circuits' [2] by Jan M.Rabaey the circuits are analysed and discussed.

1.2 Goal of the assignment and research questions

Figure 1.1 shows the main overview of clock generation circuits with the different stages. These clocks can be used for quadrature mixers which need a 25% duty cycle clock input. The divider divides two 50% duty cycle clocks into four 50% duty cycle clocks at half the input frequency. With only one single-phase sinusoidal signal the circuit would not be able to generate four accurate signals with different phases. The solution for this problem is to apply external sinusoidal clocks at two times the output frequency. The amplification stage uses these external sine wave signals to make the 50% duty cycle clock with full swing used by the divider stage. The last stage of the clock generation circuit uses the four 50% duty cycle clocks of the divider to produce a 4-phase 25% duty cycle clock.

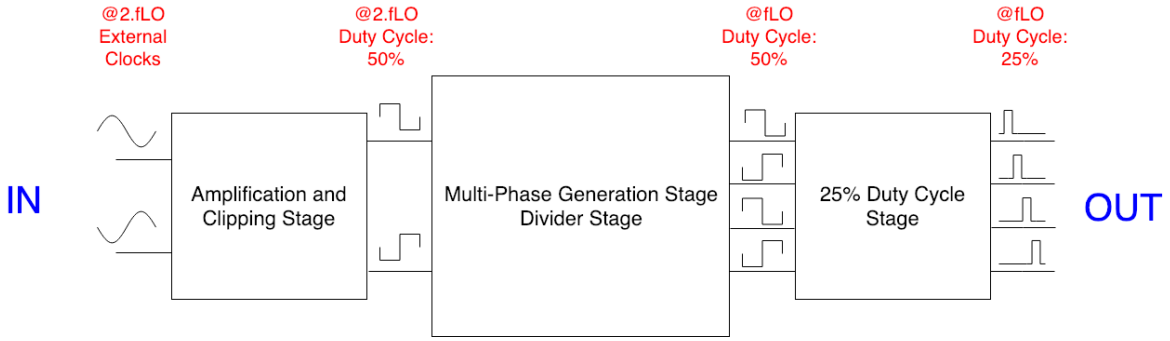

Figure 1.1: Main overview of the system with the different stages

This thesis focuses mainly on the divider stage implementation. The two implementations that are discussed are mostly designed for objectives such as operating frequency, power consumption and phase noise. Due to time limitations only power consumption and operating frequency range are analyzed and discussed. The goal is to develop a comparison method such that conclusions about the two implemented dividers can be made in relation to the points mentioned above. The following research questions are answered in this thesis.

- In what way can the two divider implementations fairly be compared?
- Which of the two implementations consumes more power and why?
- What are the operating frequency ranges of the circuits?

1.3 Boundary conditions for comparison

In order to analyze the circuits certain parameters have to be compared. To decide which parameters have to be examined, it is important to know what the circuits are used for. Clock generation circuits are used in RF front-ends. Certain boundary conditions have to be met for the stages later on to work. With the help of the committee boundary conditions are set. The requirements are shown below.

- The output should have a full swing
- The duty cycle of the output should be between 23% and 26%

The output signal amplitude has to be full swing because otherwise it can't produce the power needed for the next stage. The duty cycle is the next parameter that has to be examined. The range of the duty cycle has to be set around the ideal value. There are four clocks so the ideal value would be 25%. The system is obviously not ideal so compromises have to be made. Lower percentage duty cycle signals are preferred by the mixer to prevent overlap.

1.4 Report organization

The remainder of this report is organized as follows. First, chapter 2 discusses the theory used in this thesis. It describes the inverter, NAND gates and latches used in the researched circuits. This chapter also explains the dynamic power consumption and its relationship with load capacitance. This chapter finishes with the capacitances of circuits and how they change if multiple circuits are connected to each other.
Next, Chapter 3 examines the researched clock generation circuits. Each circuit is separated into three different stages which are explained in depth.
In Chapter 4, the method to compare the divider circuits is discussed. It shows how to compare the power consumption by determining the load capacitance of the stages and how simulations are used to verify the obtained values. It also explains how the operating frequency range is determined by examining the behavior of the power consumption, duty cycle and rise and fall time over frequency.
Chapter 5 discusses the results of the comparison using the method of Chapter 4.
Finally, Chapter 6 presents the conclusions along with recommendations for future research.

Chapter 2

Theory

2.1 Power consumption and load capacitance

Circuits consume power, this is caused by charging and discharging of capacitances. An estimation of energy consumption of the circuit can be derived when discussing the CMOS inverter. Let's first consider a low-to-high transition. In the ideal world the input waveform has no rise time which means that the NMOS and PMOS are never on at the same time. Figure 2.1 shows an equivalent circuit during this low-to-high transition. *"Each time the voltage rises from 0 to V_{DD} the load capacitor C_L gets charged through the PMOS transistor and a certain amount of energy is drawn from the power supply. Part of this energy is dissipated in the PMOS device, while the remainder is stored on the load capacitor. During the high-to-low transition, this capacitor is discharged, and the stored energy is dissipated in the NMOS transistor."* [2] The energy values of E_{VDD}, as well as the energy E_C, stored on the capacitor at the end of the transition, can be derived. The derivation is show in equation 2.1.

$$E_{VDD} = C_L {V_{DD}}^2 \tag{2.1}$$

Where E_{VDD} is the energy, C_L is the load at the output of the entity and V_{DD} is the input voltage. Each switching cycle from high to low or the other way around takes a fixed amount of energy, equal to ${C_L V_{DD}}^2$. In order to compute the power consumption, the amount of times the divice switches has to be taken into account. The power consumption is then given by equation 2.2. Figure 2.2 show the corresponding waveforms of $V_{out}(t)$ and $i_{VDD}(t)$.

$$P_{out} = C_L {V_{DD}}^2 f \tag{2.2}$$

Where P_{out} is the power produced by the input source and and f represents the maximum possible event rate of the inputs which in this case is the clock rate. Using this equation it can be concluded that the power, dissipated from the supply will

depend linearly on the switching frequency. This will result in a low power for low frequencies and a high power for high frequencies. Plotting the power over frequency will ideally end up in a straight line with the power proportional with frequency.

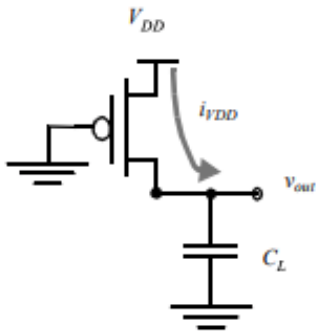

Figure 2.1: Equivalent circuit of an inverter during the low-to-high transition [2]

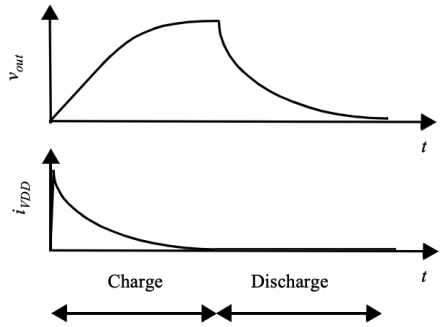

Figure 2.2: Output voltages and supply current during (dis)charge of C_L [2]

2.2 Used logic gate circuits

The clock divider circuits in this thesis use inverters, NAND gates and latches. This section explains the basic theory of these logic circuits. These logic gate circuits use PMOS and NMOS transistors based on CMOS technology.

2.2.1 CMOS Inverter

The first circuit is the CMOS inverter. Figure 2.3 shows the symbol and the basic circuit diagram of a CMOS inverter. An inverter circuit outputs a voltage representing the opposite logic-level to its input. Using transistor theory [2] it can be concluded that the PMOS transistor is on if the gate voltage is ”LOW” and the NMOS transistor is on if the gate voltage is ”HIGH”. A logic table of the CMOS inverter is seen in table 2.1.

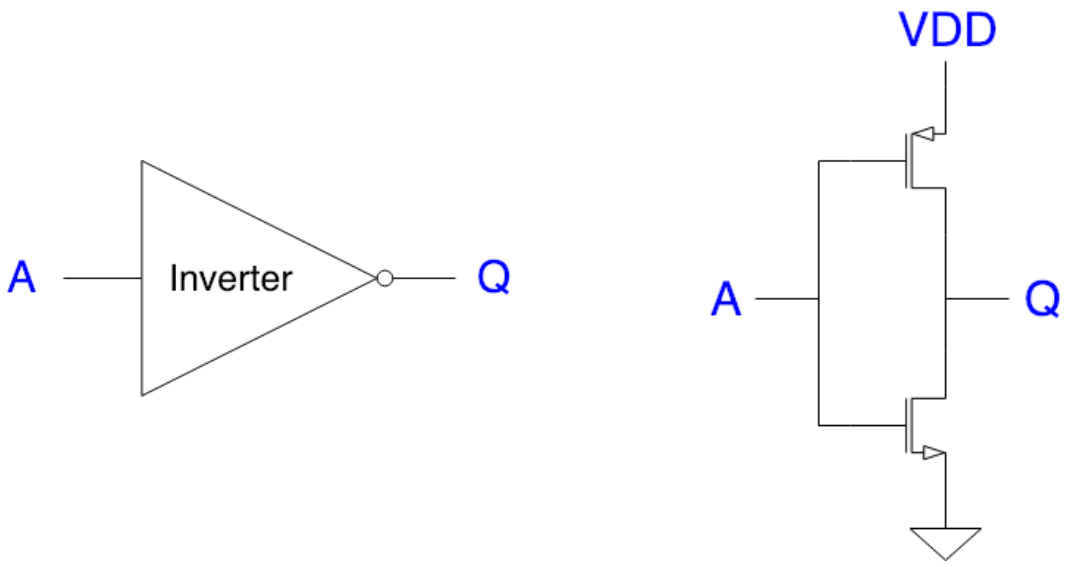

Figure 2.3: CMOS Inverter Symbol and circuit

Table 2.1: Logic table of an CMOS inverter

A	PMOS	NMOS	Q
0	On	Off	1
1	Off	On	0

2.2.2 CMOS NAND

The second logic gate circuit is the NAND gate. Figure **??** shows a CMOS style NAND symbol and circuit. The NAND (Not AND) gate has an output that is normally ”HIGH” and only goes LOW when ALL of its inputs are ”HIGH”. Table 2.2 shows the logic table of the CMOS NAND.

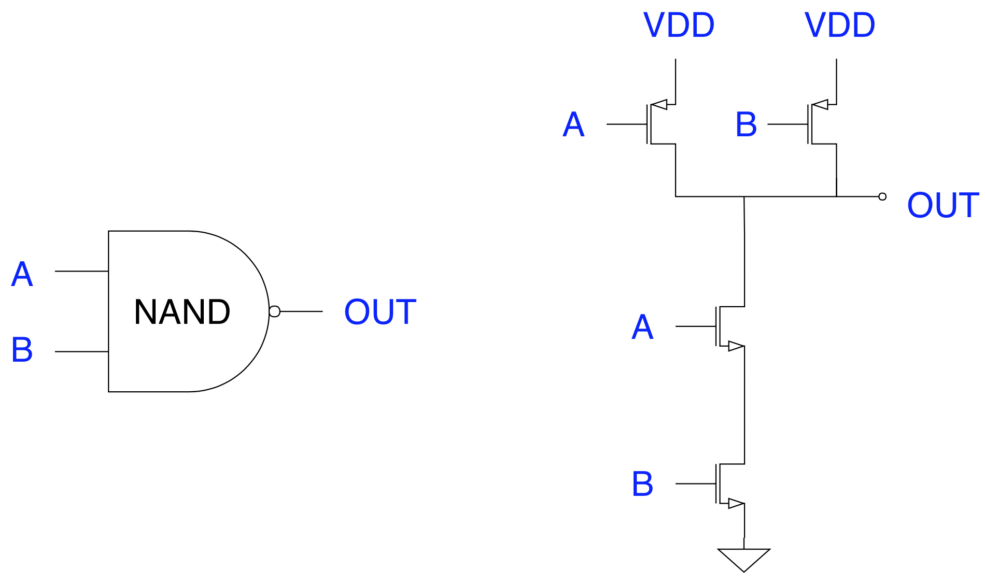

Figure 2.4: CMOS NAND Symbol and circuit

Table 2.2: Logic table of a CMOS NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

2.2.3 Dynamic and static latches

The last entity is the latch which is a circuit that has two stable states and can be used to store state information. This study shows two different implementations of the latch: a static and a dynamic latch. These two implementations are examined closer in chapter 3. Figure 2.5 shows a charge based dynamic latch. The transmission gate is an analog switch controlled by logic signals. It consists of a N and a P type MOS transistor. When the CLK is ”HIGH” the gate conducts and shorts the input and the output, otherwise it cuts off and the output floats. The value is then stored by charge of the capacitor. Capacitor leakage can cause problems with this implementation. This means the circuit can output the wrong value if the CLK is running on a too low frequency. A solution for this problem is to make the latches static. A static latch is shown in figure 2.6. By adding a feedback inverter the states will constantly be refreshed and there will be less issues holding the state.

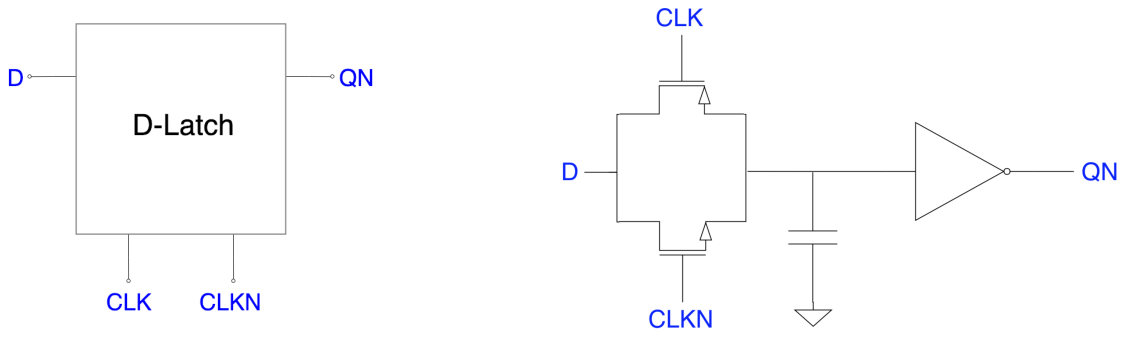

Figure 2.5: Charge based dynamic latch symbol and circuit

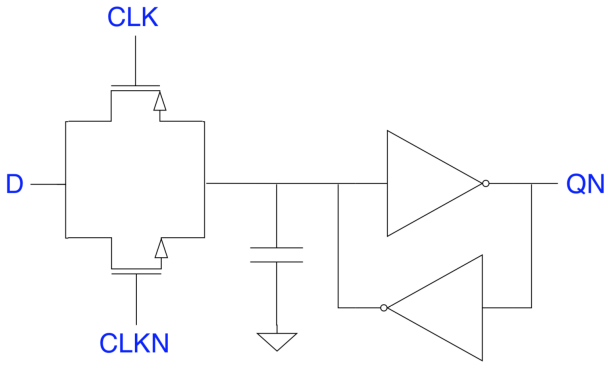

Figure 2.6: Static latch circuit

2.3 Capacitance model

This part contains the theory used to get the input and output capacitences of the different entities and why they are needed. In figure 2.7, a basic MOSFET is used to show how an entity has multiple capacitances. These capacitances are used to determine the in- and output capacitance of circuits used in this thesis. *"It is essential for the designers of high-performance and low-energy circuits to be very familiar with this model"* [2]. This model can also be used for circuits with multiple MOSFET transistors.

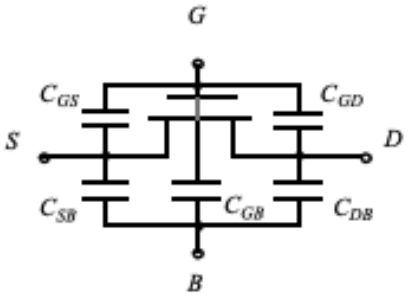

Figure 2.7: MOSFET capacitance model [2]

2.4 Capacitances of one circuit

Using section 2.1 it is known that for determining the power consumption of a circuit the load capacitance has to be known. A bigger circuit can be split up in multiple smaller circuits. These smaller circuits have in- and output capacitances which are used to determine the load capacitance of the bigger circuit. Figure 2.8 shows an inverter with its in-(C1) and output(C2) capacitance.

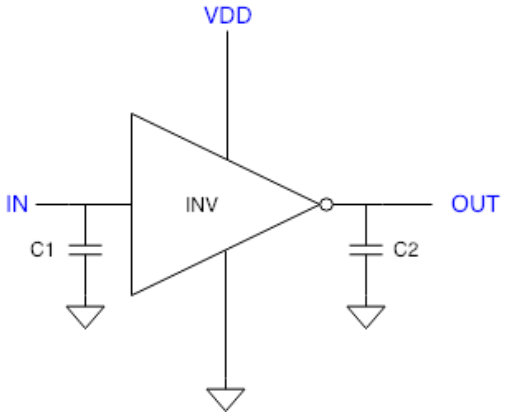

Figure 2.8: Inverter with its in- and output capacitance

2.5 Capacitances of multiple connected circuits

The implementations used in this thesis consists of multiple smaller circuits connected to each other with different in- and output capacitances. Capacitances of other instances also influence the capacitances of the components around it. An example is shown in figure 2.9. The total load capacitance of the first circuit is an addition of output capacitance(C1.2) of the first circuit and the input capacitance(C2.1) of second circuit. The figure shows that the input capacitance (C2.1) of the second

inverter comes in parallel with the output capacitance (C1.2) of the first inverter. This means that these two capacitances can be added up.

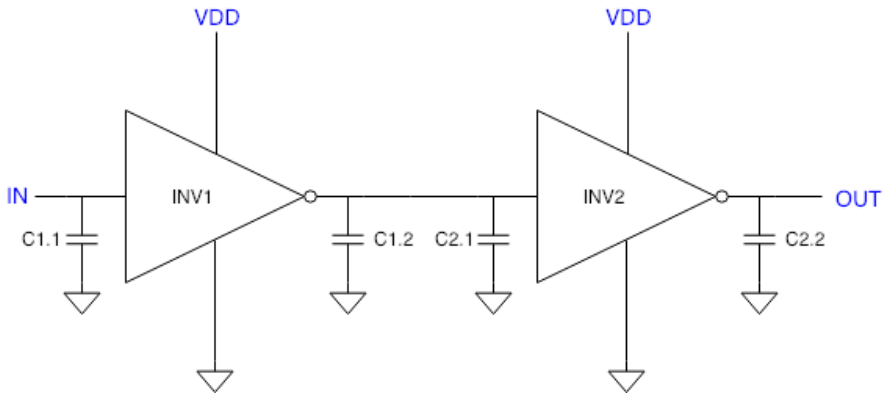

Figure 2.9: Two inverters with their own input/output capacitances

Chapter 3

Review of the circuits

The dividers that are compared in this thesis are used in clock generation circuits. This section explains all the stages of both clock generation circuits.

3.1 Static divider implementation

This section will contain the circuits of the stages of the first clock generation circuit. This implementation is called the static divider implementation because it uses static latches in the divider.

3.1.1 Amplification and clipping stage

The amplification stage is the first stage of the circuit. The two identical resistors R1 and R2 are there for impedance matching to minimize reflections and have maximum power transfer. There are couple capacitors implemented to pass through the AC signal while blocking the DC signal. The external clock is first amplified and clipped by two self-biased inverters to serve as the master clock for the remaining of the circuit. The inverter at the end improves the full swing signal. The amplification stage can be seen in figure 3.1.

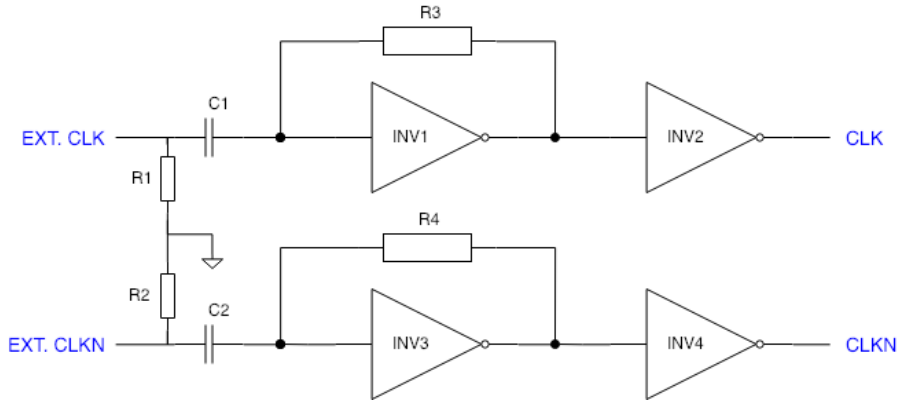

Figure 3.1: Amplification and clipping stage of the first clock generation circuit

3.1.2 Divider stage (Static divider)

The divider used in this implementation is a divide-by 2 circuit. It is made of a combination of two static latches which together form a D flip-flop. The feedback of the flip-flop creates the divider. The clock signal input changes its output on the triggering edge of the clock pulse. This combination is present to divide the CLK and $CLKN$ into 4 new square waves which are on halve the input frequency. Each signal has a 90 degree phase difference. These new 50% duty cycle square waves can be seen on the nodes: Q0, Q90, Q180 and Q270. The setup of the divider stage with the flip-flop can be seen in figure 3.2.

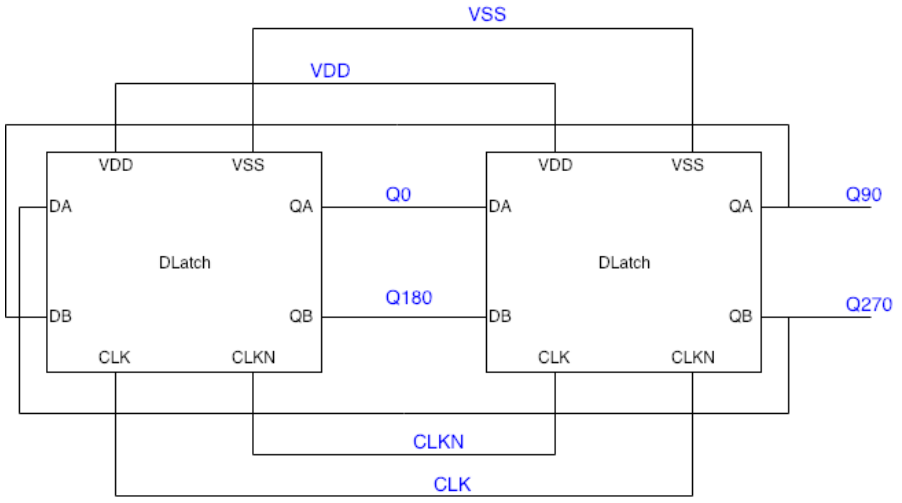

Figure 3.2: Divide-by 2 implementation of the first clock generation circuit

3.1.2.1 Implementation of the static latch

The latch shown in figure 3.3 is a static latch. The reader can see that the circuit is static because of the feedback inverter. The difference is mainly because this

implementation doesn't use a simple transmission gate. This circuit uses tri-state inverter implementations to put either VDD or VSS on the gates of the inverters of the memory stage. An advantage of the inverters is the full swing capability.

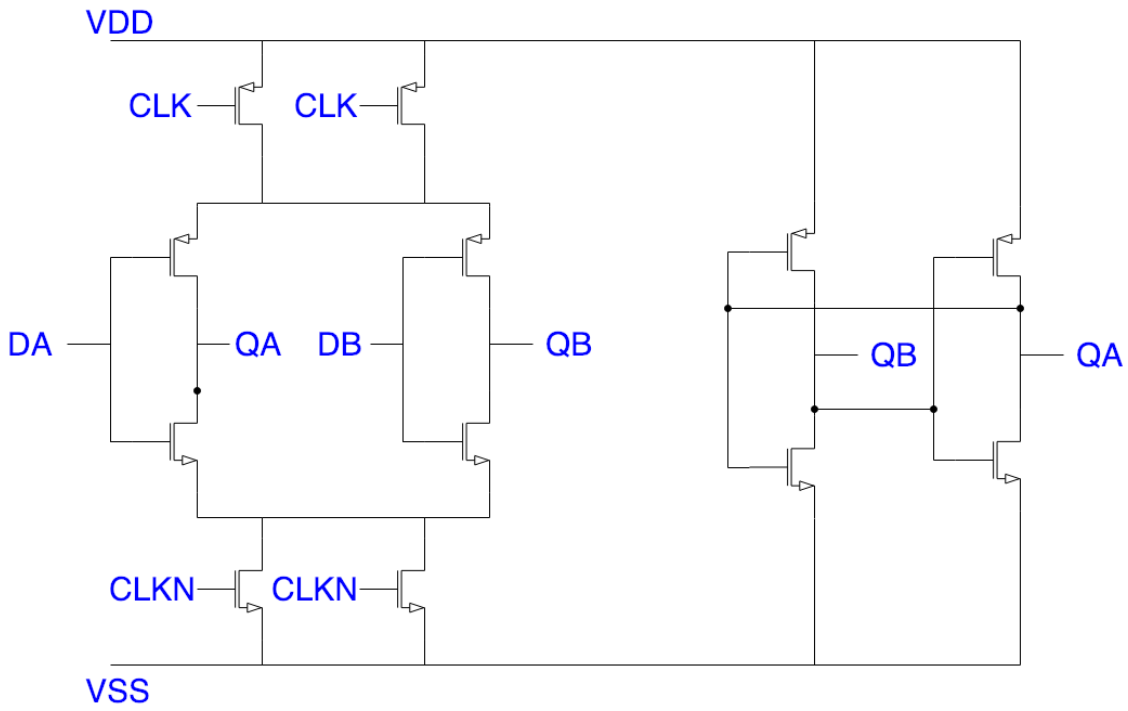

Figure 3.3: Static latch implementation of the first clock generation circuit

3.1.3 25% duty cycle stage

The last stage uses the four 50% duty cycle clocks from the divider stage and combines them to produce four 25% duty cycle clocks. Because the input signals are already phase shifted, the 25% duty cycle clocks will also be 90 degrees phase shifted. This means that in an ideal situation the clocks will not overlap. This stage does that by a setup of NAND logic gates. The inverter at the end of the output of each NAND gate is there to invert the signal so that the "HIGH" time is 25% of the time and not the other way around. The setup of the 25% duty cycle stage of the first clock generation circuit can be seen in figure 3.4. The waveforms of the outputs are shown in figure 3.5.

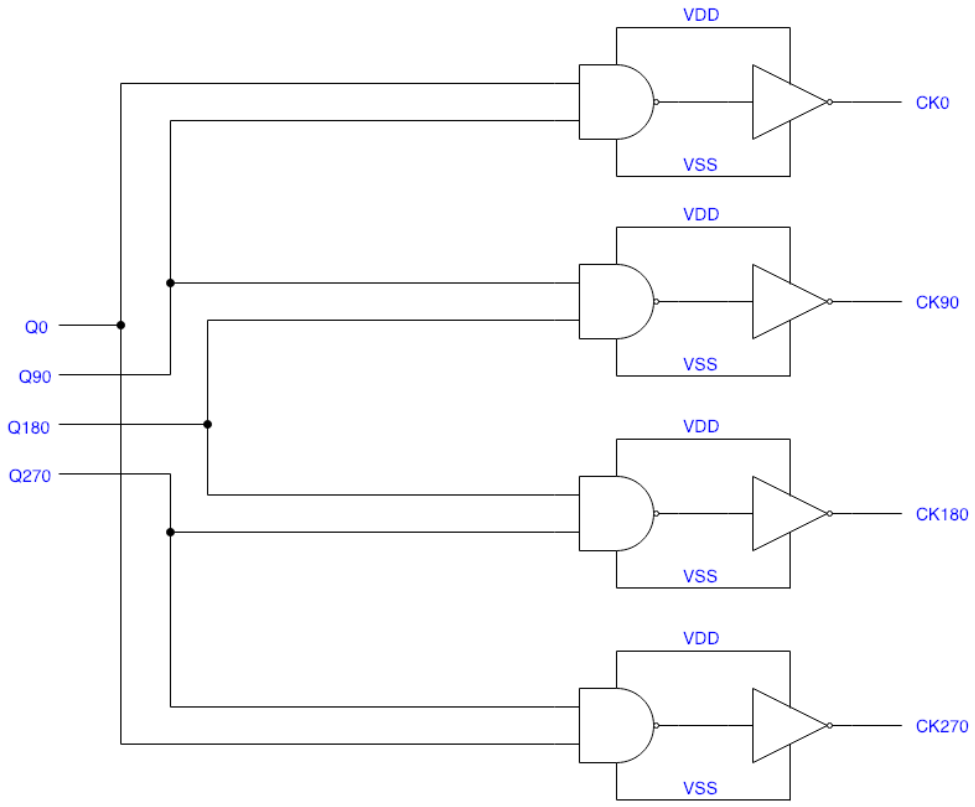

Figure 3.4: 25% duty cycle stage of the first clock generation circuit

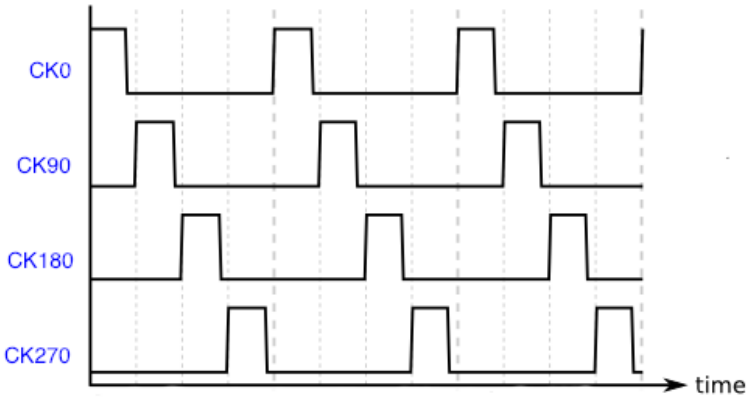

Figure 3.5: 25% duty cycle output signal

3.2 Dynamic divider implementation

This section will contain the second clock generation circuit. This implementation is called the dynamic divider implementation because it uses dynamic latches in the divider.

3.2.1 Amplification and clipping stage

The amplification and clipping stage is the first stage of the circuit and is similar to the amplification/clipping stage of the first clock generation circuit. The difference in this circuit in contrast with the first implementation is the use of extra inverters at the end of the stage. The extra inverters will improve the full swing signal of the clocks. The amplification and clipping stage can be seen in figure 3.6.

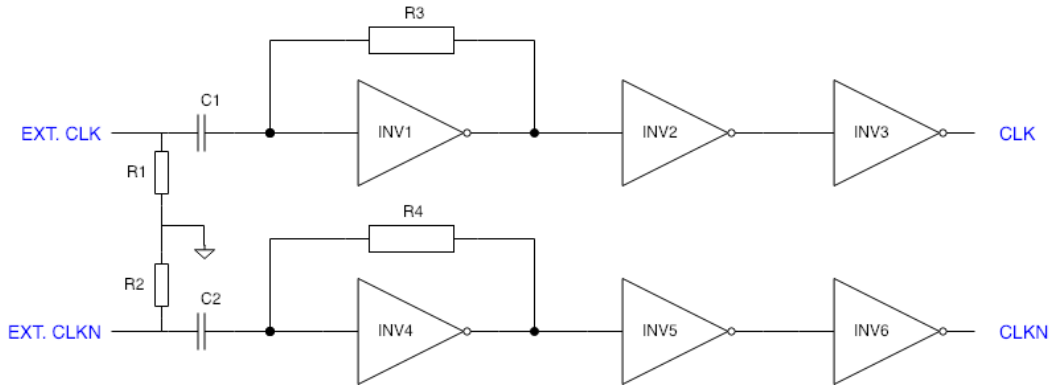

Figure 3.6: Amplification and clipping stage of the second clock generation circuit

3.2.2 Divider stage (Dynamic divider)

The divider stage used in this implementation starts with a divider and uses a shift register implementation to output the signals. Shift registers usually use flip-flops in their design. Instead of using flip-flops the circuit uses dynamic charge based latches with inverters after it. This is done to prevent overlap later on. It's seen that the CLK and $CLKN$ of the nine latches are connected to the clock input making the latches change synchronously. Ten outputs are taken from the implementation where only eight are used for further processing. The other two output signals (OUT2 and OUT9) are there to balance the load of the circuit. Another advantage of using the inverters between the latches is that it improves the full swing signal of the output clocks. The setup of the shift register used as divider stage can be seen in figure 3.7.

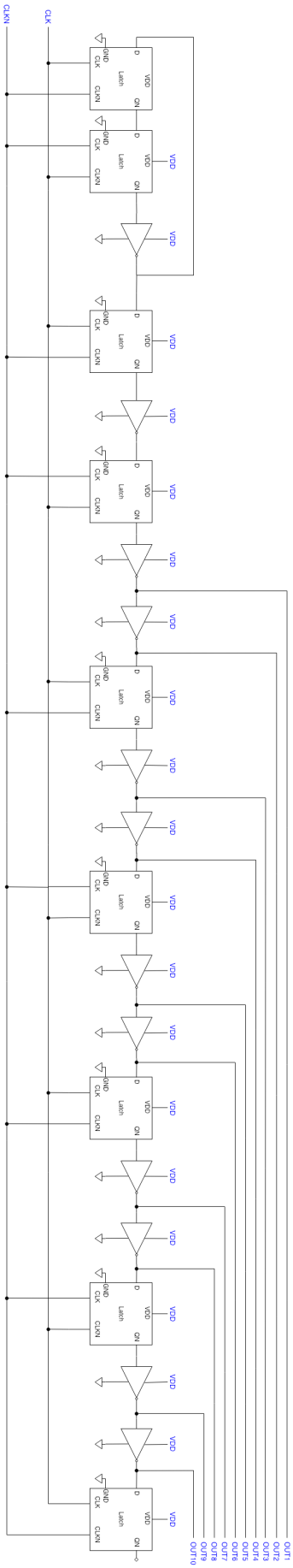

Figure 3.7: Divide-by 2 implementation of clock generation circuit 2

3.2.2.1 Implementation of the dynamic latch

The latch used in this implementation is a simple charge based latch as described in section 2.2.3. The circuit of the latch can be seen in figure 3.8

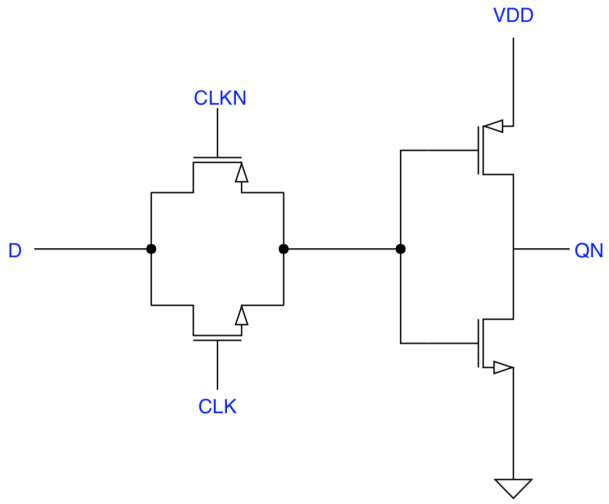

Figure 3.8: Dynamic latch implementation of clock generation circuit 2

3.2.3 25% duty cycle stage

The 25% duty cycle stage used in the second clock generation circuit is similar to the implementation of the first clock generation circuit. This circuit also makes 25% duty cycle non-overlapping signals as seen in figure 3.5 by a setup of NAND logic gates. The difference is that this implementation uses two extra dummy NAND gates to balance the load of the divider. The setup of the 25% duty cycle stage of the second clock generation circuit can be seen in figure 3.9.

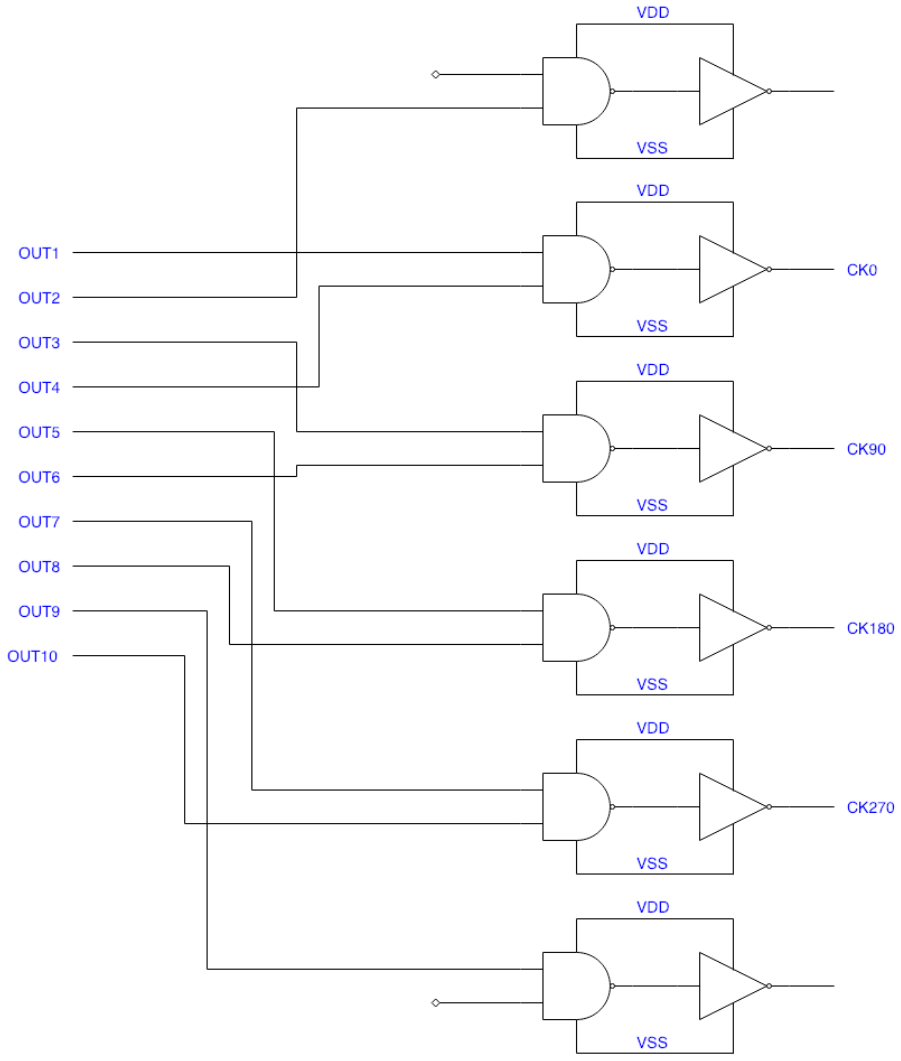

Figure 3.9: 25% duty cycle stage of the clock generation circuit 1

Chapter 4

Method of comparing the divider circuits

The circuits researched in this theses use different implementations. A method is developed and applied to make a comparison between the two circuits. If this method is used, meaningful conclusions can be drawn on power dissipation and the operating frequency range of the circuits.

4.1 Comparing power consumption

This section will discuss a way to get a comparison of power consumption between the divider circuits. A ratio between the power consumption values of the circuits can give a good estimation of which circuit consumes less power. Using the theory from section 2.1 this ratio is equal to the load capacitance ratio of the circuits. It's known from section 2.8 that a circuit has in- and output capacitances. Figure 4.1 shows the stages which are involved and their in- and output capacitances. A comparison between the different dividers can be made if the output capacitance of the amplification/clipping stage(C1) and the input capacitance of the 25% duty cycle stage(C4) are constant. This makes sure that the in-(C2) and output(C3) capacitance of the dividers are the only variables when replacing the divider stage. A total load capacitance of the stages can be determined which consists of the output capacitance of the stage itself and the input capacitance of the stage after it. To determine the in- and output capacitances of the stages they have to be split in multiple smaller circuits. The capacitances of the smaller circuits can be added up using the theory of section 2.5 and will form the in- and output capacitance of a stage.
A double check can be done by simulating the power consumption of the stages in the circuits. From these values, a simulated power consumption ratio can be made which should be approximately the same as the determined power consumption

ratio.

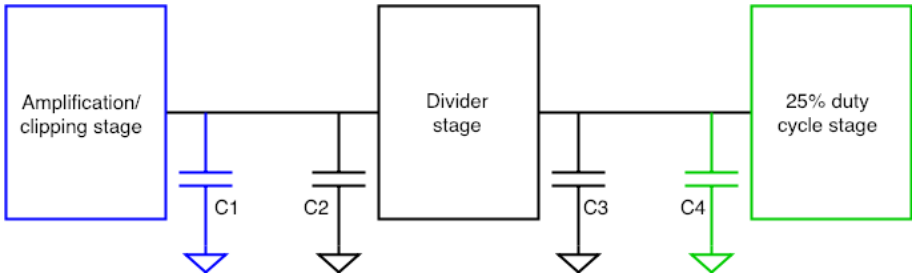

Figure 4.1: Overview of stages and their in- and output capacitances

4.1.1 Same output capacitance of the amplification/clipping stage to compare the dividers

A way to get the same output capacitance at the amplification/clipping stage is to simply use the same stage for each comparison. This is easy to do because both implementations of the divider stage have a CLK and a CLKN input which it can connect to. It is chosen to use the amplification/clipping stage of the first clock generation circuit. The amplification/clipping stage that is used to compare the divider stages can be seen in figure 3.1.

4.1.2 Same input capacitance of the 25% duty cycle stage to compare the dividers

In this implementation the input capacitance of the 25% duty cycle stage is the load of the divider stage. In this case, the input capacitance(C4) can't be replaced. The two implementations of the 25% duty cycle stage are different in the amount of NAND gates used. The solution is to replicate the same input capacitance for both 25% duty cycle implementations with extra capacitances. This way the divider stage will always see the same load. This means that the 25% duty cycle stage with the lower input capacitance has to add capacitors in front of the NAND gates such that the same value is reached as the stage with the higher input load capacitances. Figure 4.2 shows the 25% duty cycle stage with extra capacitors at the input of the NAND gates.

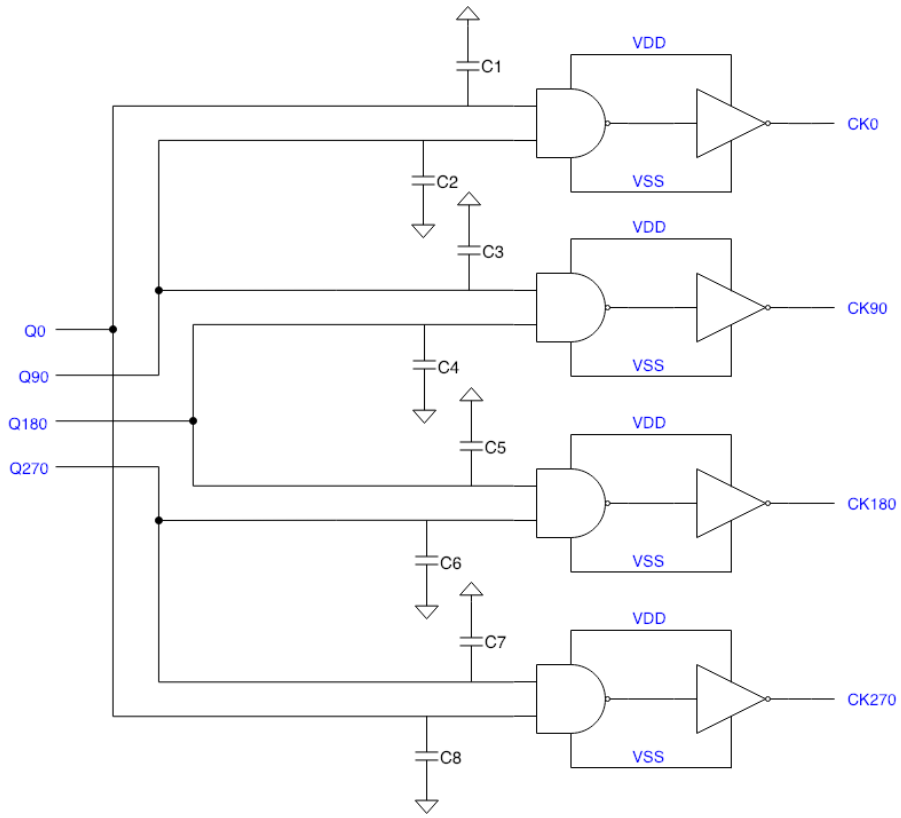

Figure 4.2: 25% duty cycle stage with extra capacitors

4.1.3 Determine input capacitance

In this section the determining of the input capacitance will be explained. Determining the input capacitance of a circuit works just like measuring a RC circuit which is shown in figure 4.3.

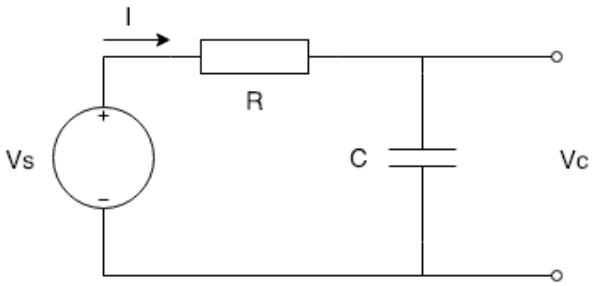

Figure 4.3: An ideal RC circuit

The input capacitance can be concluded from the charging voltage which is measured over V_C. V_C will be charged over time such that τ can be determined. Equation 4.1 shows how V_C is charged.

$$V_C = V_S \cdot (1 - e^{-\frac{t}{RC}}) \tag{4.1}$$

The time constant τ of an RC circuit is equal to the product of the circuit resistance and the circuit capacitance, i.e. $\tau = RC$. This means that if a resistor value is chosen and τ is determined that the capacitor value C_{in} for an instance can be determined. The setup of how τ is determined in the simulation is shown in figure 4.4

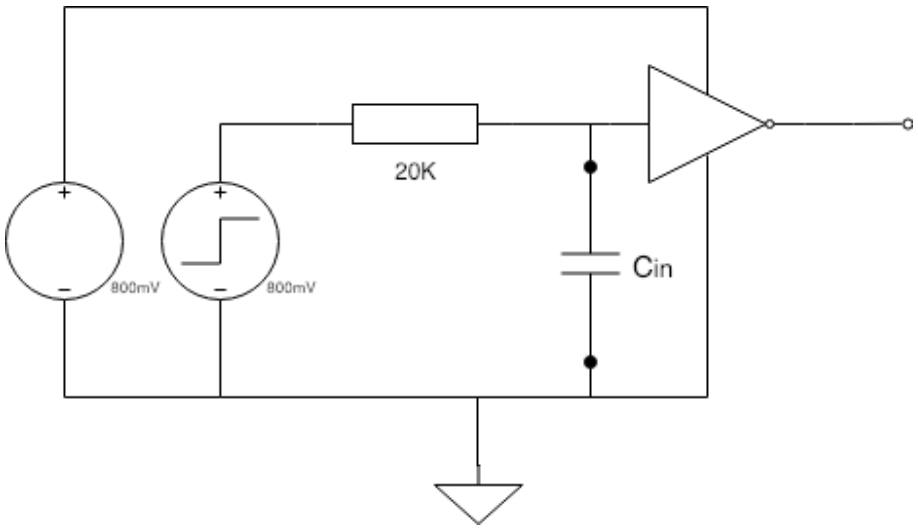

Figure 4.4: Setup to calculate input capacitance of an inverter

This setup will behave like the RC circuit described before. A double check of the determined τ can be done by simulating an ideal RC network with the determined value of the capacitor. By comparing the charging curves and τ it can be concluded that the simulation and determining was done correctly.

4.1.4 Determine output capacitance

This section explains how the output capacitance of an inverter is determined. Section 2.1 is used to see that the power consumption and the load capacitance have a linear relationship, the output capacitance can be determined if the frequency and the power consumption are known. These values of the implemented circuits can be simulated using Cadance. The setup to determine the output capacitance of a circuit is shown in figure 4.5.

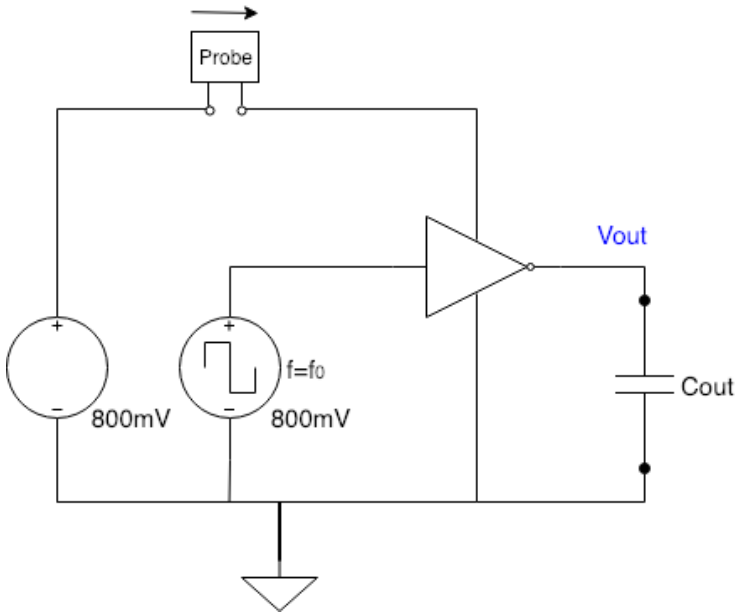

Figure 4.5: Setup to calculate output capacitance of an inverter

$$C_{out} = \frac{\Delta P_{out}}{{V_{DD}}^2 \Delta f} \tag{4.2}$$

Equation 4.2 shows the determining of the output capacitance C_{out} where P_{out} is the average power consumption, f_0 is the frequency of the square wave generator and V_{DD} is the supply voltage of the source. If this is done on multiple frequencies, the capacitance value will be more accurate.

4.1.5 Power consumption of circuits with load

To simulate the power consumption of the stages, the current that the circuits in front of the load draw has to be measured. Figure 4.6 shows the setup for a single circuit. C_{out} is the output capacitance of the inverter and load is the load capacitance. To determine the total power of the divider implementations, multiple of these circuits have to be measured at the same time. Below the Cadance equation is shown to get the average current over the time of a probe. This output value of this simulation has to be multiplied with the voltage of the source to determine the power.

```
average(i("/IPRB0/PLUS" ?result "tran"))
```

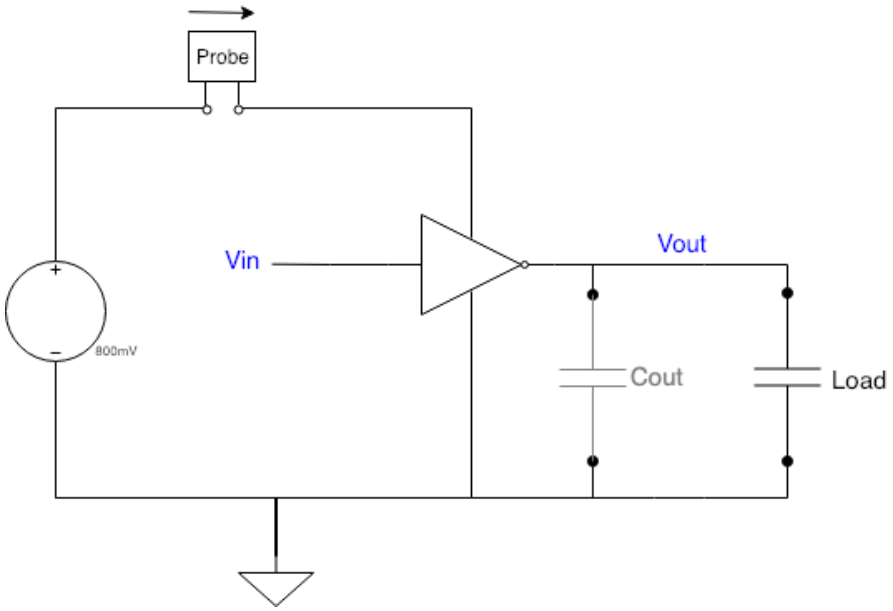

Figure 4.6: Setup to calculate power consumption of an inverter with load

4.2 Comparing operating frequency range

This section will discuss a method to determine the operating frequency range of the circuits. The boundary conditions set in section 1.3 are used to determine to what frequency the circuit is functional for processing data. Determining the operating frequency ranges of the two implementations is mainly done by simulations performed by Cadance. All the methods explained below are done over multiple frequencies between 1 GHz and 10 GHz. When the simulation results don't hold the theory or their boundary conditions anymore it can be concluded that the circuit is not working at those frequencies. All simulations are done using the amplification/clipping and 25% duty cycle stage for which the divider is designed for. These stages are explained in chapter 3.

4.2.1 Power consumption over frequency

Using section 2.1 it's known that besides the load capacitance also the frequency has a linear relationship with the power consumption. Cadance can provide a simulated values of the power consumption of the circuits on multiple frequencies. This is basically done by putting a current probe in series with the voltage source just as the method from section 4.1.5. When done on multiple frequencies, a graph can be made to see which circuit has less power consumption on which frequency. The frequency range of the divider circuit has to be known. That is why it is important to know that the amplification/clipping stage is working in that range too. Otherwise

that would be the bottleneck. This means that besides the divider also the power of the amplification/clipping stage has to be simulated.

4.2.2 Duty cycle over frequency

Also the duty cycle can be determined by simulations. One of the boundary conditions was that the duty cycle can't be higher than 26%. Cadance can plot the duty cycle of the clocks over time with the equation below. If the results are noted over multiple frequencies, a graph can be constructed which can be used to see if the boundary conditions are met over different frequencies.

```
dutyCycle(getData("/ck0" ?result "tran") ?mode "auto" ?xName "time" ?outputType "plot")
```

4.2.3 Rise and fall time over frequency

Another aspect that has to be looked at is the rise and fall time. These times are wanted as short as possible. It is difficult to say what the maximum rise or fall time should be but it is possible to let Cadance calculate it. Below the Cadance equation is shown how to get the rise and fall time of a signal $ck0$ using the riseTime and fallTime functions.

```
average(riseTime(v("/ck0"?result "tran")0.001 nil 0.799 nil 10 90 t "time"))
average(fallTime(v("/ck0"?result "tran")0.799 nil 2e-05 nil 10 90 t "time"))
```

Chapter 5

Results of comparison divider circuits

This chapter will explain the results and the simulations of the circuits that are tested.

5.1 Comparison of the power consumption

This section will compare the load capacitance and the power consumption of the two implementations of the divider stage. Keep in mind that the comparing method of section 4.1 is used for this comparison.

5.1.1 Load capacitances of the stages

This section will discuss the load capacitances of the different circuit implementations. Each circuit is split in multiple smaller circuits to determine the in- and output capacitance of the stages. These in- and output capacitances will form the load capacitance which can be used to determine the power consumption of the stage.

5.1.1.1 Static divider implementation

Using the method of sections 4.1.3 and 4.1.4 the capacitances of the smaller circuits of the static divider can be determined. Figure 5.1 shows the different smaller circuit used and their input and output capacitances.

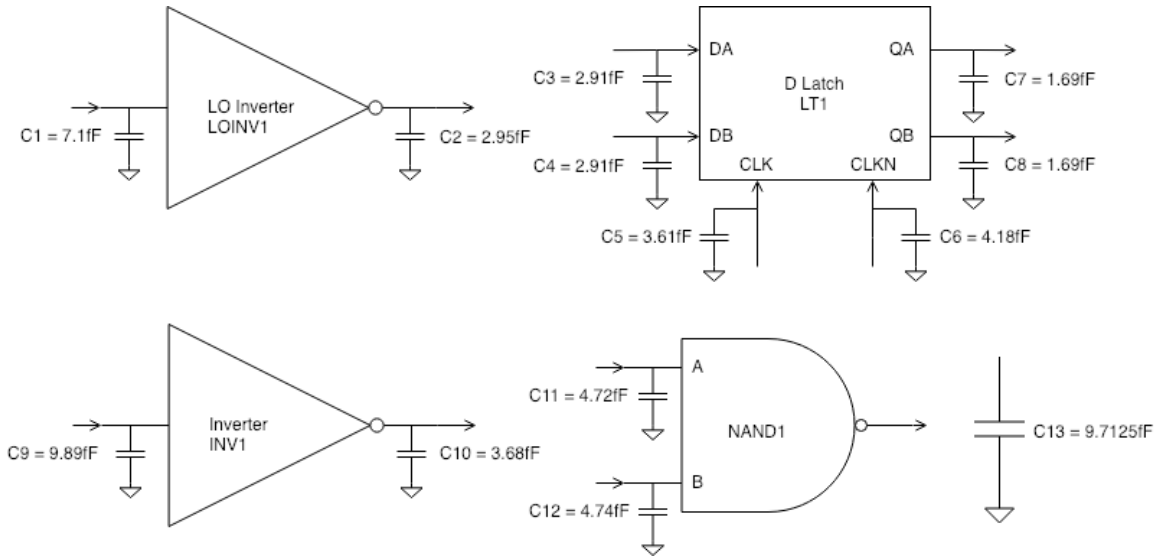

Figure 5.1: Capacitances of the circuits used in the static divider comparison

Now that the capacitances of the static divider implementation using the comparison method of section 4.1 are determined they can be added up to each other according to the theory of section 2.5. A block diagram is made to determine the total load capacitances of the stages. The block diagram is shown in figure 5.2. C_{AMP} is the total load capacitance of the amplification/clipping stage used in the static divider comparison circuit and C_{DIV} is the total load capacitance of the static divider stage.

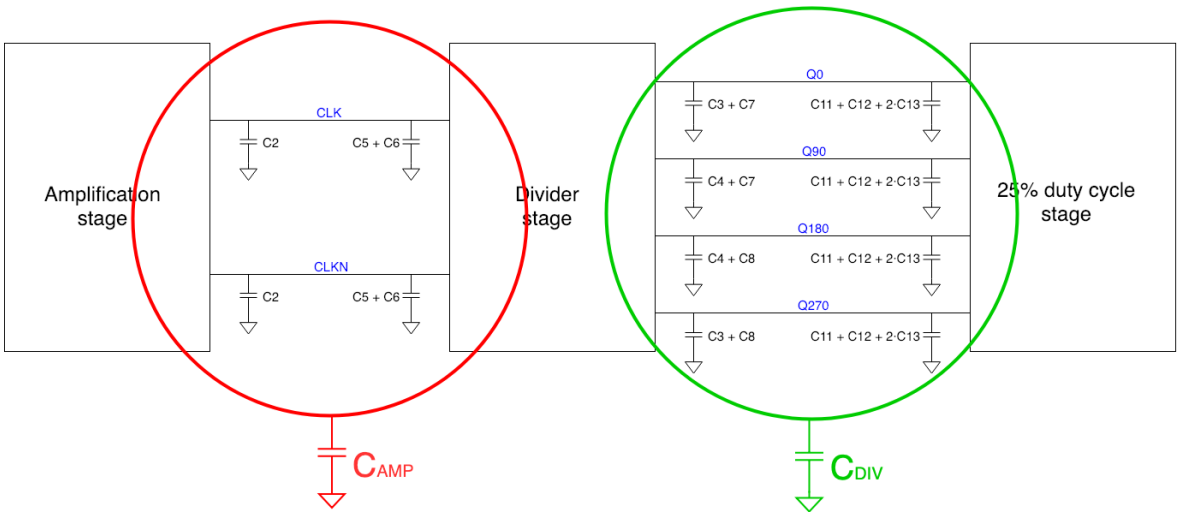

Figure 5.2: Block diagram with load capacitances of static divider comparison circuit

Load capacitance of the static amplification/clipping stage (C_{AMP})

As seen in figure 5.2 the total load capacitance of the amplification/clipping stage of

the static divider comparison circuit is the addition of the input capacitance of the divider stage and the output capacitance of the amplification/clipping stage. Equations 5.1, 5.2 and 5.3 show the calculation of the total load capacitance of this amplification/clipping stage.

$$C_{AMP} = C_{CLK} + C_{CLKN} \tag{5.1}$$

$$C_{CLK} = C_2 + C_5 + C_6 \tag{5.2}$$

$$C_{CLKN} = C_2 + C_5 + C_6 \tag{5.3}$$

Where C_{AMP} is the load capacitance of the amplification/clipping stage, C_x is the in- or output capacity of an entity shown in figure 5.1 and C_{CLK}/C_{CLKN} are the load capacitances on the clock nodes. The load capacitance of the amplification/clipping stage of the static divider comparison circuit is shown below.

$$C_{AMP_{static}} = 21.5fF$$

Load capacitance of the static divider stage (C_{DIV})

The total load capacitance of the static divider stage is an addition of the input capacitance of the 25% duty cycle stage and the output capacitance of the static divider stage. Equations 5.4 till 5.8 show the way the total load capacitances of the static divider are determined.

$$C_{DIV} = C_{Q0} + C_{Q90} + C_{Q180} + C_{Q270} \tag{5.4}$$

$$C_{Q0} = C_3 + C_7 + C_{11} + C_{12} + 2 \cdot C_{13} \tag{5.5}$$

$$C_{Q90} = C_4 + C_7 + C_{11} + C_{12} + 2 \cdot C_{13} \tag{5.6}$$

$$C_{Q180} = C_4 + C_8 + C_{11} + C_{12} + 2 \cdot C_{13} \tag{5.7}$$

$$C_{Q270} = C_3 + C_8 + C_{11} + C_{12} + 2 \cdot C_{13} \tag{5.8}$$

Where C_{DIV} is the total load capacitance of the static divider stage, C_x is the in- or output capacity of a circuit shown in figure 5.1 and C_{Q0} to C_{Q270} are the total load capacitances on the $Q0$ to $Q270$ nodes. The total load capacitance of the static divider stage is shown below.

$$C_{DIV_{static}} = 143.4fF$$

5.1.1.2 Dynamic divider implementation

Using the method of sections 4.1.3 and 4.1.4 the capacitances of the smaller circuits of dynamic divider comparison circuit can be determined. Figure 5.3 shows the different circuits used and their input and output capacitances.

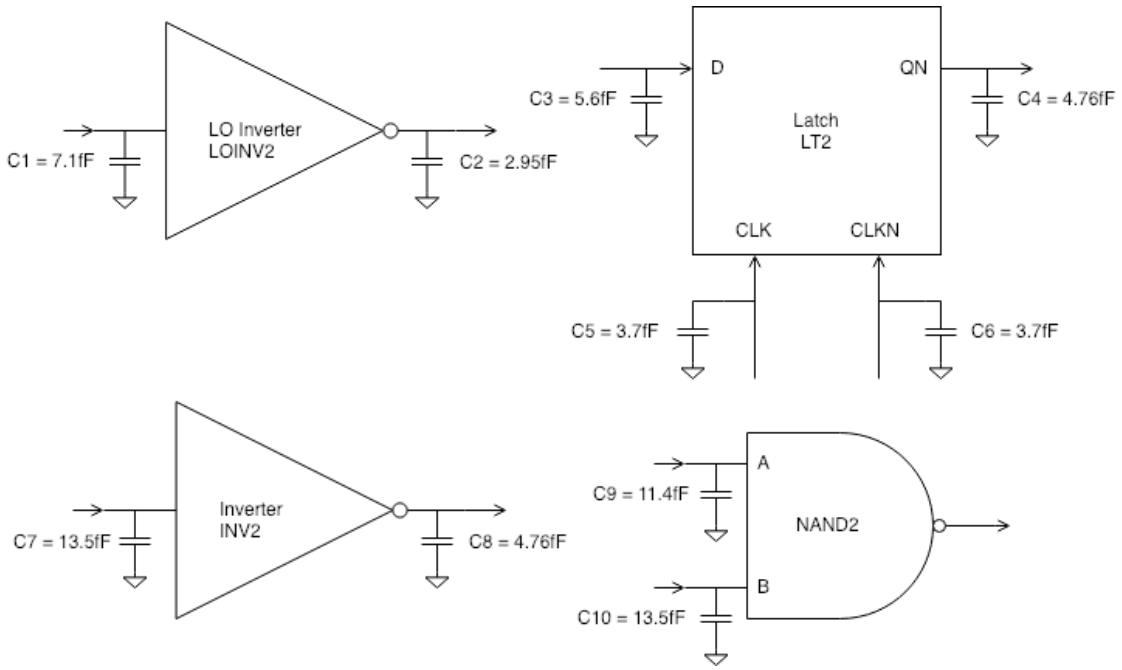

Figure 5.3: Capacitances of the circuits used in the dynamic divider comparison

Now that the capacitances of the circuits of the dynamic divider comparison circuit are determined they can be added up to each other according to the theory of section 2.5. A block diagram is made to determine the total load capacitances of the stages. The block diagram is shown in figure 5.4. C_{AMP} is the total load capacitance of the amplification/clipping stage used in the dynamic divider comparison circuit and C_{DIV} is the total load capacitance of the dynamic divider stage.

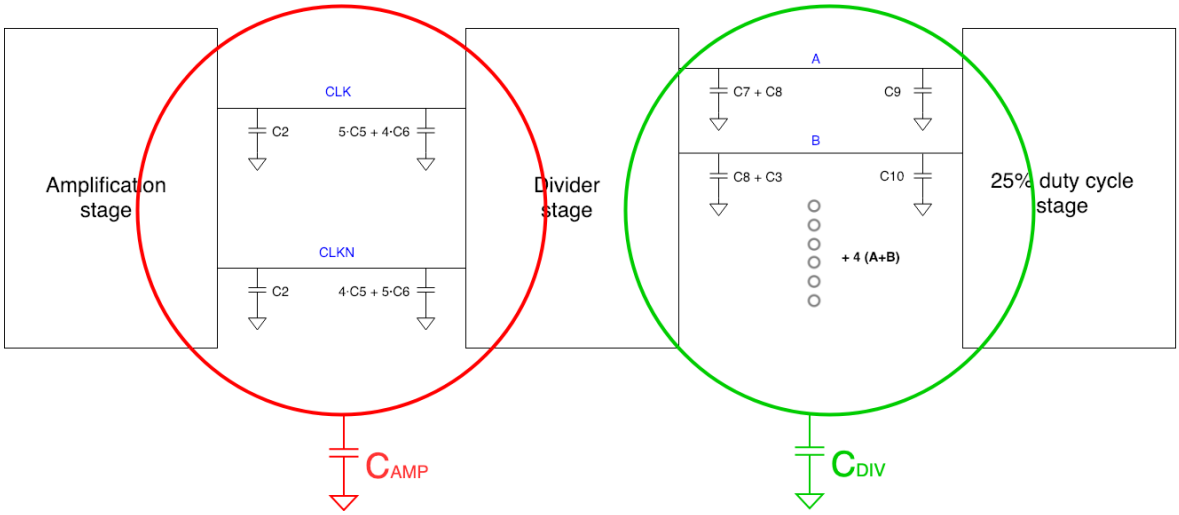

Figure 5.4: Block diagram with load capacitances of dynamic divider comparison circuit

Load capacitance of the dynamic amplification/clipping stage (C_{AMP})
As seen in figure 5.4 the total load capacitance of the amplification/clipping stage of the dynamic divider comparison circuit is the addition of the input capacitance of the divider stage and the output capacitance of the amplification/clipping stage. Equations 5.9, 5.10 and 5.11 to show the calculation of the total load capacitance of this amplification/clipping stage.

$$C_{AMP} = C_{CLK} + C_{CLKN} \tag{5.9}$$

$$C_{CLK} = C_2 + 5 \cdot C_5 + 4 \cdot C_6 \tag{5.10}$$

$$C_{CLKN} = C_2 + 4 \cdot C_5 + 5 \cdot C_6 \tag{5.11}$$

Where C_{AMP} is the total load capacitance of the amplification/clipping stage, C_x is the in- or output capacity of an entity shown in figure 5.3 and C_{CLK}/C_{CLKN} are the load capacitances on the clock nodes. The total load capacitance of the amplification/clipping stage of the dynamic divider comparison circuit is shown below.

$$C_{AMP_{dynamic}} = 60.9fF$$

Load capacitance of the dynamic divider stage (C_{DIV})
The total load capacitance of the dynamic divider stage is an addition of the input capacitance of the 25% duty cycle stage and the output capacitance of the static divider stage. Equations 5.12 till 5.14 show the way the load capacitances of the

divider stage are determined.

$$C_{DIV} = 5 \cdot C_A + 5 \cdot C_B \tag{5.12}$$

$$C_A = C_7 + C_8 + C_9 \tag{5.13}$$

$$C_B = C_8 + C_3 + C_{10} \tag{5.14}$$

Where C_{DIV} is the total load capacitance of the static divider stage, C_x is the in- or output capacity of a circuit shown in figure 5.3 and C_A/C_B are the load capacitances on the A and B nodes. The load capacitance of the divider stage the dynamic divider implementation is shown below.

$$C_{DIV_{dynamic}} = 268fF$$

5.1.1.3 Comparison of the load capacitances of the implementations

Now that the total load capacitances of the stages of the two implementations are known a ratio can be determined. Because of the theory of section 2.1 the load capacitance has a direct relation with the power consumption. That means that the load capacitance ratio between the two implementations gives a good indication which circuit consumes more power. The ratio is determined by dividing the total load capacitances of the dynamic divider comparison circuit by the total load capacitances of the static divider comparison circuit as seen in equations 5.15 and 5.16.

$$CapRatio_{AMP} = \frac{C_{AMP_{dynamic}}}{C_{AMP_{static}}} \tag{5.15}$$

$$CapRatio_{DIV} = \frac{C_{DIV_{dynamic}}}{C_{DIV_{static}}} \tag{5.16}$$

Where C_{AMP} and C_{DIV} are the load capacitances determined earlier in this section. Table 5.1 shows the load capacitance ratios of the amplification/clipping stage and the divider stage of the two implementations.

Table 5.1: Ratio of the load capacitances between the circuits

$CapRatio_{AMP}$	$CapRatio_{DIV}$
2.83	1.86

From this ratio it can be concluded that the input capacitance of the dynamic divider is bigger than the static divider implementation. This will cause the amplification/clipping stage to consume more power because the dynamic divider will be a

bigger load. The divider stage ratio leads to the conclusion that the output capacitance of the dynamic divider is also bigger than the output capacitance of the static divider. This means the divider will consume more power if the load capacitance is the same. Using the theory it can be concluded that the power consumption should have the same ratio as the load capacitance. This means that by determining the load capacitance ratio, it can be estimated how much power circuit consumes over the other using the comparison method of chapter 4.

5.1.2 power consumption of the stages

To check if the load capacitance ratio is determined correctly a power consumption ratio can be determined by simulations. As described in section 4.1.5 powers can be determined by simulating the current through current probes. The amplification/clipping stage and the divider stage of both clock generation circuits have been measured with the use of the method of section 4.1 on power consumption. Tables 5.2 and 5.3 shows the power consumption of both stages of both clock generation circuits on three different frequencies. The circuits are known to work on these three frequencies. It was chosen to take multiple frequencies to get a better representation of the ratio between the circuits. Take note that the same amplification/clipping circuit and the same load capacitance for the divider is used.

Table 5.2: Power consumption of the static divider comparison circuit on three frequencies

Frequency (GHz)	Amplification/clipping stage (W)	Divider stage (W)
1	4.92E-05	1.77E-04
2	9.76E-05	3.48E-04
3	1.46E-04	5.05E-04

Table 5.3: Power consumption of the dynamic divider comparison circuit on three frequencies

Frequency (GHz)	Amplification/clipping stage (W)	Divider stage (W)
1	1.49E-04	3.45E-04
2	3.00E-04	6.87E-04
3	4.51E-04	1.03E-03

The power consumption ratios are shown in table 5.4. These values are simply calculated by dividing the power consumption of dynamic divider comparison circuit by the one of static divider comparison circuit. These ratios represent the amount of

times the stages of the dynamic divider comparison circuit are more power consuming than the stages of the static divider comparison circuit.

Table 5.4: Ratio of the power consumption between the circuits

$PowerRatio_{AMP}$	$PowerRatio_{DIV}$
3.06	1.99

5.1.3 Comparing load capacitance and power consumption

At this point in this study it's known what the load capacitance of the amplification and divider stage is. It is also known what power consumption those stages have. Knowing the theory of section 2.1 a comparison can be made between the load capacitance ratios and the power consumption ratios. Table 5.5 shows the deviation in percentage between the load capacitance (table 5.1) and the power consumption (table 5.4) ratios. It is shown that the simulated power consumption ratio is around 7% to 8% more than the power consumption ratio determined by the load capacitances.

Table 5.5: Deviation between power consumption and load capacitance ratios

$Ratio_{AMP}$	$Ratio_{DIV}$
8.12%	6.99%

5.2 Comparison of the operating frequency range

This section will compare the circuits on different frequencies. The results of the output signal, power consumption, duty cycle and rise and fall time are noted. Simulations have been done between a range from 1 GHz to 10GHz. The first 5 GHz the simulations have been done with steps of 1 GHz and the last 5 GHz are simulated with steps of 0.5 GHz. This is done because the results in the lower frequencies are not significantly changing in comparison to the higher frequencies.

5.2.1 Power consumption over frequency

This section will discuss the power consumption versus the frequency of the circuits. Figure 5.5 shows the power consumption on frequencies between 1GHz and 10GHz. It is clear from the figure that the amplification/clipping stage of both implementations still follow the theory of section 2.1 in the frequency range of 1 GHz to

10 GHz. This means the amplification/clipping stage can't be a bottleneck for one of the dividers because it can handle the power for its load capacitance. The plot that stands out is the plot of the static divider implementation. The figure shows that the the static divider implementation isn't linear anymore in the higher frequencies. With this information it is known that for frequencies higher than 7 GHz the static divider has issues drawing the current to charge the load capacitance. Contrary to the static implementation, the dynamic implementation still has a linear behaviour even up till 10 GHz which means that the circuit can draw current to charge its load capacitance. Although the range of the dynamic divider implementation is bigger, it consumes significantly more power. That means that based on power consumption it can be concluded that the static divider implementation is the better choice up till 7 GHz. Above 7 GHz the dynamic divider implementation would be the only choice between these two implementations.

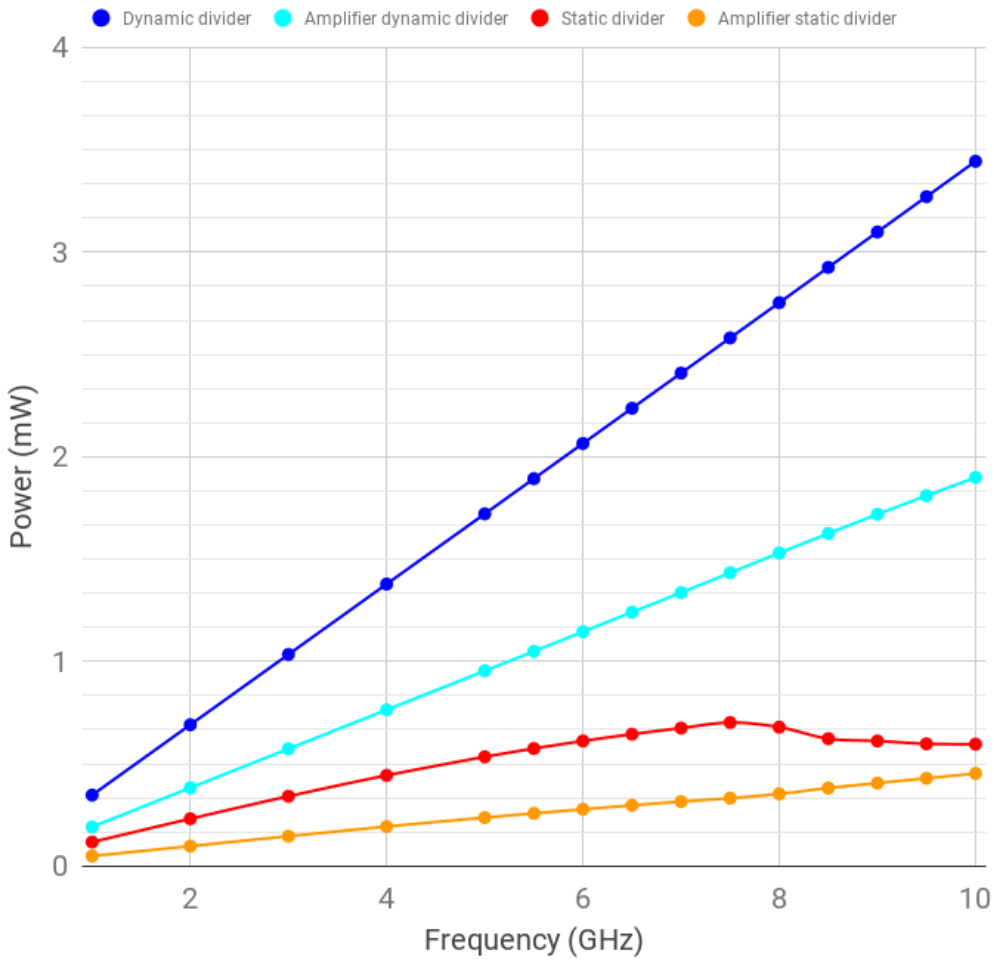

Figure 5.5: Power consumption over frequency of both implementations

5.2.2 Duty cycle

Another aspect that has been studied is the duty cycle of the output signals. Looking at the signals of section 5.2.4, the duty cycle could be estimated by eye which is not ideal. Using the method from section 4.2.2 it is possible to get a more accurate value of the duty cycle. The results can be seen in figure 5.6.

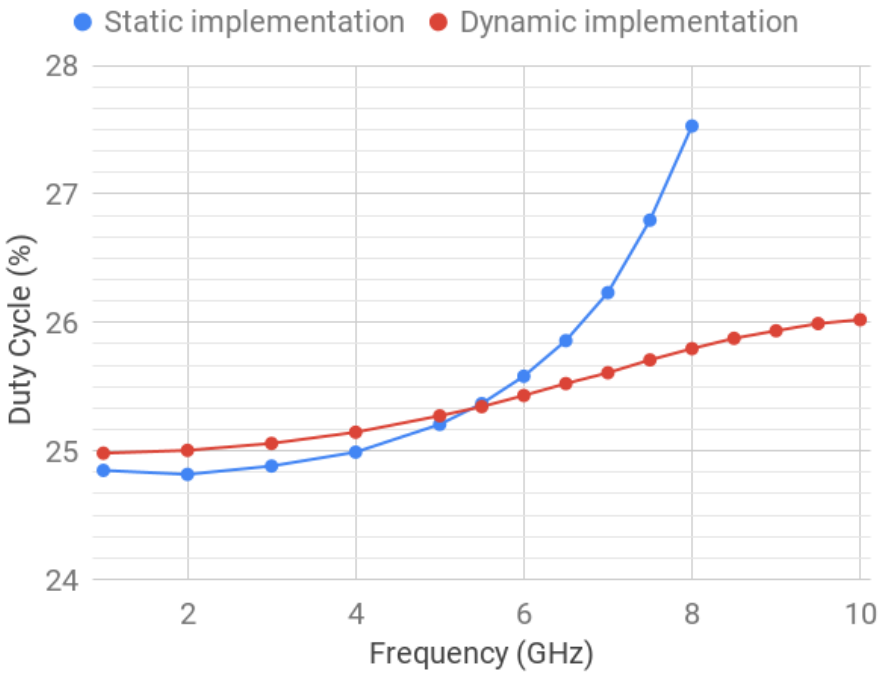

Figure 5.6: Duty cycle of both circuits

From this figure it can be seen that the static divider implementation has a lower duty cycle than the dynamic divider implementation until 5.25 GHz. Notable is the duty cycle of the static implementation that reaches above 26% duty cycle at around 6.5 GHz. This is more than the boundary conditions that have been set in the introduction. This means that following these boundary conditions the static divider implementation is not usable above 6.5 GHz.
The dynamic divider implementation has a slow upward trend which reaches 26% duty cycle around 10 GHz. Above this frequency also the dynamic divider implementation isn't sufficient anymore.

5.2.3 Rise and fall time

The rise and fall time of the circuits are shown in figure 5.7. The reader can see that the static divider implementation doesn't show a constant behaviour in the higher frequencies just as the power consumption. This means that the rise and fall time

is an extra indicator to see if the circuit is working or not. It indicates that the circuit works up to 6.5 GHz. Another thing that is noted is the difference between the rise and fall time between the circuits. The static divider implementation has a higher fall time than rise time. The static divider implementation has it the other way around. This is done intentionally by the designers of the circuits.

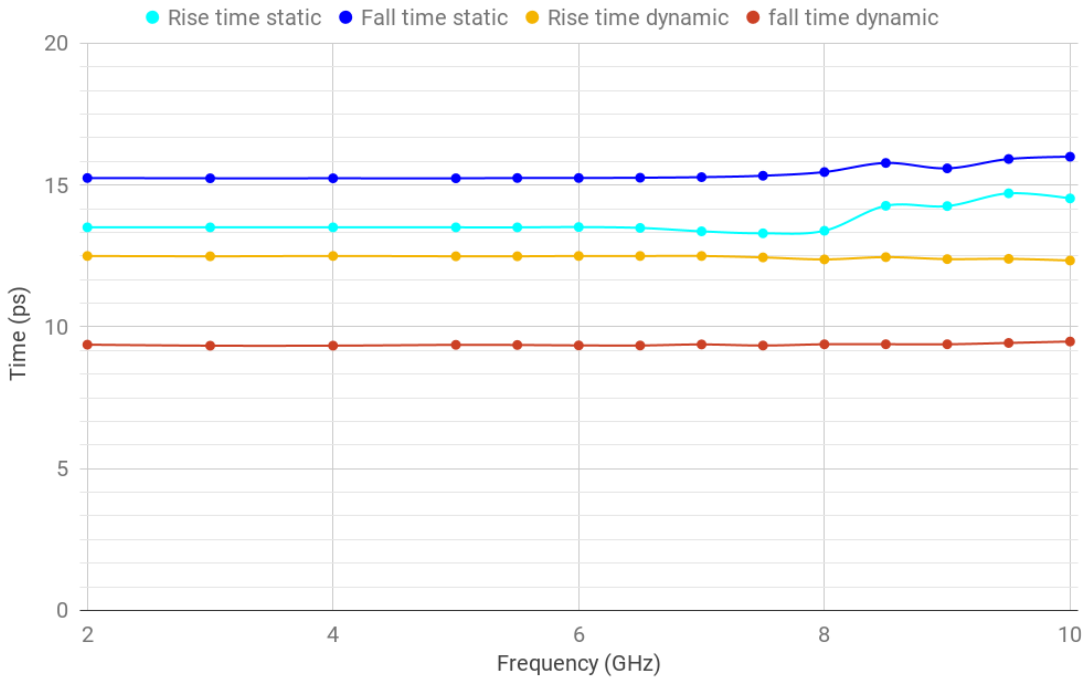

Figure 5.7: Rise and fall time of both circuits

5.2.4 Signal output clocks

This section discusses the results of the signal output clocks of both the clock generation circuits.

5.2.4.1 Output of the static divider implementation

Figures 5.8, 5.9 and 5.10 respectively show the output of the clock generation circuit at different frequencies. This output contains of four clocks with each a duty cycle of 25%. Each clock has a different phase such that two or more clocks shouldn't be overlapping. Overlapping would cause multiple clocks to be high which can be fatal for the circuit that is connected to the clock generation circuit. It can for example cause short circuiting in the next stage or change the information being send.

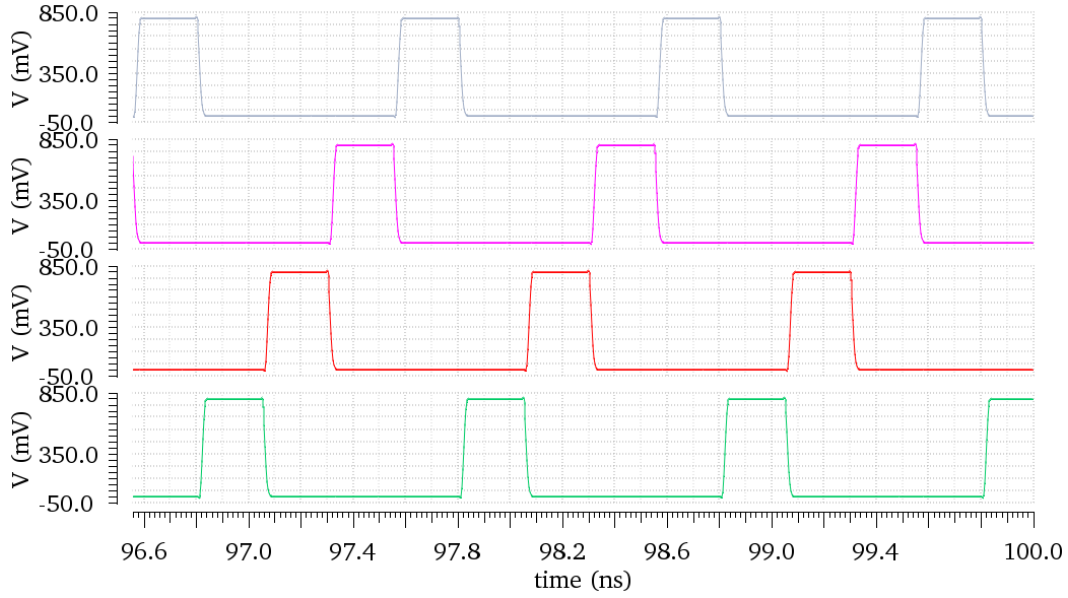

Figure 5.8: All Clocks of the static divider implementation at 1GHz

Figure 5.8 shows the four output clocks running at 1 GHz output frequency. It's clearly seen that the pulses are full swing. This, together with figures 5.5 and 5.6 leads to the conclusion that the boundary conditions are met and that the static divider implementation is usable at 1 GHz.

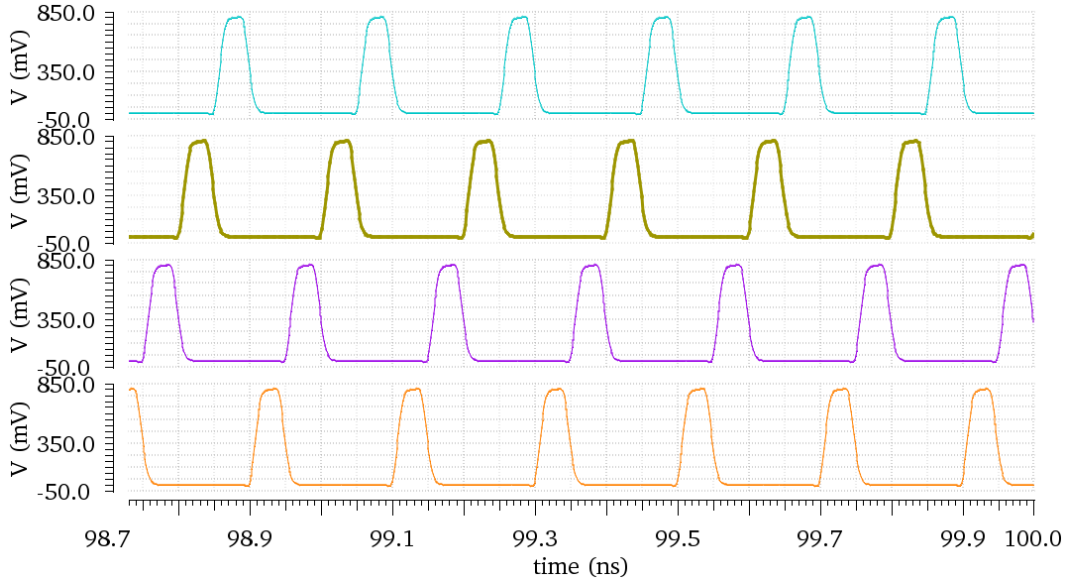

Figure 5.9: All Clocks of the static divider implementation at 5GHz

Figure 5.9 shows the four output clocks running at 5 GHz output frequency. The shape of the clocks are not as 'squared' as the signals at 1GHz but still have a full swing. This, together with figures 5.5 and 5.6 leads to the conclusion that the boundary conditions are met and that the static divider implementation is usable at

5 GHz.

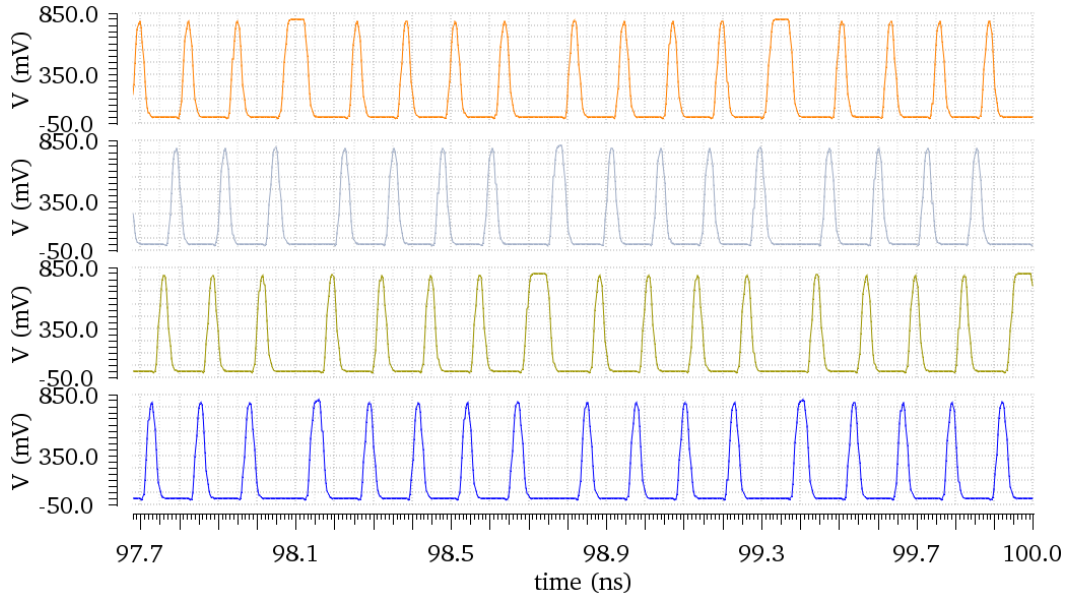

Figure 5.10: All Clocks of the static divider implementation at 8GHz

Figure 5.10 shows the four output clocks running at 8 GHz output frequency. It is clearly seen that the circuit can't handle the speed of the input clock: It shows hick ups. This already shows that the static divider implementation is not usable at 8 GHz. This was expected because of the estimated maximum operating frequency from sections 5.2.1 and 5.2.2.

5.2.4.2 Output of the dynamic divider implementation

Figures 5.11, 5.12 and 5.13 respectively show the output of the clock generation circuit at different frequencies. This output contains of four clocks with each a duty cycle of 25%.

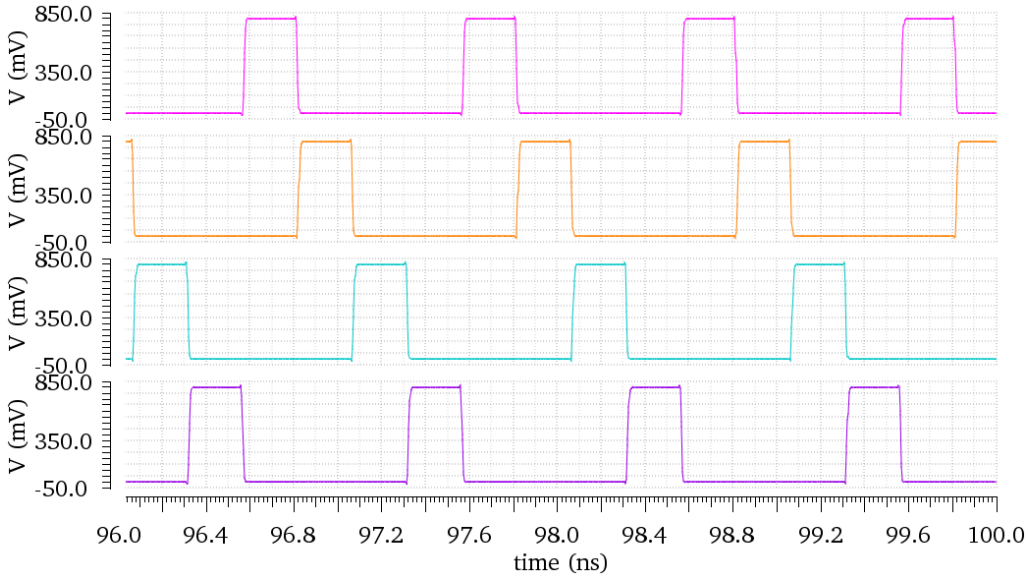

Figure 5.11: All Clocks of the dynamic divider implementation at 1GHz

Figure 5.11 shows the four output clocks running at 1 GHz output frequency. It's clearly seen that the pulses are full swing. This, together with figures 5.5 5.6 leads to the conclusion that the boundary conditions are met and that the dynamic divider implementation is usable at 1 GHz.

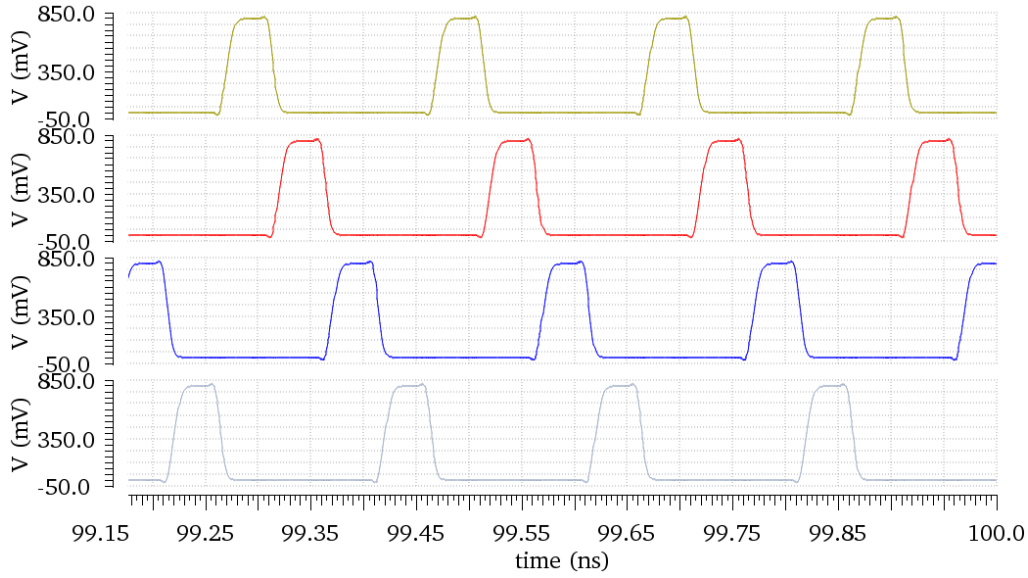

Figure 5.12: All Clocks of the dynamic divider implementation at 5GHz

Figure 5.12 shows the four output clocks running at 5 GHz output frequency. The shape of the clocks are not as 'squared' as the signals at 1GHz but still have a full swing. This, together with figures 5.5 and 5.6 concludes that the boundary conditions are met and that the dynamic divider implementation is usable at 5 GHz.

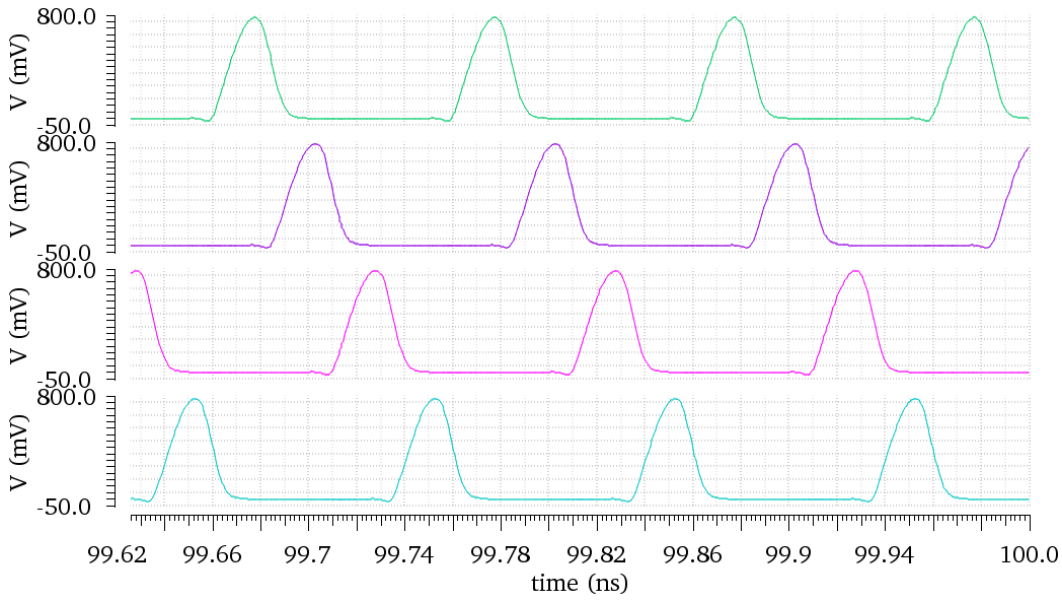

Figure 5.13: All Clocks of the dynamic divider implementation at 10GHz

Figure 5.13 shows the four output clocks running at 10 GHz output frequency. Although the shape of the pulses aren't 'squared' anymore it doesn't show any hick ups and could still be usable. The estimated values from sections 5.2.1 and 5.2.2 also confirm that the boundary conditions are still met but are not ideal because it is at the edge of the boundary conditions.

Chapter 6

Conclusions and recommendations

6.1 Conclusions

Many mixers in radio receivers use quadrature mixers with 25% duty cycle clock inputs with ideally no overlap. This thesis mainly focused on the divider which is used in the clock generation circuit capable of making these 25% duty cycle clocks. The goal was to develop a comparison method such that conclusions about two implemented dividers can be made in relation to the power consumption and the operating frequency range. Two implementations of these divider implementations are used by the IC-Design group: a static divider and a dynamic divider. To compare the power consumption the linear relation with the load capacitances has been used. To determine the load capacitances certain conditions had to be full filled. First the divider stage had to be driven by the same amplification/clipping stage such that the input capacitance of the divider is the only variable when replacing the divider stage. For the same reason also the load capacitance of the divider circuit is made the same. It's determined that the dynamic divider has a bigger input capacitance than the static divider which means that it is a bigger load capacitance for the amplification/clipping stage demanding for more power from the source. Also the output capacitance of the dynamic divider is bigger such that it has to charge more load capacitance. This means that the dynamic divider has more power consumption in the circuit. The power consumption of the stages is also simulated and verifies the found conclusions. The found power consumption ratio determined by the load capacitances between the circuits only differs less than 8% from the simulated power consumption ratio. This leads to the conclusion that the load capacitance ratio used in this method is a good indication for the power consumption ratio between the two circuits.

The operating frequency range is determined using boundary conditions. One of the conditions is that the output signal has a full swing output and the other condition is that the duty cycle of the output should be between 23% and 26%. These condi-

tions are necessary for proper operation of the quadrature mixers. Using the power consumption, duty cycle and rise and fall time conditions of the signals the operating frequency ranges of the circuits are determined. It shows that the static divider implementation has an operating output frequency range up to 6.5 GHz. Under the same conditions it established that the dynamic divider implementation even works up to 10 GHz.
This leads to the final conclusion that the static divider is proffered above the dynamic divider for output frequencies below 6.5 GHz due to the much lower power consumption. If an operating frequency higher than 6.5 GHz but lower than 10 GHz is required the dynamic divider implementation is the only choice between the two.

6.2 Recommendations

Due to time limitations only power consumption and operating frequency range of the two circuits are analyzed and discussed. In further research also the phase noise can be determined and compared.
The thesis includes rise and fall time results but those are barely used. Further research can go deeper in on the rise and fall times and how the circuit causes these times.
It can also be interesting to investigate the lowest limit of the divider implementations, especially the lowest limit of the dynamic divider.
There was an idea to make the static divider implementation work on higher frequencies by putting a higher load and putting the static dividers in parallel to each other. This way it is maybe possible to achieve a higher operating frequency range but with less power than the dynamic divider implementation. This was not done and could be interesting to do in future research.

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