Handling gate leakage in FDSOI CMOS for a Passive Discrete-Step Attenuator

R.W. Heeres, *Bachelor Electrical Engineering*

***Abstract*—In this paper an Operational Transconductance Amplifier (OTA) circuit is proposed that handles the spread in gate voltage and on-resistance, due to gate leakage and process variation, of RVT transistors bootstrapped with an RVT transistor to improve IM2- and IM3-distortion cancelling in the 22nm FDSOI CMOS technology of GlobalFoundries. The circuit is designed and simulated in the Cadence environment. The final proposed circuit is singe-supply, low-power and operates in subthreshold. The spread in gate voltage and on-resistance with process variation has been reduced. However, the distortion cancelling has degraded due to parasitics of transistors and the bandwidth of the OTA.**

Keywords*—FDSOI CMOS, Operational Transconductance Amplifier, Gate leakage, On-resistance spread, Process variation, Distortion cancelling

I. Introduction

IN [1] a novel wideband IM2- and IM3-cancellation technique for single-ended resistive discrete-step attenuators in FDSOI CMOS is proposed. An attenuator is a circuit used to reduce the power of a signal, this is required for circuits that cannot handle high power signals. A resistive attenuator means the power is reduced using resistive elements. A discrete-step attenuator has two modes of operation, a certain fixed attenuation and infinite attenuation. The mode of the attenuator is controlled using switches, implemented in this design as NMOS devices. The switches are controlled digitally. By combining multiple discrete-step attenuators, either parallel or in series, more attenuation values can be achieved. Ideally an attenuator is linear, that is, the output is a scaled version of the input signal. Due to non-zero on-resistance of the transistors a portion of the input signal is across the switch. Along with the non-linearity of transistors, the attenuator is non-linear. Consequently, harmonic distortion and intermodulation distortion is introduced to the signal by the attenuator. [1] introduces a technique to cancel the second (IM2) and third order (IM3) intermodulation distortion, based on an existing technique to cancel the third order intermodulation distortion [2]. Figure 1 shows an attenuator using the proposed technique of [1].

An important technique to cancel IM3-distortion is bootstrapping the gates of the switches in the attenuator [1] [2]. In [1] it is chosen to use a diode-connected transistor as bootstrap resistor, transistors M3, M6 and M9 in Figure 1. As described in [1] the bootstrap transistors cause a degradation in IM3-cancellation when using RVT (Regular Voltage Threshold) transistors as resistor compared to ideal resistors. This is caused by variation in the on-resistance of the switches in the attenuator (M1, M2, M4, M5, M7 and M8). This variation is caused by a combination of gate leakage in the attenuator transistors and the high bootstrap resistance. The high bootstrap resistance is desired to make the transistors more linear and reduce the input capacitance of the transistors [1]. In [1] this variation in on-resistance has been reduced by using thick-oxide transistors, as these transistors have a much lower gate leakage. However, these thick-oxide transistors are larger than RVT transistors, when sized to the same on-resistance and for the same overdrive voltage. Due to their larger size, performance at higher frequencies is limited.

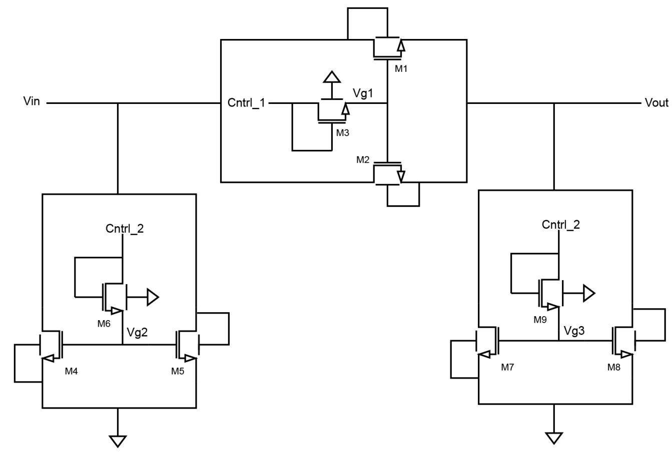


Fig. 1: A novel wideband passive discrete-step attenuator circuit [1]

The goal of this paper is to find a solution for the effect of gate leakage and the spread in on-resistance with process variation, and thus improve the IM3-cancellation of the attenuator using RVT FDSOI CMOS transistors. This leads to the following main research question: How can a circuit be designed to counteract the gate leakage and set a well-defined DC gate voltage for RVT FDSOI CMOS transistors in a passive discrete-step attenuator so the on-resistance is independent of process variation and thus improving the distortion cancelling in the attenuator?

This main question has been divided into six subquestions:

1) What circuits already exist to compensate the gate leakage in CMOS transistors?
2) What circuits already exist to keep the on-resistance independent of process variation in CMOS transistors?
3) How can a circuit handle the gate leakage and set a well-defined DC gate voltage for an RVT FDSOI CMOS transistor?

4) How can a circuit handle the gate leakage and set a well-defined DC gate voltage for an RVT FDSOI CMOS transistor so the on-resistance is independent of process variation?
5) What is the relation between the on-resistance and the gate voltage of RVT FDSOI CMOS transistors in a passive discrete-step attenuator with respect to third order distortion?
6) What influence has the designed circuit on the distortion cancelling in a passive discrete-step attenuator?

This research restricts itself to handling the gate leakage and the spread in on-resistance with process variation for RVT FDSOI CMOS transistors in a passive discrete-step attenuator as described in [1]. However the circuit proposed in this paper could probably be used in a variety of applications.

In section II existing circuits that deal with the described problem are explained and considered for (part of) the solution. Furthermore background information about the problem is given. In section III the research methods used in this paper are described. After that, in section IV the problem is analysed using Cadence simulations and a concept circuit is proposed which solves the problem. In section V the circuit is designed. Next, in section VI the results of the proposed solution are shown and compared to existing solutions. Finally, in section VII the conclusion of this research is drawn.

II. Gate leakage and Existing solutions

Gate leakage is not a new problem, research has already been done into decreasing and handling the gate leakage in CMOS transistors. In this section several techniques are explored and evaluated whether they can be used to handle the gate leakage in the FDSOI CMOS passive discrete-step attenuators. Additionally, background information about gate leakage is given.

A. Gate Leakage

As transistors keep scaling down, gate leakage starts to play a bigger role in the design of circuits [3]. In an ideal transistor the gate has an infinite resistance, however in real applications this resistance is finite. This can cause a current to leak through the gate in the range of pA to nA. This leakage is due to a smaller thickness of the oxide layer between the gate of the transistor and its channel and thus an increase of tunneling current through the oxide layer from the gate to the channel.

When bootstrapping the gate with a high-ohmic resistance, this gate leakage causes a considerable voltage drop over this resistance. In [1] and Figure 2b this high-ohmic resistance is implemented as a diode-connected transistor (M2). To properly bias the gate, this voltage drop can be compensated for using a higher voltage. However as gate leakage of M1 and on-resistance of M2 are influenced by process variation, this voltage drop is not constant over the process. Due to improper biasing, the on-resistance of M1 changes. This results in a scaling of distortion currents in the attenuator, this causes the currents to not match and thus resulting in a decrease in performance of IM3-cancellation of the attenuator.

B. Transistor types

Changing the materials or architecture of MOSFETs by using a different transistor type can reduce gate leakage [4]–[6].

In [1] it was chosen to implement all transistors as NMOS thick-oxide low voltage threshold transistors instead of RVT transistors. The benefit of this is a lower gate leakage due to the thicker oxide layers. Furthermore the maximum voltage of these transistors is higher then the RVT transistors, 1.8V and 0.8V respectively. However, these thick-oxide transistors are bigger than the RVT transistors with the same on-resistance and cannot handle frequencies as high as the RVT transistors can.

Next to the NMOS thick-oxide there is also a PMOS super-low voltage threshold thick-oxide transistor available for the bootstrap transistor. This transistor has a lower bootstrap resistance for the same size as the NMOS thick-oxide, and thus the voltage drop is less for this bootstrap transistor.

C. Transistor stacking

In [7] a technique called transistor stacking is used to decrease the total gate leakage of a circuit. As the transistors should be stacked, this technique is applicable to a limited topology. Furthermore this technique only reduces the gate leakages of transistors when turned off.

D. SVL Circuit

A self-controllable-voltage-level (SVL) circuit is another technique used to reduce gate leakage in transistors [8]. Like transistor stacking, this technique is also only applicable to a limited topology, as the drain and source should be connected to a voltage supply and ground respectively. Furthermore the gate leakage is only reduced when the transistor is turned off.

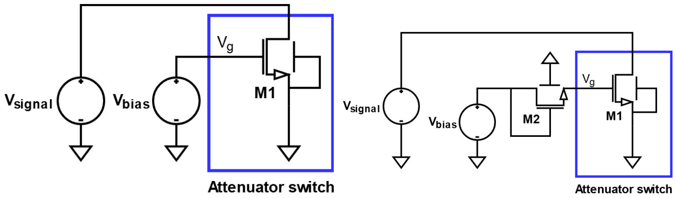
E. Evaluation

Evaluating the above-mentioned solutions, no viable solution to the research question can be found. The transistor type cannot be changed as the goal is to use RVT FDSOI CMOS transistors from GlobalFoundries, so the materials and architecture are fixed. The transistor stacking and SVL circuit techniques are also not viable as the gate leakage should be reduced in the on-state. Furthermore these techniques limit the way in which the transistors can be used.

In conclusion a new technique should be developed to handle the effect of the gate leakage.

III. Method

The research questions mentioned in section I are answered using several research methods. The first and second sub-questions are answered by using a qualitative research method. A literature study is done to collect answers which in turn are evaluated. The third and fourth sub-questions are answered using a quantitative research method. First a specification is determined to which the circuit must comply, next a circuit



(a) Direct gate voltage drive (b) Bootstrapped

Fig. 2: Transistor topologies using voltage source and bootstrapping

is designed meeting the requirements. This circuit is then tested and verified trough simulations whether it actually is an adequate solution, in case it is not, a new circuit is designed. The fifth sub-question is also answered using a quantitative research method, comparing data from simulations of the proposed attenuator circuit in [1]. The last question is answered using a quantitative research method, the designed circuit is tested and compared with the final circuit in [1] using simulations. Finally the main research question is answered using both qualitative and quantitative methods. This question is answered by combining answers of the sub-questions and drawing a conclusion.

All simulations are performed in Cadence using the 22nm FDSOI technology libraries and models of GlobalFoundries. Nominal simulations are done using the tt_pre model library using single run simulations. The spread simulations, with process variation, are done using the mc_pre model library and Monte Carlo Sampling simulations with 1000 points.

As the simulation is based on libraries containing statistical data of components, the real circuit will most probably not be equal to the nominal simulations and there is a margin of error due to process variation. For this, Monte Carlo simulations are done. Monte Carlo simulations include the statistical data of process variation of the transistors.

IV. Problem Analysis And Proposed Solution

To determine the requirements for the solution, first the problem and the existing thick-oxide solution are analysed. Figure 2a shows a circuit in which the gate of a transistor is driven directly by a voltage source. In Figure 2b a circuit is shown with a transistor bootstrapped by a diode-connected transistor. In both cases the drain of M1 has a voltage of 1mV provided by a voltage source and the source of M1 is connected to ground. The voltage sources connected to the gates of transistors M1 provide the maximum voltage the transistor can handle, 0.8V and 1.8V for RVT and thick-oxide transistors respectively. Properties of importance for the analysis are the spread of the drain-source on-resistance of transistors M1, the spread of the gate voltage of M1 and the spread of the gate current leakage of M1. Transistor M1, for both the RVT and thick-oxide transistor, is sized to have a drain-source on-resistance of 50Ω. To maximize bootstrap performance, a high resistance and a low capacitance are desired for transistor M2 [1]. A small transistor accomplishes this, hence for all setups M2 is minimum sized [1]. Table I, Table II and Table III show the on-resistance, gate voltage and gate current leakage spreads of M1 respectively. It can be seen that the spread in on-resistance of thick-oxide, NMOS and PMOS, bootstrapped thick-oxide transistors is smaller than the spread of RVT bootstrapped RVT transistors. In addition, the mean of the RVT-RVT setup is not very close to the desired 50Ω, unlike the other setups. It can be seen that the PMOS thick-oxide bootstrap variant performs the best of all available solutions, when looking at only the spreads in current leakage, gate voltage and on-resistance.

TABLE I: R_{M1} spread

M1 Type	M2 Type	1σ [Ω]	Mean [Ω]	Min [Ω]	Max [Ω]
RVT	None	1.758	50.06	44.55	56.79
RVT	RVT	2.565	54.67	47.59	63.91
Thick-oxide	None	1.43	50.03	46.08	54.05
Thick-oxide	Thick-oxide	1.44	50.97	47.08	55.071
Thick-oxide	Thick-oxide P	1.414	50.02	46.11	54.03

TABLE II: V_g spread

M1 Type	M2 Type	1σ [mV]	Mean [mV]	Min [mV]	Max [mV]
RVT	None	0	800	800	800
RVT	RVT	19.8	730	668.4	780.3
Thick-oxide	None	0	1800	1800	1800
Thick-oxide	Thick-oxide	2.445	1763	1752	1768
Thick-oxide	Thick-oxide P	0.0031	1800	1800	1800

TABLE III: I_g spread

M1 Type	M2 Type	1σ [pA]	Mean [pA]	Min [pA]	Max [pA]
RVT	None	191.2	452.6	131.5	1465
RVT	RVT	103.5	282.1	95.51	797.4
Thick-oxide	None	0.003374	0.04576	0.03793	0.06118
Thick-oxide	Thick-oxide	0.00246	0.03758	0.03167	0.04849
Thick-oxide	Thick-oxide P	0.003373	0.04576	0.03794	0.06124

Increasing the size of the RVT bootstrap transistor, would reduce the bootstrap resistance and the voltage drop over the transistor, resulting in a better defined bias voltage. Unfortunately, with increased size there is still a voltage drop that changes with process variation. Increasing the size of the transistor too much results in a bootstrap resistance that is too low or a capacitance that is too high, making the gate function as an AC ground again.

In earlier mentioned solutions [4]–[8] the gate leakage of transistors is minimized, however this may not be necessary to obtain a solution robust to process variation. As the gate leakage of transistors varies with process and the gate voltage should remain at a defined DC level, a circuit can be designed which measures the gate voltage and applies current to the gate as needed. To maintain the bootstrapping benefits in the attenuator, the circuit should have a high output and input impedance. Also, a high input impedance minimizes the required current to obtain the defined voltage level.

The proposed circuit is an Operational Transconductance Amplifier (OTA) with negative feedback. The unity gain fre-

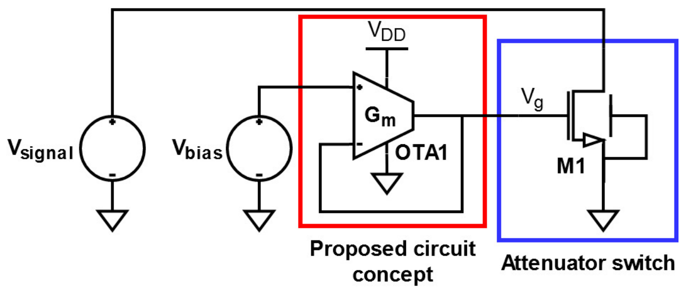


Fig. 3: Proposed concept

quency of the OTA should be smaller than the minimum operating frequency of the attenuator, otherwise the gate voltage is also forced to 0.8V for the operating frequencies of the amplifier. This is not desired as this counteracts the portion of the attenuator signal over the gate, making the transistor less linear [1]. The attenuator in [1] has been designed for signals with frequencies equal to or higher than 1Mhz, so the unity gain frequency should be smaller than 1MHz.

An ideal circuit as described above is depicted in the red rectangle in Figure 3, M1 is an RVT transistor of the attenuator. The proposed circuit has a voltage gain less than unity for frequencies equal to or higher than 1MHz, else the voltage gain is G_mR_L. G_m is the transconductance of OTA1, R_L the load resistance. The inputs of OTA1 are the desired voltage level and the actual gate voltage. OTA1 produces a current which sets the gate voltage due to the gate resistance of M1. Furthermore, supply voltages are connected to OTA1, an upper supply voltage of V_{DD} and as lower supply voltage, ground. Transistor M1 is an RVT transistor sized to 50 Ohm.

V. Circuit Design

As mentioned in section IV the circuit should have a limited bandwidth to ensure proper function of the attenuator. The unity gain frequency is equal to the Gain-Bandwidth Product (GBP), so the GBP should be smaller than 1MHz. The minimum phase margin is determined at 70 degrees, as the overshoot should be minimized and not exceed 0.9V. Additionally the gain margin should be at least 10dB, so the circuit is still stable for an increase in loop gain with a factor up to 3 due to a change in device parameters.

The voltage gain of the proposed circuit determines the precision, the bandwidth and the slew rate of the amplifier. As can be seen in Figure 3, OTA1 is in a closed-loop configuration. The DC closed-loop gain of the circuit is described by equation 1.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{V_g}{V_{bias}} = \frac{G_mR_L}{1+G_mR_L} \tag{1}$$

R_L is determined by the resistance of the gate of M1 and the input resistance of OTA1. As OTA1 is ideal, its input resistance is infinite. Simulating the gate resistance of M1, shows that it decreases with increasing gate current. Moreover, simulating the spread of the gate resistance shows it varies with process. The minimum gate resistance due to process variation with a gate voltage of 0.8V is 546.2$M\Omega$. To determine the minimum gain, it is chosen to allow a 1mV offset in the gate voltage. This 1mV offset is chosen after simulating the spread in on-resistance of an RVT transistor in the setup of Figure 2a with a varying V_{bias} voltage. This results in a minimum gain of 799, using the minimum load resistance of OTA1, the minimum transconductance can be determined. In the attenuator, the circuit is connected to two parallel transistors, so the load resistance consists of two parallel gate resistances. This results in a minimum load resistance of 273.1$M\Omega$. Using this, the minimum G_m is calculated as 3μS. The maximum required output voltage is 0.8V, so V_{DD} is chosen as exactly 0.8V as no higher voltage output is required.

As speed is not the goal of this concept, the slew rate of the amplifier is not important in designing the circuit for this application.

Knowing all parameters of the ideal circuit, the proposed concept is DC simulated to test whether it is robust to process variation. Table IV shows that the proposed concept is very close to the direct voltage source driven RVT transistor set-up and sufficiently robust to process variation. Additionally, the bootstrapping capabilities have been maintained, as the input and output impedance of an ideal OTA are infinite.

TABLE IV: R_{M1} spread

Spread	1σ	Mean	Min	Max
R_{M1} [Ω]	1.76	49.94	43.42	55.95
V_g [mV]	0.1281	799.7	799	799.9
I_g [pA]	192.2	456.3	132.8	1492

As the proposed circuit concept is functional, the OTA itself is designed. It is chosen to design the amplifier using only one stage, a differential pair. This is done because the input signal is a differential signal and the required transconductance is not very high. Additionally, the differential pair has a very high input impedance and is capable of having a high output impedance. Also, having only one stage simplifies the stability of the amplifier as only a limited amount of extra poles is introduced. Figure 4 shows the design of the OTA outlined by the green rectangle.

The differential pair is biased using a current source. By biasing the differential pair with a current source, the gain of the amplifier is not dependent on the Commom-Mode of the input signals. The current source is implemented with the current mirror consisting of transistors M6 and M7. This is done so the current can be supplied using an external current source, provided M6 and M7 are in saturation. The pair is active loaded with the current mirror consisting of M2 and M3. Due to the current mirror, i_{out} is equal to $I_{d2} - I_{d4}$, provided M2 and M3 are in saturation. As the output current is $I_{d2} - I_{d4}$, the output voltage is dependent on the load resistance.

V_{DD} was chosen as 0.8V, however in the transistor design there is a voltage drop over M3. Due to this, V_{DD} should be increased. It is chosen to increase it to 1.8V, as this voltage supply is already available. Due to the increase of V_{DD}, the voltage drops over all transistors will also increase. RVT transistors can handle a maximum voltage difference of 0.9V across its terminals, so it is chosen to implement the transistors in the OTA design as thick-oxide transistors. These transistors can handle a maximum voltage difference of 1.8V. Furthermore, the gate resistance is considerably higher in thick-oxide transistors, so M4 and M5 have a very high input impedance.

To reduce the required area of the circuit and to reduce the parasitics of the transistors, M2, M3, M6 and M7 should be as small a possible. On the other hand, for good matching of the transistors the size should not be minimum-sized. For these reasons it is chosen to use 2 times the minimum size of the transistor. As the transistors are thick-oxide, the widths are 320nm and the lengths 300nm. At this point only I_{bias} and the size of M4 and M5 need to be determined. The width of both M4 and M5 is denoted by $W_{4,5}$ and the length by $L_{4,5}$. As described in [9], the transconductance of the circuit is determined using equation 2, with $\Delta V_{in} = V_{in1} - V_{in2}$ and $\Delta I_D = I_{D1} - I_{D1}$:

$$G_m = \frac{\delta \Delta I_D}{\delta \Delta V_{in}} = \frac{1}{2}\mu_n C_{ox}\frac{W_{4,5}}{L_{4,5}}\frac{\frac{4I_{bias}}{\mu_n C_{ox}\frac{W_{4,5}}{L_{4,5}}} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{bias}}{\mu_n C_{ox}\frac{W_{4,5}}{L_{4,5}}} - \Delta V_{in}^2}} \quad (2)$$

For $\Delta V_{in} = 0$ equation 2 becomes equation 3 and is equal to the transconductance of each device [9].

$$G_m = g_m = \sqrt{\mu_n C_{ox}\frac{W_{4,5}}{L_{4,5}} I_{bias}} \quad (3)$$

Equation 3 can be used to solve for I_{bias} with a given g_m, $\mu_n C_{ox}$ and $W_{4,5}/L_{4,5}$. Again M4 and M5 are chosen 2 times minimum-size, for the same reasons as before. Using the minimum transconductance, the minimum bias current is calculated as 75nA. The bias current is very low, so it can be expected that the transistors are in subthreshold, not in saturation. This can be solved by increasing the bias current. However, the transistors can also be used in the subthreshold region.

In the subtreshold region V_{ds} influences the drain current of the transistor as can be seen in equation 4 [10].

$$I_d = I_o \frac{W}{L} exp(\frac{V_{gs} - V_{th}}{nV_T})(1 - exp(-\frac{V_{ds}}{V_T})) \quad (4)$$

This influence is unwanted as the drain current ideally should only depend on V_{gs}. The influence of V_{ds} can be minimized by setting V_{ds} at least 4 times as high as V_T. This reduces the negative exponential significantly to a maximum of 0.018 and thus has a minimal influence on the drain current. At room temperature $V_T = 26mV$, so V_{ds} should be at least 104mV.

A DC simulation of the OTA-design shows all transistors have a V_{ds} much greater than 104mV. The bias current is reduced to 4nA to reduce the power usage of the circuit. At 4nA all transistors have a V_{ds} just above 104mV. AC simulating the circuit by setting a 1nV AC signal on V_{in2}, gives an output current of 67.3fA for frequencies up to 5kHz, after which it increases. So the transconductance of the circuit is at least 67.3m, which is more than sufficient.

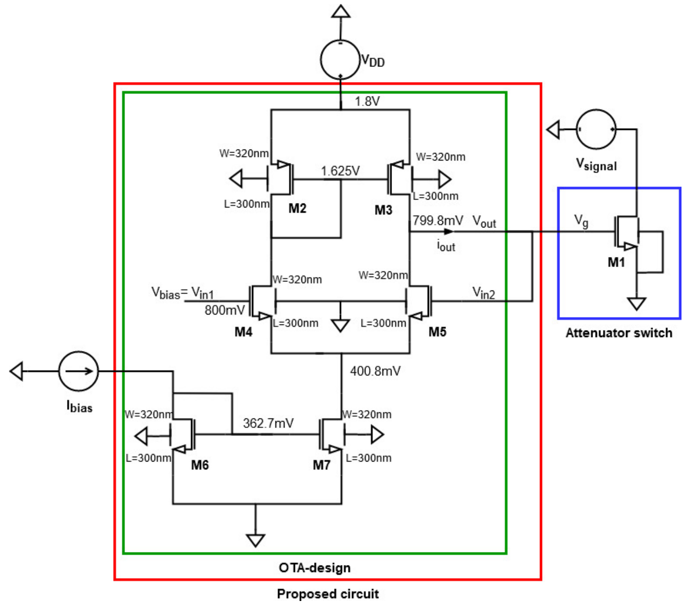


Fig. 4: Final proposed circuit design

A DC simulation of the circuit, configured as the proposed circuit with attenuator switch in Figure 4, results in a V_g of 799.8mV. As all parameters are determined, the proposed circuit in Figure 4 is the final circuit. Table V shows the final parameter values of the elements of the proposed circuit. The widths and lengths of transistors are denoted with a subscripts corresponding to the transistor numbers.

TABLE V: Final parameter values

Parameter	Value
W_1	5.781um
L_1	20nm
W_{23}	320nm
L_{23}	300nm
W_{45}	320nm
L_{45}	300nm
W_{67}	320nm
L_{67}	300nm
Ibias	1.7nA
Vdd	1.8V

VI. Results

Figure 5 shows the results of a stability analysis. The proposed circuit has a phase margin of 86.2 degrees and a gain margin of 13.4dB, both more than sufficient to be considered stable. Furthermore the unity gain frequency is 1.5MHz, higher than the maximum 1MHz. This results in a decrease of bootstrap performance in the 1-1.5MHz range, as can be seen in the bootstrap performance comparison.

Figure 6a shows using transient analysis that the settle time of the circuit 1us, with no overshoot. The voltage settles to

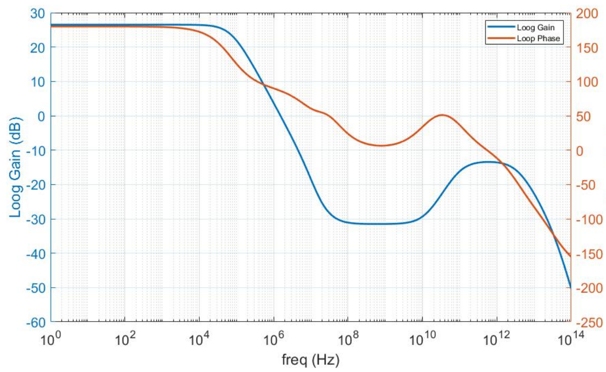
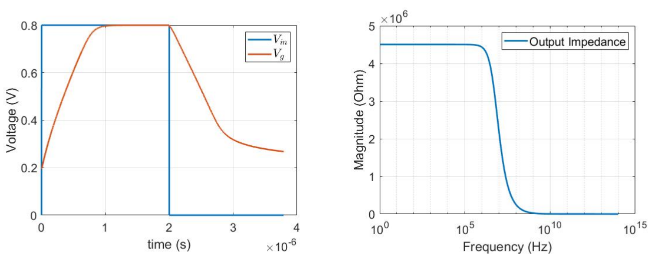


Fig. 5: Stability analysis of the final circuit

799.8mV, which is within the allowed error of 1mV. The circuit has quite a slow turn-off time, the discharging of capacitors is limited by the small gate leakage of the attenuator switch. Furthermore the circuit never discharges fully to ground, as M7 is biased by the current source, which causes a drain-source voltage not equal to zero.

Figure 6b shows the output impedance of the proposed circuit. The output impedance decreases significantly over frequency, this is caused by parasitic capacitances of the transistors. However, the output impedance might still be big enough, as the impedance of the transistor capacitances also decreases over frequency.



(a) Transient analysis (b) Output impedance

Fig. 6: Transient and output impedance analysis

Table VI and Table VII show the gate voltage spreads and the on-resistance spreads of the proposed circuit, the proposed circuit concept and existing solutions. These spreads are simulated with process variation and mismatch for all transistors.

Comparing the proposed concept with the designed circuit shows that the ideal circuit performs better than the non-ideal circuit. The mean of the gate voltage in the non-ideal circuit is still within the desired 1mV range, however the spread is bigger. This results in a bigger spread in on-resistance, while the mean of the on-resistance is still around 50Ω. The difference in on-resistance spread is, in contrast to the gate voltage spread, small.

When looking at the performance of the circuit compared to the NMOS thick-oxide bootstrapped thick-oxide transistor, it can be seen that the gate voltage spread is larger in the designed circuit and the mean is closer to its desired value. This results in a larger on-resistance spread while the mean is closer to 50Ω. However, the differences in spread and mean of the on-resistance are small.

Compared to the PMOS thick-oxide bootstrap variant, the spread in gate voltage of the proposed circuit is larger, but the difference of the spread in on-resistance is not big. The means are both very close to the desired value, for both the gate voltage and the on-resistance.

The proposed circuit does perform much better than the RVT bootstrapped RVT transistor. The gate voltage spread has been halved, which results in a smaller on-resistance spread. The mean is also much better, as can be seen in both the mean of the gate voltage and the mean of the on-resistance.

The proposed circuit approaches the on resistance spread and mean of the RVT transistor without bootstrapping.

TABLE VI: V_g spread

M1 Type	M2 Type	1σ [mV]	Mean [mV]	Min [mV]	Max [mV]
RVT	None	0	800	800	800
RVT	RVT	19.8	730	668.4	780.3
Thick-oxide	None	0	1800	1800	1800
Thick-oxide	Thick-oxide	2.445	1763	1752	1768
Thick-oxide	Thick-oxide P	0.0031	1800	1800	1800
RVT	Ideal OTA	0.1281	799.7	799	799.9
RVT	Non-ieal OTA	9.568	799.3	762.7	830.4

TABLE VII: R_{M1} spread

M1 Type	M2 Type	1σ [Ω]	Mean [Ω]	Min [Ω]	Max [Ω]
RVT	None	1.758	50.06	44.55	56.79
RVT	RVT	2.565	54.67	47.59	63.91
Thick-oxide	None	1.43	50.03	46.08	54.05
Thick-oxide	Thick-oxide	1.44	50.97	47.08	55.071
Thick-oxide	Thick-oxide P	1.414	50.02	46.11	54.03
RVT	Ideal OTA	1.76	49.94	43.42	55.95
RVT	Non-ideal OTA	1.826	49.97	43.17	55.95

Figure 7 shows the results of an AC-simulation of the final circuit with an input signal V_{signal} of 1nV. It can be seen that the bootstrapping performance of the proposed circuit is worse than all existing solutions. Not only has the bandwidth decreased, but also the portion of the attenuator input signal over the gate has decreased. Moreover, the curve is not a flat curve inside the operating range of the attenuator, this decreases the linearity even more.

At the higher frequencies there is a decrease in bootstrapping performance, due to parasitic capacitances of the transistors in the design. At the lower frequencies the performance has also decreased, but this is not of importance until inside the range of operation of the attenuator. Unfortunately, the bootstrap performance in the range 1-10MHz has also significantly decreased, due to the unity gain frequency being higher than 1MHz. The portion of the attenuator input signal over the gate has decreased due to the output impedance of the OTA. With a higher output impedance, the AC gate voltage over the gate is more towards the desired $0.5V_{signal}$.

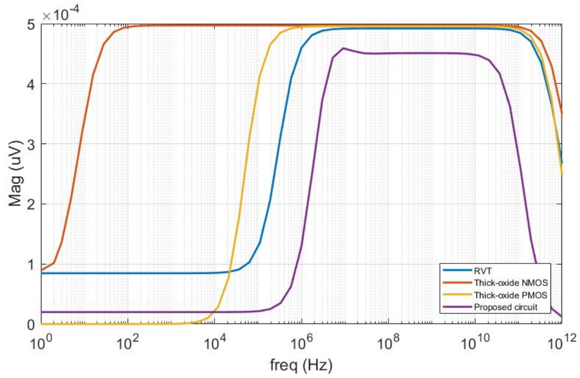


Fig. 7: Bootstrap performance over frequency comparison

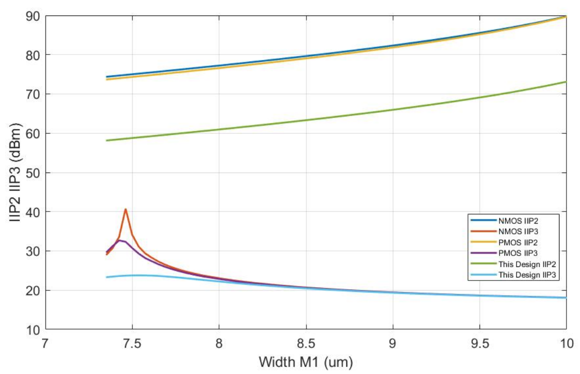


Fig. 8: IIP2 and IIP3 at 1GHz of this design and the NMOS and PMOS thick-oxide variants implemented in the attenuator of [1]

In Figure 8 it can be seen that the proposed design degrades the linearity of the attenuator quite significantly. The second order linearity is reduced, but has the same dependence on the width as the other solutions. The peak of the third order linearity has almost completely disappeared, this is caused by the decreased bootstrap performance of the OTA. This is also visible for the PMOS variant, as the IIP3 peak is somewhat lower than the NMOS variant, just like the bootstrap performance. The optima of the thick-oxide NMOS, PMOS and proposed design are 7.462um, 7.425um, 7.499um respectively.

In Table VIII and Table IX the spreads of the IIP2 and IIP3 optima of the circuits can be seen. The IIP2 and IIP3 spread are smallest in the proposed design, while the on-resistance and gate voltage spreads are biggest in the design. So this might be caused by a smaller spread in bootstrap resistance, due to the bigger size of the transistors.

VII. Conclusion

In this research a circuit is designed to make the on-resistance of an RVT FDSOI CMOS transistor independent of process variation by setting the DC gate voltage to a well-defined value. This is desired to improve the distortion cancelling of a discrete-step attenuator, as described in [1]. The usage of an RVT transistor is preferred over the usage of thick-oxide transistors, as RVT transistors have a smaller size for the same on-resistance and overdrive voltage and thus less parasitics, which should result in better performance at high frequencies.

TABLE VIII: IIP2 optima spread at 1GHz

M1 Type	M2 Type	1σ [dBm]	Mean [dBm]	Min [dBm]	Max [dBm]
Thick-oxide	Thick-oxide	1.4	74.94	71.09	80.6
Thick-oxide	Thick-oxide P	1.275	74.08	70.61	79.32
RVT	Non-ideal OTA	0.5109	58.75	57.3	60.64

TABLE IX: IIP3 optima spreads at 1GHz

M1 Type	M2 Type	1σ [dBm]	Mean [dBm]	Min [dBm]	Max [dBm]
Thick-oxide	Thick-oxide	3.773	32.64	23.92	40.99
Thick-oxide	Thick-oxide P	2.818	30.61	23.19	44.85
RVT	Non-ideal OTA	2.207	23.93	18.43	36.49

From the results of this research it can be concluded that the proposed circuit is not a viable solution to the research question. The proposed circuit does perform quite well in controlling the on-resistance of the attenuator transistor over process variation, it even approaches the RVT transistor directly driven by a voltage source. However, the circuit performs insufficient in the frequency domain. This is caused by parasitics in the circuit, due to the size of the transistors, and the bandwidth of the OTA. As a result, the distortion cancelling in a passive discrete-step attenuator is impacted negatively, compared to the thick-oxide solutions.

Multiple circuit exist to decrease the gate leakage in CMOS transistors, but these circuits only decrease the leakage in stand-by mode, not the on mode. Furthermore these techniques can only be applied in a limited topology.

No existing research has been found which designed a circuit that makes the on-resistance of CMOS transistors independent of process variation.

An OTA with unity negative feedback can handle gate leakage and set a well-defined DC gate voltage for an RVT FDSOI CMOS transistor and make the on-resistance almost independent of process variation.

This design has a slightly bigger on-resistance spread than the thick-oxide variants and a much bigger gate voltage spread. However, the bigger spread in on-resistance and gate voltage do not have a big impact on third order distortion. The third order distortion is mostly influenced by the bootstrap resistance.

The designed circuit negatively influence the distortion cancelling in a passive discrete-step attenuator, compared to the existing solutions.

Unfortunately, during a last check of this paper it was discovered the IIP2 and IIP3 simulations of the proposed circuit were conducted wrongly. The wrong type of transistor in the attenuator has been used, thick-oxide instead of RVT, but there was no time left to correct this mistake.

Due to limited time the OTA has not been designed for a specific bandwidth, which was originally a requirement during the design process. With more time and better understanding of the theory poles and zeroes in amplifiers this would be feasible. Furthermore, not much theory or research was available for circuits that deal with process variation and gate leakage when a transistor is turned ”on”, this complicates the understanding of the problem and the road to the solution. Also, due to limited time the subthreshold operation region of transistors has not been explored thoroughly using analyses, but rather using simulations.

In this research the voltage supply and the current supply have been considered ideal, this is however never the case. Furthermore, temperature changes have not been considered, but these do have a significant impact on the performance of circuit, due to the transistors operating in the subthreshold region. The temperature changes have to be compensated for in the circuit, so this circuit cannot be used in an environment with a temperature other than room-temperature. Also, the operation of the circuit in the subthreshold has mainly been determined using simulations. Using large and small signal analysis new insights can be gained in the subthreshold region which could improve its performance. In this design it was chosen, for simplicity, to use one stage, more stages however, could improve the performance at the cost of surface area. All these factors should be

VIII. Recommendations

- The OTA in this research has not been designed for a maximum bandwidth. Designing the OTA with a bandwidth smaller than 1MHz could improve the performance.
- The proposed circuit in this research does not have a very high output impedance, an enhanced circuit could be designed to increase the output impedance and improve the distortion cancelling.
- In this OTA design thick-oxide transistor are used, designing a circuit with RVT transistors could improve the performance at high frequencies.
- In this research the operation of the OTA in the subthreshold region has been determined mainly using simulations. The operation could be improved by doing a the large and small signal analysis in the subthreshold region and size the transistors and bias current to its optima.
- Do research whether an OTA with more stages can be designed for increased distortion cancellation.
- When the attenuator transistor should be turned off, the gate voltage never reaches ground. This can be solved by introducing a switch to ground at the gate of the transisor.

References

[1] E. Zijlma *A wideband IM2-and IM3-cancellation technique for single-ended resistive attenuators in FDSOI CMOS* University of Twente - ICD, Netherlands, 2020

[2] Wei Cheng, M. Oude Alink, A. J. Annema, G. Wienk and B. Nauta, *”A wideband IM3 cancellation technique for CMOS attenuators”* 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 78-80, doi: 10.1109/ISSCC.2012.6176937.

[3] HeungJun Jeon, Yong-Bin Kim and MinSu Choi, *”A novel technique to minimize standby leakage power in nanoscale CMOS VLSI”* 2009 IEEE Instrumentation and Measurement Technology Conference, Singapore, 2009, pp. 1372-1375, doi: 10.1109/IMTC.2009.5168670.

[4] B. Doris et al., *”High performance FDSOI CMOS technology with metal gate and high-k”* Digest of Technical Papers. 2005 Symposium on VLSI Technology, 2005., Kyoto, Japan, 2005, pp. 214-215, doi: 10.1109/.2005.1469272.

[5] Z. Krivokapic et al., *”Nickel silicide metal gate FDSOI devices with improved gate oxide leakage”* Digest. International Electron Devices Meeting,, San Francisco, CA, USA, 2002, pp. 271-274, doi: 10.1109/IEDM.2002.1175830.

[6] Leland Chang, K. J. Yang, Yee-Chia Yeo, I. Polishchuk, Tsu-Jae King and Chenming Hu, *”Direct-tunneling gate leakage current in double-gate and ultrathin body MOSFETs”* in IEEE Transactions on Electron Devices, vol. 49, no. 12, pp. 2288-2295, Dec. 2002, doi: 10.1109/TED.2002.807446.

[7] S. Mukhopadhyay, C. Neau, R. T. Cakici, A. Agarwal, C. H. Kim and K. Roy, *”Gate leakage reduction for scaled devices using transistor stacking”* in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 11, no. 4, pp. 716-730, Aug. 2003, doi: 10.1109/TVLSI.2003.816145.

[8] M. Drazdziulis and P. Larsson-Edefors, *”A gate leakage reduction strategy for future CMOS circuits”* ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), Estoril, Portugal, 2003, pp. 317-320, doi: 10.1109/ESSCIRC.2003.1257136.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits, Second Edition*, University of California, Los Angeles, 2017, ISBN 978-0-07-252493-2

[10] C. Yadav and S. Prasad, *”Low voltage low power sub-threshold operational amplifier in 180nm CMOS”* 2017 Third International Conference on Sensing, Signal Processing and Security (ICSSS), Chennai, 2017, pp. 35-38, doi: 10.1109/SSPS.2017.8071560.