Measurement Protocol for Stress Induced Leakage Current in MOS-Capacitors

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***Abstract*—Stress induced leakage current (SILC) has two known parts, a steady state current and a transient current. The steady state current mainly dominates the negative impact of SILC on metal oxide semiconductor (MOS) devices such as MOS-capacitors. Therefor the steady state current needs to be isolated from the transient current. In this paper the transient current of SILC post stressing and post annealing is investigated. Subsequently, a new measurement protocol is established for performing SILC measurements where the steady state current is isolated from the transient current, by applying a zero volt bias step post stress and post annealing. The new measurement protocol is tested, showing the transient current is only present post stress and does not occur post annealing. Applying the zero volt bias step in the measuring protocol post stress positively affects the behaviour of the capacitor, by removing the transient current almost completely. It reduces the transient effect of the SILC current between 50% and 72%. SILC measurements post annealing are not affected by the transient current and therefore the zero volt bias step is not necessary.**

***Keywords*—SILC, MOS-devices, trap population, annealing, measurement protocol**

I. Introduction

Flash memory makes use of floating gates of MOS-devices to store data. The oxide layer keeps the charge carriers on the floating gate. To read/write data an electric field is applied to the gate, forcing the charge carriers to tunnel through the oxide layer. This tunneling damages the oxide layer by generating traps inside the oxide layer. The effect of the traps is that they lower the required energy to tunnel through the oxide layer, meaning that the charge carriers can leak out the floating gate, resulting in a loss of the data being stored. However, it has been found that the SILC in some cases is reversible by annealing the MOS-device [6]. Currently, an accurate prediction on the life expectancy of the MOS-devices can not be made. This is partly because the SILC consists out of two parts, a steady state current and a transient current. Another reason is that a complete model on the recovery of SILC by annealing is missing. In this paper we are going to focus on the SILC and the effect of the transient component in SILC measurements. Moazzami *et al.* [5] reported a decaying reverse current when the Fowler-Nordheim stress is interrupted. Until now this effect has been ignored, however, it has not been investigated if the transient current can indeed be ignored. De Blauwe *et al.* [1] do take the transient current in to account by conducting multiple long measurements and ignoring the first few measurements. In this paper we will briefly explain SILC and its complications, further more we will discuss the found problem in literature, and the process of how a new more efficient measuring protocol is established and its effectiveness. These part will be found in the sections: Theory [II], Method [III], Optimizing Measuring Methodology [IV], and Results and Discussion [V] respectively.

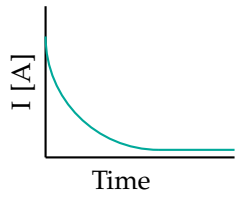


Figure 1: Decaying current[5]

II. Theory

A. Stress Induced Leakage Current

The tunneling mechanism used in this paper is called Fowler-Nordheim tunneling, which is attained by exposing the charge carriers to a high electric field. There is however a downside to forcing charge carriers to tunnel, the tunneling introduces traps inside the SiO_2 layer which result in the charge carriers needing a lower energy to tunnel [3]. This in turn results in a leakage current, reducing the reliability of the MOS device. While performing SILC measurements Fowler-Nordheim tunneling is still induced, this will results in light stressing of the MOS-capacitors.

B. Annealing

Riess *et al.* [6] has investigated the annealing kinetics of SILC generated using Fowler-Nordheim electron injection.

They discovered that for significant annealing to take place under 200 °C a bias voltage is needed. They concluded that SILC annealing is field assisted, suggesting that when performing SILC measurements the SILC can reduce due to the applied bias voltage. This is also confirmed by Cester *et al.* [2].

C. Transient current

Besides the fact that the SILC can decrease while performing measurements, an other time dependent problem is mentioned by Moazzami *et al.* [5]. In this paper they measured a decaying reversed current flow when interrupting the Fowler-Nordheim stressing as depicted in Fig. 1. 'It is attributed to the gradual depopulation of traps generated during stress' [5]. The current follows a t^{-1} decay as predicted by the trap-assisted tunneling model [4]. They report that the decay time is in the order of 10^2 to 10^3 seconds and the current decreases more in oxide thicknesses larger than 85 Å.

Currently the transient current is ignored when performing SILC measurements, since the devices used are in the thickness range below 85 Å for which no significant depopulation seems to be recorded [5]. However it is unclear what the effects of the transient current are, so this paper investigates the effects of the relaxation on the SILC measurements. We propose to add a 0 V bias part in between the Fowler-Nordheim stressing and SILC measurements, as well as before the SILC measurement post-annealing. The expected effect of adding this step can be seen in Fig. 2. It is expected to depopulate most of the traps, resulting in no trap depopulation while performing a SILC measurement.

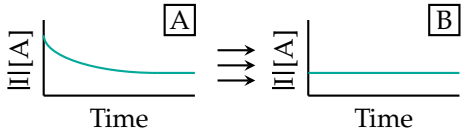


Figure 2: Expected results of the proposed measurement protocol. A: I-t curve of the old protocol. B: I-t curve of the new protocol

III. Method

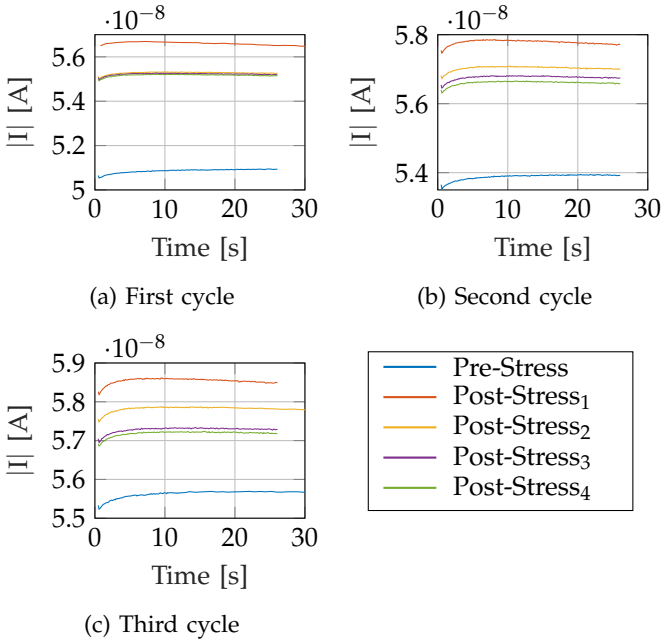
We investigate MOS-capacitors with a 75 Å SiO_2 layer, heavily doped polysilicon as the gate, and Si as the bulk material. The exact doping concentrations are unknown. The perimeter of this capacitor is 13.215 mm and the area is 9.6 mm^2. It is a polyplate capacitor on an active plate. It has a guard rail, which is kept floating.

The stress voltage is −8 V, unless specified otherwise. The anneal temperature, T_{anneal}, is 150 °C. All measurements are perfromed at room temperature, T_{room} = 22.4°C. The parameter analyzer is the Keithley 4200A-SCS with the 4200-PA Remote PreAmp on the measuring channels. The probe station is the Model 11000 from Cascade Microtech. The software used is Clarius.

To anneal the capacitors an AEG hotplate is used.

IV. Optimizing measuring methodology

To establish a measurement protocol, we first have to establish a basis of how the MOS-capacitors behave, and to investigate if the by Moazzami *et al.* reported effects are also existing in our devices. First the effects of applying a stress to the MOS-capacitors is investigated. For this a series of I-t measurements are performed where $v_{bias} = v_{gate} = -7$ V, and the capacitors are stressed for 60 s. Each measurement is 200 samples long. First a control measurement is done `Pre-Stress`, then a stress is applied for 60 s after which four measurement are performed to see what happens to the SILC as the measurement is interrupted, `Post-Stress`. This is repeated 3 times.



(a) First cycle

(b) Second cycle

(c) Third cycle

Figure 3: Current behaviour of the MOS-capacitors when applying a stress

In Fig. 3 the results can be seen. As expected the current post-stress is higher than the current pre-stress. It can be seen that in the first 10 seconds the current increases, which can be related to the population of traps. It is also interesting to see that this increase in current becomes larger with each stress cycle, as can be seen in Fig. 4. The expected cause of this is the fact that applying a stress creates traps, meaning more traps have to be repopulated while the same electric field is applied, thus resulting in a longer trap population period. Interestingly the graph for `Cycle 1` increases after stressing. A possible reason

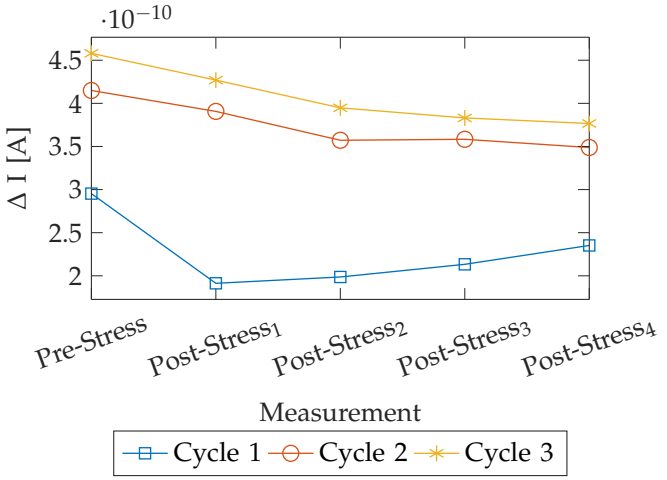


Figure 4: ΔI of the first 10 seconds for each SILC measurement

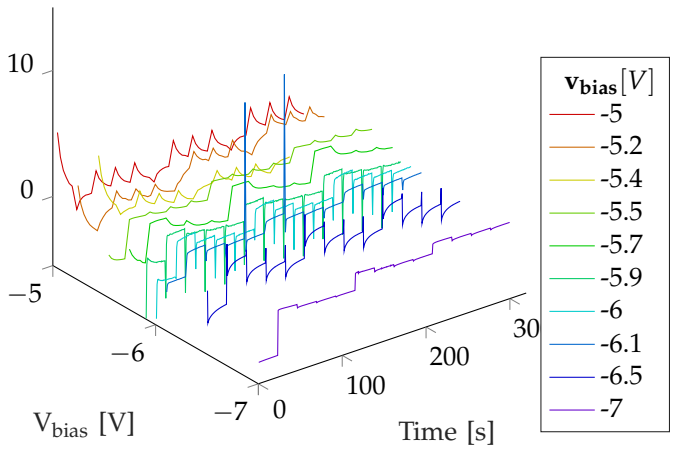


Figure 5: I-t plots for a range of bias voltages

for this is that the SILC measurement is performed at $-7\,\mathrm{V}$. This bias voltage can stress the capacitor, resulting in more traps. Since $-7\,\mathrm{V}$ is close to $-8\,\mathrm{V}$ this effect will be larger for the first measurement.

In section II we mentioned that it is not desirable when the MOS capacitor is being stressed while performing measurements, so to prevent this for the next sets of measurements, v_{bias} is set between $-5\,\mathrm{V}$ and $-7\,\mathrm{V}$. A similar measuring protocol is used as before, however only for the first stress a pre-stress measurement is done. Also the number of samples is lowered to 50, since it would take too long at the lower bias voltages, since the lower currents will take more time to sample. The results are plotted in series creating a continuous graph for each bias voltage. Since the integration time takes longer for smaller currents, the sample time is inconsistend. Therefor the smallest time is taken, which is 23 s. So the first 23 s of the data is taken. The same settings are used for the stress voltage and stress duration.

Because the current changes exponentially with the bias voltage, the data is normalized such that is has a center of zero and a standard deviation of 1. Now the graphs can be compared to each other.

Interestingly there is a difference in the shape of the graph depending on the bias voltage, this can be seen in Fig. 5. It can be seen that for a bias voltage of $-5\,\mathrm{V}$ the graph is a decaying exponential, where as for $-6.5\,\mathrm{V}$ it is an increasing exponential. This can be linked to the fact that the tunneling current is dependent on the applied electric field. As the applied bias voltage implies the electric field strength, for lower bias voltages the tunneling current is lower, resulting in a more distinguishable decaying exponential of the normal capacitor behaviour. Since we want to minimize the relaxation of the SILC, having another time dependent current, the afore mentioned decay in current, is not desirable. So

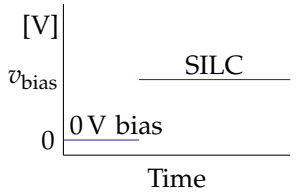


Figure 6: Measuring protocol

a bias voltage in the range of $-6.5\,\mathrm{V}$ to $-7\,\mathrm{V}$ has to be chosen.

To investigate the preferable bias voltage, the capacitors are biased at a voltage between $-6.5\,\mathrm{V}$ and $-7.5\,\mathrm{V}$, where the current is measured for 634 samples. The protocol for these measurements can be seen in Fig. 6. A 0 V bias part has been added to make sure that any charge left in the capacitor is removed. This measurement is repeated three times for greater reliability.

Measurements are conducted on four MOS capacitors, two of the data sets had interference problems and are thus discarded. In Fig. 7 the $\Delta I_{\%}$ over 150 seconds is expressed against the bias voltage. Where `1` and `2` represent the two devices on which the measurements are performed.

For larger v_{bias} the change in current is greater, this is probably due to the population of traps being non linear. It must be noted that for lower v_{bias} the time it takes to measure 634 samples is larger then that for a larger v_{bias}. For $v_{\mathrm{bias}} = -6.5\,\mathrm{V}$ it takes over 250 seconds, whilst for $v_{\mathrm{bias}} = -7.5\,\mathrm{V}$ it takes only 70 seconds.

The current changes about 70% less when using a bias voltage of $-6.5\,\mathrm{V}$ compared to a bias voltage of $-7.5\,\mathrm{V}$.

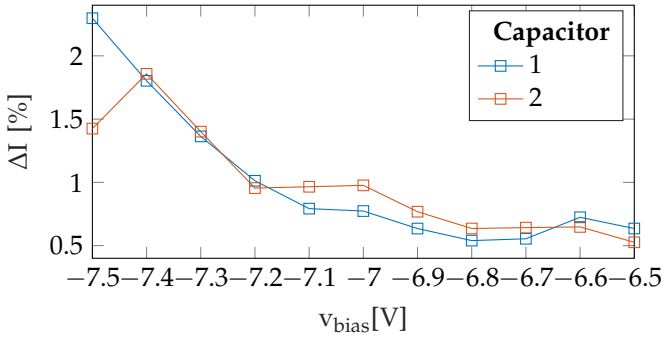


Figure 7: Change in current over 634 samples expressed as a percentage versus v_{bias}

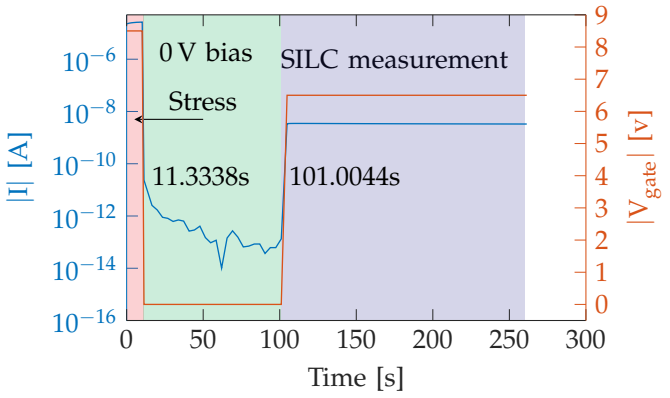
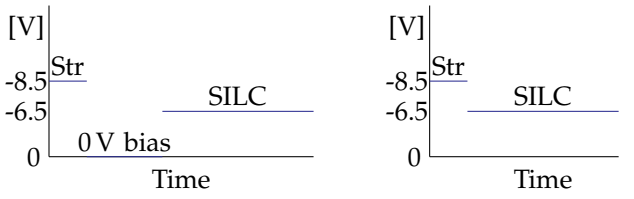


Figure 9: Voltage and Current versus time, measuring protocol with zero volt part

A. Establishing the Proposed Measurement Protocol

First a series of stress cycles are performed using the protocols seen in Fig. 8a and Fig. 8b. Fig. 8a will test the effect of adding a 0 V bias part in between stressing and performing a SILC measurement. Fig. 8b is as a control for comparing against. The measurements are repeated 10 times, with a small break between the 5th and 6th cycle. The stress time `Str` is 11 s, the 0 V bias time `0V bias` is 90 s, and the SILC measurement time `SILC` is 150 s. From this point on the stress voltage is −8.5 V. This is because we have used this in other research as well and it is further away from −6.5 V reducing the possible stressing effect during SILC measurements.



(a) With 0 V bias part (b) Without 0 V bias part

Figure 8: Measuring protocol for testing hypothesis

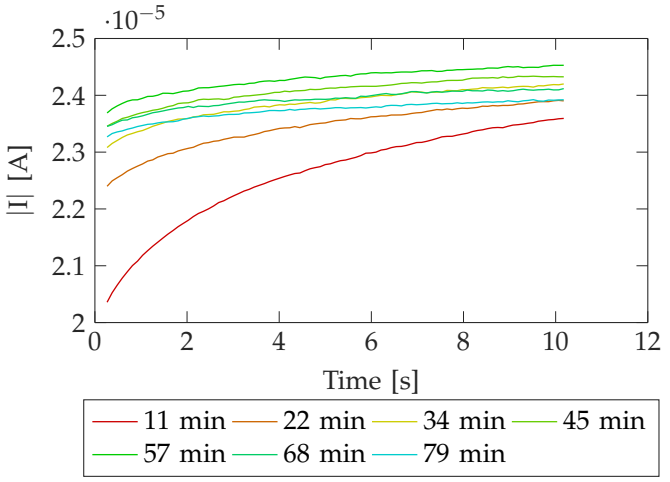


Figure 10: Current during stressing, $v_{\text{bias}} = -8.5$ V, old protocol

In Fig. 9 and Fig. 11 the supplied voltage and measured current can be seen for both with a 0 V bias part and for one without it. In Fig. 9 the time stamps show when the 0 Vbias part starts and ends. The red section is the stress. When looking closely to this, a gradual increase in current can be seen. This is better visible in Fig. 10. It can also be seen that the current decreases after a few stress cycles. This is likely due to the fact that the amount of trap that can be generated is reducing, and a hardening of the SiO_2 layer happens. Previously generated traps are now recovered and in turn are harder to be regenerated again. This happens for both protocols. The green section in Fig. 9 indicates the 0 V bias step. The current can be seen decreasing over time. Due to the fact that the currents are around the accuracy range of the Keithley 4200A-SCS, more variation in the current is seen. The blue section is the SILC measurement.

In Fig. 12 and Fig. 13 the results of the first five measurements can be seen. Nothing new is visible in these graphs that has not been mentioned before. Something new appears when the $\Delta I_{\%}$ over 150 seconds is plotted against the stress time for both plots as seen in Fig. 14. For the measurements without a zero volt part, the last 5 measurements were not usable due to bad contact. A clear improvement can be seen for the measurement with a 0V bias part. The improvement becomes greater the more stress is applied. For the first stress a 49.7% improvement is noted, where as for a total stress time of 57 seconds a 67% improvement is obtained. This is likely due to the depopulation of traps during the 0 V bias step. There is however still a 5% change in current for the new protocol. One part of this is the population of traps, which happens in the first 10 seconds. After which the current slowly

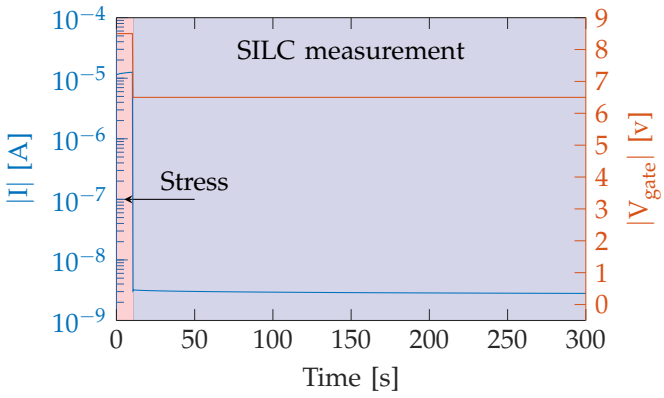


Figure 11: Voltage and Current versus time, measuring protocol without zero volt part

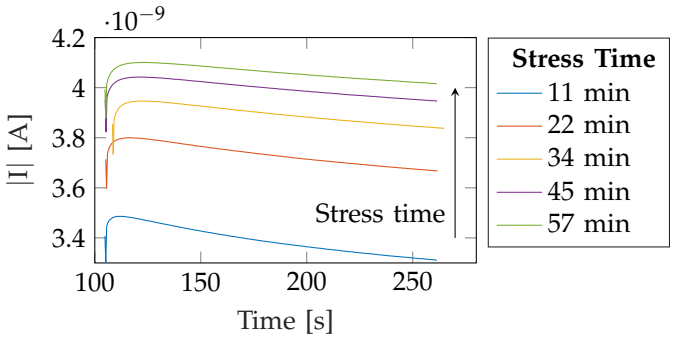


Figure 12: I-t measurement with $v_{\text{bias}} = -6.5\,\text{V}$, with 0V part

decreases. This could be due to the effect mentioned by Cester *et al.* [2]. However, the change does decrease with more stress time, so it is an effect related to stress time and probably also the bias voltage.

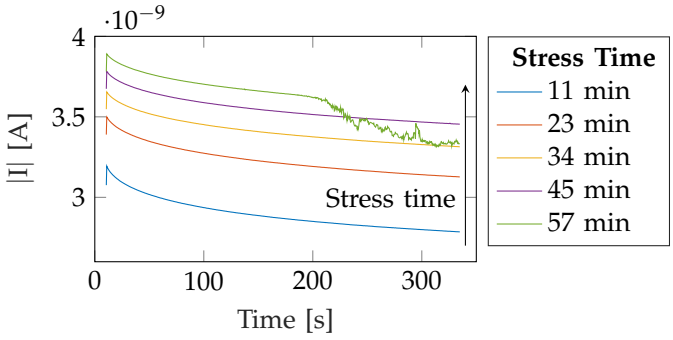


Figure 13: I-t measurement with $v_{\text{bias}} = -6.5\,\text{V}$, without 0V part

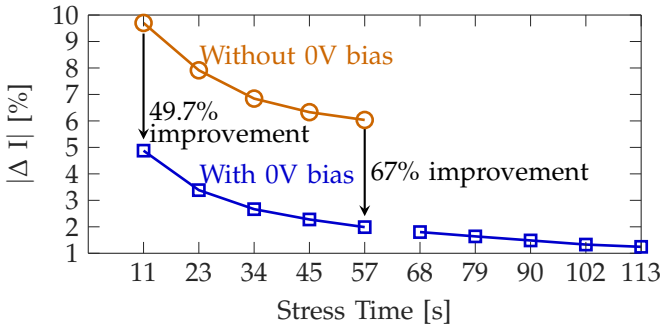


Figure 14: ΔI over 150 seconds at a bias voltage of $-6.5\,\text{V}$ post stress

B. *Proposed measuring protocol*

In Fig. 15 the proposed measuring protocol can be seen. Where $v_{\text{stress}} = -8.5\,\text{V}$ and $v_{\text{SILC}} = -6.5\,\text{V}$. The stress time is set to 91 samples, which is roughly equal to 11 seconds. The delay time is set to 26 samples, which is roughly equal to 90 seconds. During the Stress cycle the SILC measurement is 381 samples, and for a normal Measurement cycle the SILC measurement is 371 samples. Both are over 150 seconds so the difference in length does not matter. As mentioned before, Clarius does not support an easy way of specifying a bias voltage for a fixed amount of time, and thus a List of samples has to be made by hand.

The `Stress Cycle` is repeated 7 times for a total stress time of 77 seconds. More stress cycles does not increase the SILC significantly enough that it is worth the extra time. After Annealing the Measurement Cycle is repeated three times for greater reliability.

This new measuring protocol is tested against a similar protocol without the `0V bias` parts.

First a fresh measurement is performed on each of the MOS-capacitors. The measurement protocol is the same as the protocol for a measurement after annealing.

When looking at Fig. 3, it can be noted that the shape is similar to that of Fig. 12. However the measurements performed for Fig. 3 did not include a zero volt part. It turns out that when using the stress feature inside the Subsite function of Clarius. The Subsite function runs all the programs inside of it. So when a I-V measurement needs to be done after a I-t measurement, both these programs can be put inside the Subsite. Running the Subsite will execute the programs in order, in between the programs the probes are set to zero volt. The Subsite can also be set to run for multiple cycles, either with a delay or a stress between the cycles. However the behavior during stressing cannot be seen, as the current is not plotted while stressing. To obtain a continuous measurement the sample list has to be used.

To further optimize the measuring protocol the length of the 0 V bias is changed. The previous mentioned phenomenon suggests that the device can be set to zero

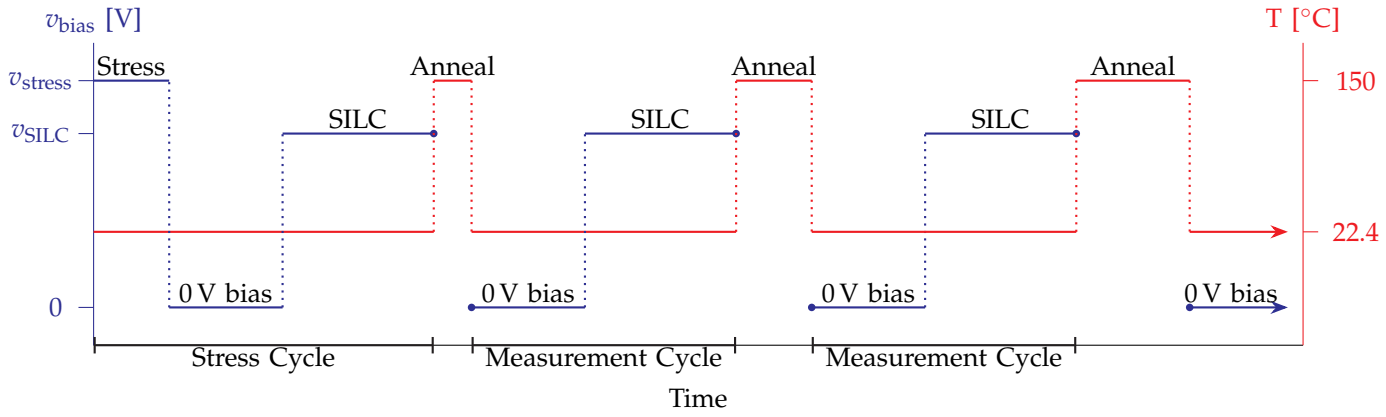


Figure 15: Proposed measuring protocol

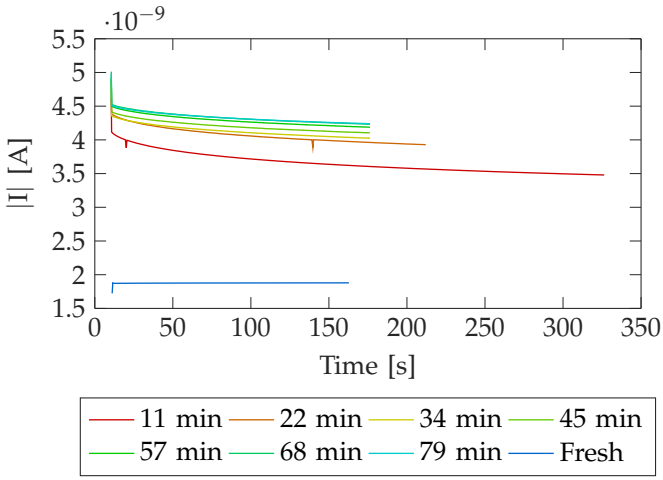


Figure 16: SILC after stressing, old protocol

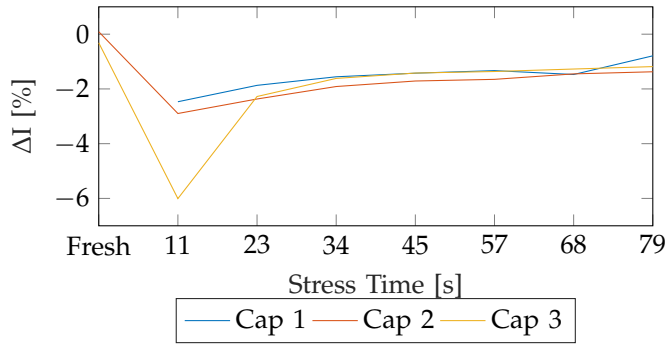


Figure 17: ΔI of the first 10 seconds, old protocol, post stress

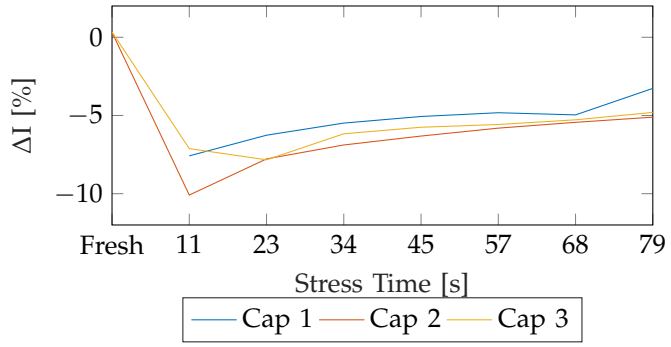


Figure 18: ΔI of $t = 10\,\text{s}$ to $t = 150\,\text{s}$, old protocol, post stress

volts for a brief moment of time. To test this, a series of measurements are performed where the device is set to zero volt for, zero, one, two, and three samples.

V. Discussion and Results

The measurements are performed as mentioned in Section IV. The results are separated in three parts: Stressing, Annealing, and Future Optimizations.

A. Stressing

First, we will discuss the old protocol, then the new protocol, and compare them.

In Fig. 16 the results of the old protocol can be seen. The decaying current is clearly visible on the left hand side of the graph. Lowering the potential from $-8.5\,\text{V}$ to $-6.5\,\text{V}$ releases the carriers occupying these higher energy traps, and leaving the traps unoccupied, therefor the decaying current. This is also supported by the fact that stressing the device for longer will not generate more traps in the long run. As can be seen, the spacing between each consecutive stress cycle decreases. When looking at the first 10 seconds we can see that the ΔI decreases with more stress, Fig. 17. If we follow the theory proposed by Moazzami *et al.* [5], this would suggest that the depopulation of traps becomes less the more its

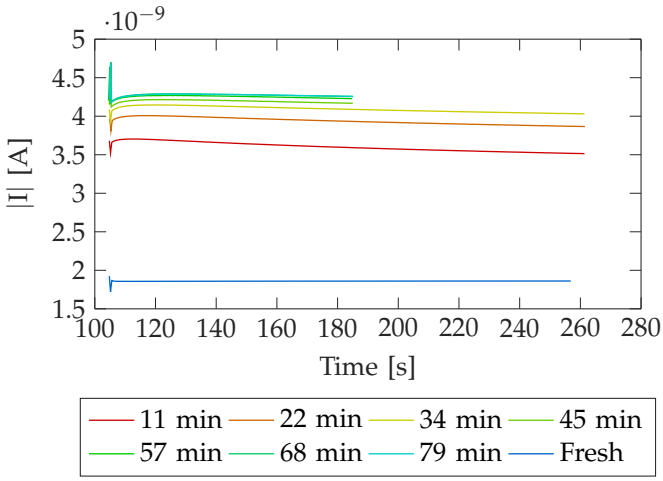


Figure 19: SILC after stressing, new protocol

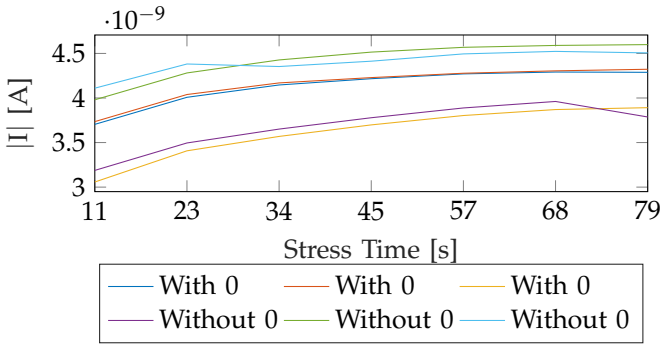


Figure 20: Maximum measured SILC current

stressed, this can be related to the fact that the current while stressing also decreases with more stress time, so less traps are populated when switching bias voltage.

In Fig. 19 the results of the new protocol can be seen. It is clearly visible that the sharp peak is not present. When we look at the first 10 seconds of the graphs, we can again see that the ΔI is increasing, just as we found in Fig. 4.

In Fig. 20 the maximum current is plotted for both protocols against the stress time. There is a small difference between the old- and new protocol, however, this is more than likely related to the small differences in the devices themselves. There is an outlier for both the old- and new protocol suggesting this is not due to the protocol. It does clearly show that for both protocols the maximum current has an exponential shape.

These plots however, do not clearly show the effects of the zero volt part. To show this more clearly, the change in current over time is expressed as a percentage and plotted against the total stress time as can be seen in Fig. 23. It can be clearly seen that the current changes significantly less when the device is set to zero volts

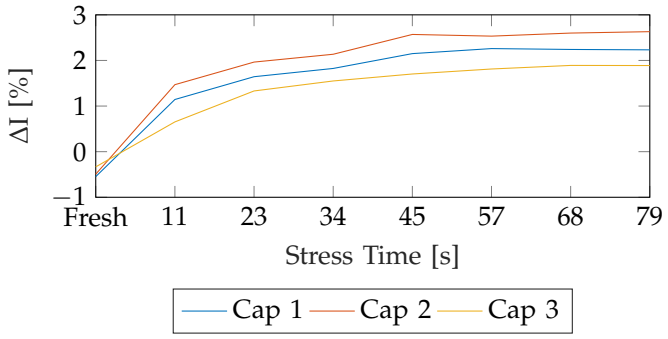


Figure 21: ΔI of the first 10 seconds, new protocol, post stress

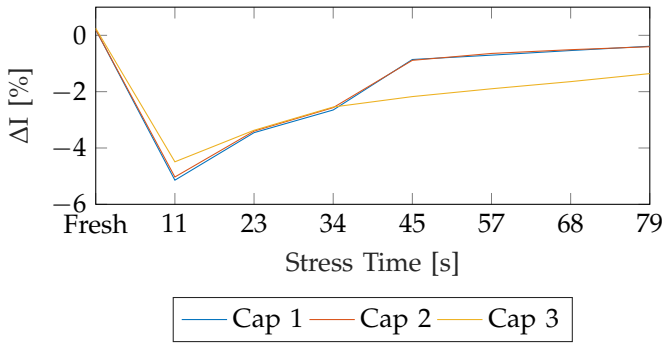


Figure 22: ΔI from $t = 10\,\mathrm{s}$ to $t = 150\,\mathrm{s}$, new protocol, post stress

between stressing and performing a SILC measurement.

If we compare Fig. 17 and Fig. 21, we can see that the ΔI decreases for the old protocol and increases for the new protocol the more the MOS capacitors are stressed. This suggests that adding a 0 V bias step does depopulate almost all traps, as for the old protocol the depopulated traps are being populated more and more, and more traps are generated the more the MOS capacitors are

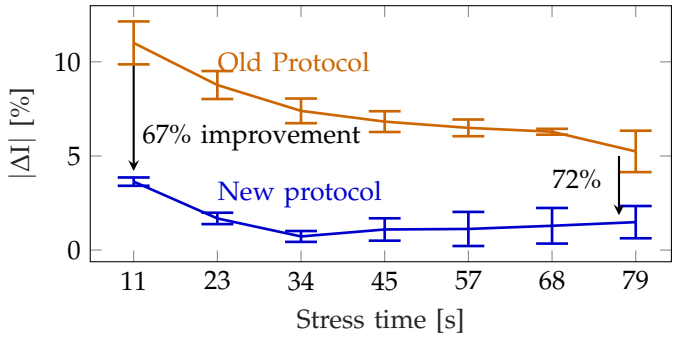


Figure 23: Change in current over 150 seconds, measured post stress

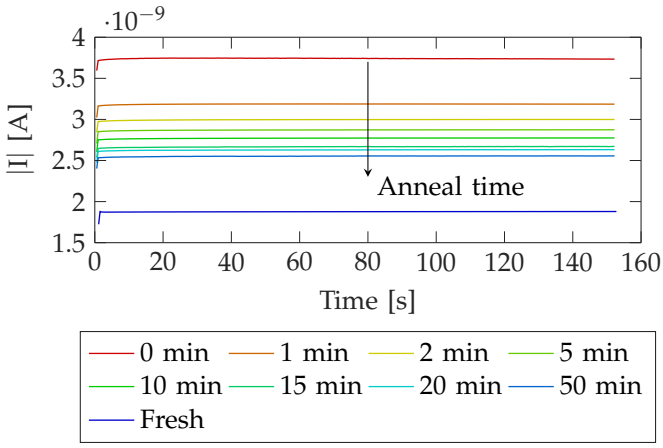


Figure 24: Averages of the measurements after Annealing and the fresh measurement. Old protocol

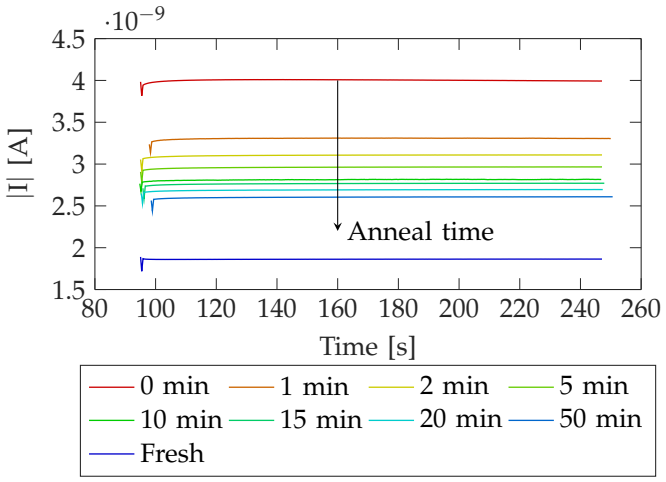


Figure 25: Averages of the measurements after Annealing and the fresh measurement. New protocol

being stressed. This results in an increasing current, but decreasing ΔI. For the new protocol it is the other way around. Every time the MOS capacitor is set to 0 V the traps are being depopulated, and when the MOS capacitor is being stressed these traps are populated again, while more traps are generated by the stress. Resulting in an increase in current and increase in ΔI. For both cases it reaches a steady state as the more stress is applied, the less traps are generated.

B. Annealing

First, we will discuss the old protocol, then the new protocol, and compare them.

In Fig. 24 the results of the SILC measurements performed on one device can be seen. The measurements of the other devices can be seen in appendix A. The effects of annealing can be clearly seen, as the graphs tend towards the `Fresh` graph when looking at the anneal time. The X-axis is the measurement time, whilst the plotted graphs are per anneal time, as shown in the legend.

The new protocol gives a similar graph as can be seen in Fig. 25. Note, this figure includes a zero minute anneal, meaning it is measured after the stress cycle is finished. Other than that the Figures are very similar.

The fact that they are very similar can also be seen when ΔI is expressed as a percentage and plotted against the anneal time Fig. 26.

As can be seen in the figure, the change in current is between 0.5 and 1.5 percent regardless of the used protocol. There is one outlier at 1 minute anneal time, this is due to an inconsistency in the measurement.

In Fig. 27 the final average value of the current over 150 seconds can be seen plotted against the anneal time. As can be seen the graphs lie within 0.5 nA of each other.

C. Further Optimizations

In Fig. 28 $|\Delta I_{\%}|$ can be seen for a certain number of 0 V samples. We can see that for no zero volt samples

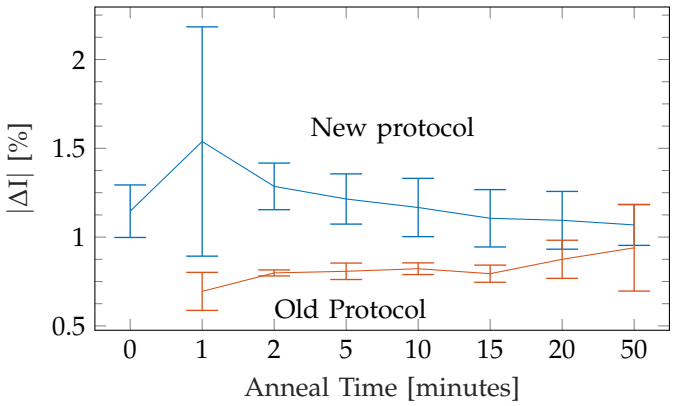


Figure 26: ΔI over 150 seconds expressed in percentages against the anneal time in minutes

the ΔI is generally quite large. While for the any number of zero volt samples the ΔI is as we would expect when using the new protocol. These measurements are done on the same MOS-capacitros used to test the new protocol, meaning these are not fresh devices. Only three sets of zero volt samples are investigated, therefore no concrete conclusion can be given. For this more measurements on fresh capacitors should be performed.

VI. Conclusion

In literature when the Fowler-Nordheim stress is interrupted a decaying reverse current has been reported [5]. They suggest that the reverse current is linked to the depopulation of traps. Since this reverse current has not been reported outside their paper, is has been ignored. However, it has not been investigated whether or not the depopulation of traps actually forms a problem for the MOS capacitors we use. So in this paper we aim to

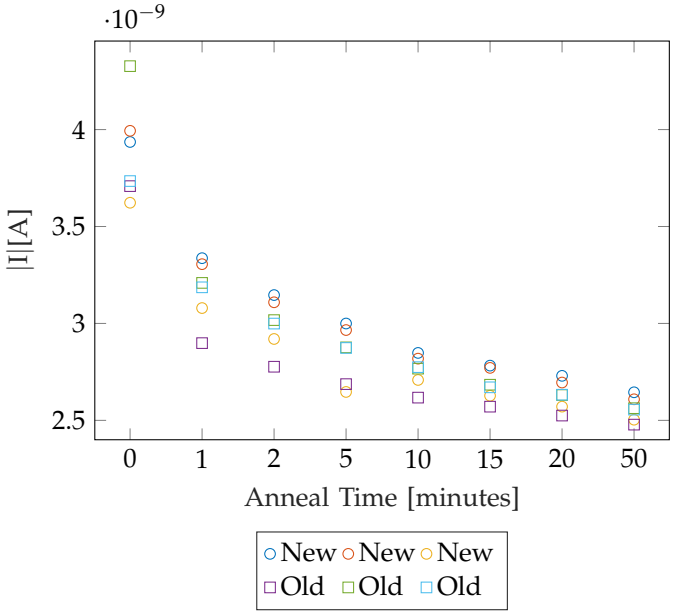


Figure 27: Current after 150 s versus anneal time

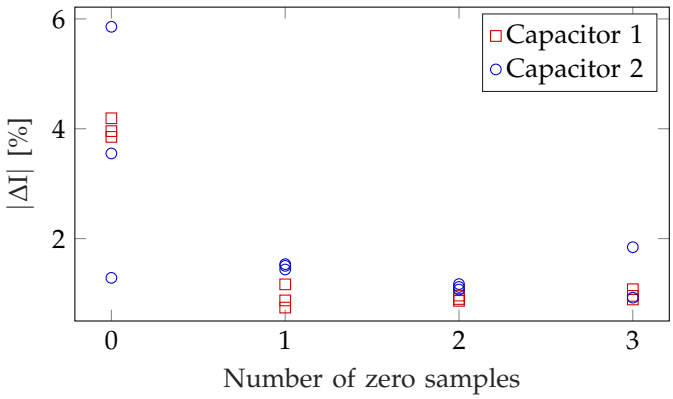


Figure 28: ΔI over 150 seconds per number of 0 V samples

establish if the depopulation of traps occurs for our MOS capacitors. We also investigate a proposed measurement protocol for SILC that makes use of a 0 V bias part to reduce the effect of depopulating traps.

It is found that the depopulation of traps only plays a for SILC measurements post stressing, and does not occur during SILC measurements post annealing. When using a 0 V bias step an improvement between 50% and 72% is achieved. This improvement is based on the ΔI of 150 seconds while performing SILC measurements. This is most likely due to the fact that after applying a stress, the traps inside the oxide layer are almost fully populated, meaning an equilibrium is reached between populating and depopulating traps. So when the stress bias voltage is removed, or lowered for SILC measurements, the equilibrium is disturbed and less traps are being populated than depopulated until a new equilibrium is established. This is represented as a decaying current curve. However, when a 0 V bias is applied, the population of traps is stopped and the traps are being fully depopulated. When a new bias voltage is applied to measure the SILC, the traps are being populated again, which is visible as an increasing exponential.

The length of the 0 V bias step does not seem to affect the improvements, however more research needs to be conducted before a concrete result can be given.

Besides these findings, we also found that there is relation between the type and amount of traps that are generated by the stress. This is concluded form the fact that the SILC current has an exponential relation with the stress time. Depopulation of traps also seems to be related with the stress time, as it becomes less for longer stress times.

VII. Future Recommendations

As mentioned previously, more research needs to be done on the length of the 0 V bias step. For this we suggest that a similar method is used, where the length of the 0 V bias step is gradually increased. The depopulation and re population of traps should also be investigated more in depth, such that a relation can obtained between the de-/re- population of traps and the bias voltage. Another effect that has not been discussed in this paper is the fact that with the new protocol, a ΔI is measured between 5% and 2%, meaning there is still a time dependent component in the SILC. This time dependent component seems to be related to the stress time as it decreases with more stress time.

We recommend that a 0 V bias step is added post stressing, as it results in a 50% to 72% drop in ΔI over 150 seconds.

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APPENDIX

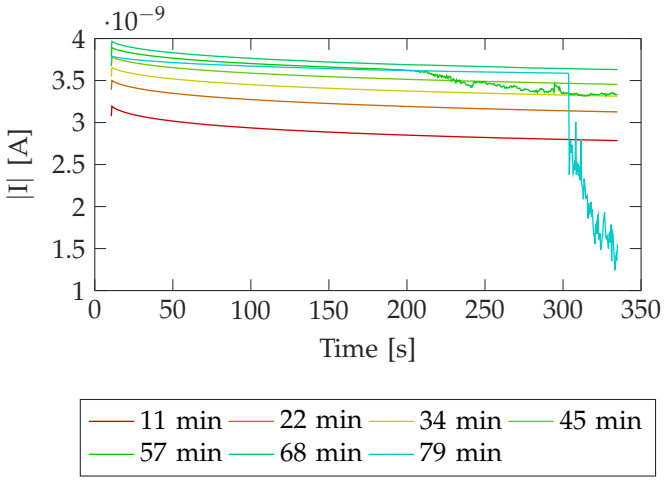

Figure 29: SILC after stressing, old protocol

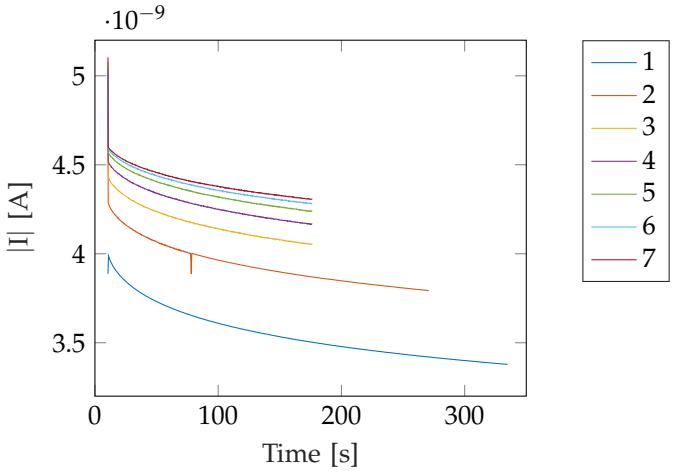

Figure 30: SILC after stressing, old protocol

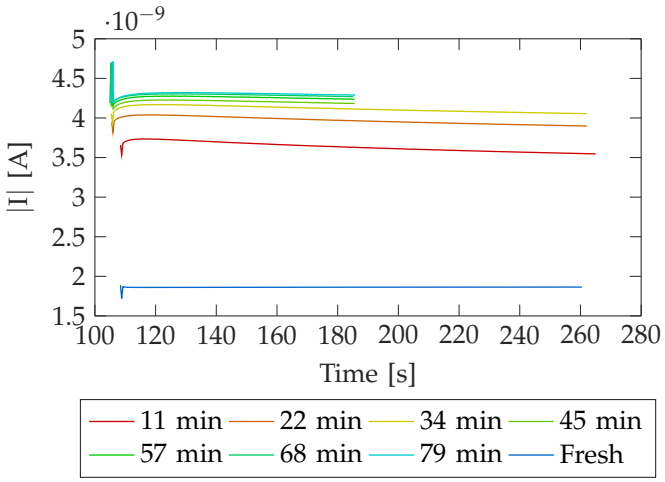

Figure 31: SILC after stressing, new protocol

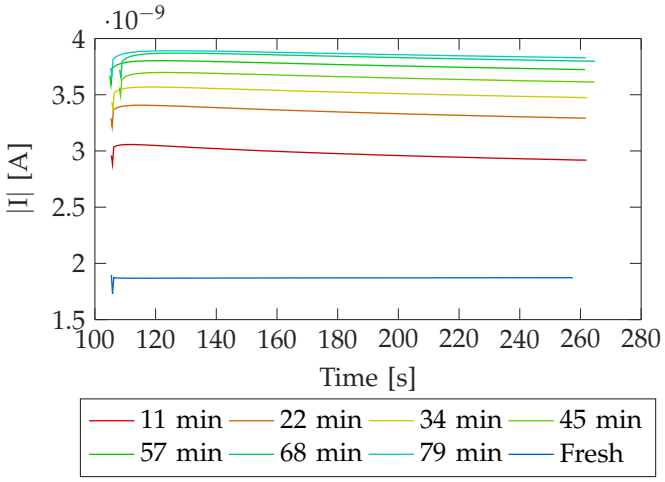

Figure 32: SILC after stressing, new protocol

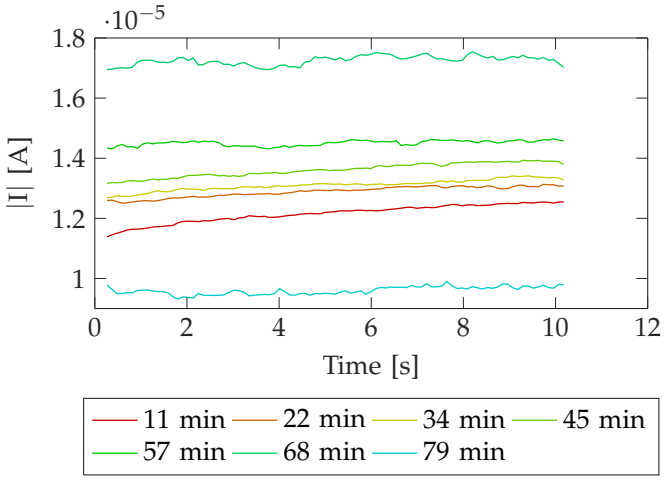

Figure 33: Current during stressing, $v_{\text{bias}} = -8.5\,\text{V}$, old protocol

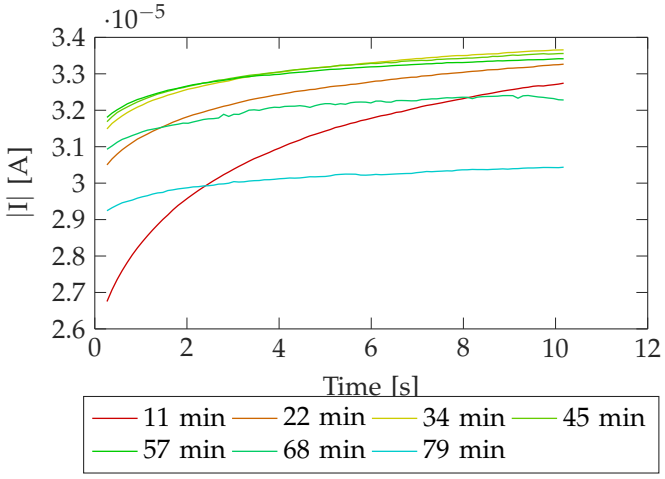

Figure 34: Current during stressing, $v_{\text{bias}} = -8.5\,\text{V}$, new protocol

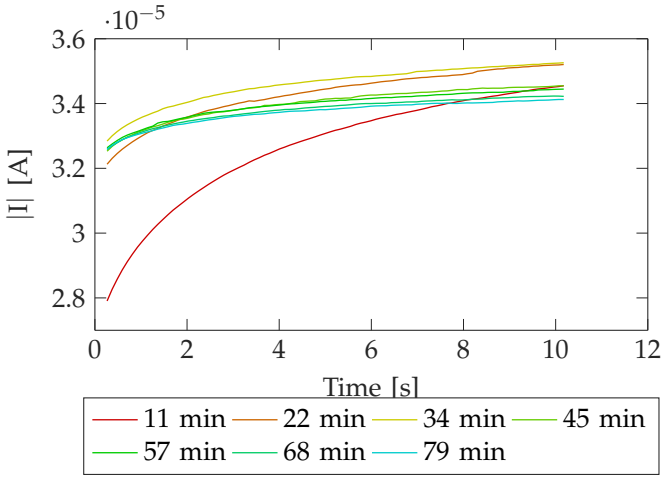

Figure 35: Current during stressing, $v_{\text{bias}} = -8.5\,\text{V}$, new protocol

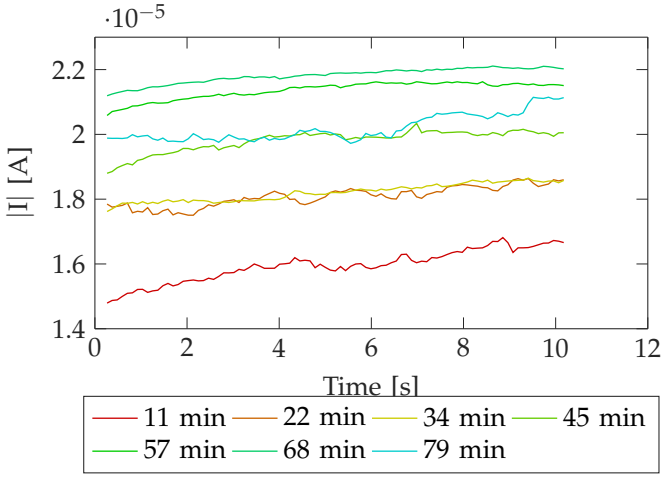

Figure 36: Current during stressing, $v_{\text{bias}} = -8.5\,\text{V}$, new protocol

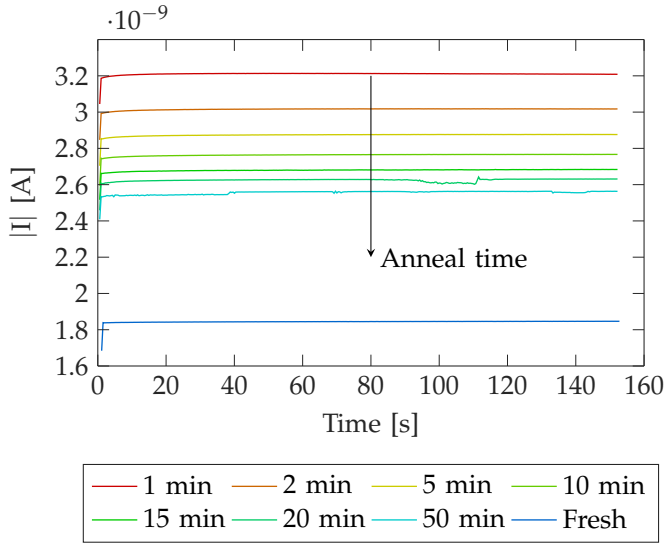

Figure 37: Averages of the measurements after Annealing and the fresh measurement. Old protocol

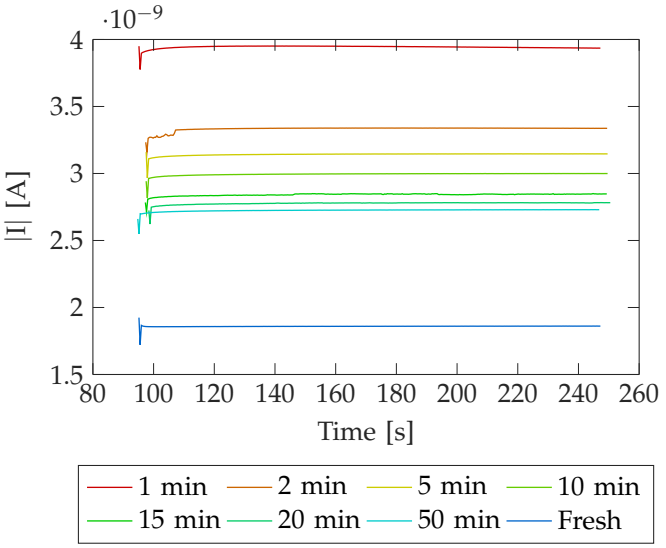

Figure 39: Averages of the measurements after Annealing and the fresh measurement. New protocol

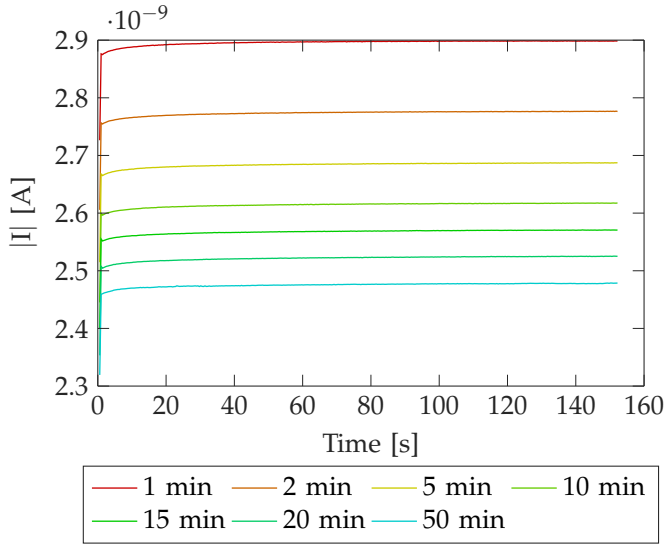

Figure 38: Averages of the measurements after Annealing and the fresh measurement. Old protocol

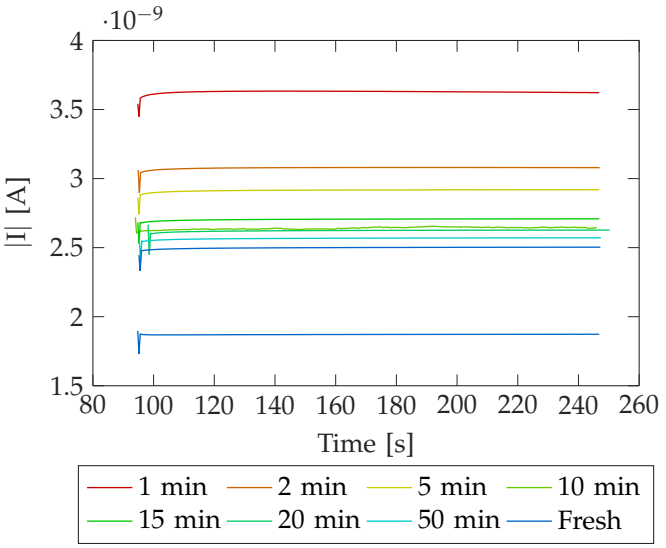

Figure 40: Averages of the measurements after Annealing and the fresh measurement. New protocol